Electronics for a Pixel Upgrade

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Third Hit System:

- Assume this is a continuation of two-hit system, so there is no new electronics activity for this. Do not discuss further...

B-layer Upgrade:

- Assume that this is the first significant upgrade opportunity.
- However, assume that it is based on identical module geometry to that of present detector, in order to preserve basic services and mechanical design.
- Electronics would concentrate on segmentation and functionality.

Total Pixel Replacement for SLHC:

- The date and scope for this is largely unknown. Luminosity goal could be as high as 10^{35}, but time structure is unknown. Could be close to DC (almost unbunched beams) or could be bunch-based with higher crossing frequency (e.g. 80MHz).
- At this point, would re-examine all assumptions (chip size, module geometry, pixel size and layout). Would also consider L1 trigger functionality for VTX triggering.

B-Layer Upgrade

Assume same basic module geometry and specifications:

- B-layer would still be built with similar geometry staves, similar services and similar current budget for module operation.

Assume we will migrate to the next generation of CMOS:

- Not clear what the lifetime of the 0.25μ will be, but IBM frame contract is being extended to 2007. Nevertheless, we see limitations in radiation hardness, and it would be very difficult to improve the segmentation below the present design.
- Present CERN plan is to skip 0.18μ and jump to 0.13μ (IBM CMOS8). This seems like a reasonable step for pixels. This generation is already a commercial process for micro-processor giants (Intel, TI, Xilinx are in high-volume production), and is stabilizing from IBM. CERN has not yet started to move forward on corresponding frame contract, but expects to do so shortly.
- First characterization results now available from CERN/RAL based on test structures from an IBM internal MPW, and look extremely promising. Major issue is high cost: mask costs go from about 125K$ for 0.25μ to about $600K$ for 0.13μ, so barrier to prototyping becomes very high.
- Access is available through MOSIS, and we have an NDA in place already. Minimum die size is 10mm^2, and cost is 50K$ for 40 die.

Major issues for the chip design:

- What is the right front-end concept: Zero-crossing for timing ? TOT or peak-sensing for charge ? This depends critically on expected occupancy (allowed single pixel deadtime) and scaling of current budget with pixel size/count.
- What is the right pixel size ? Do we give priority to improving segmentation in the narrow or the long direction ?
- What is the right chip size ? Present total module electronics footprint of 22.2mm x 60.6mm gives an active area of 16.4mm x 60.8mm, or only 74% live fraction.
- Maximum die size is 21.4mm in height, so could imagine a single chip with column pairs containing 512 rows of 32μ pixels with perhaps 3mm of overhead at the bottom of the chip. The pixels could be 200μ wide, with 32 column pairs. The FE chip would have 32K channels in an area of 19.4mm x 12.8mm (3 times the current FE chip). Such a chip would probably have 40-50M transistors. Could it provide the required performance without requiring significantly more current ? This seems unlikely, so a new scheme would be needed to avoid explosion of service burdens. A module based on such a chip would use only 5 FE chips to provide 160K pixels and about 85% live fraction. All of the ganged pixels would be eliminated.
- What can be done to combat power management and services issues ? Expect to use internal regulators in each FE chip. Can one imagine a current-mode powering scheme instead of the traditional voltage mode ? Serial powering concept has been investigated by Bonn, and presents many challenges. Further thought required...

Next Steps:

- Work with CERN/RAL/FNAL on next generation design environment.
- Further study on radiation-hardness issues, and allowable transistor geometry. Initial results suggest the process (dominant effect is VT shifts in PMOS) is much more radiation hard than 0.25μ. Appears to be no need for guard-rings around NMOS, and for wider devices, no need for annular NMOS at all.
- Begin studying analog design issues. Matching coefficients are similar, and so expect that many analog transistors cannot shrink (but their capacitance will grow compared to 0.25μ). Limited supply range imposes new approaches to dynamic range management (even bandgap references sit beyond the supply rail).
- Begin study of “nanometer” design flows for digital design. Wiring issues and signal integrity become even more critical than for 0.25μ, since not only placement but actual routing critically affects performance (dominant capacitances are to neighboring wires). Look at developing SEU-tolerant and very TID-tolerant standard cells.

Program of action for near term:

- If we decide to move ahead in this area in the near-term, would want to follow foundational work above with fabrication of prototype chips.
- Will need guidance on optimization of geometry at a very early stage (before we have any real experience with operating the first-generation pixel detector).

Total Replacement Scenario

- This scenario would arise once the accelerator performance had increased to the point where major tracker improvements were required. It would be part of a larger picture of extending pixel-like detectors to larger R, replacing straws with strips, etc.
- Would naively imagine a “high volume” pixel optimization for larger R, and a “high performance” pixel optimization for small R. Both would evolve from present design in different directions. The “high volume” path would need to minimize power/ current per unit area to reduce material, and optimize for very large die size in a mature (low cost, high yield) process. The “high performance” path would need to use a cutting-edge process to get maximum segmentation and performance.
- A major issue at that time would be the triggerability of the pixel system. From the FE electronics point of view, a triggerable system would be a simple extension, just providing direct outputs from the EOC buffers instead of storing data until L1 appear. However, either the core trigger functions would be off-detector, in which case massive improvements in data transmission technology would be needed, or core functions would be on-detector, in which case massive R&D would be needed to create very sophisticated digital processors in the pixel volume. Personally, believe the trigger problem for LHC is so challenging that one would need to transmit the data over multi-Gbit optical links. This might require SiGe development for high-radiation environments, plus a conversion to single-mode fiber infrastructure, and would clearly be very challenging within a limited volume and power budget.