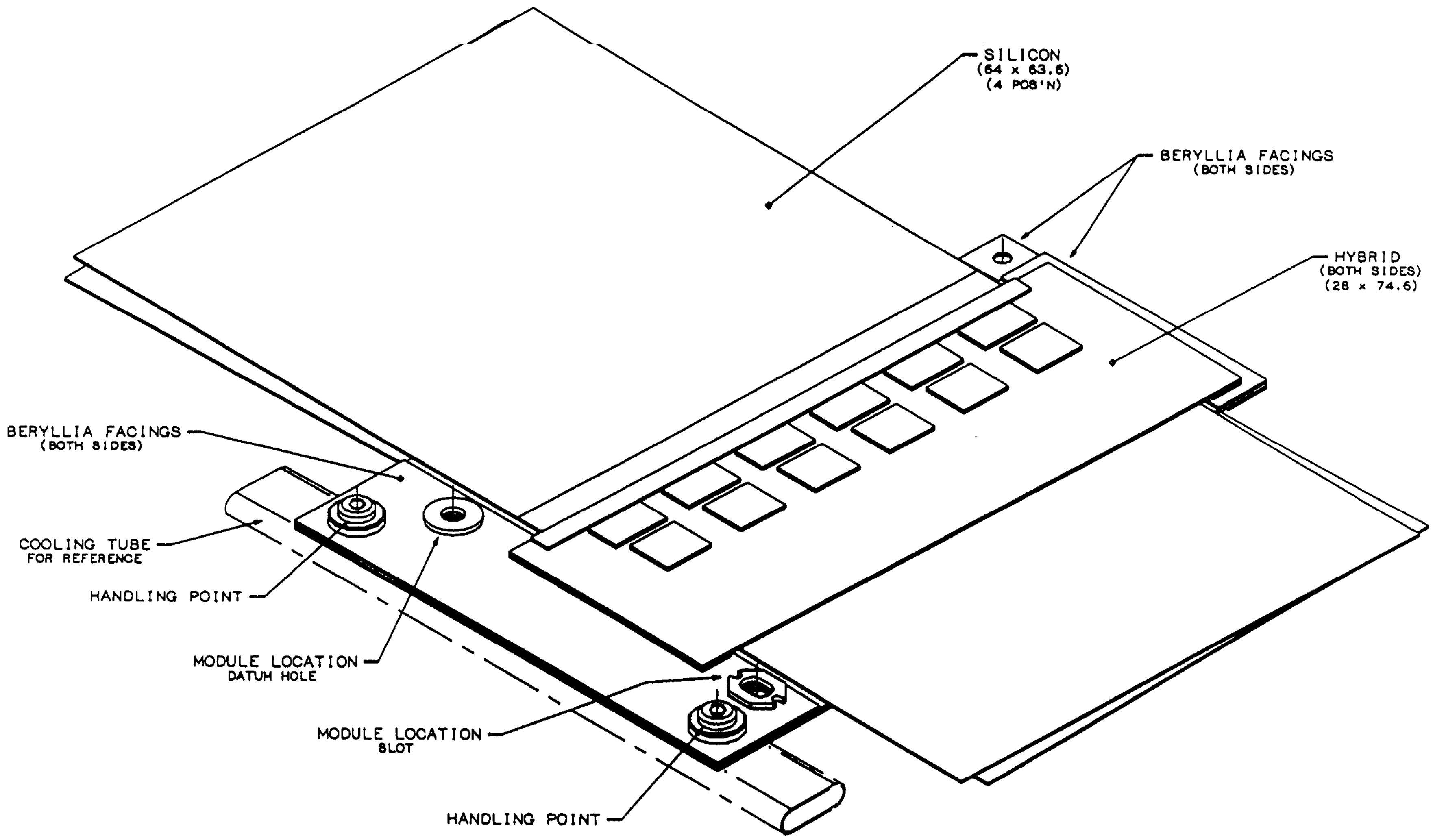
Silicon Strips

WBS 1.1.2

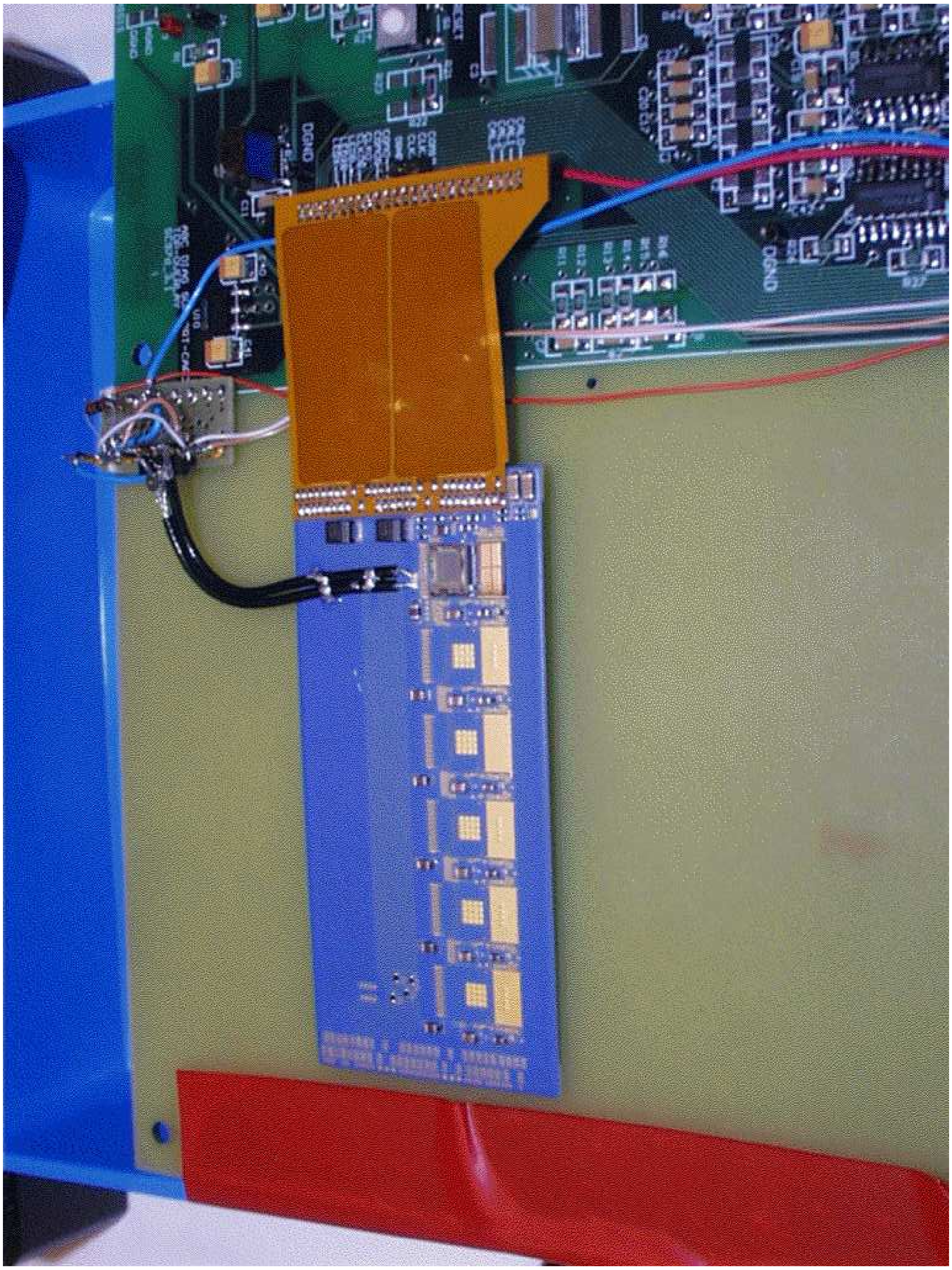
A. Seiden
BNL
October, 1998

Outline

1. Detectors
2. Electronics
3. Hybrids and Modules
4. Cost and Schedule



SILICON
(64 x 63.6)
(4 POS'N)
BERYLLIA FACINGS
(BOTH SIDES)
HYBRID
(BOTH SIDES)
(28 x 74.6)
BERYLLIA FACINGS
(BOTH SIDES)
COOLING TUBE
FOR REFERENCE
HANDLING POINT
MODULE LOCATION
DATUM HOLE
MODULE LOCATION
SLOT
HANDLING POINT


DGND

Detectors

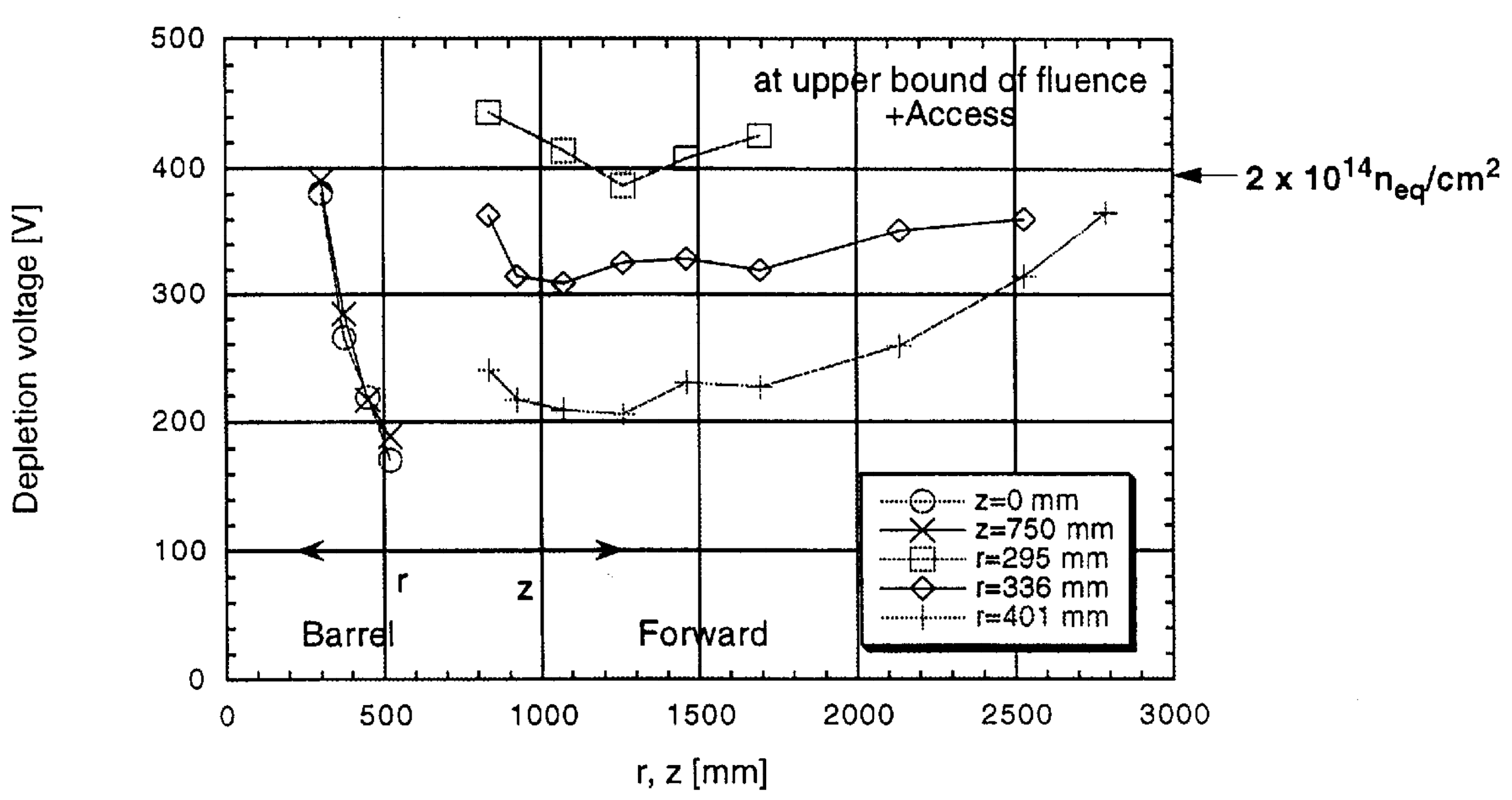
SCT Community has moved to p-on-n detectors based mainly on cost considerations. A p-on-n design can meet the 10 year lifetime requirement at 1.5 $\times$ nominal fluence by:

(1) Raising voltage limit from 300 V (old n-on-n value) to 350 V.

(2) Thinning inner detectors: Inner ring to 250 μm, inner barrel to 270 μm.

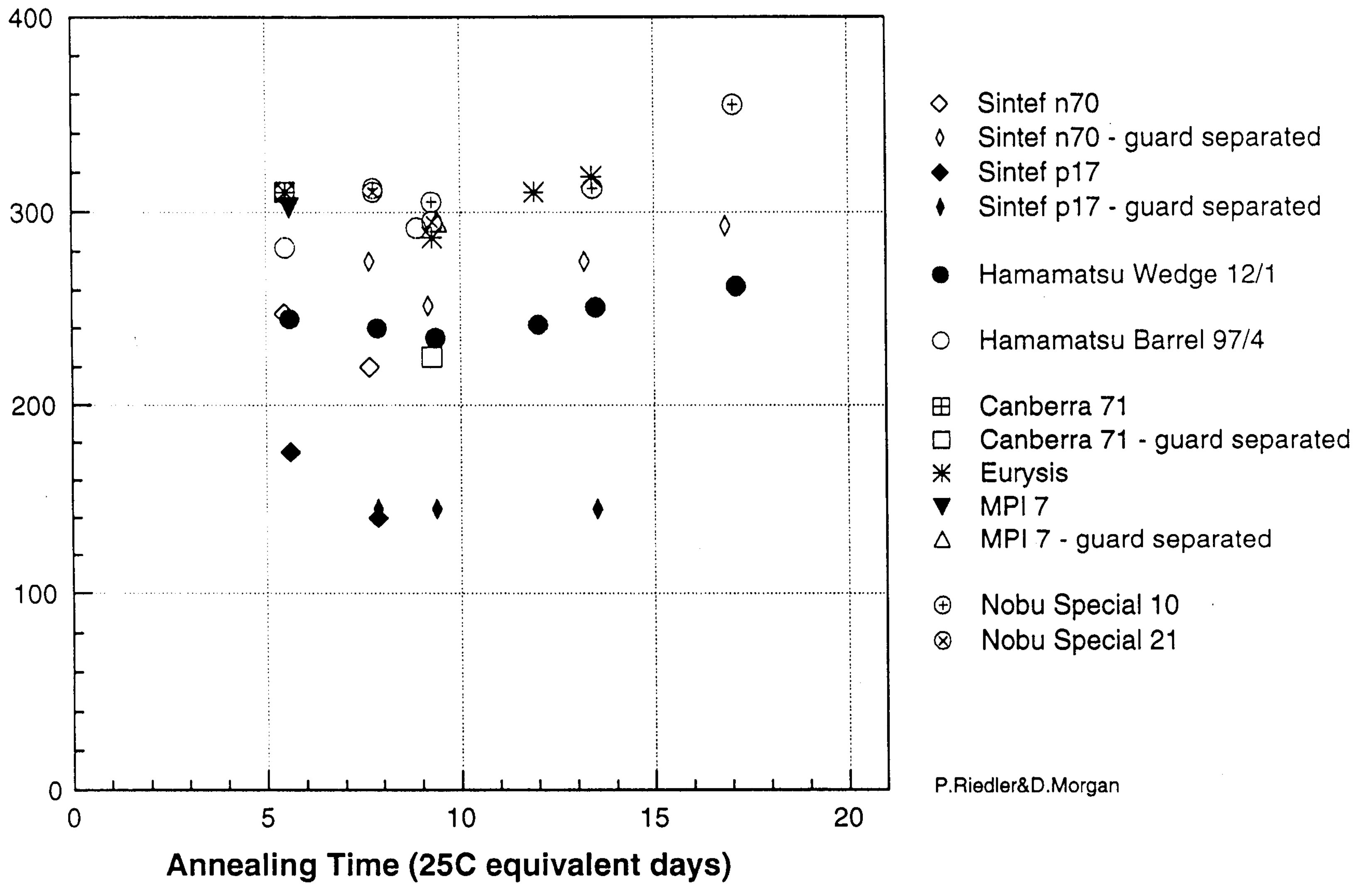
Work is ongoing with vendors to ensure that we get high quality AC coupled detectors.

Full depletion voltages in SCT

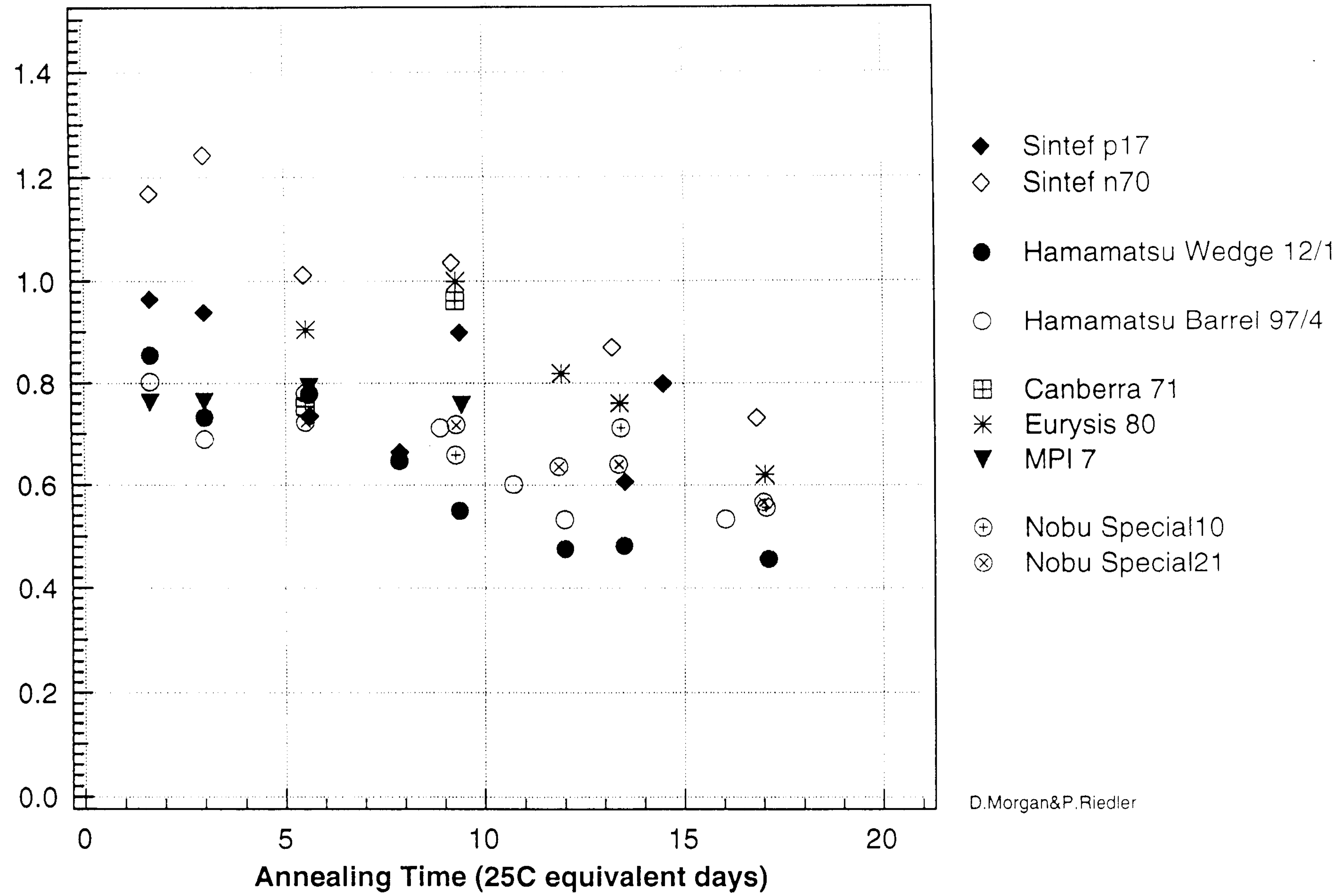


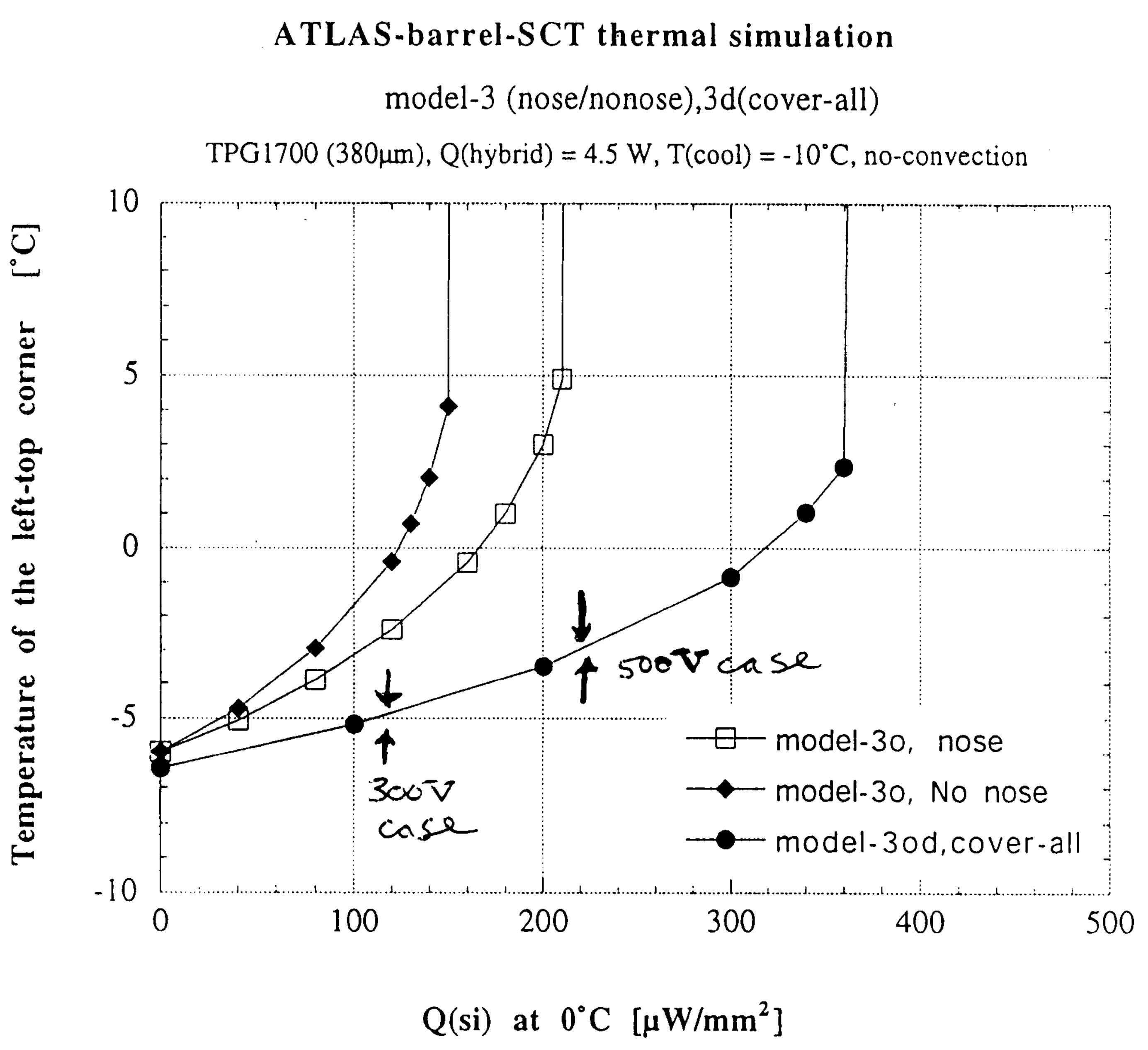
Expected depletion voltages for barrel and forward modules. at the upper bound of expected fluence and an access scenario of 2 days at 20 °C and 14 days at 17 °C every year (ref: Inner detetor TDR)

Depletion Voltages for the Warm-Up Cycle
Estimated from C-V measurements at 100 Hz

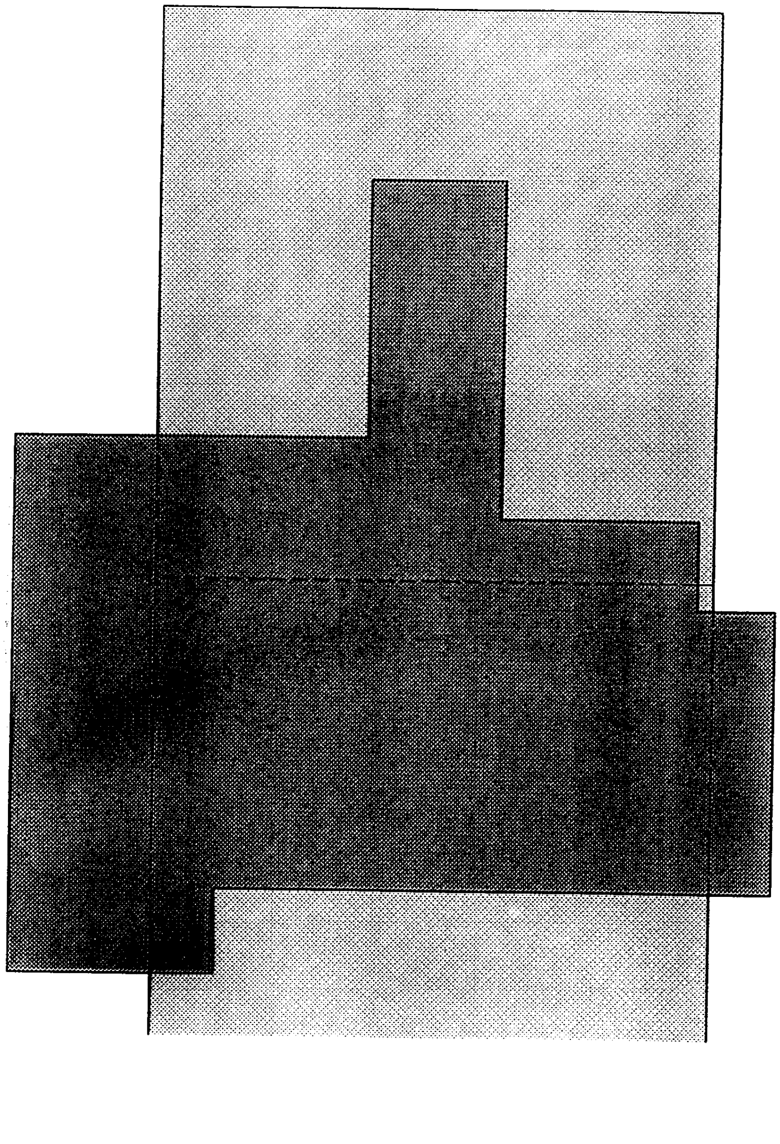


Total Leakage Current Measured at 400V for the Warm-Up Cycle
(Normalised to -10C)





ATLAS-barrel-SCT thermal simulation
model-3 (nose/nonose),3d(cover-all)
TPG1700 (380μm), Q(hybrid) = 4.5 W, T(cool) = -10°C, no-convection
Temperature of the left-top corner [°C]
10
5
0
-5
-10
0
100
200
300
400
500
Q(si) at 0°C [μW/mm²]
model-3o, nose
model-3o, No nose
model-3od,cover-all
500V case
300V case



Silicon Strips: Hybrids

Status:

Prototype ceramic "diagnostic" hybrid (BeO) developed for the Cafe-M and ABC chips successfully fabricated.

Cafe-M and ABC chips are under test on these hybrids both irradiated and un-irradiated. Preparing to mount on detector module.

Design is correct. Yield low due to (correctable) problems at vendor. Hybrids are bowed, while acceptable this will be addressed in a second fabrication run. Strategy to reduce the bow has been developed.

Similar ABCD design developed and fabricated at CERN.

Second approach, a full kapton design, designed and fabricated for ABCD. Potential of lower mass and integrated cables. Some concern about manufacture and reliability. Tested on first batch of ABCD. Design for Cafe-M, ABC complete.

Third approach, thin aluminum on PG, offers high thermal conductivity and low mass. Tested on ABCD chips. New design, with even higher thermal conductivity being developed.

Hybrid technology choice is currently under discussion. Possibilty of early choice or else choice to be made at same time as IC vendor selection.

Selection of encapsulants and adhesives are under study including irradiations. Some acceptable materials have been identified.

Open questions:

(1) Fully loaded hybrid set with detectors still to be demonstrated $\rightarrow$ need chips.

(2) Front to back interconnect options to be studied.

(3) Mechanical bowing on ceramic design–confirm that new approach is better.

(4) Adhesive and encapsulant selections.

(5) Hybrid technology choice.

(6) Procurement plan for hybrid manufacture and assembly needs to be settled across collaboration.

Work plan and goals for next year:

(1) Continued testing of prototype with available chips, leading to measurements with fully loaded and irradiated detectors.

(2) Explore front to back interconnect options.

(3) Fabricate second small set of ceramic hybrids to address vendor yield and bowing issues.

(4) Produce layout of non-diagnostic ceramic hybrid.

(5) Fabricate and test kapton hybrid for Cafe-M and ABC.

(6) Identify and test adhesives and encapsulants, including irradiations.

Silicon Strips: Modules

Status:

Module design is highly evolved to address thermal and electrical performance, mass, and manufacture.

Early design electrical prototypes have been fabricated and tested but present generation awaits supply of chips.

Baseline module construction process has been described in the TDR and accepted by the collaboration. Prototype assembly systems are under evaluation at 5 sites including USA.

System installed at LBNL is functional and being used to study assembly precision issues. Full set of dummy components in-hand. Three mechanical modules have been fabricated using a manual procedure (final system to be automated). Early metrology results exist.

Post assembly metrology to use optical inspection system.

Automatic wirebonders up and running at US sites.

Open questions:

(1) Electrical performance, pre and post-irradiation await chips for full evaluations.

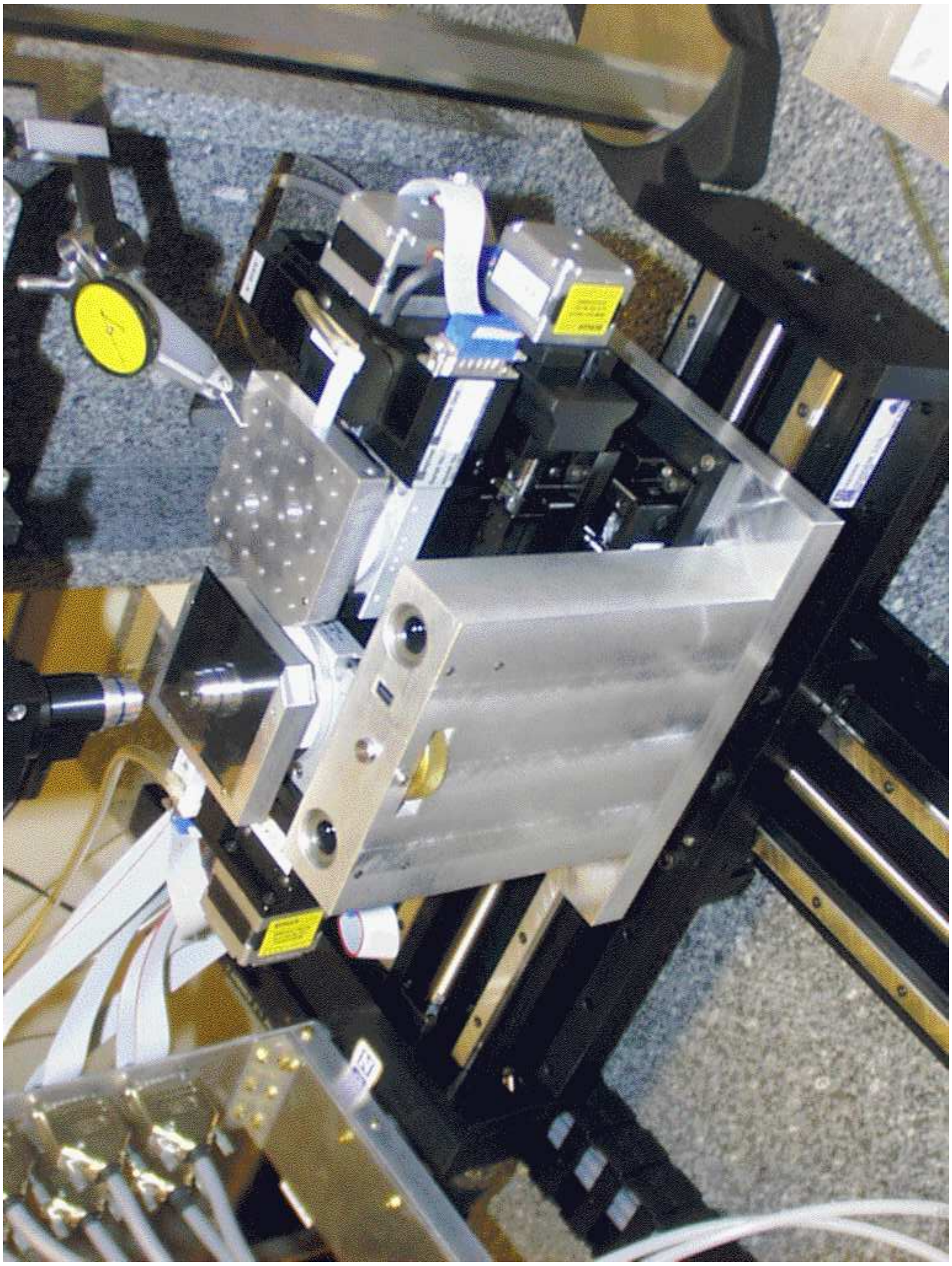
(2) Ability of assembly system to meet construction specifications must be fully demonstrated. Preliminary results are encouraging. Certain details of system and process still to evolve.

Work plan and goals for next year:

(1) Continued development of assembly system including inspection and alignment software.

(2) Precision assembly tests to demonstrate performance of assembly system. Move to final assembly process.

(3) Assembly of fully functional modules once chips are available.



WBS 1.1.2 Schedule: IC Electronics

Item		
17	BCP for 2nd prototype submitted	8/14/98
19	BCP approved	9/29/98
16	Procurements in place for 2nd prototype	10/9/98
31	Frame contract in place	4/15/99
20	Final design review for 2nd CAFE-M	9/15/98
48	Submit 2nd CAFE-M/ABC	10/30/98
21	Final design review for 2nd ABC	10/23/98
49	Submit 2nd ABC	11/16/98
22	Final design review for 2nd ABCD	12/11/98
50	Submit 2nd ABCD	1/27/99
54	Complete fab of 2nd CAFE-M	4/19/99
55	Complete fab of 2nd ABC	4/19/99
56	Complete fab of 2nd ABCD	6/30/99
65	1st ICs available for 2nd proto-hybrid	5/18/99
74	Select IC vendor	12/10/99
35	Final design review	3/3/00
77	Complete preproduction fab	9/1/00
79	1st ICs available for preprod hybrid	10/13/00
38	Production Readiness Review	3/2/01
81	Release/start full production	3/30/01
86	1st ICs avail for production hybrids	8/14/01
90	Production testing complete	11/21/02

WBS 1.1.2 Schedule: Module Assembly and Test

Item		
182	Complete design of proto mod assy/test	6/14/99
202	Complete fab of tools for proto mod/assy	6/14/99
204	Complete assembly of proto modules	11/29/99
206	Complete test/measure proto modules	12/27/99
216	Complete fab of tools for preprod modules	11/10/00
225	Prod facilities, equip, tooling complete	11/13/00
219	Complete preproduction modules	2/23/01
221	Complete preproduction module test	4/11/01
193	Module production readiness review	4/11/01
230	Start full strip module production	6/5/01
236	Complete production modules	4/29/03
238	Complete rework of production modules	5/27/03
246	Complete shipping of production modules	8/26/03
	Key IC Dates:	
	1st ICs for 2nd proto-hybrid	5/18/99
	1st ICs for preprod hybrid	10/13/00
	1st ICs for production hybrids	8/14/01

WBS 1.1.2 Schedule: Hybrids/Cables/Fanouts

Item		
94	Complete design 2nd prototype hybrid substrate, cable, fanout	10/29/98
126	Complete fab 2nd prototype hybrid substrate, cable, fanout	3/11/99
137	Complete test of 2nd prototype hybrid	12/8/99
144	Select hybrid substrate type	12/10/99
111	Hybrid final design review	2/11/00
146	Complete fab of preprod hybrid substrates	6/23/00
116	Hybrid production readiness review	4/11/01
98	Complete prod hybrid substrate, cable fanout design	5/8/01
148	Complete fab of prod hybrids	12/31/02
	Key IC Dates:	
	1st ICs for 2nd proto-hybrid	5/18/99
	1st ICs for preprod hybrid	10/13/00
	1st ICs for production hybrids	8/14/01

U.S. ATLAS
WBS Summary Cost Estimates

Source: All

ons: All

Funding Type: Project

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	Description	Base Cost (k$)	Cont Cost (k$)	Cont %	Total Cost (k$)	EDIA Labor (k$)	Mfg Labor (k$)	EDIA Matls (k$)	Mfg Matls (k$)	FTEs Project	FTEs Other
	Silicon Strip System	6296	1437	23	7733	624	812	22	4837	25.8	9.8
	IC Electronics	4142	873	21	5015	471	0	0	3671	8.4	4.8
.1.1	**Design**	373	82	22	455	373	0	0	0	3.6	3.6
.1.2	**Development and Prototypes**	249	154	62	403	46	0	0	203	2.3	0.6
.1.3	**Production**	3521	637	18	4158	52	0	0	3469	2.5	0.6
	Hybrids/Cables/Fanouts	1089	236	22	1325	75	185	0	829	5.1	3.2
.2.1	**Design**	0	0	0	0	0	0	0	0	0.0	1.6
.2.2	**Development and prototype fab**	81	15	18	95	0	0	0	81	0.0	0.1
.2.3	**Production**	1008	222	22	1230	75	185	0	748	5.1	1.5
	Module Assembly and Test	1064	328	31	1393	78	627	22	337	12.3	1.8
.3.1	**Design of assembly and test to**	120	40	33	159	78	42	0	0	1.1	0.7
.3.2	**Development and prototypes**	111	25	23	137	0	79	0	32	0.9	0.0
.3.3	**Production**	833	263	32	1097	0	506	22	305	10.3	1.1

U.S. ATLAS
WBS Summary Cost Estimates

Funding Source: All **Funding Type:** Project

Institutions: All

WBS Other Number	Description	Base Cost	Cont Cost (k$)	Cont %	Total Cost	EDIA Labor	Mfg Labor	EDIA Matls	Mfg Matls	FTEs	FTEs Project
1.1.2	Silicon Strip System	5184	1064	21	6248	716	812	22	3634	26.4	10.9
1.1.2.1	IC Electronics	3031	499	16	3530	563	0	0	2468	9.0	5.9
1.1.2.1.1	Design	464	88	19	552	464	0	0	0	4.2	4.7
1.1.2.1.2	Development and Prototypes	436	25	6	461	46	0	0	390	2.3	0.6
1.1.2.1.3	Production	2130	387	18	2516	52	0	0	2078	2.5	0.6
1.1.2.2	Hybrids/Cables/Fanouts	1089	237	22	1326	75	185	0	829	5.1	3.2
1.1.2.2.1	Design	0	0	0	0	0	0	0	0	0.0	1.6
1.1.2.2.2	Development and prototype	81	15	18	95	0	0	0	81	0.0	0.1
1.1.2.2.3	Production	1008	222	22	1231	75	185	0	748	5.1	1.5
1.1.2.3	Module Assembly and Test	1064	328	31	1393	78	627	22	337	12.3	1.8
1.1.2.3.1	Design of assembly and test	120	40	33	159	78	42	0	0	1.1	0.7
1.1.2.3.2	Development and prototypes	111	25	23	137	0	79	0	32	0.9	0.0
1.1.2.3.3	Production	833	263	32	1097	0	506	22	305	10.3	1.1

U.S. ATLAS
WBS Profile Estimates

Funding Source: All **Funding Type:** Project
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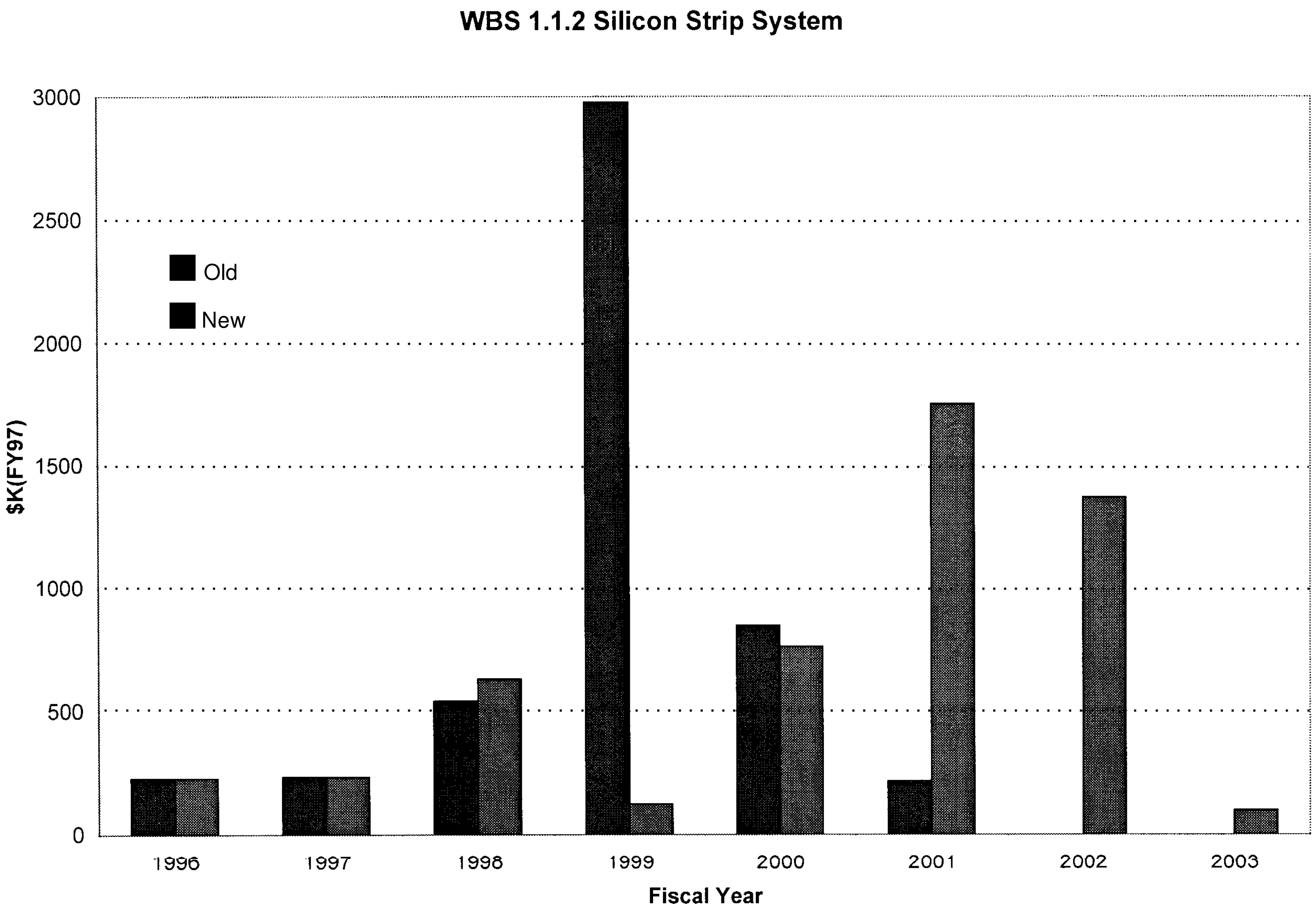
Institutions: All

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.2	Silicon Strip System	226	232	630	121	762	1749	1369	95	0	0	5184
1.1.2.1	IC Electronics	226	193	432	65	524	1072	518	0	0	0	3031
1.1.2.1.1	Design	88	144	169	63	0	0	0	0	0	0	464
1.1.2.1.2	Development and Prototypes	138	49	247	2	0	0	0	0	0	0	436
1.1.2.1.3	Production	0	0	16	0	524	1072	518	0	0	0	2130
1.1.2.2	Hybrids/Cables/Fanouts	0	38	42	0	119	451	408	31	0	0	1089
1.1.2.2.1	Design	0	0	0	0	0	0	0	0	0	0	0
1.1.2.2.2	Development and prototype	0	38	42	0	0	0	0	0	0	0	81
1.1.2.2.3	Production	0	0	0	0	119	451	408	31	0	0	1008
1.1.2.3	Module Assembly and Test	0	0	155	56	119	227	444	64	0	0	1064
1.1.2.3.1	Design of assembly and test	0	0	36	0	84	0	0	0	0	0	120
1.1.2.3.2	Development and prototypes	0	0	79	33	0	0	0	0	0	0	111
1.1.2.3.3	Production	0	0	41	23	35	227	444	64	0	0	833



WBS 1.1.2 Silicon Strip System
3000
2500
2000
1500
1000
500
0
$K(FY97)
Old
New
1996
1997
1998
1999
2000
2001
2002
2003
Fiscal Year