WBS 1.1 Silicon Subsystem

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(LBNL)

DOE/NSF Review
October 1998

WBS 1.1 Institutions

SUNY Albany
UC Berkeley/LBNL
UC Irvine
University of New Mexico
University of Oklahoma/Langston Univ.
UC Santa Cruz
University of Wisconsin

Ohio State University has joined ATLAS and would work on the Pixel System(WBS 1.1.1)

Deliverables - Goals

1.1.1 Pixel System(Preliminary)

- 1.1.1.1 Mechanics - design, assemble and install disk system(100%)
- 1.1.1.2 Sensors - design(30%) + procure and test 250 wafers(20%)
- 1.1.1.3 Electronics - design(40%)+procure and test 8500 ICs(25%)
- 1.1.1.4 Hybrids - design, fabricate, test(25%)
- 1.1.1.5 Modules - design, fabricate and test disk modules(100%)

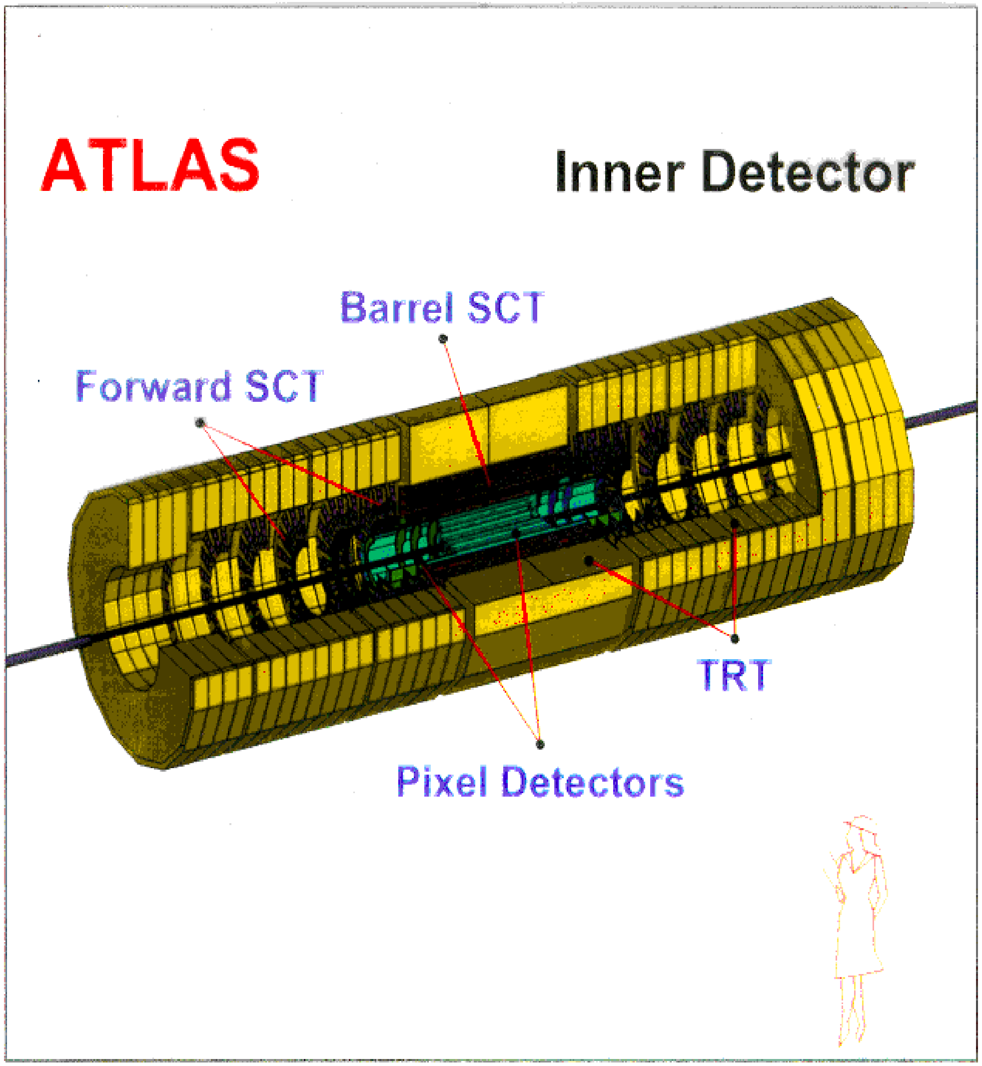
1.1.2 Silicon Strip System

- 1.1.2.1 Electronics - design(25%)+procure and test ICs(50%)
- 1.1.2.2 Hybrids - barrel design (100%) + procure all needed for US modules
- 1.1.2.3 Modules - deliver 670 modules(15%)

1.1.3 Read-out Drivers

- Test beam support - pixel support boards(3 generations), DSP modules(50) + preprototype RODS(16)
- Design, fabricate, test and install pixel (100%) and SCT(75%) RODs.

No major changes since February review



Summary Status

- **1.1.1 Pixel System**
  - Very substantial technical progress made in all areas
  - Pixel Technical Design Report completed(May 30)
  - LHCC approved
  - Detailed schedule and resources developed for already approved pre-baseline R&D funding

1.1.2 Silicon Strip System

- Significant delay in completion of development of integrated circuits => delays in all other items
- Revised schedule and resources developed

1.1.3 Read-Out Drivers

- Test beam support provided on schedule and on budget
- Preprototype ROD development on schedule and on budget
- More detailed schedule developed

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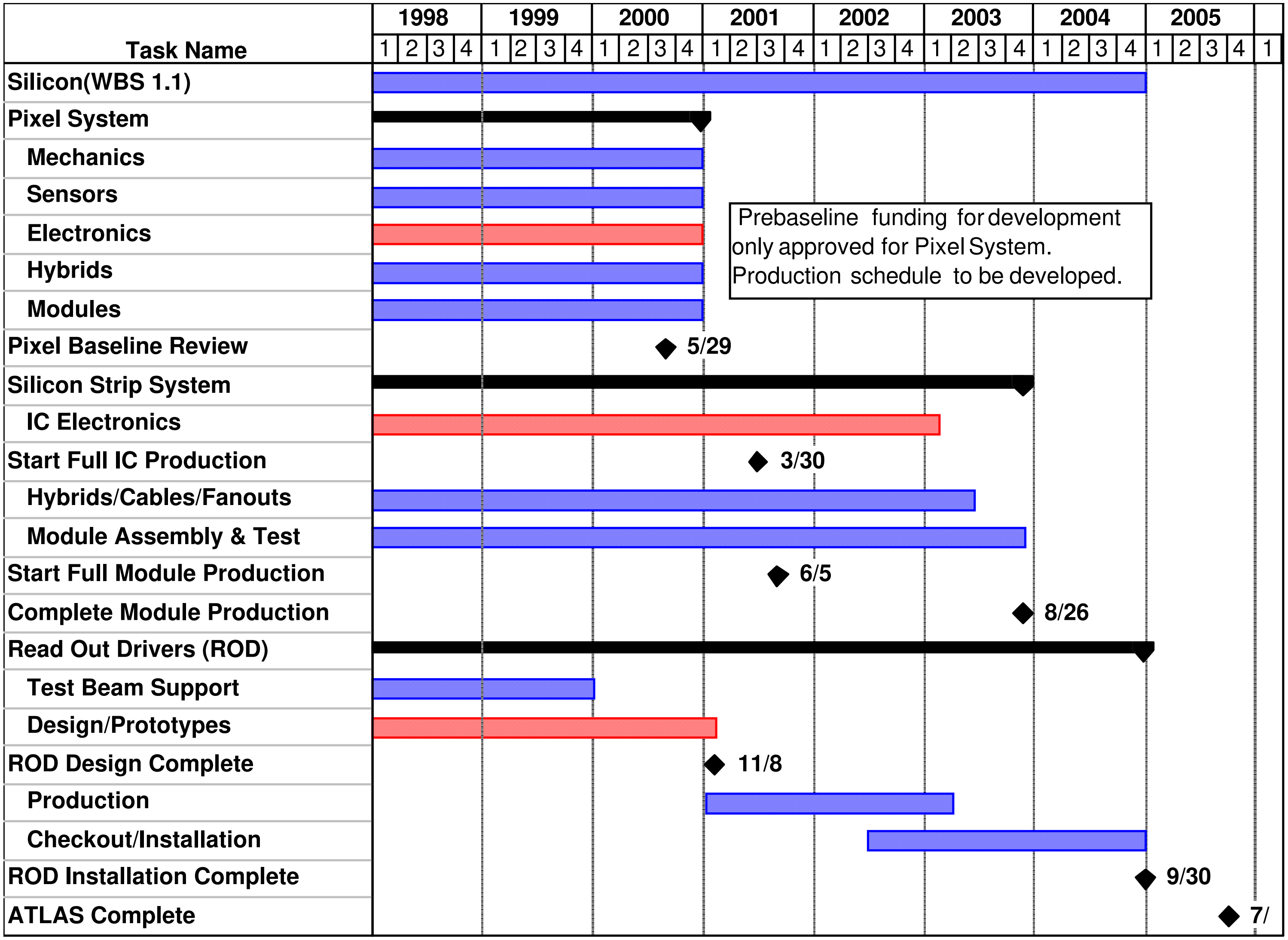
WBS 1.1 Summary Schedule



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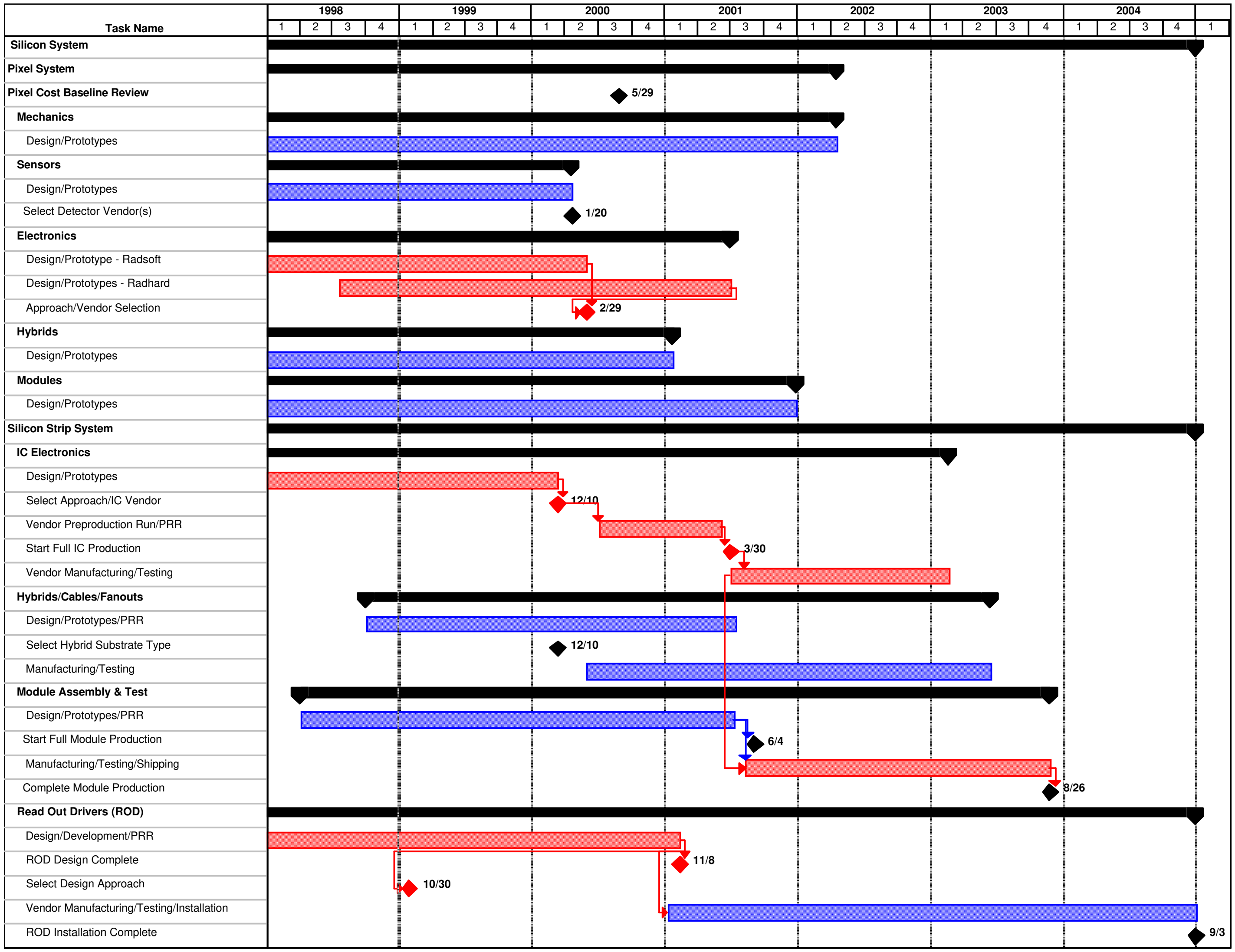
WBS 1.1 Summary Schedule



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WBS 1.1.3 Read-Out Drivers

- Test beam support
  - Digital Signal Processor(DSP) modules for both pixel and silicon strip laboratory and test beam measurement.
    - Ongoing for last two years.
    - Last 24 modules were received in June and have been tested
    - Available to collaboration
  - Pixel support
    - First generation test chips supported by custom test boards - this work is complete
    - Custom VME boards for most recent, full-scale prototype pixel electronics - initial work completed for test beam use this year.
    - These boards are part of dedicated, PC-based test system developed. Under high demand as standard. Additional boards under fabrication.

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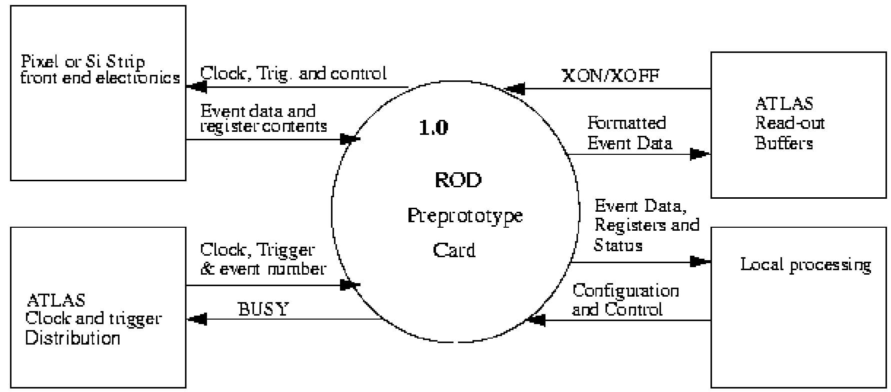
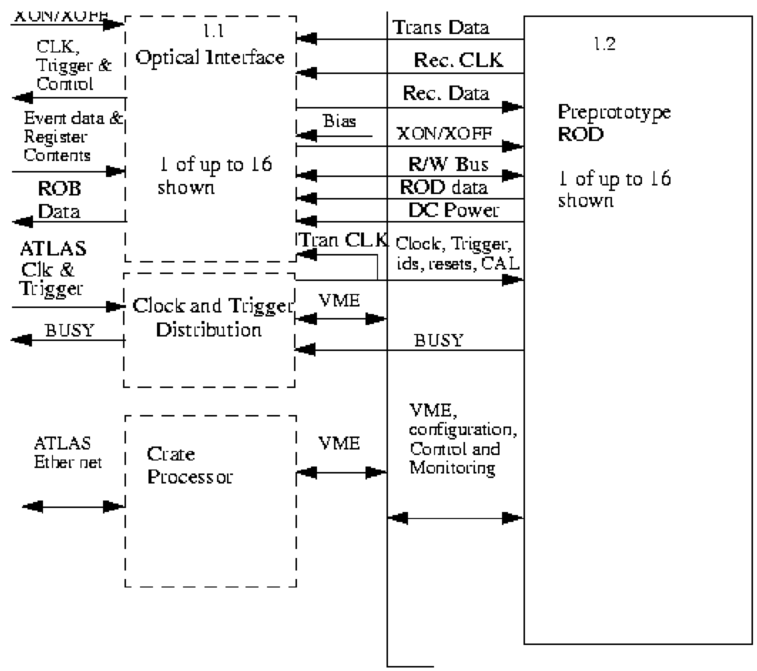
WBS 1.1.3 Read-Out Drivers

- **Preprototype(ROD99)**
  - **Requirements review completed.**
  - **Essential model reviewed**
  - **Preliminary interface documents reviewed**
  - **Implementation models underway and reviewed**
    - **DSP solution**
    - **FPGA solution**
  - **Compare and select by end October**
  - **Build first 3 modules by April 1999**





WBS 1.1.3 Read-Out Drivers

- **Cost and Schedule**
  - **Test beam support**
    - **On budget**
    - **Just in time-delivery of pixel test components, but worked well**
    - **Minor delays in DSP delivery => no impact**
  - **ROD99**
    - **On budget**
    - **Design milestones met so far(PDR was ahead of schedule)**
    - **Delays in silicon strip system relieve pressure to fabricate many ROD99s for next summer.**
    - **Increased emphasis on ROD99 as ROD prototype and less on use in SCT or pixel systems tests**
  - **ROD Design and Production**
    - **More detailed schedule developed.**
    - **No changes in estimated cost - need experience of ROD99.**

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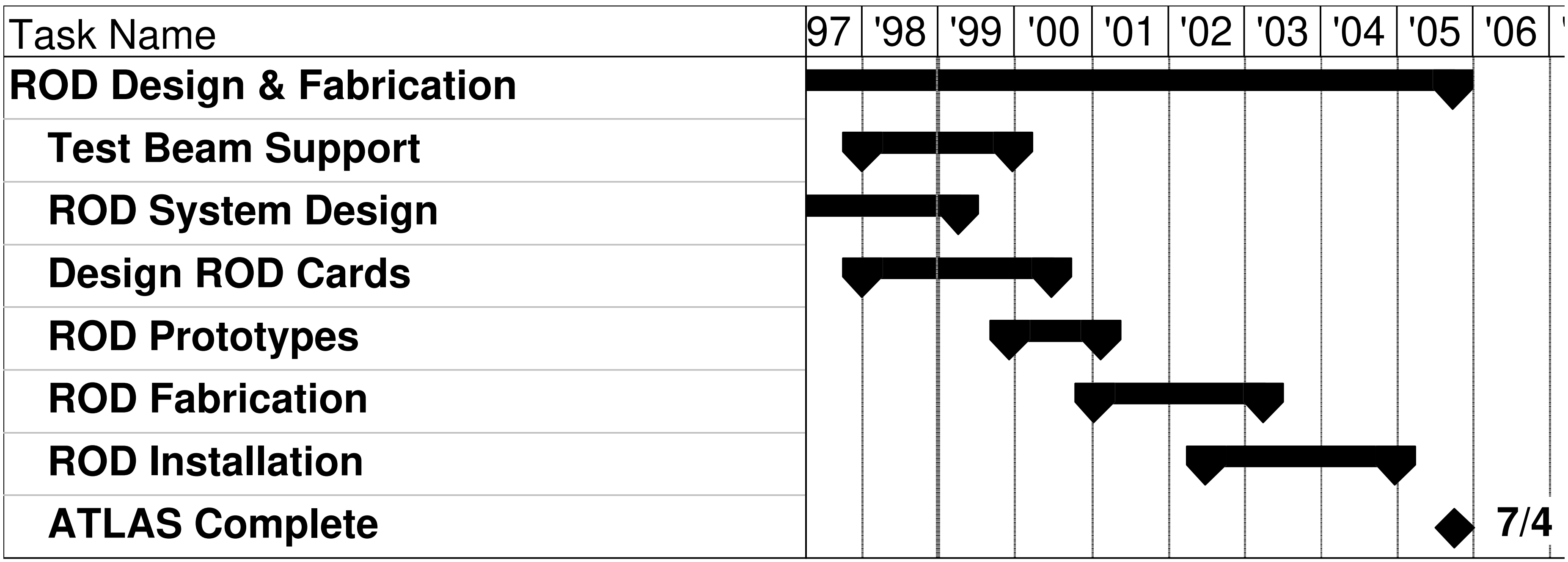
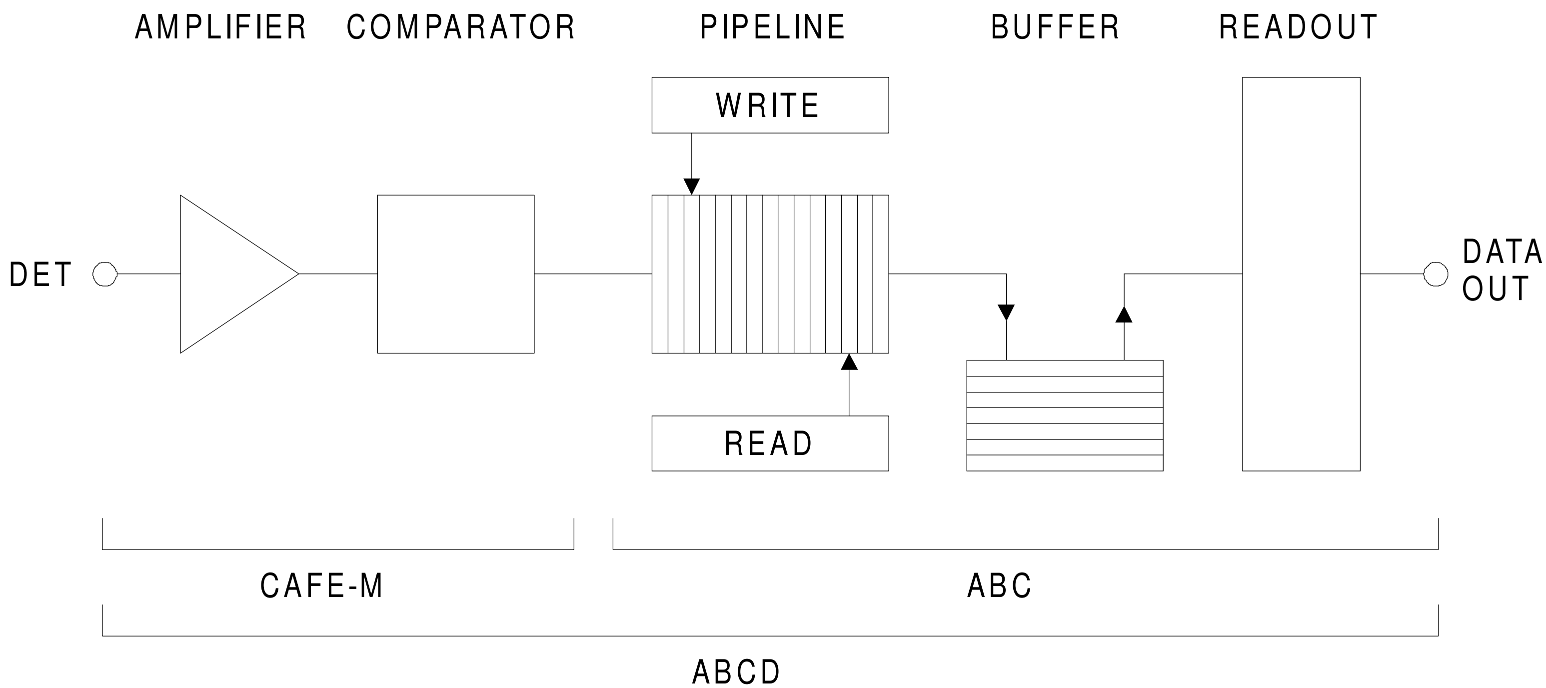
WBS 1.1.3 Read-Out Drivers - Schedule



WBS 1.1.2.1 Silicon Strip IC Electronics

- **Two rad-hard solutions under development**
  - **CAFÉ-M(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips. This is the US cost baseline.**
  - **ABCD(BiCMOS from Temic) - 1 chip. Expected to be significantly cheaper than cost baseline.**



WBS 1.1.2.1 Silicon Strip IC Electronics

- **CAFÉ-M**
  - Fully functional before irradiation
  - Small design error found after irradiation => increased threshold dispersion => threshold increase from about 1 fC to 1.2 fC after lifetime dose.
  - Error understood, corrected design well underway at Santa Cruz. Final design review completed.
  - Polarity also must be reversed for p-on-n detectors.
- **ABC**
  - Significant design flaws. Not operational(major error in clock reception).
  - Some few ICs(now about a dozen) have been repaired to a usable extent by focussed ion beam surgery.
  - Believe we have found all design errors.
  - Repaired chips functional after irradiation
  - Have mounted repaired die along with CAFÉ-M on hybrids and tested successfully so far(including after irradiation)
  - Design was done at RAL. Added design manpower at LBNL(no previous involvement) to speed up process(doubled manpower). Support for this manpower was provided by an approved baseline change proposal(BCP).
  - Detailed status review complete.

WBS 1.1.2.1 Silicon Strip IC Electronics

- **ABCD**
  - Digital section nearly fully functional(minor errors and indication of insufficient speed margin in few blocks)
  - Major problems with analog section before irradiation. Large threshold dispersion. Unstable near operating threshold.
  - Source of poor analog behaviour not fully understood.
  - However, clear that bipolar aspects of DMILL process not fully established at Temic and that process monitoring not sufficient. Source of problems may be processing deviations
  - Major design change agreed to(threshold trim on each channel) to mitigate threshold dispersion even if process brought under control.
  - Working closely with vendor to improve process monitoring.
  - Redesign work underway largely at CERN but also some at LBNL, and expect CAFÉ-M designer at Santa Cruz to participate when CAFÉ-M is completed. US work also supported by BCP.
  - Preliminary status review complete
- **Bottom line**
  - Need second prototype runs for all three chips
  - Significant delay - see next page

WBS 1.1.2.1 Silicon Strip IC Electronics

Milestones	Old	New
Submit 2nd CAFÉ-M	----	10/30/98
Submit 2nd ABC	----	11/16/98
Submit 2nd ABCD	----	1/27/99
Complete fab of all 2nd chips	----	6/30/99
Select IC vendor	5/15/98	12/10/99
Start preproduction run	9/1/98	3/31/00
Release/start full production	5/3/99	3/30/01
Complete IC testing	3/1/01	11/21/02

- If 2nd prototypes are "preproduction quality", schedule could be shortened - but we are not assuming this.
- We have shortened the production fabrication period. IC vendors strongly prefer one year fabrication time.

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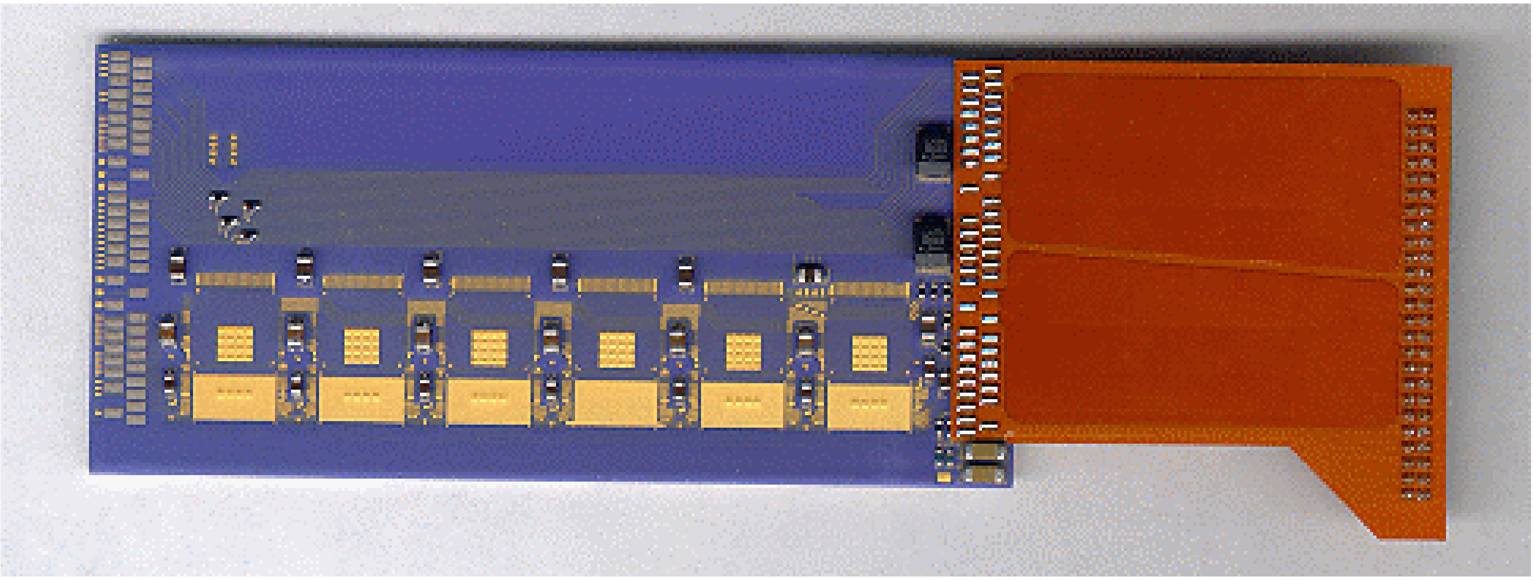
WBS 1.1.2.2 Hybrids

- Prototype beryllia hybrids designed, fabricated and tested.
- Issues: yield from vendor was less than hoped and some bowing was observed.
- Cost of lower yield was absorbed by vendor allowing us to make another prototype run in future(for 2nd prototype ICs) with existing funds to resolve these issues.
- Schedule is tied to IC electronics schedule. Essential for IC testing. No difficulties in meeting required schedule.



WBS 1.1.2.3 Modules

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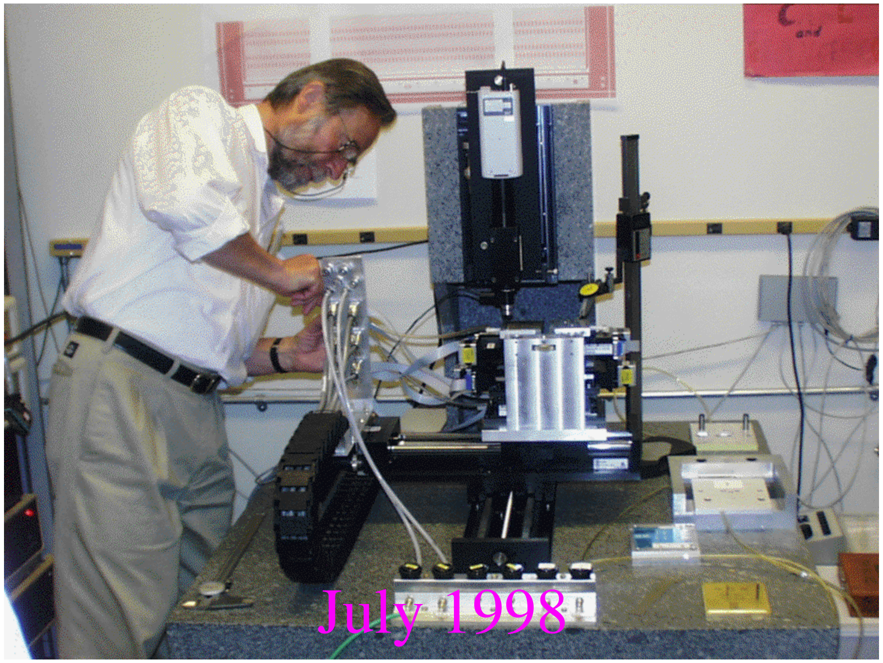
- Tooling and equipment for module assembly is largely in place at LBNL, although some aspects(primarily related to measurements after assembly) will appear only in FY99.
- Dummy parts ready and have started dummy module fabrication to debug system. First dummy modules fabricated.
- Planning is underway for “clean room” facilities.
- The module effort is on budget and there is considerable slack in the early part of the schedule, given delay in the IC electronics



WBS 1.1.2 Silicon Strips - Impact of Delay

- **Cost impact of delay**
  - A baseline change proposal was submitted and approved for adding $65K in FY98-early FY99 for additional IC design manpower at LBNL and $30K in FY99 at UCSC.
  - A baseline change proposal was submitted in August for the US contribution to the 2nd prototype round IC fabrication.
  - Hybrid and module costs have not been affected by the delay and are not expected to be affected.
- **Schedule delay mitigation possibilities under study**
  - Shorten module construction time(eg. double shifts)
  - Remove slack from installation/checkout schedule
  - Revise installation schedule(for all of Inner Detector) to allow later arrival of SCT
  - Some or all of the above

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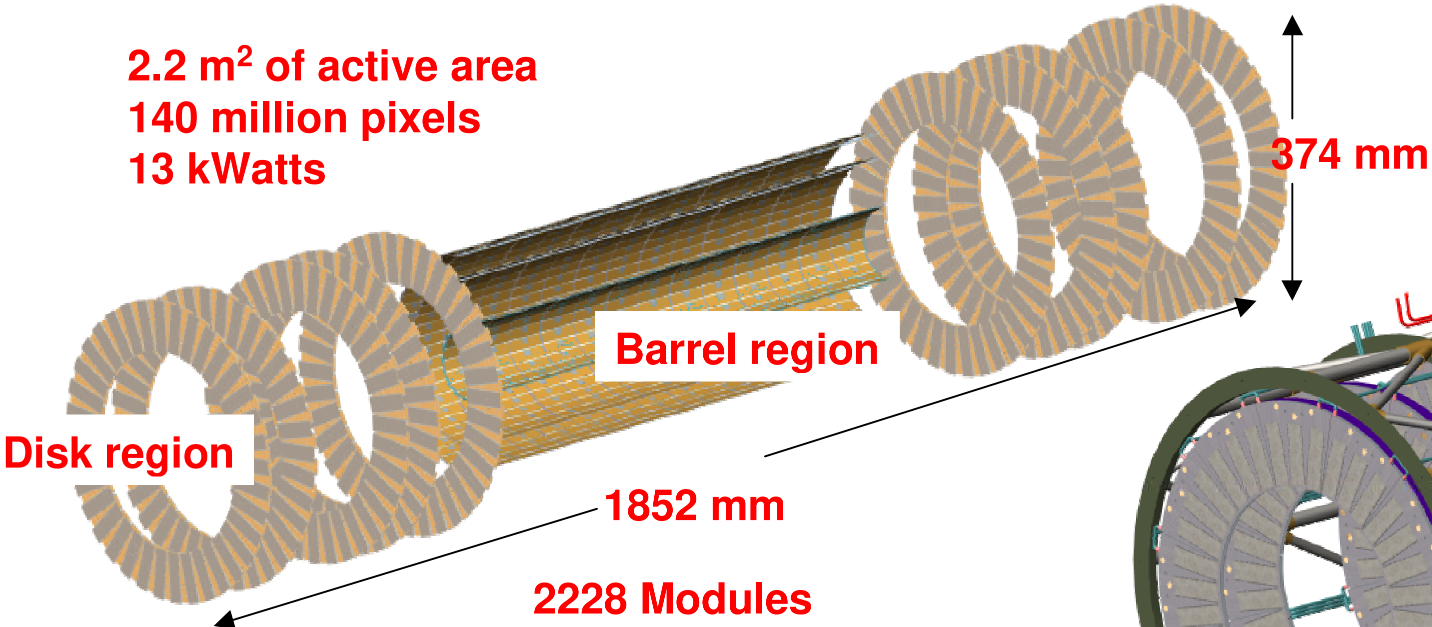
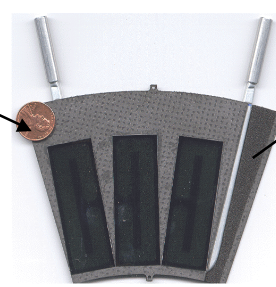
WBS 1.1.1 Pixel System

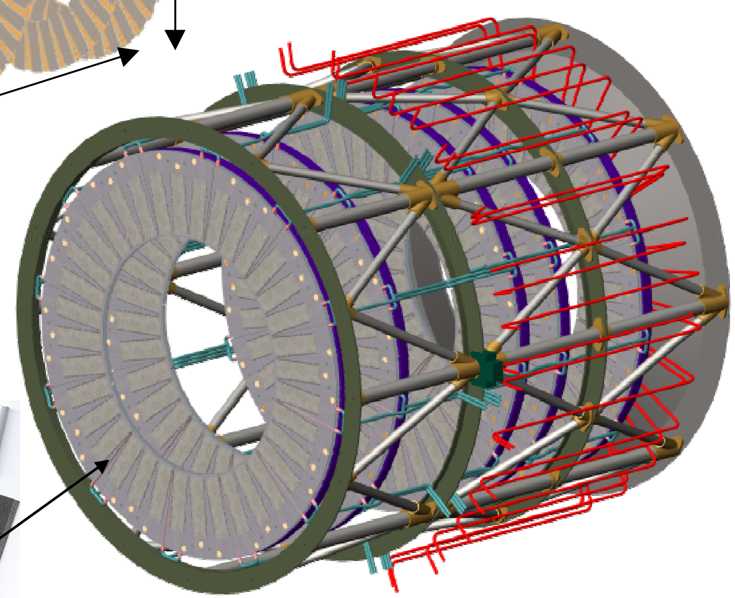
- **Pixel Technical Design Report completed on May 30, 1998.**
- **LHCC review July 7, 1998. LHCC approval in September.**

2.2 m^2 of active area
140 million pixels
13 kWatts



2228 Modules
118 Barrel Staves
120 Sectors





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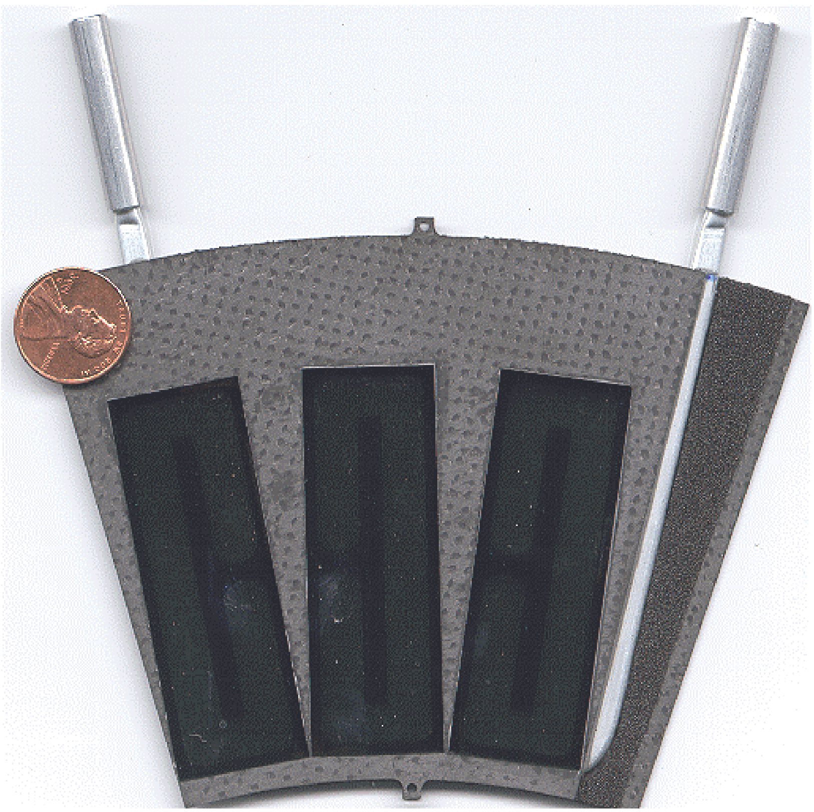
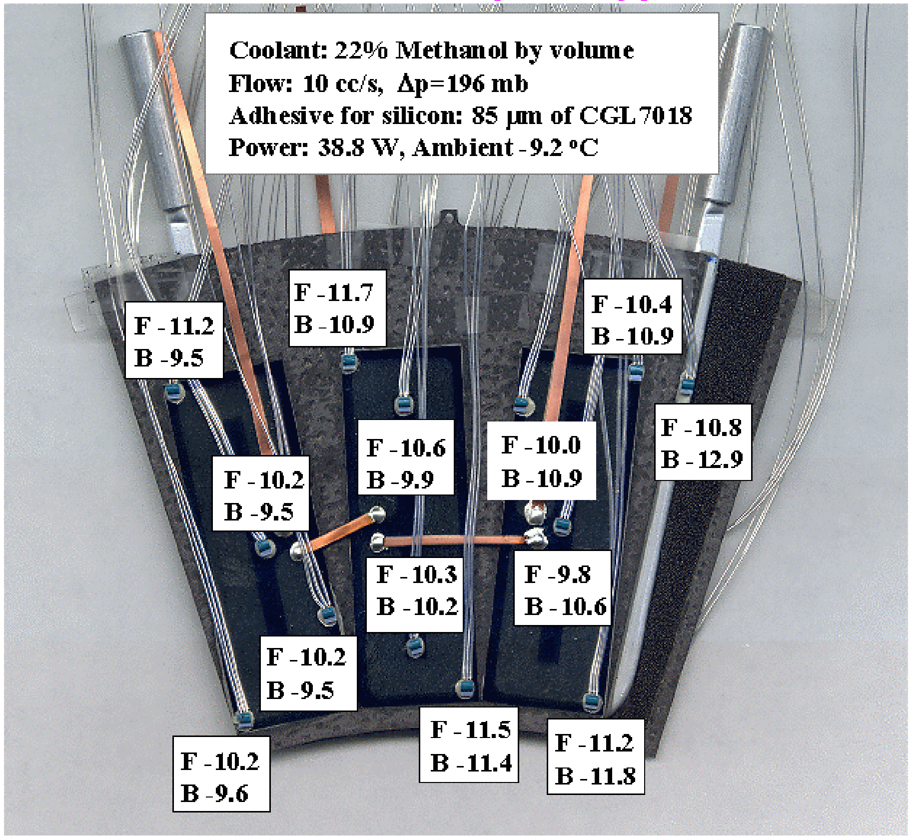
WBS 1.1.1.1 Pixel Mechanics

- **Technical Status - Disks**
  - **Multiple prototype sectors constructed and tested successfully**
  - **Prototype tests with evaporative cooling are better than specs.**
  - **Thermal specifications met and stability goals appear possible**
  - **Moving ahead now to many-sector fabrication and full-disk prototype**





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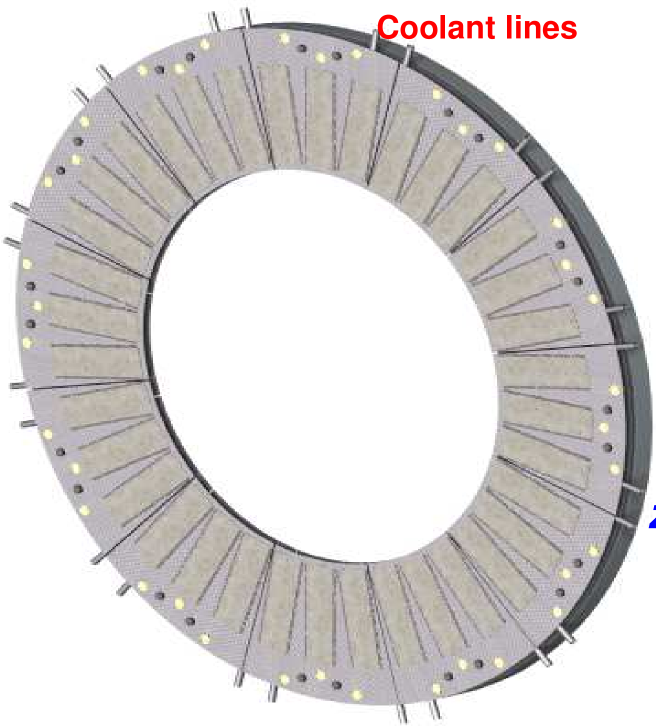
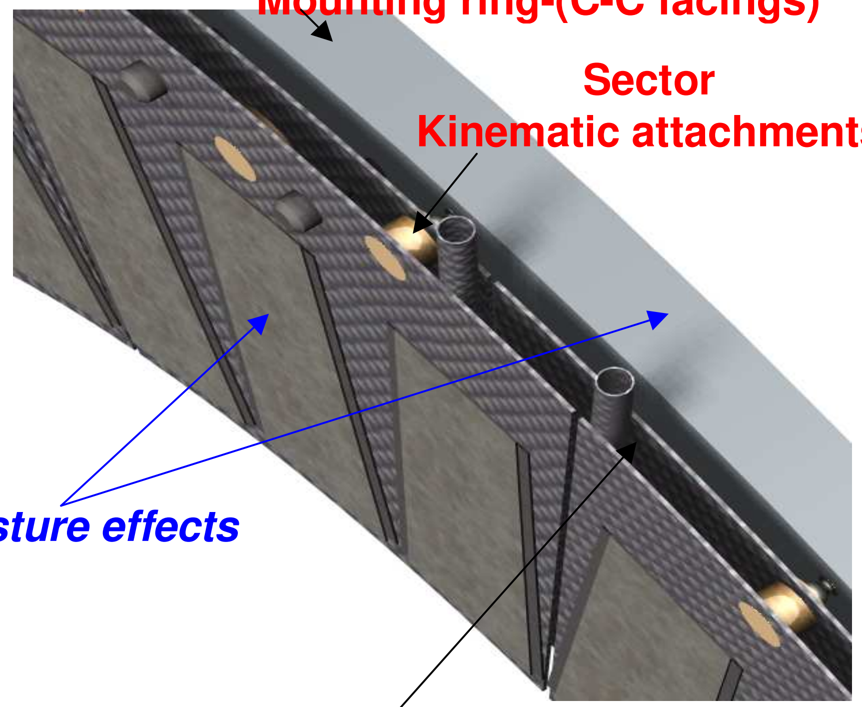
WBS 1.1.1.1 Pixel Mechanics

Composite Materials-Sandwich Construction
Carbon-Carbon Materials

Disk with 12 Sectors



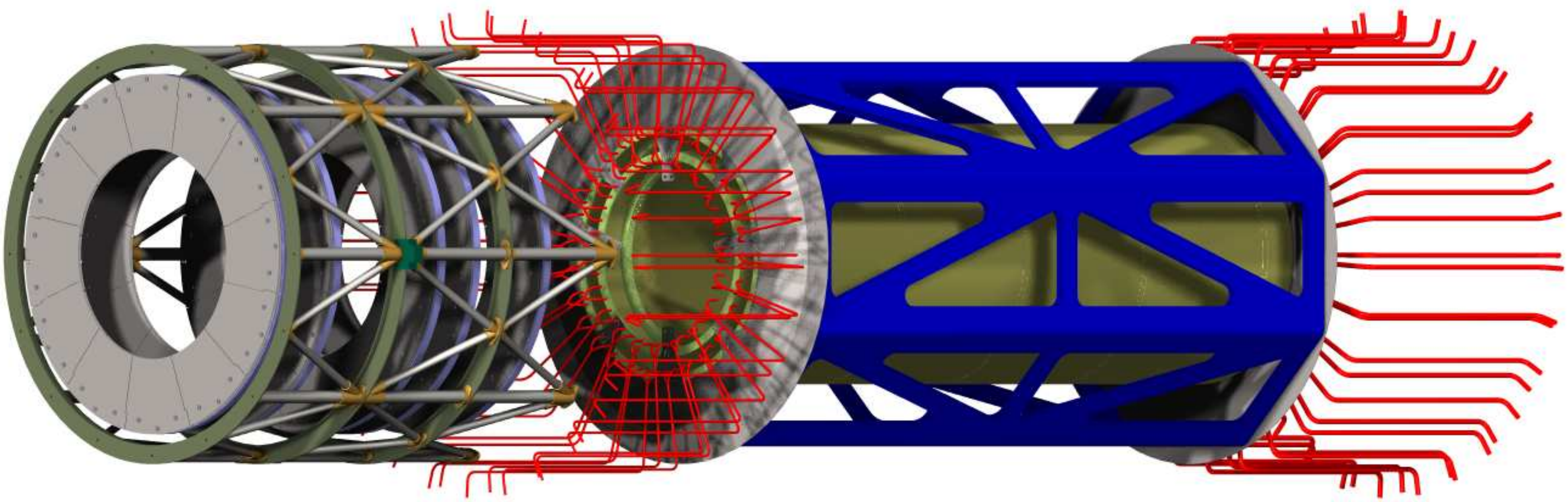
Sector support, cantilevered
from outer edge



Carbon-Carbon thermostructure
(fiber core omitted)

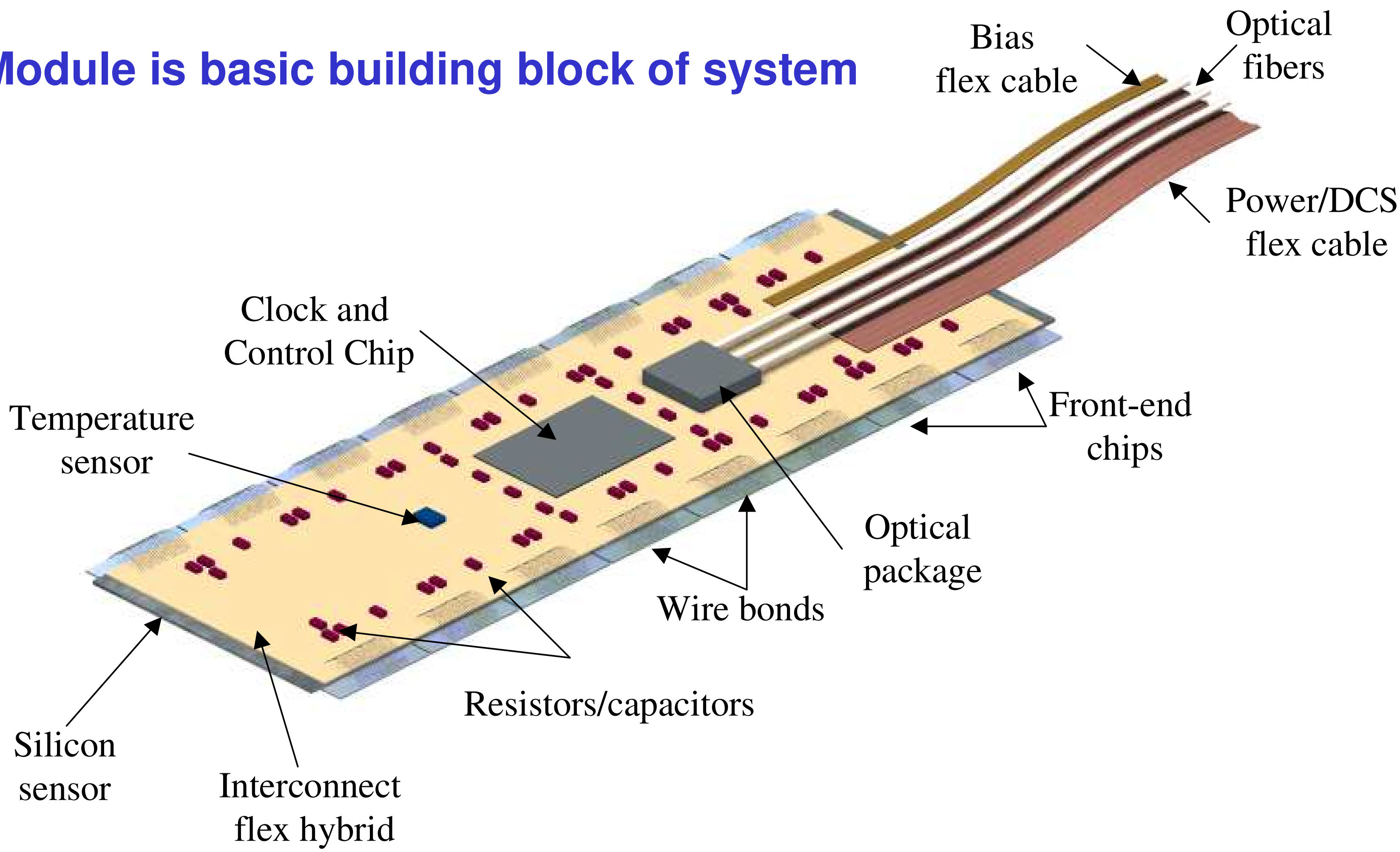
WBS 1.1.1.1 Pixel Mechanics

- **Technical Status - Structure and Integration**
  - **LBNL engineer at CERN since Dec. 1997 as lead for integration(50% CERN supported).**
  - **Multi-national contract completed with Hytec, Inc for conceptual design of support structures.**
  - **Detailed 3D model and preliminary finite-element-analysis completed**
- **Cost**
  - **On budget but rely heavily on SBIR Phase II(2 of them) for some design, prototypes and measurement(TV holography)**
- **Schedule**
  - **OK so far.**



Pixel Module

Module is basic building block of system



WBS 1.1.1.2 Pixel Sensors

- **Technical Status**
  - Fabrication of first round of full size prototypes was completed nine months ago with two vendors(CIS in Germany and Seiko in Japan).
  - Wafer probing completed
  - Extensive lab and beam tests with electronics, including with irradiated detectors - see beam test results summary
- **Cost**
  - On budget(in US)
- **Schedule**
  - Seiko decided to get out of business
  - Additional first prototypes(with few design changes) ordered now from CIS to meet need for more testing - more parts, particularly irradiated
  - Some delay in starting 2nd prototype design, but first prototypes close to satisfying requirements.
  - No impact on overall schedule - electronics critical path item.
  - Preproduction, then production follows 2nd prototypes

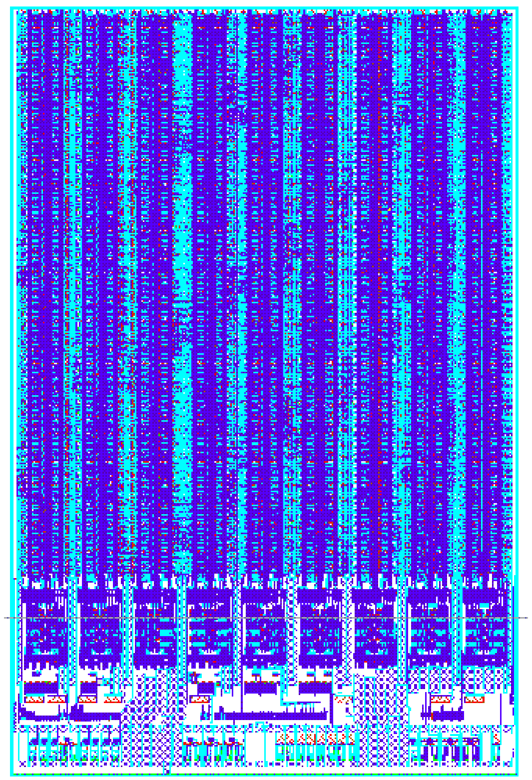
WBS 1.1.1.3 Pixel Electronics

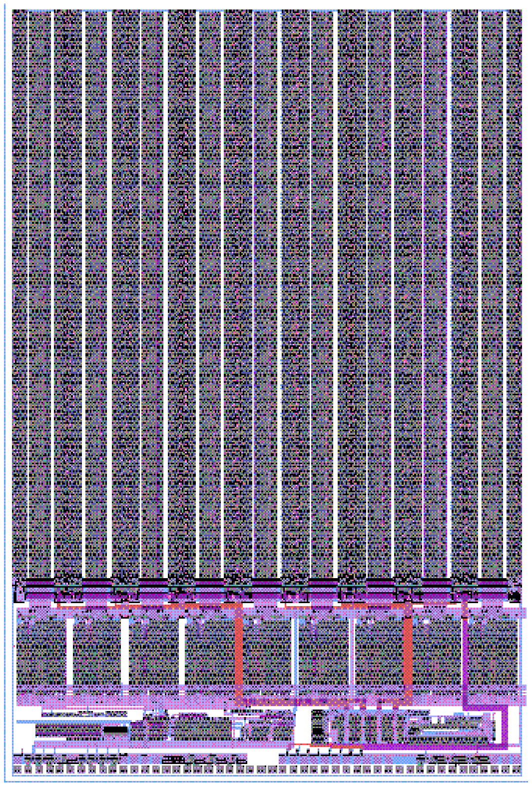
- Technical Status
  - Pre-prototype program completed successfully by end 1997.
  - Full-scale prototypes fabricated in rad-soft technologies this year and tested extensively. Different design approaches. FE-A, FE-B, FE-C.
  - FE-A(AMS -> Temic/DMILL). First delivery in February. Functional. Yield about 5%. Second run delivered in July(all CMOS version FE-C). Yield appears higher, about 80%.
  - FE-B(HP -> Honeywell Sol). First delivery in April. Functional. Yield about 93%.
  - MCC(AMS -> Temic/Honeywell). First delivery in July. Functional. Yield about 80%.
  - Unified design approach adopted for rad-hard design FE chips => all working on same design to be implemented in the two rad-hard processes
- Cost
  - Costs for future prototype fabrication understood. Combined international funding in place for prototypes in 1999.
- Schedule
  - Critical path items
  - Two rad-hard prototype rounds in schedule before preproduction

WBS 1.1.1.3 Pixel Electronics

- **FE-A and FE-B bonded to prototype detectors, including irradiated detectors.**
  - **18x160 pixels(50x400 micron pixel size). Complete analog and digital to ATLAS specs. Final goal is 50x300 micron pixel.**
  - **Essential requirements met(efficiency, time resolution, noise, threshold,….)**
  - **Multiple test beam runs at CERN. Extensive lab tests. Principle established.**

FE-A



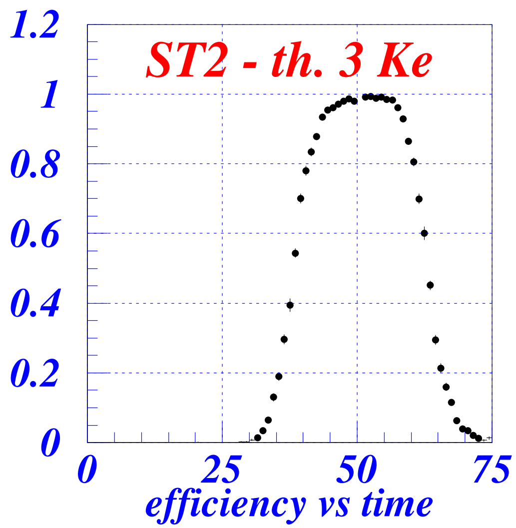


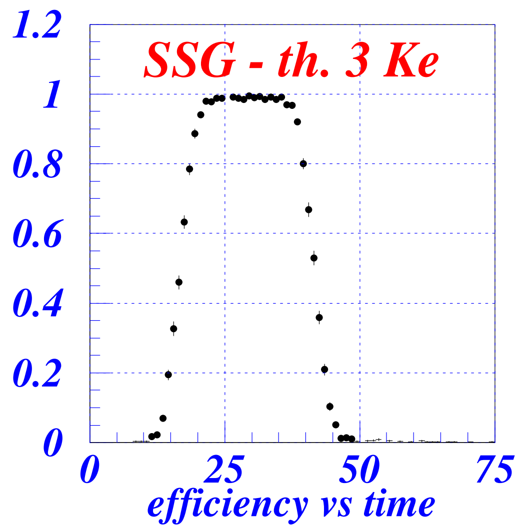
FE-B

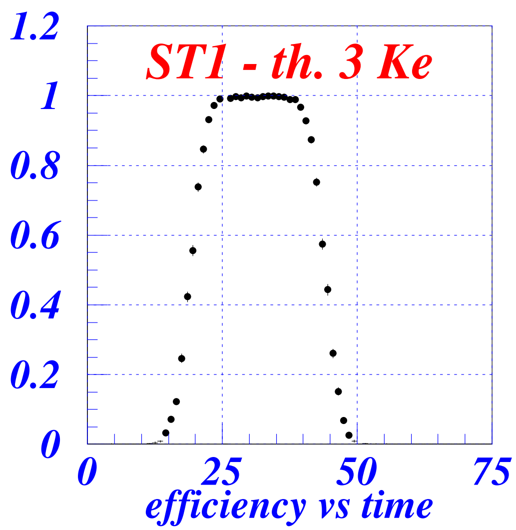
Lab and Test Beam Results - Summary

- Extensive lab tests and three test beam runs have occurred this year. Very successful.
- Highlights
  - Dozens of single-chip/detectors have been operated successfully with multiple detector types and front-end ICs
  - 16 chip modules have been operated successfully
  - Detectors irradiated to lifetime fluence expected at LHC(10^{15}) have been read-out in a test beam with efficiency near 100%
  - Operation below full depletion voltage demonstrated
  - Preferred detector type identified in these studies
  - Timing performance needed to identify bunch crossings has been demonstrated.
  - Operation at thresholds 2,000-3,000 electrons demonstrated
  - Threshold uniformity demonstrated.
  - Spatial resolution as expected
- Conclusion
  - Proof-of-principle of pixel concept successful

Lab and Test Beam Results - Examples







Efficiency vs time of particle passage for three different detector types before irradiation. The efficiency is near 100% in each case and there is a substantial plateau, indicating good timing performance of the electronics

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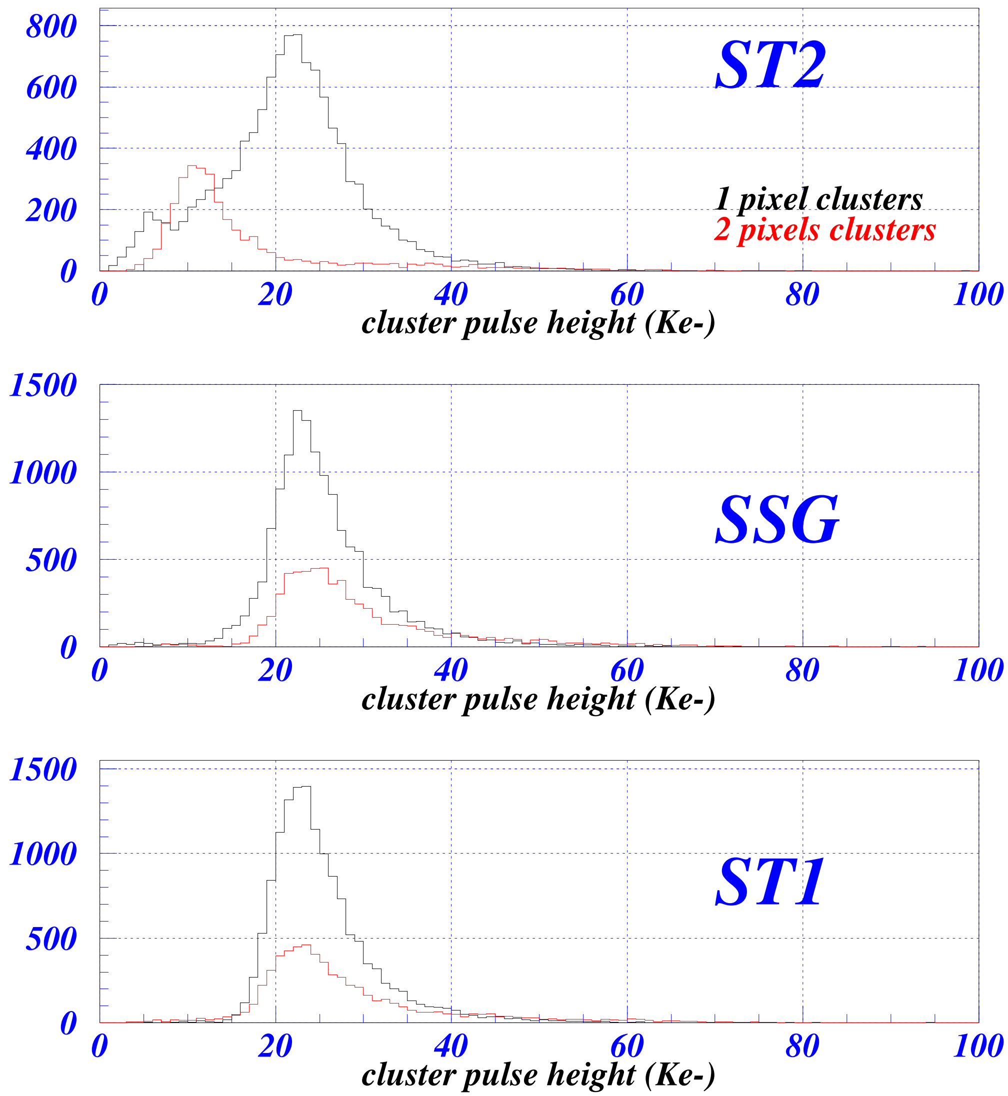
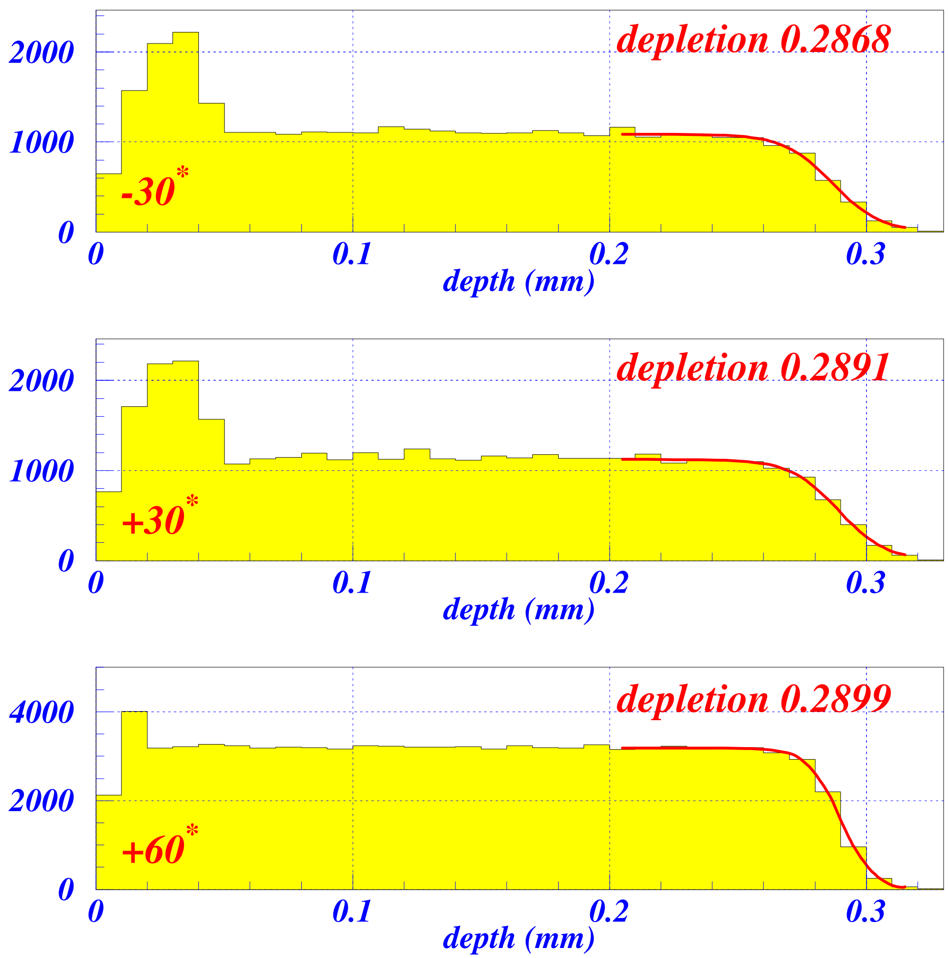
Lab and Test Beam Results - Examples



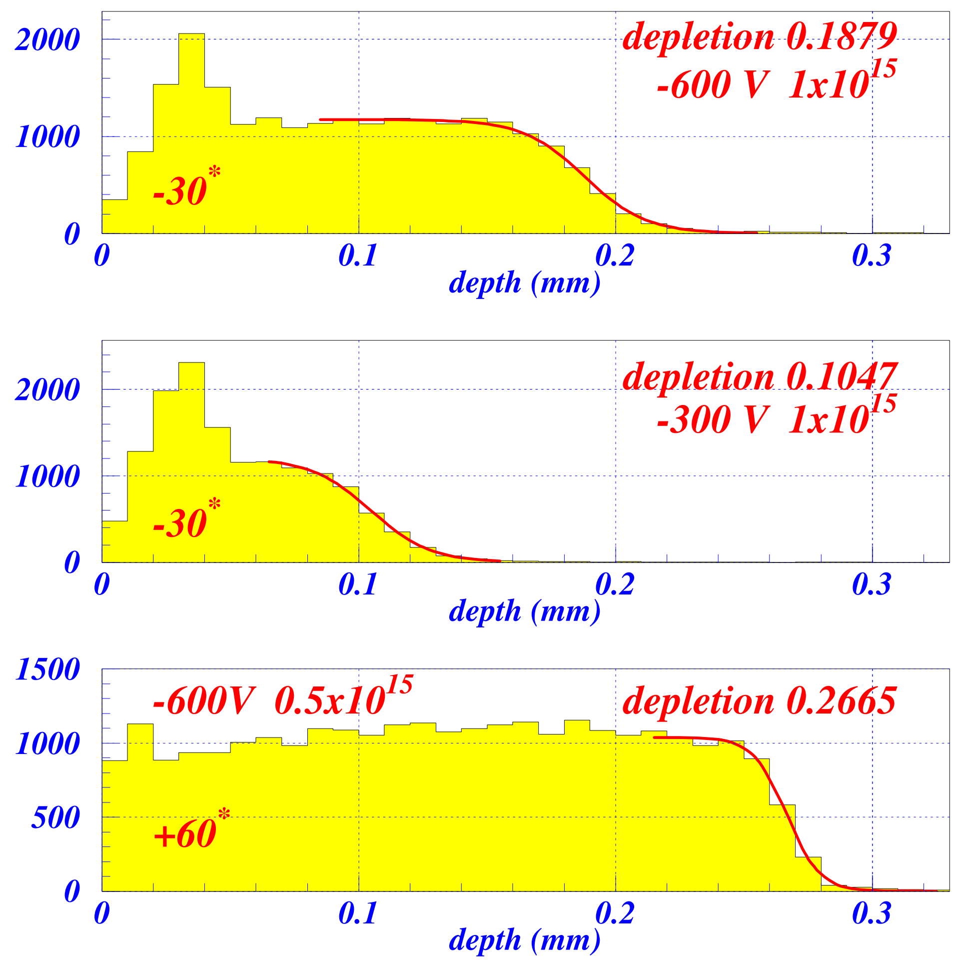
Charge distributions for three detector types. The difference between ST2 and the others is indicative of small charge losses, which has guided us in the design of additional prototype detectors under fabrication.

Lab and Test Beam Results - Examples

Not irradiated - depletion depth

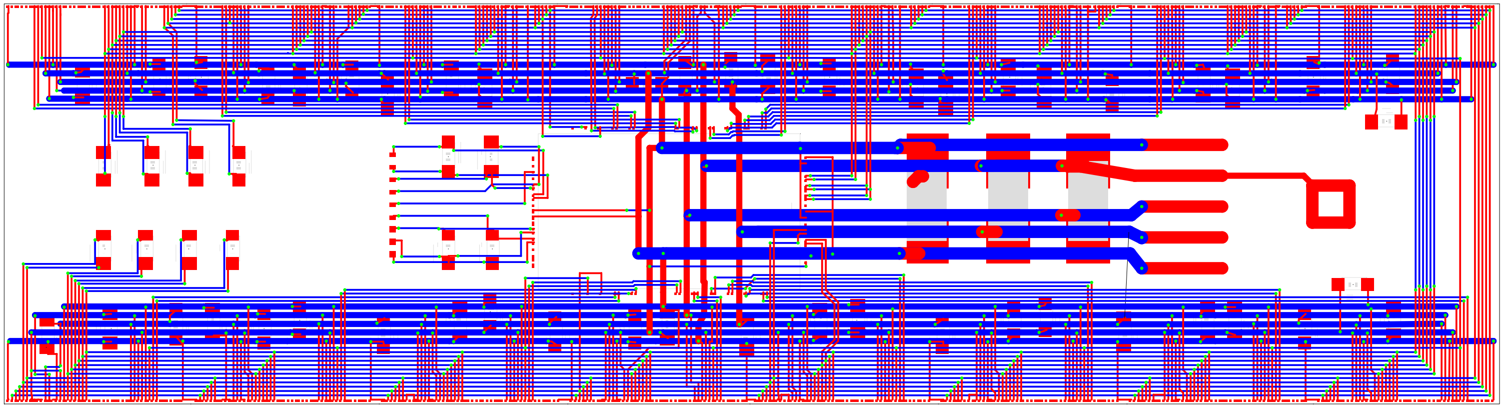


Irradiated - depletion depth



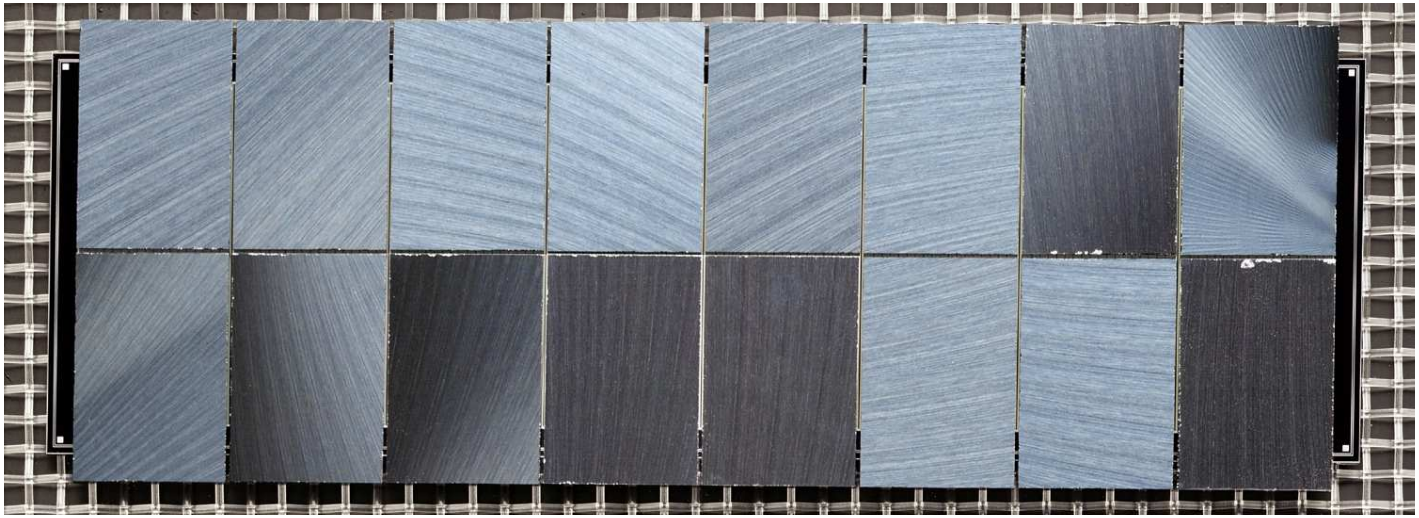
WBS 1.1.1.4 Pixel Hybrids

- **Technical Status**
  - Prototype design of flex hybrid completed by Oklahoma
  - First prototypes fabricated at CERN(in Cu on kapton)
  - Testing underway in US and in Europe
  - Contract in place with GE to have additional vendor, will begin fabrication after first prototypes from CERN are understood(can make small design changes)
- **Cost**
  - On budget
- **Schedule**
  - Design completed few months later than hoped.
  - Not able to meet test beam schedule this year. However, laboratory tests(including with sources) are adequate to assess performance
  - Three prototype rounds included in our schedule



WBS 1.1.1.5 Pixel Modules

- **Technical Status**
  - Bump bonding has been successful with multiple vendors. Dozens of single chip-detector assemblies work. Indium and solder bumping works.
  - 16 chip modules assembled successfully with FE-B ICs(all ICs working after assembly)
  - Assembly of complete module prototypes(sensors bonded to electronics and flex hybrid but with electrical connections - no optical yet) is underway in Italy and the US.
- **Cost**
  - On budget
- **Schedule**
  - First prototype round now before hybrid-type selection
  - Two additional rounds included in schedule before preproduction



WBS 1.1.1 Pixel Schedule

- We have completely revised the pixel development schedule and milestones since February to match the approved pre-baseline funding.
- We believe the pre-baseline funding is adequate to complete the development needed to thoroughly understand production costs and schedule.
- Our proposed plan is to complete major vendor selections and most prototype rounds before a baseline cost review by June 2000. The key point is to complete the baseline review in time to establish the FY01 budget.

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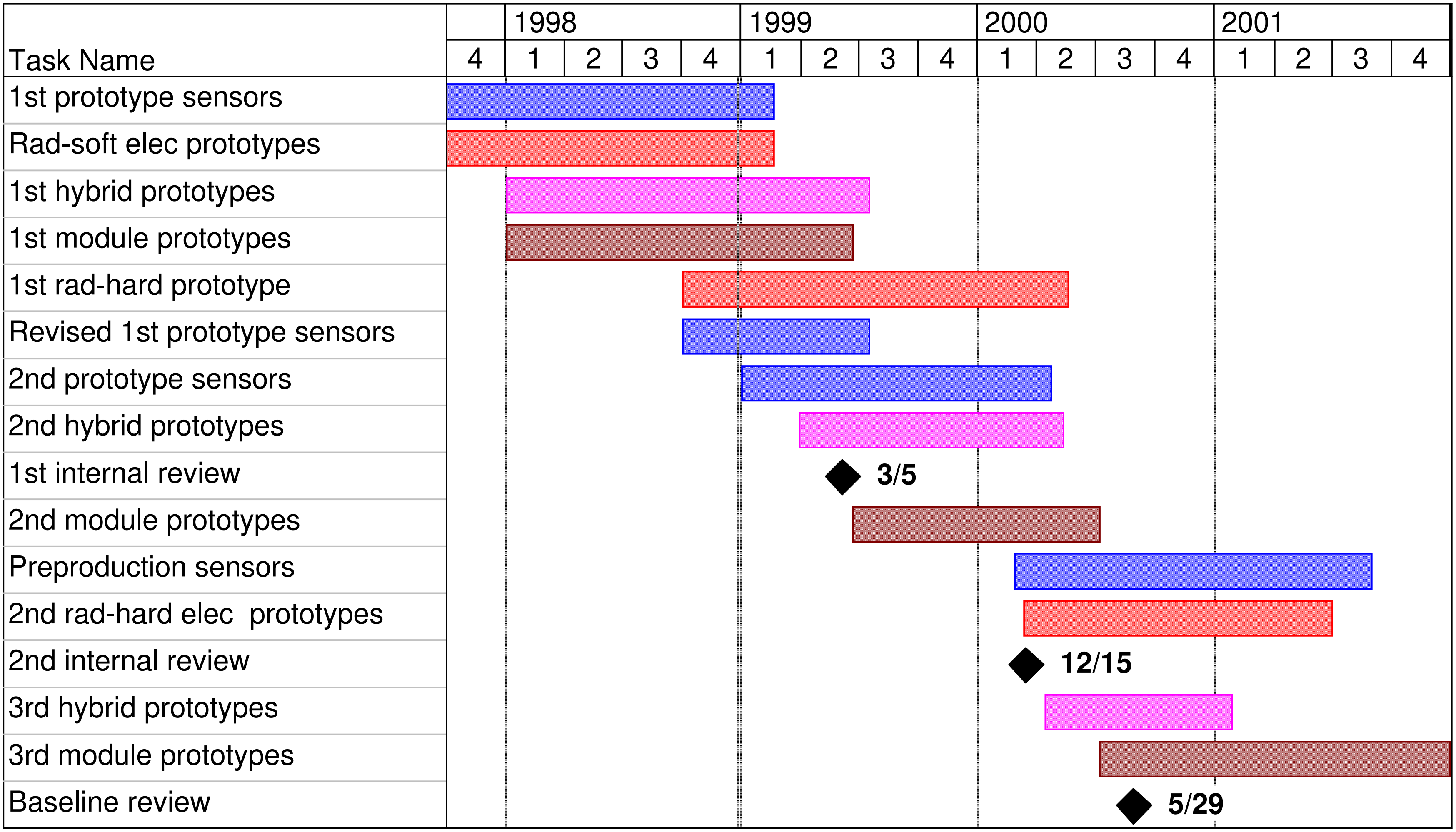
WBS 1.1.1 Pixel Schedule



Mechanics schedule not shown

Responses To February Review

- *Baseline the SCT and ROD deliverables at the initial project baseline scope proposed by U.S. ATLAS and outlined above in Section 3.1.2.*
  - Done
- *Provide 1.74 million of pre-technical baseline funding in FY1997 dollars, including contingency, for pixel R&D, in addition to the $0.84 million already allocated. This provides the requested funding to achieve baselining of the pixel subsystem.*
  - Done
- *Conduct a DoE/NSF baseline review of the pixel system in about one year, following approval of the pixel TDR and after schedules and final cost estimates are established. The U.S. ATLAS management should conduct an intermediate internal review in six months, using the TDR and preliminary costing information.*
  - It is our current proposal to have a baseline review of the pixel system before September 1, 2000. The rate of technical progress in the pixel system has been very rapid and the pixel TDR was completed by May 30, 1998. The pixel TDR provides a comprehensive description of the current state of the pixel detector development and preliminary plans for production. However, substantial developments in implementing rad-hard ICs and constructing prototype modules, the fundamental building block of the system, are only now in progress. And the responsibilities within the collaboration for final design and fabrication of the mechanical systems have not yet been set. It will be possible to formulate a more accurate cost estimate and schedule when these developments, including beam tests, are completed by Fall of 1999. This would then lead to selection of vendors for all of the major components by early 2000. The already-approved pre-baseline funding(including contingency) should be adequate to maintain the appropriate rate of development through FY00.
  - The pixel TDR was reviewed by the LHCC on July 7-9, 1998. Although no formal decision was taken at the July review, the comments from the referees were very positive. Additional reviews will occur in September 1998, and approval by the LHCC is anticipated to occur by this time. Test beam runs have occurred in April, June and July-August 1998. Prototype module fabrication has started but tests of these modules will not be completed until November-December 1998, leading to a choice of module construction technique by early 1999. Thus a reasonable time for a first internal review would be by March 1999. This review will be conducted by the U.S. ATLAS Project Office and will include external reviewers.

Responses To February Review

- *Work with the international SCT and ATLAS management to develop effective procedures for component procurement and distribution of materials to assembly sites; procurement delays at CERN in the rad-hard ICs and SCT module components or inefficient distribution of components to assembly sites could result in delays and cost increases, reducing the final U.S. deliverables.*
  - As a result of significant delays in the completion of prototype development of the rad-hard ICs and some delays in the development of the detector program, very little progress has been made to develop detailed procurement plans. Progress has been made to develop a Frame Contract from CERN for procurement of the rad-hard ICs, but the formal process at CERN is a very long one. This contract is not yet in place, but is expected to be in place by April 1999, well in advance of the time necessary for procurement of preproduction rad-hard ICs. Procurement plans for other major elements of the SCT have been formally initiated in the last few months, but are not yet complete.
- *Complete a critical path analysis of the schedule for the silicon trackers by the U.S. ATLAS Project Office as soon as possible.*
  - A revised, and more detailed, schedule for the SCT system has been completed. The critical path item leading up to and through early module construction is the design, fabrication and testing of the rad-hard ICs. An analysis of the critical path after the early phase of production module testing remains to be completed. More experience in module construction is needed to identify the critical path during this phase.
  - A preliminary schedule for the development of the pixel system has been completed. In this system also, the critical path item is the design and development of the rad-hard ICs.

Cost/Schedule Status Reporting

- 1.1.1 Pixels
  - Have been treated until now as level of effort => no CSSR.
  - Will start after this review
- 1.1.2 Silicon Strips
  - Major schedule revision => CSSRs not helpful but will be after acceptance of current schedule
- 1.1.3 RODs
  - As of July, about $81K behind plan
  - Primarily results from redefinition of preprototype ROD to include more functionality(=> immediate delay but no impact on production), which is now included in schedule prepared for this review.

Institutional Responsibilities

	ALB	LBL	UCI	UCSC	UNM	UOK	UW	OSU
1.1.1 Pixels								
1.1.1.1 Mechanics		x						
1.1.1.2 Sensors	x				x	x		
1.1.1.3 Electronics		x						x
1.1.1.4 Hybrids	x					x		
1.1.1.5 Modules	x	x		x		x		x
1.1.1.6 Common	x	x	x	x	x	x	x	x
1.1.2 Silicon Strips								
1.1.2.1 IC Electronics		x		x				
1.1.2.2 Hybrids		x		x				
1.1.2.3 Modules		x		x				
1.1.3 RODs			x				x	

OSU added - otherwise same

U.S. ATLAS

Management - The Same

1.1.1 Pixels	**M. Gilchriese**
1.1.1.1 Mechanics	D. Bintinger
1.1.1.2 Sensors	S. Seidel
1.1.1.3 Electronics	K. Einsweiler
1.1.1.4 Hybrids	P. Skubic
1.1.1.5 Modules	M. Gilchriese
1.1.1.6 Common	M. Gilchriese
1.1.2 Silicon Strips	**A. Seiden**
1.1.2.1 IC Electronics	A. Grillo
1.1.2.2 Hybrids	C. Haber
1.1.2.3 Modules	C. Haber
1.1.3 RODs	**A. Lankford/R. Jared**

U.S. ATLAS

WBS 1.1 Summary

- 1.1.1 Pixels
  - Excellent technical progress
  - Approved pre-baseline funding adequate to complete development over next two years.
  - Development schedule/profile completed.
- 1.1.2 Silicon Strips
  - Major delay in IC development => base cost increase for additional IC engineering and prototypes.
  - Revised US schedule/profile completed.
  - Impact on overall SCT schedule under study by Collaboration
- 1.1.3 Read-Out Drivers
  - Test beam support successful and preprototype ROD(ROD99) on budget and schedule.
  - More detailed schedule completed.