Concluding Summary
WBS1.1.2 SCT Subsystem

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Conclusions From Last Year

1. Rest of this Fiscal Year: very important to establish that the technical design of the SCT detector is sound through building and simultaneous operation of a of a number of modules.

2. The first 9 months of Fiscal Year 01 will focus on pre-production to establish and quantify our ability to do testing and construction.

3. Starting summer 2001 go into full production.

How are we doing on these goals?

- Verification of Technical Design:
  Have irradiated and tested six modules, also have run six modules in system test.

  Will culminate in system test with:

  18 barrel modules

  6 new modules for PS irradiation

  These are the target goals prior to hybrid/module FDR in May, followed by integrated circuit PRR in July.

- # Readiness for Testing and Construction

  Readiness for chip testing: Need to complete wafer tester. This is nearly done. Crucial to reduce test time from 22 hrs/wafer (original CERN tester) to about 5 hours/wafer, our target. Expect to meet target. Will have common wafers tested at all three test locations and with CERN tester to verify that test results are robust.

  Readiness for module construction: Status, now completing mechanics. Plan is to then construct 20 dummy modules. This will be in 2 groups of 10, using successively more realistic parts. Active modules will also be constructed in parallel.

Short Term Schedule (2001)

WBS	Description	Previous	Forecast
1.1.2.1.1 Electronics Design	Production Readiness Review	June 15	July 4
1.1.2.1.3 Electronics Production	Complete Pre-production Fab.	Feb 28	March 30
1.1.2.2.1 Hybrid Design	Hybrid/Module Final Design Review	April 16	May 25
1.1.2.2.3 Hybrid Production	Pre-production Hybrids Available	June 4	Sept 1
1.1.2.3.1 Module Design	Final Design Review	April 16	May 25
1.1.2.3.2 Module Development	Complete Assembly Proto Modules	March 5	May 1
1.1.2.3.3 Module Production	Complete Pre-production Module Assembly	July 30	Oct 30

Some Key Dates:

5/23/01	Complete IC Pre-production Design Verification
	Needed for hybrid/module FDR May 24-25
7/6/01	Start Full Electronics Production
	Follows PRR for Front-end Chips
11/23/01	First IC Lots Delivered
12/16/02	Production Testing of Chips Complete
1/7/02	Start Module Production
	Will Ship 670 Modules
10/13/03	Complete Shipment of Production Modules

Details Shown in Line of Balance Plan

WBS 1.1.2 SCT Wafers and ICs

Line Of Balance Data

All numbers are CUM complete numbers as of 1st of month

Shipments to LBNL shown; remainder of ICs to other assembly sites

	WafersReceived	At UCSC						
	by CERN	Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd	Dice to:	LBNL
Dec-01	120							
Jan-02	120	60	10					
Feb-02	320	60	40	12	776	388		120
Mar-02	320	160	70	40	2,592	1,684		519
Apr-02	520	160	113	70	4,537	3,564		1,099
May-02	520	260	156	113	7,316	5,926		1,827
Jun-02	720	260	199	156	10,095	8,705		2,683
Jul-02	720	360	242	199	12,874	11,484		3,540
Aug-02	920	360	285	242	15,653	14,263		4,396
Sep-02	920	460	328	285	18,432	17,042		5,253
Oct-02	949	460	371	328	21,211	19,821		6,109
Nov-02		475	414	371	23,990	22,600		6,966
Dec-02			457	414	26,769	25,379		7,822
Jan-03			475	457	29,548	28,158		8,679
Feb-03				475	30,666	30,107		9,279
Mar-03						30,666		9,452
Apr-03								
May-03								
Jun-03								
Jul-03								
Aug-03								
Sep-03								
Oct-03								
Nov-03								
Dec-03								
Jan-04								

Status

	WafersReceived	At UCSC						
	by CERN	Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd	Dice to:	LBNL
Plan								
Acita;								
Delta								

WBS 1.1.2 SCT Modules

Line Of Balance Data

All numbers are CUM complete numbers as of 1st of month

Components as proposed by collaboration March 2001

	FE ICs	Silicon Detectors	Thermal Baseboards	Kapton Hybrids	Assembled Hybrids	Tested Hybrids	Assembled Modules	Tested Modules	Shipped Modules
Oct-01			20						
Nov-01			40						
Dec-01		104	60	30					
Jan-02		208	90	60					
Feb-02	120	312	120	120					
Mar-02	519	416	170	180	10				
Apr-02	1099	520	220	240	35	9			
May-02	1827	728	270	359	70	34	9		
Jun-02	2683	936	330	478	110	68	32	9	
Jul-02	3540	1144	390	597	150	107	65	32	9
Aug-02	4396	1352	450	716	200	146	101	63	31
Sep-02	5253	1560	510	750	250	194	138	99	63
Oct-02	6109	1768	570		300	243	184	135	98
Nov-02	6966	1976	630		350	291	230	181	134
Dec-02	7822	2184	690		400	340	276	226	179
Jan-03	8679	2392	750		450	388	323	271	223
Feb-03	9279	2600			500	437	369	316	268
Mar-03	9452	2808			550	485	415	361	313
Apr-03		3016			600	534	461	406	357
May-03		3063			650	582	507	452	402
Jun-03					700	631	553	497	447
Jul-03					750	679	599	542	491
Aug-03						728	645	587	536
Sep-03							691	632	581
Oct-03								677	625
Nov-03									670

Status

	FE ICs	Silicon Detectors	Thermal Baseboards	Kapton Hybrids	Assembled Hybrids	Tested Hybrids	Assembled Modules	Tested Modules	Shipped Modules
Plan									
Actual									
Delta									

ETC01vs ETC00 Comparison

1.1.2.1 Electronics

Increase in cost of engineering and materials for IC test system+system test support.

Decrease in cost of ICs, more favorable $/Euro rate.

Decrease in systems engineering costs.

Correction of accounting errors and revised inflation estimate based on new schedule.

1.1.2.2 Hybrids

Correction of accounting errors and revised inflation estimate based on new schedule.

1.1.2.3 Modules

Correction of accounting errors and revised inflation estimate based on new schedule.

		ETC 00			ETC 01		
	ETC		TPC	ETC 01		TPC 01	
	Access	Actuals	Access	New Access	Actuals	New Access	
WBS	(in FY00 $s)	Thru FY99	Plus Actuals	(in FY00 $s)	Thru FY00	Plus Actuals	Delta
1.1.2	4,996.4	911.0	5,907.4	4,611.9	1,414.3	6,026.2	(118.8)
1.1.2.1	3,628.2	771.0	4,399.2	3,208.9	1,184.5	4,393.4	5.8
1.1.2.2	463.9	67.0	530.9	488.6	107.9	596.5	(65.6)
1.1.2.3	904.3	73.0	977.3	914.4	121.9	1,036.3	(59.0)

Contingency

Management Contingency in original SCT Plan was $988k, all in IC production costs.

Cash Contingency left for IC Electronics is about $1M.

Cash contingency left for Hybrids and Modules is about $400k.

Total Cash contingency appears more than adequate to cover risks for baseline scope.

Risk Analysis

Items: Parts supplied by other groups (Kapton Hybrids and Baseboards), chips, rate of chip testing and hybrid and module construction.

1. Hybrid (without front-end chips) and baseboard schedules are projected to be well ahead of other construction items.

2. Some possible risk scenarios involving chips and modules:

a) FE IC yield is roughly 1/2 that expected and Atmel delivers extra wafers to meet the contractual guarantee of minimum yield or we have a 6 month delay in starting production. Doubling the number of wafers to test or late start should be handled by a modest increase in manpower costs (doubling the manpower would add about $0.1M), there is already an additional probe station (if needed) in the budget and having multiple test systems (ie, various electronics boards) at each site is already in the budget.

b) There are additional losses of ICs during handling and assembly and about 15% more wafers have to be procured and tested. Procuring an additional 15% wafers would be about $0.3M.

c) We have to roughly double the steady-state rate of module assembly/test, resulting from unexpected delays in delivery of components. Our conclusion is that the current cash contingency for hybrid and module assembly/test (about $0.4M) is probably too low by about $0.1M for this scenario.

Baseline Deliverables:

45% of front-end chips,

670 modules.

Goal with management contingency allocated is to provide 65% of front-end chips.

Rest of SCT has significant cost over-runs in items such as cables and power supplies, which we can't help with. Therefore important to try to supply the full 65% of the chips. We believe there is a good chance that we can do this (and cover risks) within the current cash contingency for the Silicon Strips.