WBS 1.1 Silicon Subsystem

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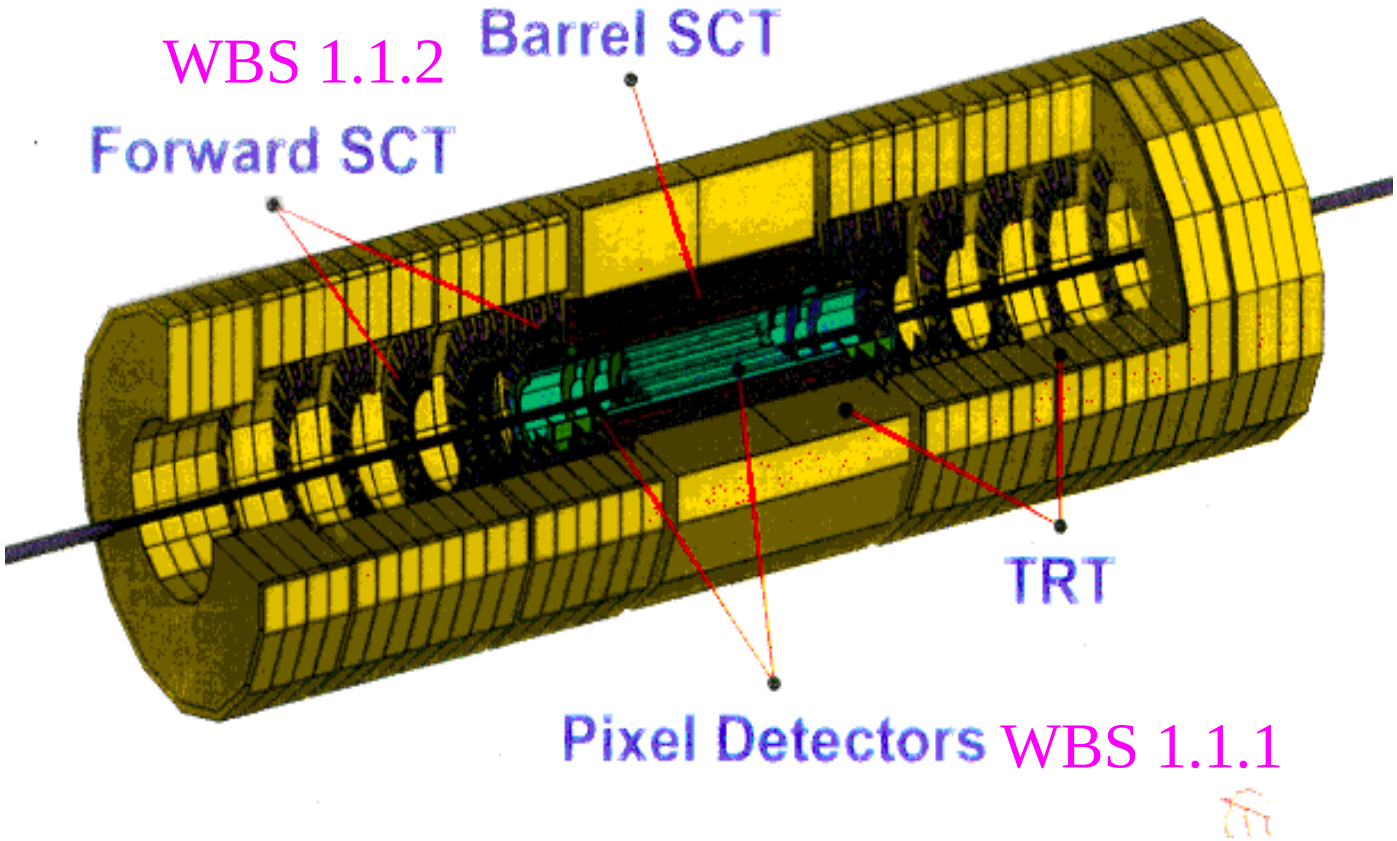
Lawrence Berkeley Laboratory

Silicon Subsystem



ReadOut Drivers - WBS 1.1.3

Organization

- **Institutions and responsibilities - no changes**
- **Management**
  - **Senior physicist and engineer added to pixel team**
  - **Otherwise no changes at Level 4 or above**
- **Other personnel**
  - **Engineering added**
  - **Modest increase in technical staff**

Institutions

SUNY Albany
Iowa State University
UC Berkeley/LBNL
University of New Mexico
Ohio State University
University of Oklahoma/Langston Univ.
UC Santa Cruz
University of Wisconsin

Management

1.1.1 Pixels(Gilchriese)
1.1.1.1 Mechanics/Services(Gilchriese, Anderssen)
1.1.1.2 Sensors(Seidel, Hoeferkamp)
1.1.1.3 Electronics(Einsweiler, Denes)
1.1.1.4 Hybrids(Skubic, Boyd, Gan)
1.1.1.5 Modules(Garcia-Sciveres, Goozen)

1.1.2 Silicon Strips(Seiden)
1.1.2.1 IC Electronics(Grillo, Spencer)
1.1.2.2 Hybrids(Haber)
1.1.2.3 Modules(Haber, Senior Techs)

1.1.3 RODs(Jared, Fasching, Meyer)

(Physicist, Engineer or Senior Tech)

Highlights Since Last Review

- **Pixels**
  - Design of Pixels and Inner Detector changed to allow insertion or removal of Pixels without removing rest of Inner Detector => gain >1 year in pixel critical path schedule
  - Production baseline cost and schedule established
- **Silicon Strips**
  - Preproduction order of rad-hard front-end integrated circuits(40+ wafers) delivered
  - Baseline design of barrel modules established
- **ReadOut Drivers**
  - Prototype ROD fabricated and under test

Silicon Performance Data

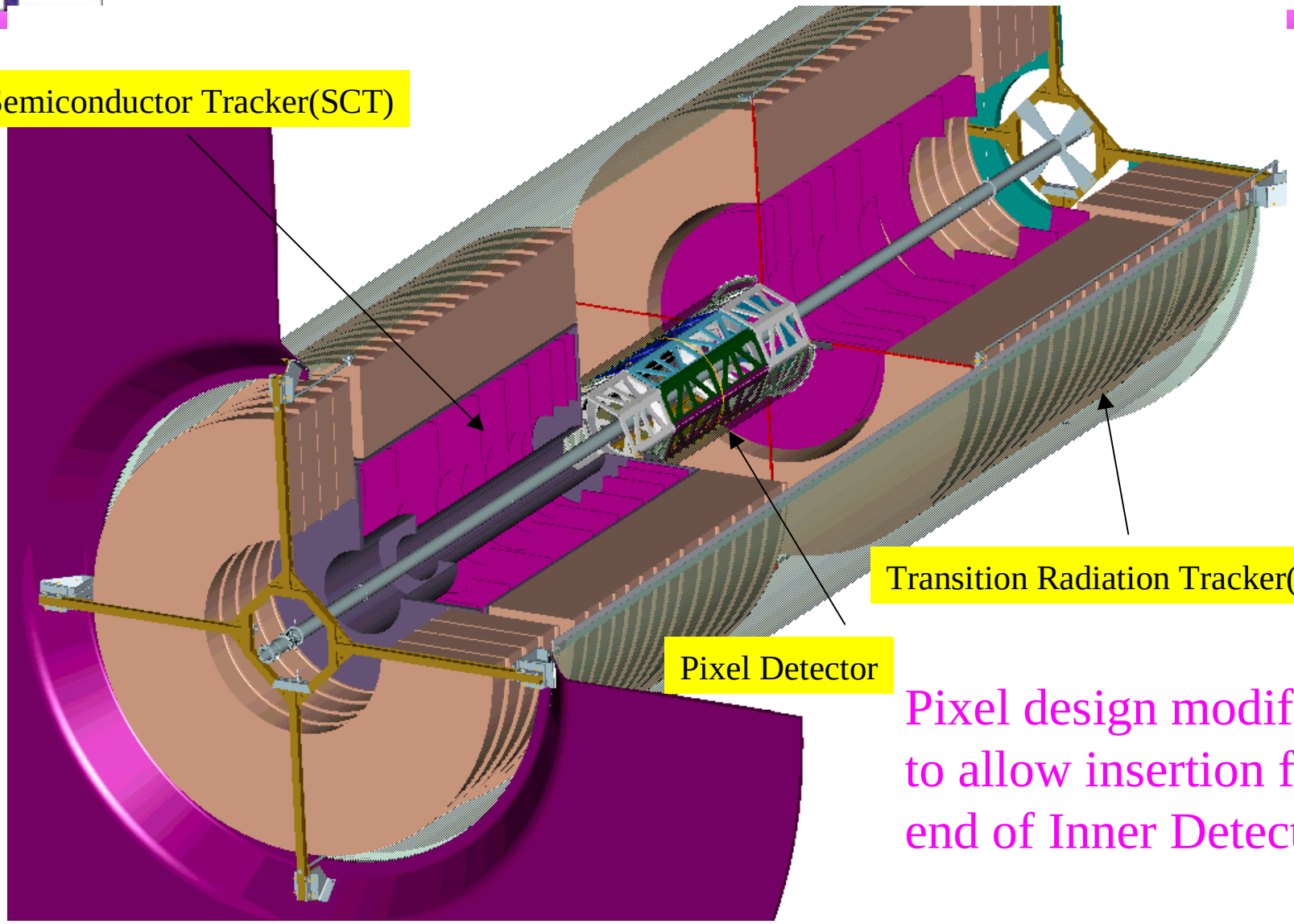
Comparison Against ETC00 Baseline

WBS Level 3 through 1/31/01

WBS	Description	BCWS	BCWP	ACWP	SV	CV
Silicon						
1.1.1	Pixels	2,787,269	2,787,269	2,185,800	-	601,469
1.1.2	Silicon Strip System	4,403,865	4,385,805	3,927,380	(18,060)	458,425
1.1.3	RODs	1,252,803	1,057,053	1,181,667	(195,750)	(124,614)
	Total	8,443,937	8,230,127	7,294,847	(213,810)	935,280

- **Some delay in silicon strip system(ICs)**
- **Delay in prototype ROD -> production delay**
- **Details to follow after technical status described**

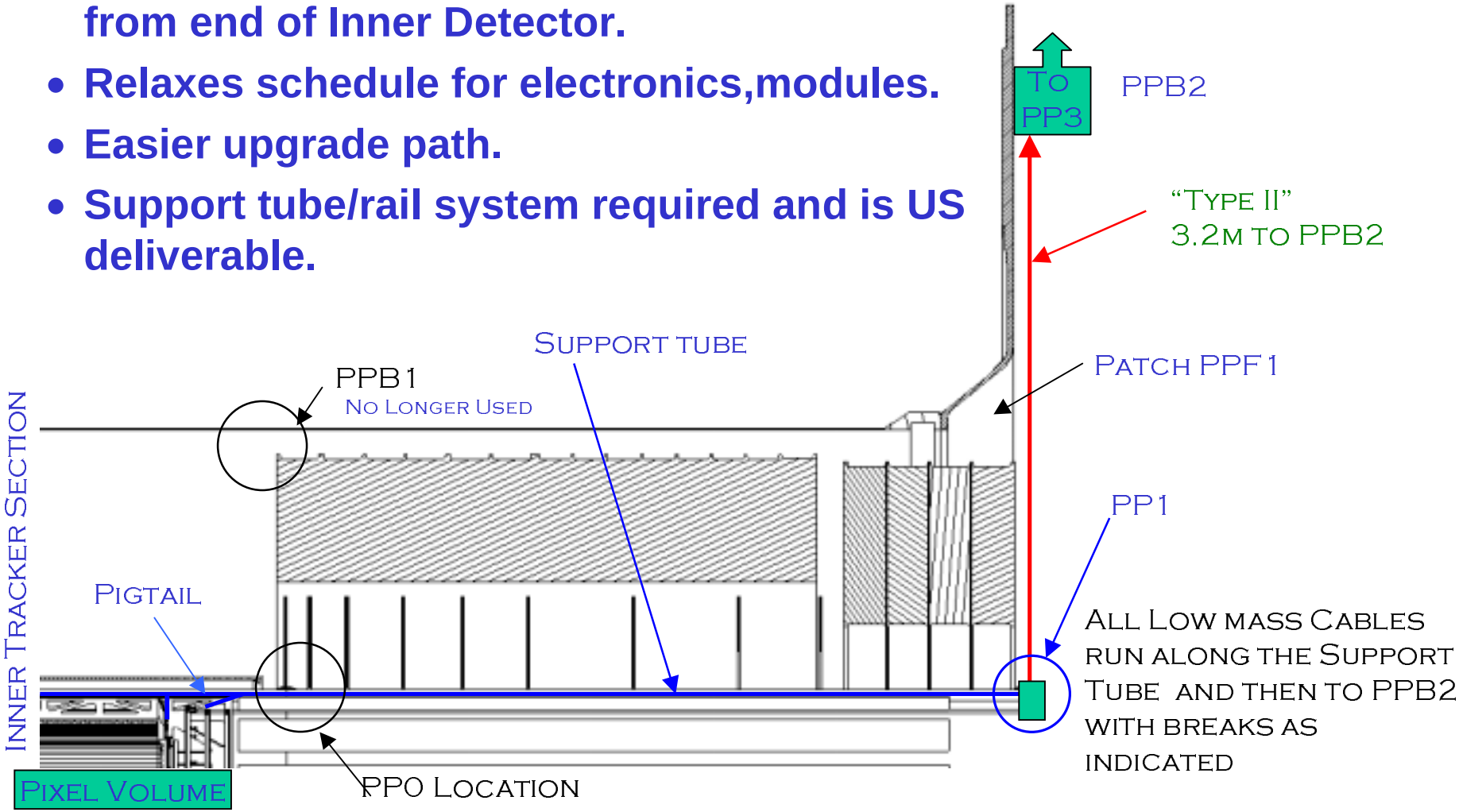
Technical Status - 1.1.1 Pixels



Pixel design modified to allow insertion from end of Inner Detector

Technical Status - 1.1.1 Pixels

- **Insertion/removal of complete Pixel System from end of Inner Detector.**
- **Relaxes schedule for electronics,modules.**
- **Easier upgrade path.**
- **Support tube/rail system required and is US deliverable.**



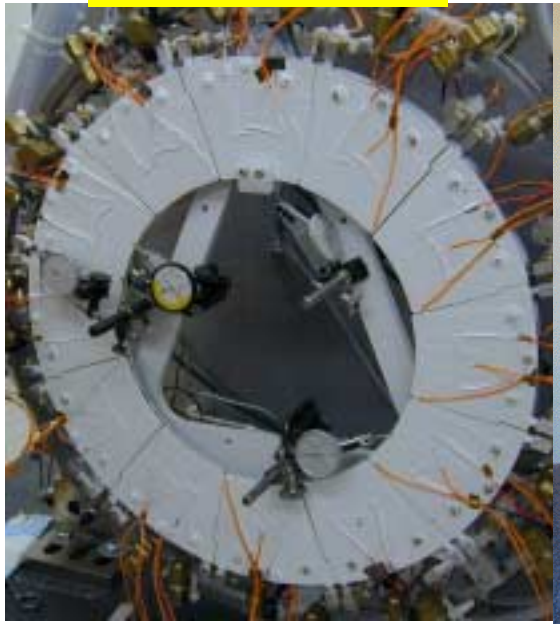
Technical Status - 1.1.1 Pixels

- Scope reduction(less active area) required to implement removable system. Pixel System gets smaller.
- A “3-hit” system is required to achieve full ATLAS performance goals. This requires three barrel layers and 2x3 disks.
- However, the performance of a “2-hit” system is judged to be adequate for the initial operation of ATLAS. This is based on simulations done already in 1997, new simulations underway.
- The US baseline is thus a “2-hit” system. This requires 2 barrel layers and 2x2 disks.
- Release of Management Contingency(currently 600K) is needed to achieve a “2-hit” system.

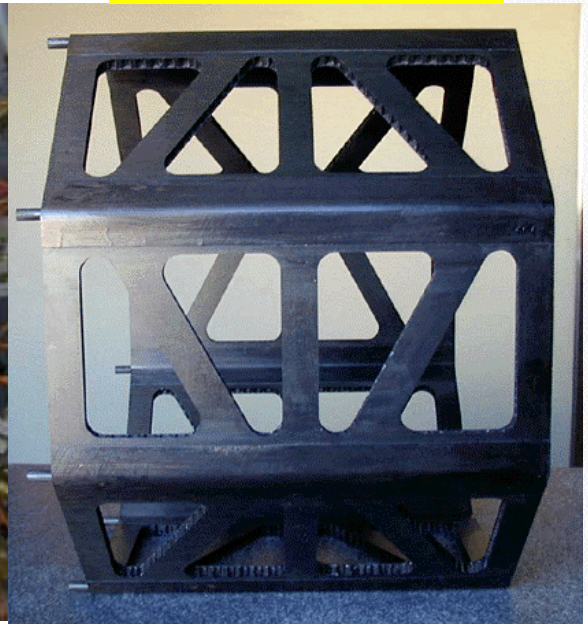
Technical Status - 1.1.1 Pixels

- **Prototypes of all US deliverables for mechanical structure either already built or to be fabricated within about next year.**
- **Design work advancing well**

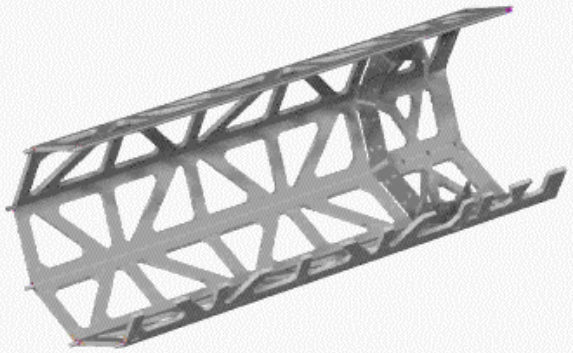
Disk Prototype



Frame Prototype

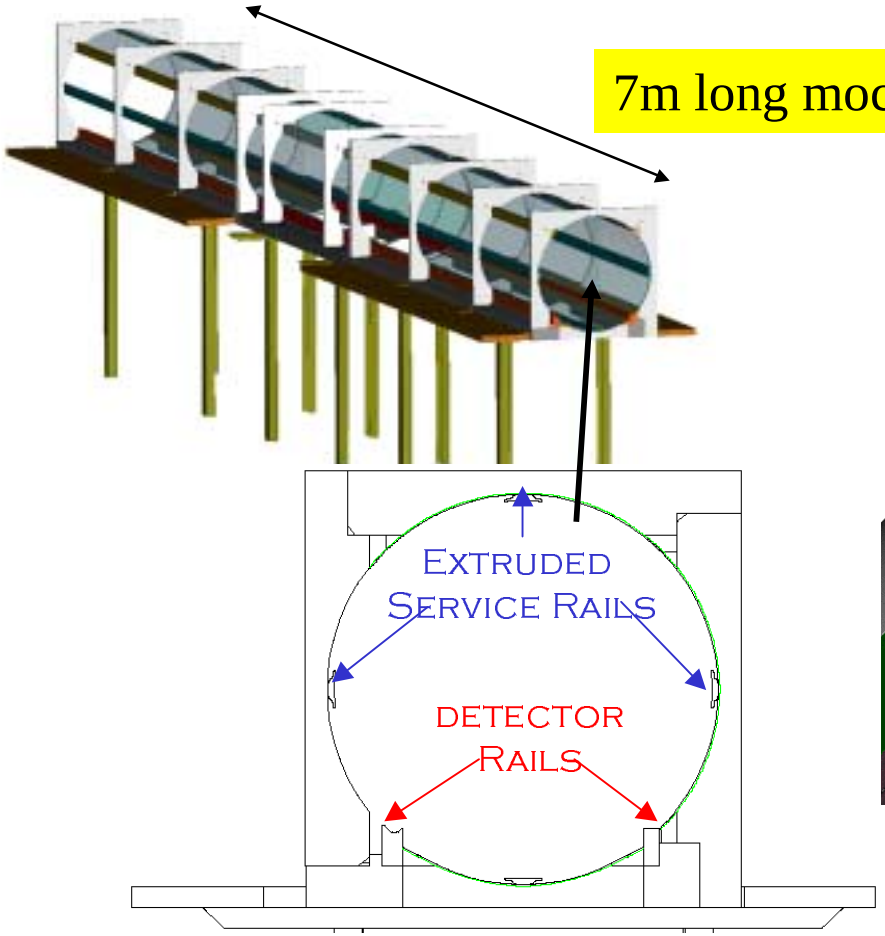


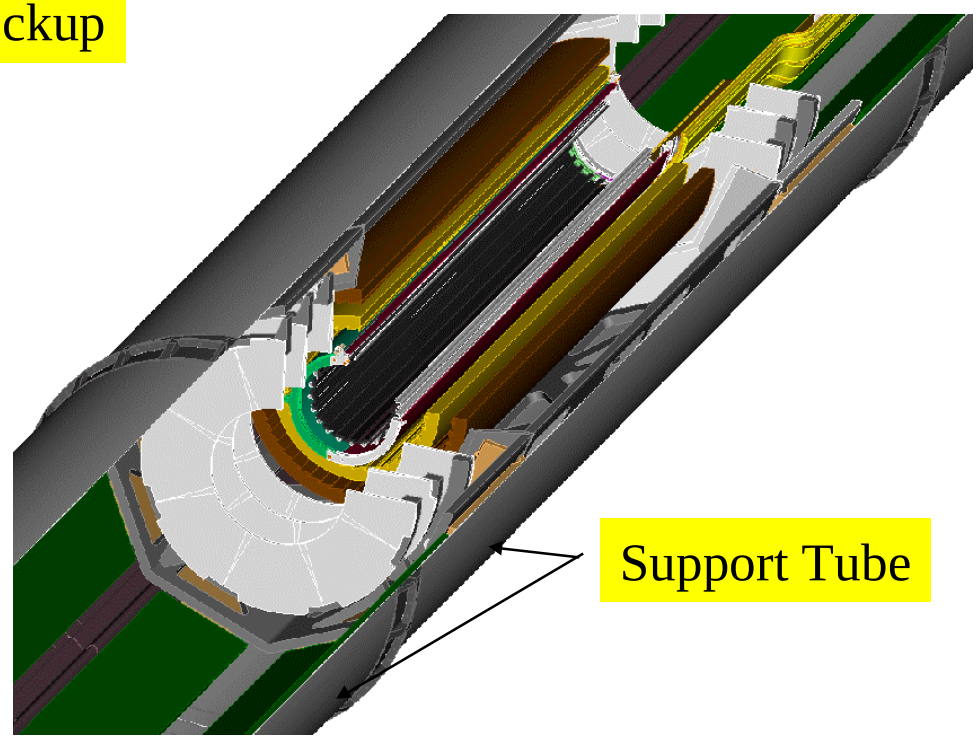
Support Frame



Technical Status - 1.1.1 Pixels

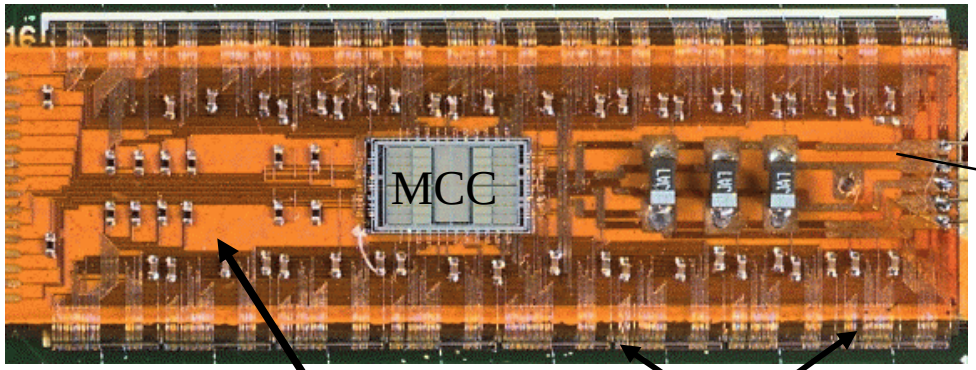
- **Full mockup of support tube under construction at LBNL to be ready for first studies next month.**
- **Design of support tube and interfaces underway.**





Technical Status - 1.1.1 Pixels

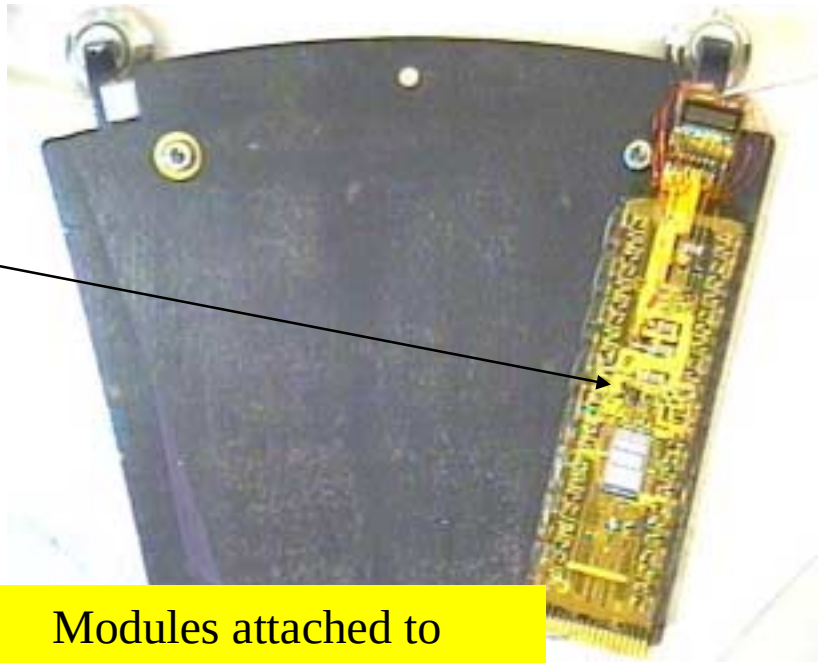
- **Module is basic building block of system.**
- **Module consists of silicon sensor, 16 front-end(FE) chips, flex hybrid with Module Control Chip(MCC) and passive components and interconnect(pigtail) to power and optical signal transmission.**
- **Connection between sensor and FE chips is made by Pb/Sn or In bump bonding.**



Kapton hybrid

Front-end chips

Kapton hybrid glued to sensor



Modules attached to mechanical/thermal structure

Technical Status - 1.1.1 Pixels

- **Sensors**
  - Production Readiness Review completed
  - Production contract between CERN and two vendors in place
  - First preproduction lots completed and under test, OK so far
- **Hybrids**
  - ATLAS Final Design Review of flex hybrids completed
  - Two generations of prototype flex hybrids made and used for module assembly, 3rd under design to be made this year
  - First prototypes of optical hybrids fabricated and under test
- **Module assembly**
  - ATLAS Final Design Review of bump bonding completed and prospective production vendors identified.
  - First generation of assembly tooling completed, dummy and active modules assembled, tested.

Technical Status - 1.1.1 Pixels

- Four rad-hard integrated circuits are required: front-end(FE), optical ICs(VDC and DORIC) and Module Control Chip(MCC).
- Development first in DMILL(Atmel) and then Honeywell began in late 1998.
- First DMILL run(FE-D1) - more than one year ago
  - Prototypes of all four chips included.
  - Major conclusion was that yield of FE chip was essentially zero.
  - Circuit elements(transistors) that were responsible for bad yield found, but root cause in production process not understood after extensive investigation by ATLAS, vendor and consultants.
- Honeywell(after merger with Allied Signal) eventually confirms large price increase - design started but dropped in Fall 2000.
- Collaboration immediate began ramp up of effort on 0.25 micron processes, IBM and TSMC(used by all other LHC expts)
- CERN completes Frame Contract with IBM.

Technical Status - 1.1.1 Pixels

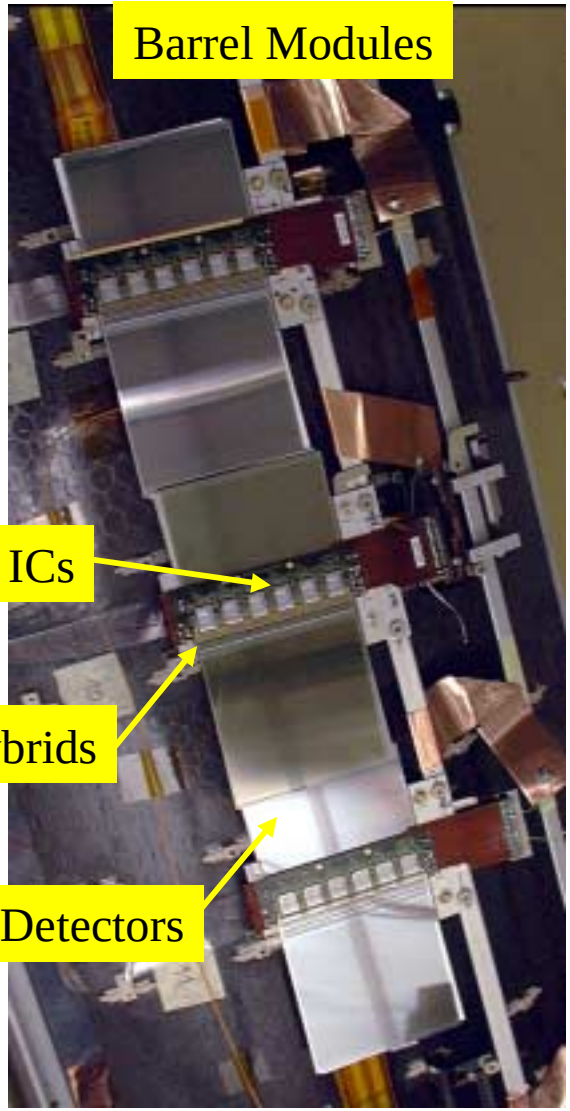
- **Second DMILL run(FE-D2) delivered in November 2000**
  - **Known design errors in FE from first run fixed successfully.**
  - **Two versions of FE chip made.**
    - **One with just fixes(yield still zero)**
    - **One with redesign to eliminate suspect circuit block but some other critical circuit blocks had to be eliminated in redesign to fit within existing 400 micron long pixel size. Yield of this chip good enough to continue testing program.**
  - **First irradiations(of FE with redesign) completed last month. Performance not acceptable so far. More irradiations to come.**
  - **Preliminary results on other chips indicate Atmel possible candidate for optical ICs. Yield of MCC prototype low(about 10%).**
  - **DMILL design work has been suspended in favor of 0.25 micron for now. Irradiations and testing are continuing. Gives information on design + irradiation methodology.**

Technical Status - 1.1.1 Pixels

- **0.25 micron processes**
  - Rapid progress on conversion of designs
  - Test chips submitted to TSMC in Jan and Mar this year. Also IBM in Feb.
  - On track for first multi-wafer engineering run(IBM) with all ICs by July
  - Taking maximum advantage of work by other experiments(CMS, BTeV, ALICE, LHCb…that all rely on this)
- **US baseline for ICs assumes**
  - 0.25 micron(IBM) for FE, TSMC backup vendor
  - DMILL(Atmel) for VDC and DORIC(small chips, total production is only a few wafers).
  - MCC is solely European cost responsibility, likely to be 0.25 micron.

Technical Status - 1.1.2 Silicon Strips

- US deliverables are front-end integrated circuits, test system for ICs and barrel modules.
- Front-end IC baseline chosen about one year ago(ABCD)
- Barrel module baseline established.



Technical Status - 1.1.2 Silicon Strips

- A Frame Contract with the ABCD vendor(Atmel) and CERN was established. It has a minimum yield guarantee.
- Five preproduction lots(8 wafer each) of ABCD3 have been delivered as of early February.
- The yield varies significantly from wafer-to-wafer and lot-to-lot. Yield is around 15%(perfect chips) and about twice this for chips with single bad channel.
- Minimum guaranteed yield from vendor is 26%. Will deliver additional wafers to meet minimum guarantee, trying to understand source of poor yield.
- A number of wafers had obvious defects(scratches, misalignments…) that can be eliminated. Even so the yield for perfect chips is below the minimum on average.

Technical Status - 1.1.2 Silicon Strips

- Atmel now suspects one of their subcontractors that provides wafers with epitaxial silicon. Is processing an additional 36 wafers(part with old vendor, part with new vendor) at their expense aimed at greater understanding of the yield. These will be delivered in the next two months.
- A design modification was made between the 2nd and 3rd preproduction lots to fix a problem seen after high-dose-rate irradiation. This will be tested in April.
- An additional problem after high-dose-rate irradiation at about 50% of lifetime dose was seen in about 20% of chips and continues to be investigated.
- Need for more irradiation testing and probing of 36 wafers is projected to delay start of electronics production from 4/01 to 7/01.

Technical Status - 1.1.2 Silicon Strips

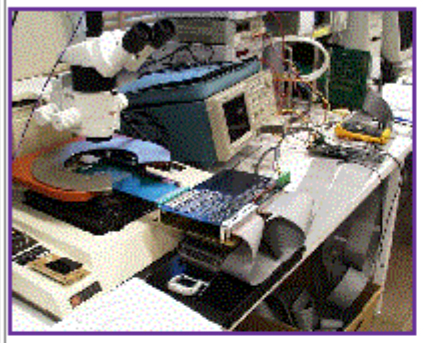
- New, high speed test system for IC wafer probing and verification designed and built by LBL is nearing completion. Needed to cope with production volume.
- Will be used at Santa Cruz, RAL and CERN for wafer probing and first systems are at all three sites.
- Detailed verification of test system in progress at all three sites.
- Plan to have two complete systems available at each site. Nominally one is spare to maintain high reliability but could be used with additional probe stations to increase probing rate, if needed(total volume assuming minimum guaranteed yield is about 1000 wafers in about one year). Have capacity to do more or go faster.

Technical Status - 1.1.2 Silicon Strips

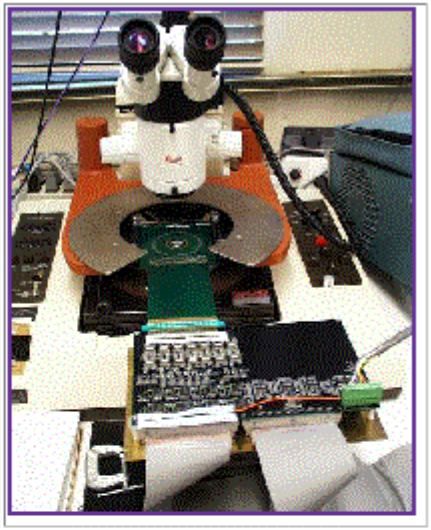
ABCD
Test System

Three boards
+ probe card

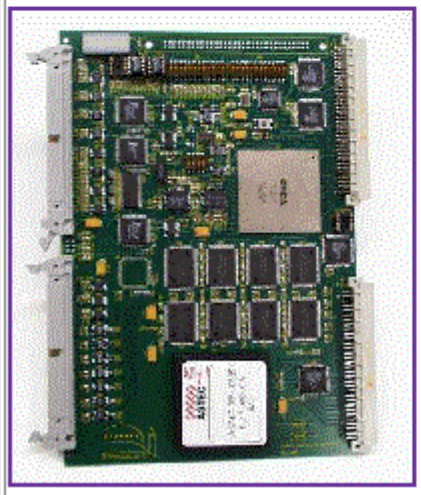
Setup



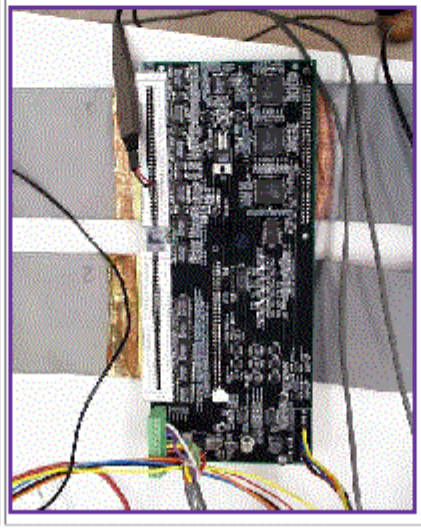
Probe station



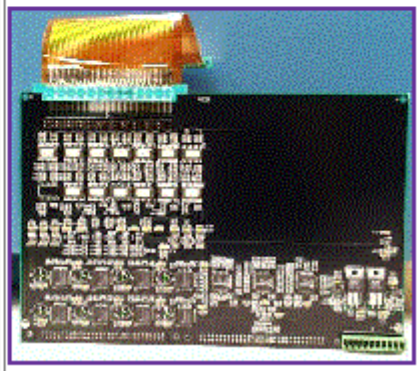
VME Board



Pindriver Board



Concard



Technical Status - 1.1.2 Silicon Strips

- Barrel module baseline design established
- Active modules constructed and tested in beam and in ongoing “system” test at CERN.
- Some production tooling remains to be fabricated
- Have removed some slack in schedule and slightly modified production sequence to cope with delays in electronics. End date for module completion same as last year.
- Lack of collaboration-wide, production planning raised last year is still a concern although progress made in last month or so.

Technical Status - 1.1.2 Silicon Strips

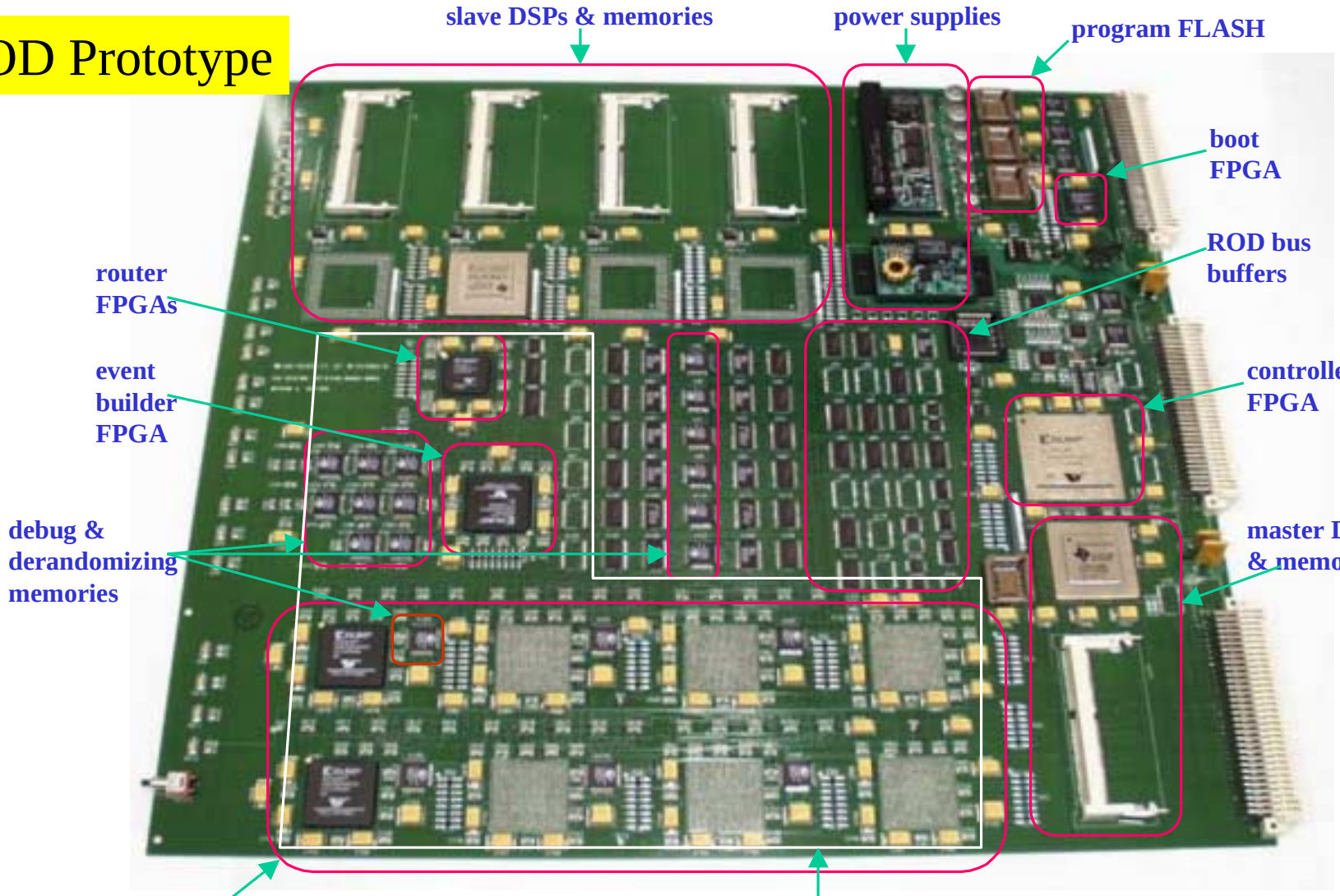
- **Basic module assembly equipment and facilities are largely complete but not yet in production status.**
- **Assembly and test procedures being debugged using dummy modules and few active modules. Staff being trained.**

Technical Status - 1.1.3 RODs

- Components of the Pixel/SCT Off Detector Electronics
  - Back Of Crate (BOC) card (optical interface), Cambridge
  - Read Out Driver (ROD), Wisconsin
  - Timing Interface Module (TIM), University College London
  - Crate Backplane, Oxford
  - SCT DAQ, Cambridge + others to join
  - Pixel DAQ, Iowa State + others to join
- First prototypes of components built and under test individually

Technical Status - 1.1.3 RODs

ROD Prototype



Technical Status - 1.1.3 RODs

- Preliminary Design Review of ROD complete
- Two, partially loaded, prototype boards received and debugging underway.
- Plan to fabricate 6 more with (hopefully) minor modifications after initial debugging complete.
- No showstoppers yet but also no demonstration all specs met according to documented test plan.
- Delays in fabrication and slower debugging + better understanding of need for system test of all components propagate directly into delay of ROD production start by about 4-5 months.
- Integrated test of BOC-ROD-TIM planned to start next month at Cambridge.

ETC01 vs ETC00

Silicon

WBS Level 3

Access Comparison (Silicon Level 3)
(Project FY00K$s)

	ETC 00			ETC 01			
WBS	ETC Access (in FY00 $s)	Actuals Thru FY99	TPC Access Plus Actuals	ETC 01 New Access (in FY00 $s)	Actuals Thru FY00	TPC 01 New Access Plus Actuals	Delta
111 Pixel System	8,256	1,005	9,261	6,382	1,910	8,291	970
112 Silicon Strip	4,996	911	5,907	4,612	1,414	6,026	(119)
113 Read-out Drivers	2,186	630	2,816	1,829	1,019	2,847	(31)
Total	15,439	2,546	17,985	12,822	4,343	17,165	820

Explanation of ETC01 Cost Changes

- **Pixels(1.1.1)**
  - TPC below original estimate.
  - Why? 0.25 micron ICs, scope cut, increased contingency + savings during development phase.
- **Silicon Strips(1.1.2)**
  - Increases in engineering + materials for high-speed IC tester(US responsibility) needed to cope with potential for low yield.
  - Decreases in IC costs(fixed in Euros, $ stronger than last year).
- **ReadOut Drivers(1.1.3)**
  - No change in estimate except for inflation
  - No calls on contingency yet

ETC01 Funding Profile

Silicon

WBS Level 3 Funding Profile

Silicon ETC 01 Access Profile (Project K$s)

WBS	FY01	FY02	FY03	FY04	FY05	FY06	Total
111 Pixel System	1,933	1,927	2,084	408	30	0	6,382
112 Silicon Strip	3,616	731	264	0	0	0	4,612
113 Read-out Drivers	1,081	604	52	45	46	0	1,829
1.1 Total (FY00$s)	6,630	3,263	2,401	454	76	0	12,822
1.1 Total (AY$s)	6,795	3,431	2,595	504	87	0	13,413

ETC01 Milestone Changes

Level 2 Milestones

Subsystem	Schedule Designator	Description	ETC Schedule Date	ETC 01 Schedule Date
Silicon	Sil L2/1	Start Full Silicon Strip Elec Prod	23-Apr-01	6-Jul-01
	Sil L2/2	Start Full Strip Module Production	26-Nov-01	7-Jan-02
	Sil L2/3	ROD Design Complete	14-Jun-01	1-Oct-01
	Sil L2/4	Compl Shipment of Silicon Strip Modules Prod	13-Oct-03	13-Oct-03
	Sil L2/5	ROD Production/Testing Complete	13-Mar-03	24-Jun-03
	Sil L2/6	Pixels 1st IBM Prototype Submitted	N/A	26-Jul-01
	Sil L2/7	Pixels Start IBM Production	N/A	13-Mar-03
	Sil L2/8	Pixels Start IBM Outer Bare Module Production	N/A	22-Oct-03
	Sil L2/9	Pixels 'Disk System at CERN'	N/A	13-Oct-04

Level 4 Milestones (Baseline Scope)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC Planned Completion Date	ETC 01 Planned Completion Date	ATLAS Required Date	ETC 01 Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Compl Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	**-6**
1.1.3	Sil L4/2	RODs 45% Production Compl	4/02	9/02	6/03	9
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	N/A	10/04	12/04	2

Explanation of ETC01 Milestone Changes

- **Pixels(1.1.1) - baseline established.**
- **Silicon Strips(1.1.2)**
  - **Delay in rad-hard qualification of front-end ICs by about 3 months**
  - **Full module construction start delayed, but can start without ICs for few months + have removed some slack => end date kept same.**
  - **Conflict with (old) ATLAS need date remains. Impact of new ATLAS schedule to be assessed.**
- **ReadOut Drivers(1.1.3)**
  - **Delay in fabrication and debugging of prototype.**
  - **Better understanding of full prototype system test needs(not just ROD)**
  - **Total delay 4-5 months in production**

Conclusions

- **Pixels(1.1.1)**
  - **Production baseline established**
- **Silicon Strips(1.1.2)**
  - **TPC about same as last year**
  - **Few month delay in start of IC production projected**
  - **Completion date for modules same as last year**
- **ReadOut Drivers(1.1.3)**
  - **TPC same as last year**
  - **Delays in prototypes delay production**
  - **But significant float remains in schedule**