WBS 1.1.1 Pixel System

Sensors, Opto-links, and On-detector Electronics

Major Topics:

- Sensors (WBS 1.1.1.2): Status and Issues
- Opto-links (WBS 1.1.1.3 and 1.1.1.4): Status and Issues
- On-Detector Electronics and Test System (WBS 1.1.1.3): Status and Issues

Details of our 0.25μ electronics program and schedule will follow in the talk of P. Denes

Summary and Conclusions

Prototype Results in Appendix

Sensor Concepts

Basic requirement is operation after 10^{15} NIEL fluence:

- Requires partially depleted operation. Chosen n^+ pixels in n-bulk material as basic configuration (does require double-sided processing).
- Two isolation techniques studied for the n^+ pixel implants. Selected low dose p-implantation over the whole wafer (so-called p-spray) approach. With p-spray technique, observe only bulk leakage in I/V curve after full dose. Does not require critical high-dose p implantation between n^+ implants, so yield should be high.

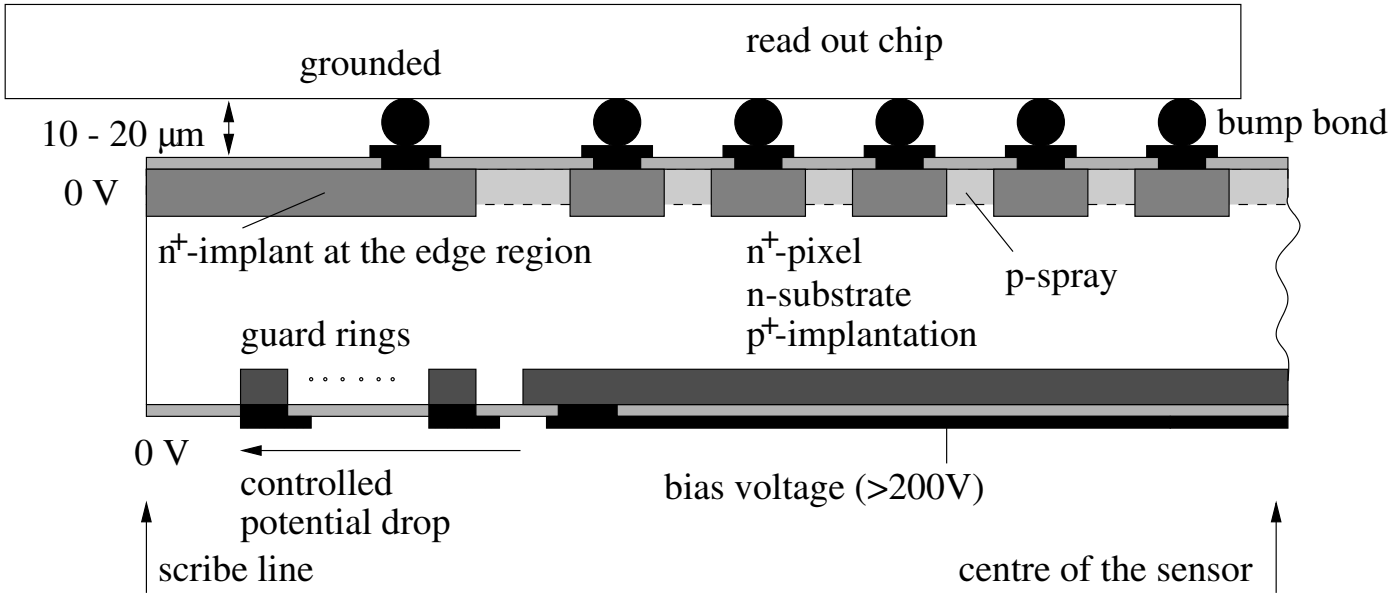


Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

Final Sensor Design (Sensor 2)

- Final design is based on small gap, and includes bias grid to allow testing (hold all pixel implants at ground for I/V characterization) and to keep unconnected pixels from floating to large potential in case of bump-bonding defects. It uses "moderated" p-spray to improve pre-rad breakdown voltage (better yield).
- Sensor 2 wafer layout had 3 module tile designs ("no dot", "small dot", and "large dot" bias structures). SMD (small dot) chosen based on yield and performance:

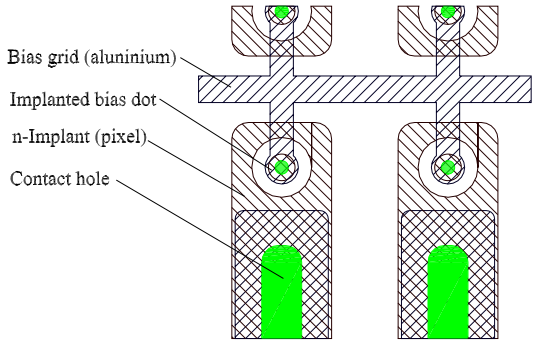
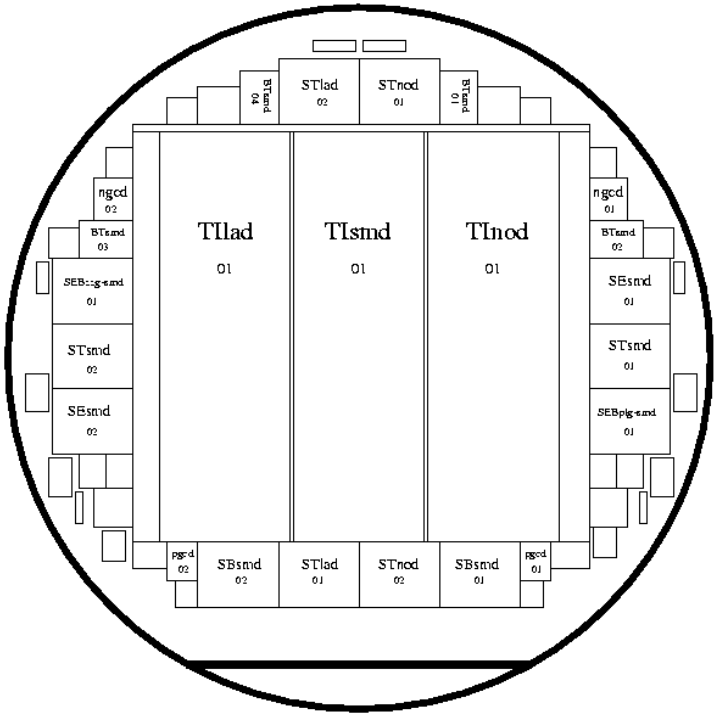
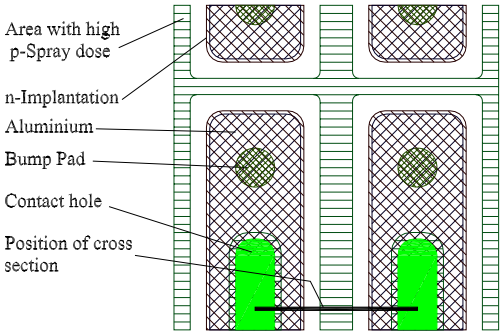
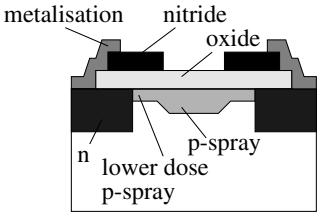


Fig. 10. Design detail of the bias grid in the second sensor prototype.



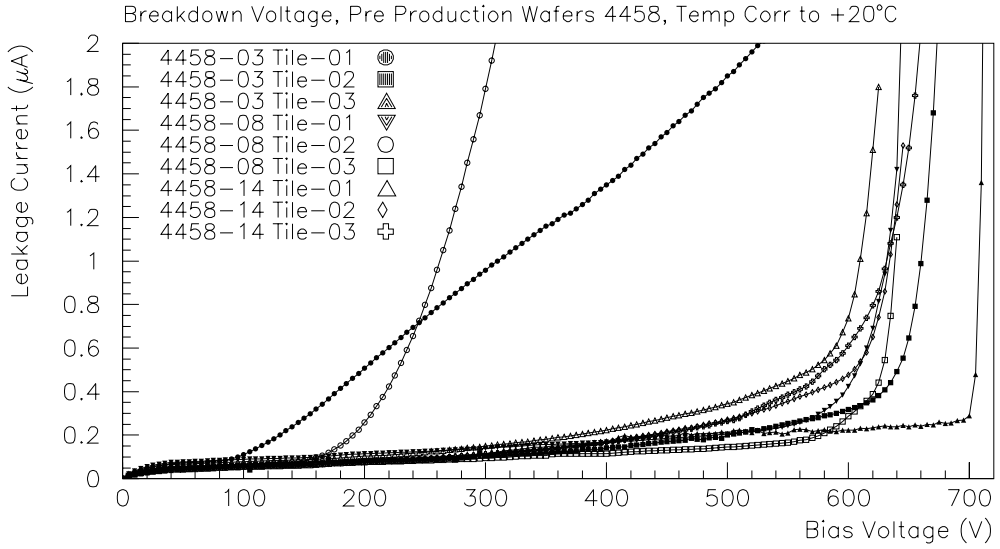


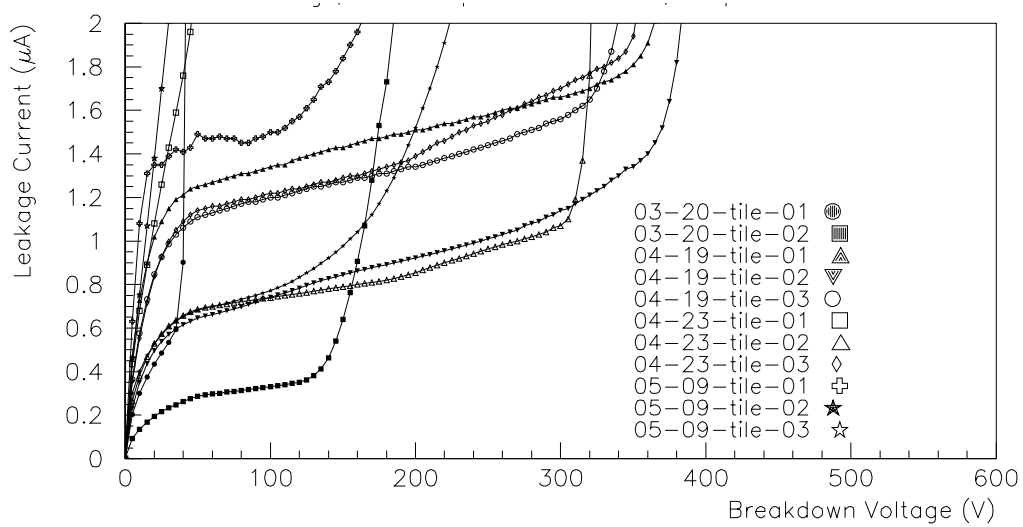


Prototype History:

- **Sensor 1 designs:** Initial designs from 1997 covering a wide range of concepts with CIS and Seiko. Extensively tested in the lab and testbeam in 1998, including irradiation of single chips and subsequent flip-chip to rad-soft electronics.
- **Sensor 1b designs:** Evolution of p-spray designs to include version very close to final production concept (SSGb). Only CIS was a vendor. Extensively tested in lab and beam in 1999. A second identical run (sensor 1c) was used to compare yield for standard and moderated p-spray.
- **Sensor 2 designs:** Emphasis on final wafer layout, significant orders to exercise vendors and allow us to build a large number of modules. Uses latest technology, including moderated p-spray and 50% of wafers oxygenated using ROSE recipe.
- **Oxygenation:** Technique involves diffusion into wafers for 16 hours at 1150 C in O atmosphere. Only useful when irradiation is predominantly charged particles (neutron damage un-affected). Two major effects (other properties unchanged):
- Modification of reverse annealing behavior by “saturating” the total reverse annealing. This gives about half depletion voltage for a fixed large dose. For B-layer, roughly doubles lifetime dose (ignoring trapping effects).
- Increase of reverse annealing time constant by about 4. This gives reduced effect of room temperature exposure on irradiated sensors, and considerably relaxes access scenarios. Largely understood in terms of defect phenomenology.
- FDR (Dec 3 99) and PRR (Feb 2 00) successfully completed.

- Pre-production order launched with two vendors: CIS and Tesla
- First wafers received from CIS in Jan and Tesla in Feb of this year:





- First plot shows I/V results for CiS module tiles. Breakdown is excellent, leakage is low, and yield is good.
- Second plot is for Tesla. Leakage and breakdown are not as good, but still acceptable on most tiles.
- Foundry does I/V characterization too, and only delivers wafers with 2 or 3 good tiles. Agreement with lab measurements is good.

US Roles:

- There are four active testing sites in pixels (Dortmund, New Mexico, Prague, and Udine). Test procedures and acceptance criteria are defined in great detail.
- UNM has performed US share of wafer probing up to the present, and has necessary equipment set up.
- Team is led by Seidel (physicist) and Hoeferkamp (engineer).
- University of Oklahoma could operate as a second site for testing if necessary.

Next Steps and Remaining Issues:

- Complete evaluation of pre-production prototypes from two vendors. Assemblies are in the process of being bump-bonded using FE-D2S chips.
- Pre-production wafer quality looks good to excellent, so all indications are that the two vendors are ready to fabricate production wafers.
- US schedule has procurement occuring in FY02. There appear to be no obstacles to keeping this schedule.

Deliverables:

US Responsibilities include the following:

- Participate in the design and testing of the sensors.
- Contribute roughly 20% towards the common procurement of prototype and production sensor wafers.
- Cost estimate for production is based on tender quotes. Funding is included in the Management Contingency category with high priority for release.

U.S. ATLAS E.T.C.
WBS Profile Estimates

Funding Source: All **Funding Type:** Project 3/6/01 12:17:25 PM

Institutions: All

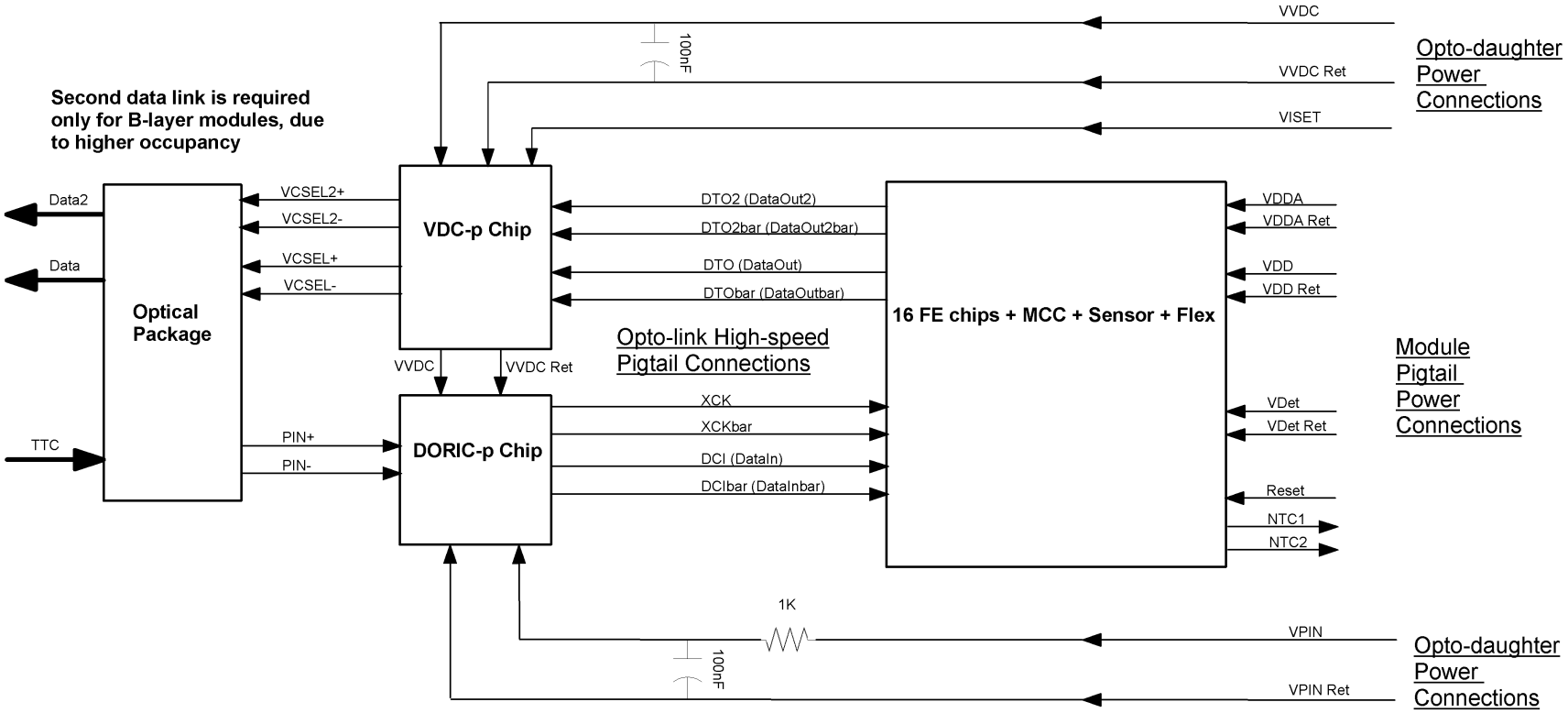
WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.2	Sensors	0	0	0	0	0	97	35	0	0	0	133
1.1.1.2.1	Design/Engineering	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.1.1	Test design	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.1.1.1	Design - New Mexico	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.3	Production	0	0	0	0	0	62	0	0	0	0	62
1.1.1.2.3.1	Barrels, Disks and B-layer(s	0	0	0	0	0	62	0	0	0	0	62
1.1.1.2.3.1.1	Preproduction	0	0	0	0	0	16	0	0	0	0	16
1.1.1.2.3.1.2	Production	0	0	0	0	0	0	0	0	0	0	0
1.1.1.2.3.1.3	Testing	0	0	0	0	0	46	0	0	0	0	46

On-Detector Electronics, Opto-links, Power Distribution

System Design:

- **Pixel Array (Bonn/CPPM/LBL):** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is “requested” by sending LVL1 signal with correct latency. FE chip then transmits corresponding digital hits autonomously.
- **Module Controller (Genova):** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command/control. The 16 FE chips on module connect to MCC in star topology to eliminate bottlenecks and increase fault tolerance.
- **Opto-link (OSU/Siegen/Wuppertal):** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Basic link is 5x5x1.5mm package, and there are two additional small optolink chips with LVDS interfaces. The fibers are rad-hard silica-core stepped-index multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling on module. Low-mass power tapes used to reach patch panels at end of support (PP0, 1m) followed by Al round cable to transition on cryostat wall (PP2, 7m), then conventional cables to USA15 cavern. Filtering, transient protection, and possibly local voltage regulation would be performed on intermediate patch panels.

Summarize all connections required for module operation:



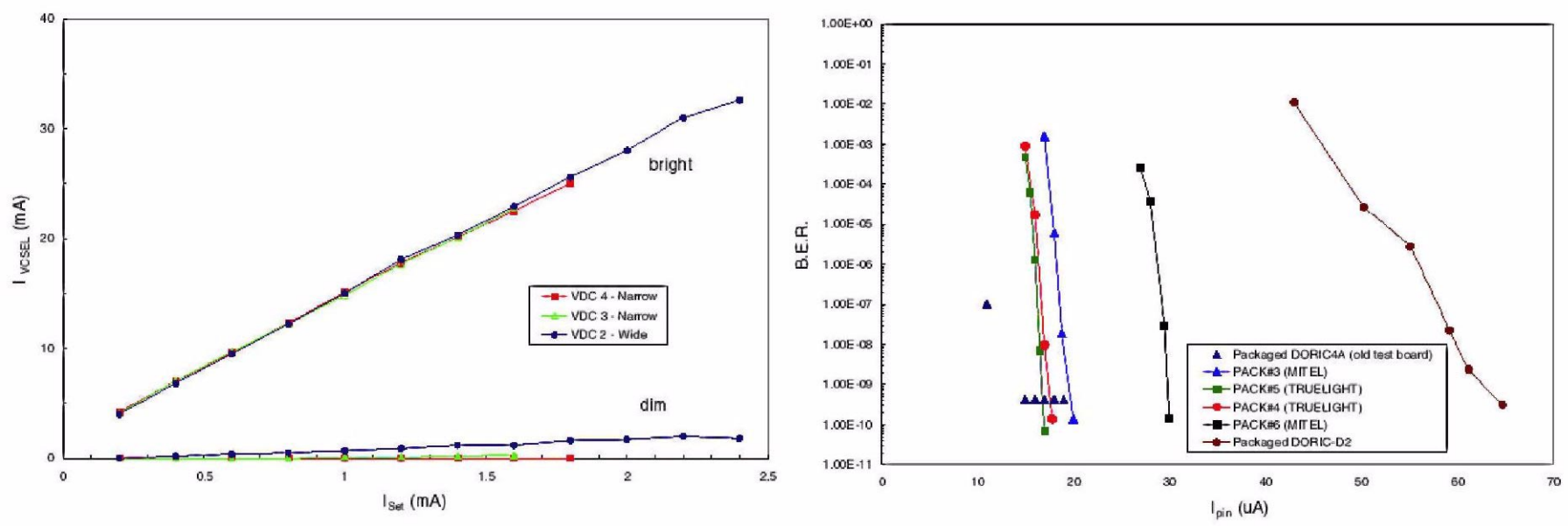
- There are five power supply voltages with their separate returns, and one control voltage that uses VVDCRet as a reference.
- VVDC powers both the DORIC and the VDC, and VPIN may connect directly to the opto-package instead of routing through the DORIC.
- Present concept is that DORIC, VDC and their passive components, plus the Opto-package are placed on Opto-card. Interface requires 3-4 LVDS signal pairs.

Pixel Opto-links:

- All AC signals (clock/commands/data) are transmitted optically to modules:
- **Receiver:** Fiber output is converted using an epitaxial Silicon PIN diode. The output (small current signal) is sent to the DORIC chip, which receives the 40 MHz crossing clock and a bi-phase mark encoded command stream as a single 40 Mbit/s serial stream. It uses a delay-locked loop to extract the clock (providing a high quality 50% duty-cycle clock) and decode the command stream. Note the command stream includes the synchronous LVL1 trigger commands, plus other synchronous commands, and slow configuration commands. An LVDS electrical interface is used to the MCC chip.
- **Driver:** The VDC chip converts LVDS data output streams from the MCC into current pulses suitable for driving the VCSELs chosen for data transmission. For pixel applications, the outer layers plan to use a single 80 Mbit/s output stream (provides roughly a factor 4 of safety), and the B-layer will use two 80 Mbit/s data streams. The format is NRZ, so the 80 Mbit/s link consists of sending a bit on each 40 MHz clock edge. The VCSEL drive current is adjustable using a remotely-controlled voltage. This allows in situ I/L curves, and also periodic operation at high bias to force rapid annealing of radiation damage.
- SCT groups (RAL/Oxford collaboration) have designed and produced two basic chips in pure bipolar AMS design. They work well, but do not withstand pixel doses. For several reasons, pixels have converted designs to rad-hard CMOS.

Status of Pixel DORIC and VDC:

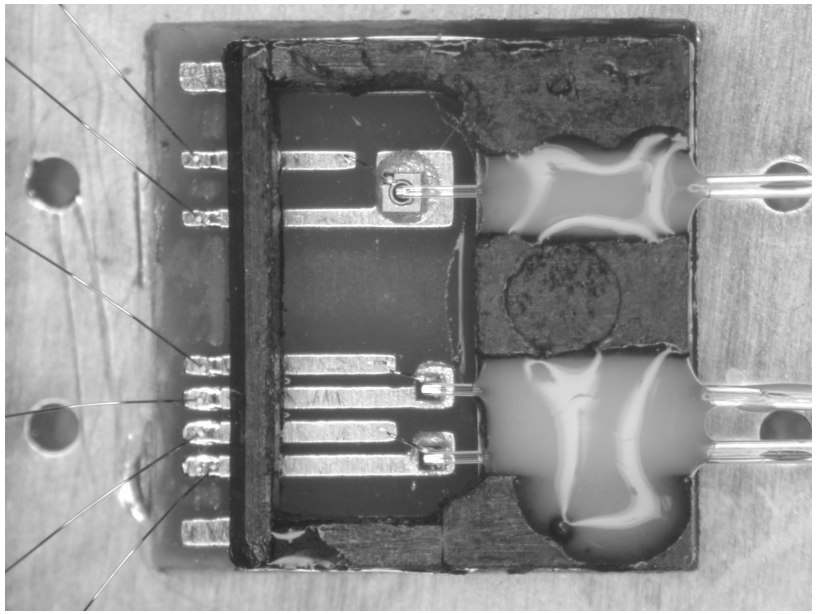
- OSU and Siegen converted SCT design from AMS bipolar to DMILL CMOS. Chips included in FE-D1 submission. VDC-D1 worked fairly well, DORIC-D1 had several design errors related to poor modeling of parasitics.
- Second generation fabricated in FE-D2 submission. DORIC-D2 now works fairly well, but only when used as a bare die very close to opto-package:

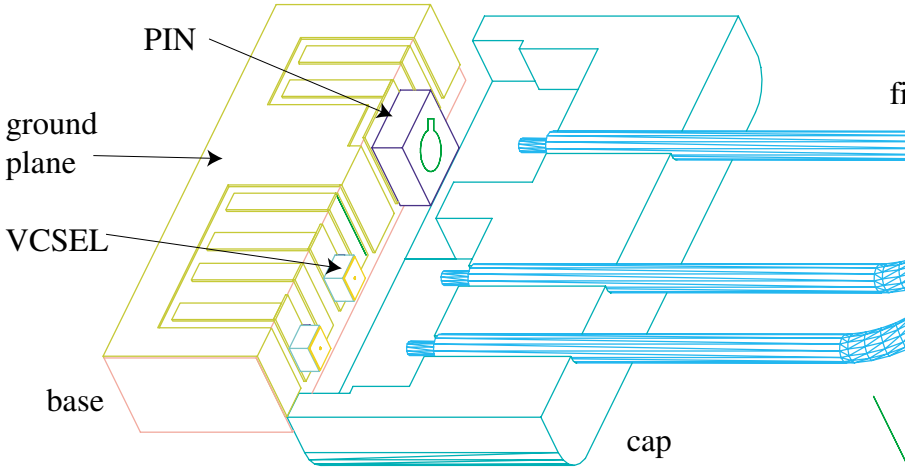


- VDC-D2 shows problem with behavior of dim current (should be constant 1mA).
- DORIC-D2 suffers from preamp DC offsets, and general has a somewhat higher error rate than the SCT DORIC-4A chip. However, it appears to meet specs.
- In Feb, submitted 0.25µ prototype VDC-I and DORIC-I with fixes for these errors. For now, treat both DMILL and 0.25µ as candidate technologies for opto-chips.

Status of Opto-package development:

- Original SCT development was done with Marconi. Package design appeared very expensive and complex. Idea was to develop a cheap and simple package.
- Both Taiwan and OSU have worked on different approaches to this problem.
- Agree to use SCT-qualified PIN (Centronics) and VCSEL (Mitel). These elements have been evaluated in neutron, gamma, and proton beams up to pixel fluences.

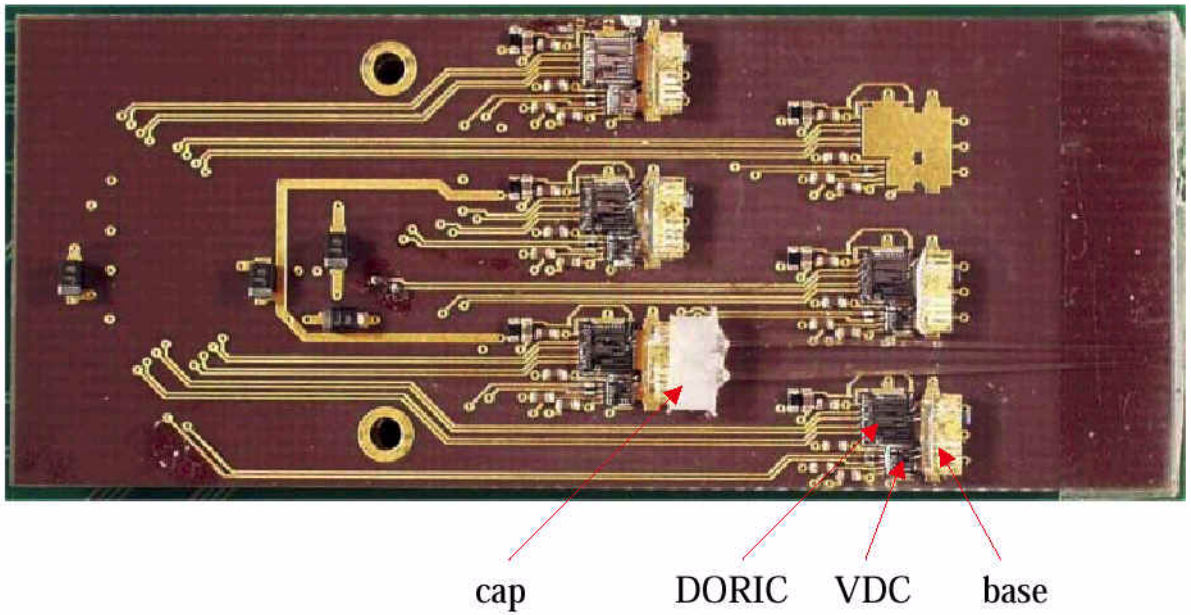




- Taiwan package (left) uses layered PCB, special 45 degree fiber cleaving, and active alignment to achieve good performance.
- OSU package (right) uses molded components and precise tooling to build in performance at low cost, but with larger dispersion in output power.

Opto-Card Concept for Mounting Opto-links

- Original concept was to keep fast timing signals in optical form until very close to the pixel module. Given the very challenging services integration in the pixel detector, especially the barrel, this has proven to be difficult.
- Present concept involves grouping opto-links at the ends of the Global Support structure (attaching them to PP0). This consolidates fiber interface and opto-packages onto a single card with electrical connection to PP0. This separate unit can be fully tested and burned in prior to installation. In addition, all opto-links are at a radius of 15cm, decreasing problems due to SEU effects at smaller radii. This does require high quality electrical pigtails to pixel modules to avoid EMI.

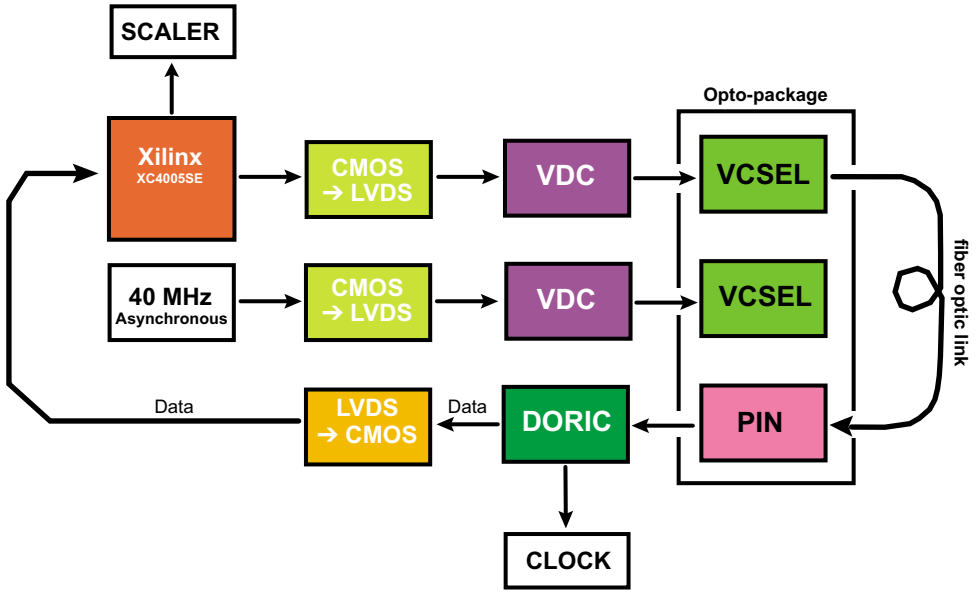


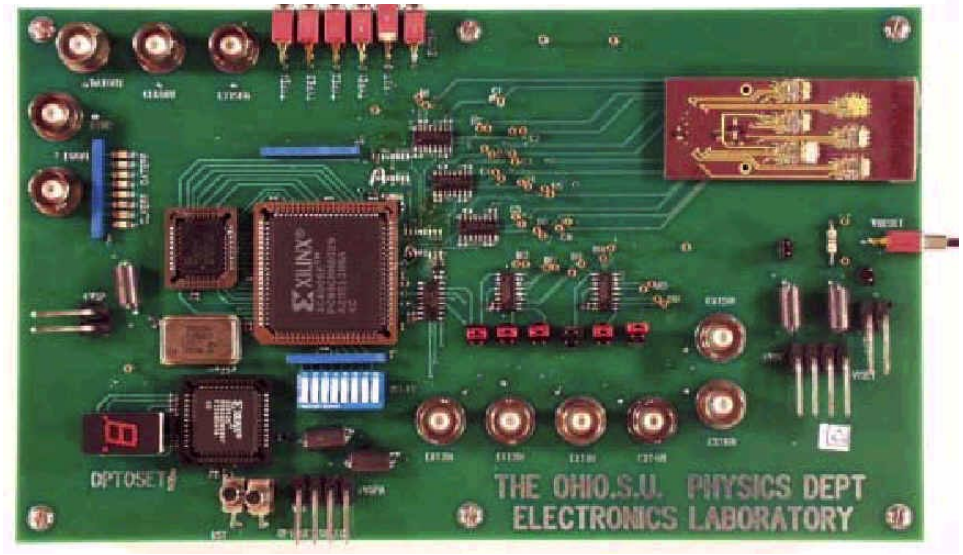
Prototype OSU opto-card.

Final version would be more compact, use BeO ceramic for support, and would use more optimal opto-package design with separate PIN and VCSEL packages.

Test System for Opto-chips and Opto-links

- OSU has built a first prototype of a high-performance opto-link tester, designed to be used for testing a complete opto-card.





- Use VDC and VCSELs as data source, and DORIC and PIN as data decoder/receiver.
- Can loop-back within the same opto-package for now since opto-packages are rare.
- Final system would use off-detector elements coupled by realistic fiber ribbon to opto-card under test.
- This means using a BPM chip and VCSEL array to generate input data, and a DRX chip and PIN array for receiving output data.

Irradiation qualification:

- Collaborative effort of SCT and pixels (Wuppertal from pixels) have performed systematic irradiation studies of optical fibers and opto-elements (PINs and VCSELs) up to pixel fluences. Results show no significant risks, provided PIN is operated with adequate bias voltage (up to about 7V), and provided VCSELs are operated with sufficient bias current (up to about 20mA).
- Only known issue at this time is single event upsets caused by interactions in the very thin epitaxial layer of the PIN diode. Irradiations at PSI showed a significant effect, but at the new radius of the opto-cards, this should not produce a BER of more than about 10^{-9}.
- Pixels has recently significantly upgraded the MCC command set to be highly fault tolerant. Critical commands (particularly LVL1) are successfully decoded under any single bit error, and are only mis-interpreted under double bit error.

Next Steps:

- During April 01 PS run, a complete opto-card will be irradiated, and evaluated during the irradiation using OSU opto-link test system.
- New 0.25µ versions of opto-chips submitted in Feb, expected back by end May.
- Have scheduled ATLAS review to decide on opto-package supplier in June 01.
- Finalizing design of opto-package and opto-card to match requirements of services layout for Insertable Pixel design.

Deliverables

US Roles

- Contribute to design of opto-chips (VDC and DORIC) in DMILL and 0.25μ processes.
- Contribute 50% towards opto-chip fabrication. Baseline in cost estimate is conservatively assumed to be DMILL.
- Probe 50% of opto-chips.
- Supply fraction of opto-cards corresponding to number of modules in the disks.

Electronics Challenges and Requirements

Main challenges are in FE chips:

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an “in-time” threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 300e) and low noise (about 300e).
- Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- Meet specifications with nominal analog power of 40μW/channel and nominal total power for FE chip of 200mW (worst case budget is 70μW and 350mW).

Status of MCC chip:

- First version fabricated by Genova in AMS technology. Chip is roughly 70 mm^2, and 400K transistors. Other than a few very minor errors, it works well.
- Second generation (final design) fabricated in DMILL process. Chip is 100 mm^2. Observed yield is poor (less than 10%), so now working on 0.25μ version.

FE Electronics Prototypes

Several generations of prototypes have been built:

- First “proof of principle” chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C). These were 18 column, 160 row chips with 50μ x 400μ pixels.
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Initial rad-hard activity focussed on common design DMILL chip (FE-D), followed by common design Honeywell chip (FE-H).

Features of initial rad-hard FE design:

- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

Initial Radiation Hard Strategy

Pursued essentially identical designs with two vendors:

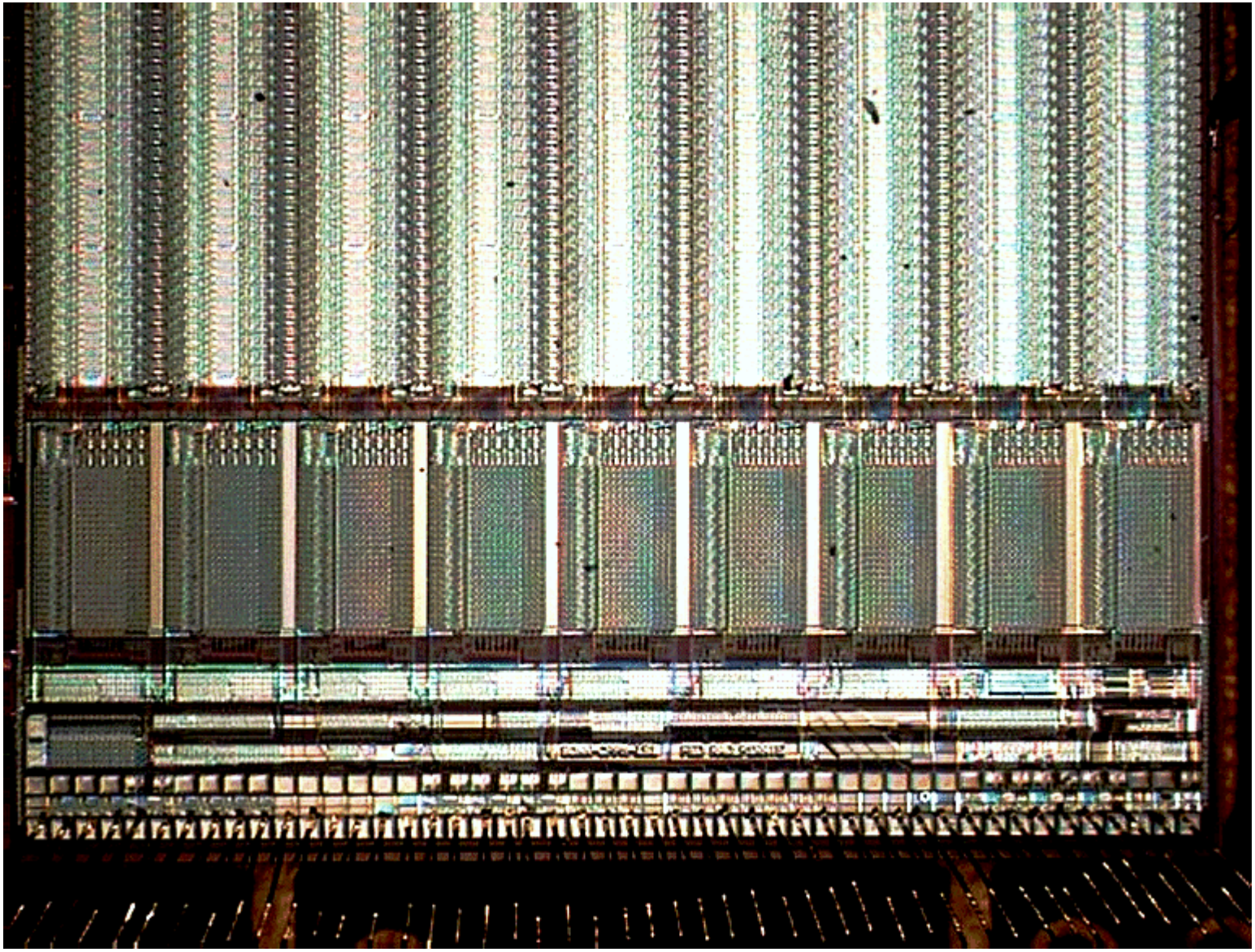
- **ATMEL/DMILL:** Began first work on FE-D in Summer of 98. FE-D1 run was submitted to TEMIC on Aug 10 99. Design contained some “simplifications” in digital readout from FE-B design to fit into DMILL constraints, as well as some improvements. Performance targeted at outer layers, with 400μ pixel and 24 EOC buffers per column pair.
- Comments: Initial version of front-end chip (FE-D1) showed very poor yield, concentrated in two circuit blocks. Second set of wafers for initial run were processed (FE-D1b), and showed same behavior. Extensive testing pointed towards technology problems. Second run was made, with two versions and many minor bug fixes (FE-D2). Will summarize these results.
- **Honeywell/SOI:** Began serious work on FE-H in Fall 99. At this time, only LBL and CERN had TAA agreements in place to do design. In addition, Honeywell was in process of revising Layout Rules, which caused significant delays. A number of minor improvements relative to FE-D, taking advantage of better device density and third metal layer. Design was made more robust, and performance was targeted at B-layer as well (400μ pixel with 32 EOC buffers).
- Comments: Had completed almost all layout work and were just starting verification in July 00, when we learned of cost increase to $20K$/wafer in large quantities. This made continued work impractical, and this path was abandoned.

Summary of FE-D1 DMILL Run

Reticle included many die (10 in total):

- Two pixel FE chips (FE-D). Several errors were found and reproduced in simulation. Two significant yield problems are believed to originate in TEMIC fabrication problems, and made operation of the chips very difficult.
- Prototype MCC chip. A prototype of several key elements of final MCC, about 20mm^2 core size. Included FIFO block for final chip, plus large synthesized command decoder block. Observed yield of about 80% for small die. Irradiations of 8 packaged die to 30MRad carried out at PS in Oct 00. All die survived irradiation, but many no longer function correctly after several months. Problems under investigation.
- Prototype CMOS opto-link chips (one DORIC-p and three VDC-p). Results discussed previously.
- Additional test chips: LVDS buffer for rad-hard test board, PM bar with W/L arrays and special pixel transistors, Analog Test chip with all critical FE-D analog elements. All work well, and transistor parameter measurements suggest run is slightly faster than typical. Many detailed characterizations of Analog Test Chip.
- Second half-lot (FE-D1b) processed several months later with minor metal layer changes, and observed same poor yield results for FE-D chips.

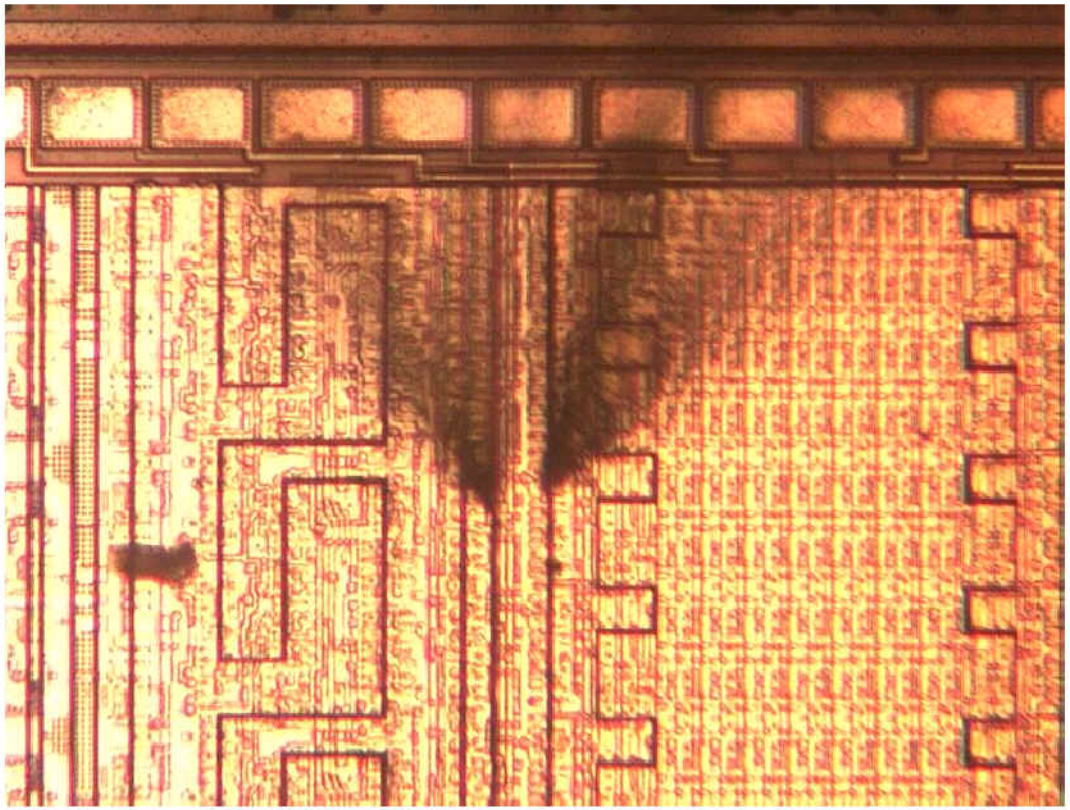
Details of Bottom of Chip:



- Layout is very dense, with 400μ pixel and overall die completely full of circuitry.

Example of Defect Analysis in Yield Studies

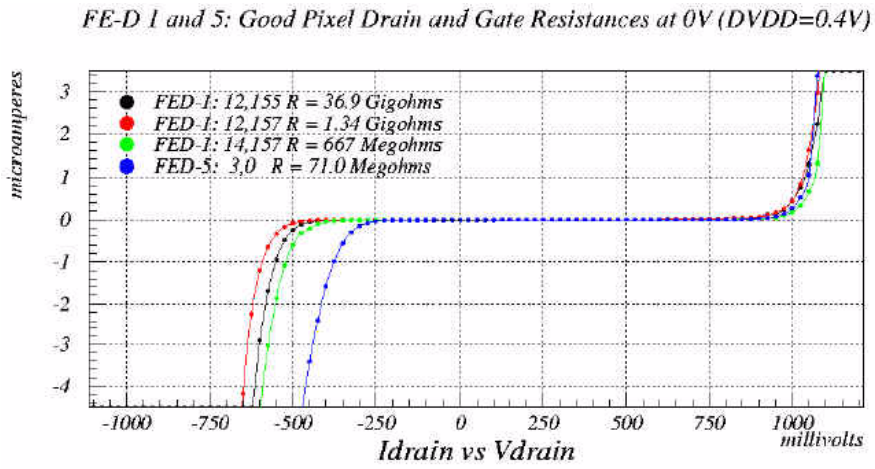
- Two chips which had been characterized in the lab had series of 20 small (8μx8μ) pads deposited by FIB surgery to allow probing of suspect “leaky NMOS”.
- Measurements were made of DC performance of the suspect device (somewhat complex to interpret since they are done in situ), as well as the dynamic performance (using an FET Picoprobe) of waveforms during operation.

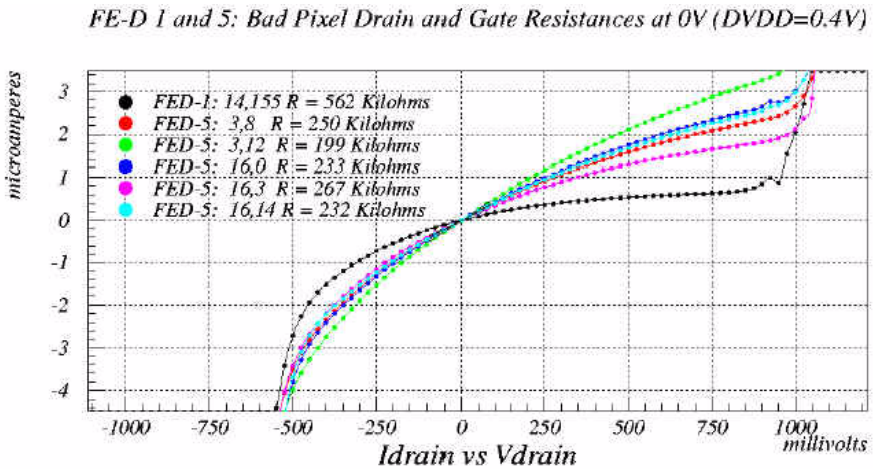


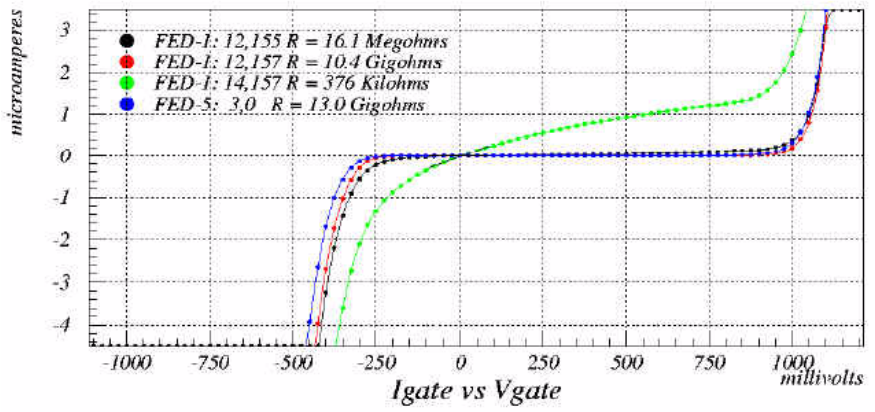
- Two 10μ probe needles place on pads. One pad was on the drain, the second on the gate of the suspect NMOS.

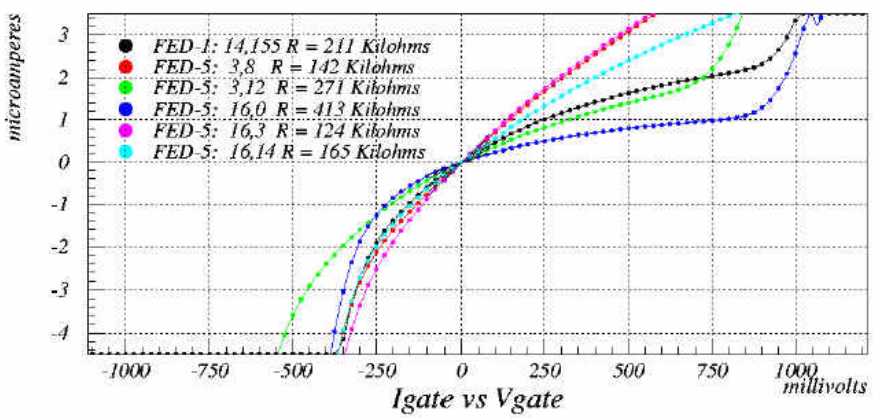
- Both DC and dynamic measurments confirm existence of defective NMOS’s.

DC curves for pixels previously classified good/bad:



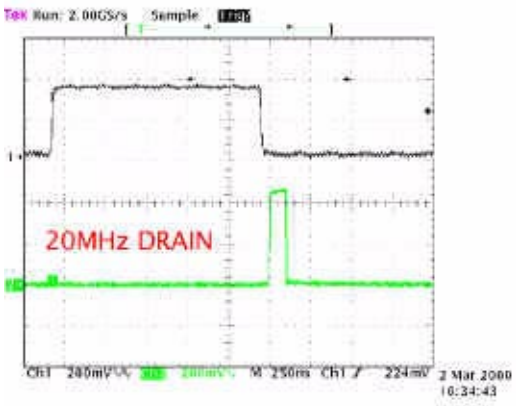


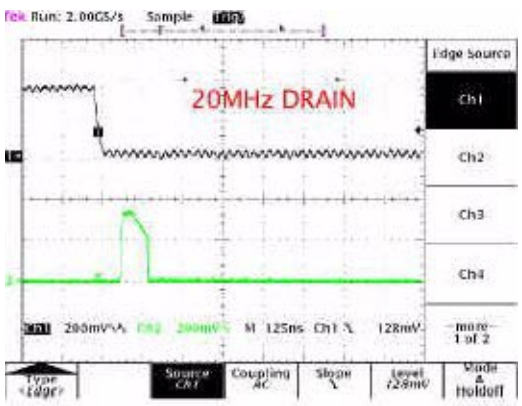


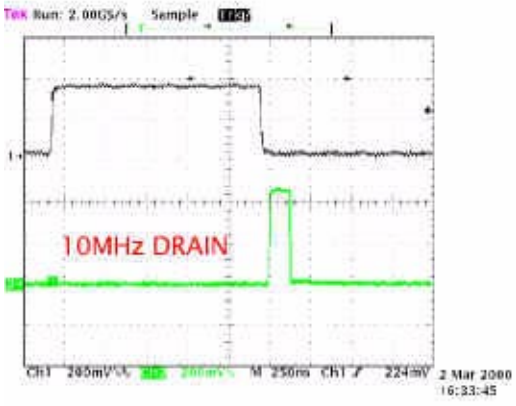


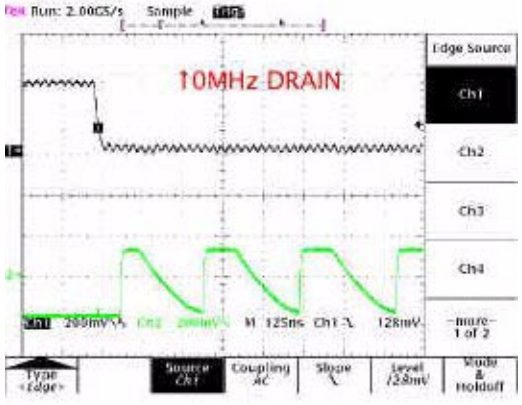
- Bad pixels consistently show apparent drain-source resistance in off state of a few 100's of KOhms. Good pixels show resistance of many orders of magnitude larger, with actual value most likely limited by Tungsten residue after FIB pad deposition.

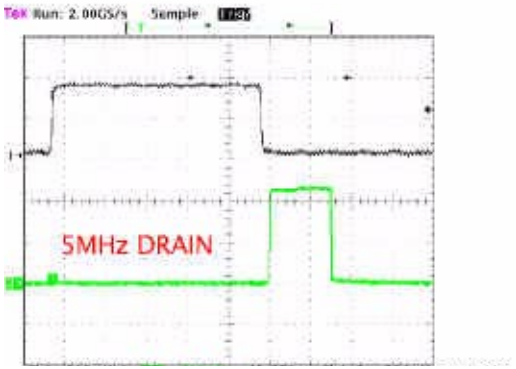
Dynamic measurements of a good and a bad pixel:

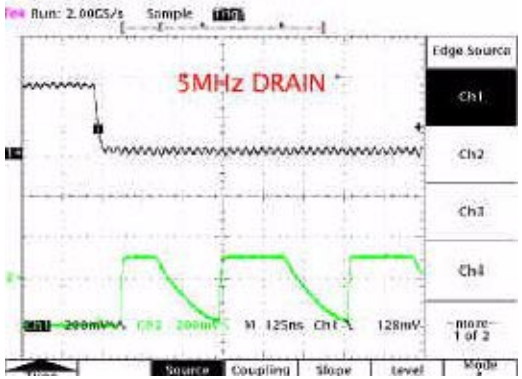








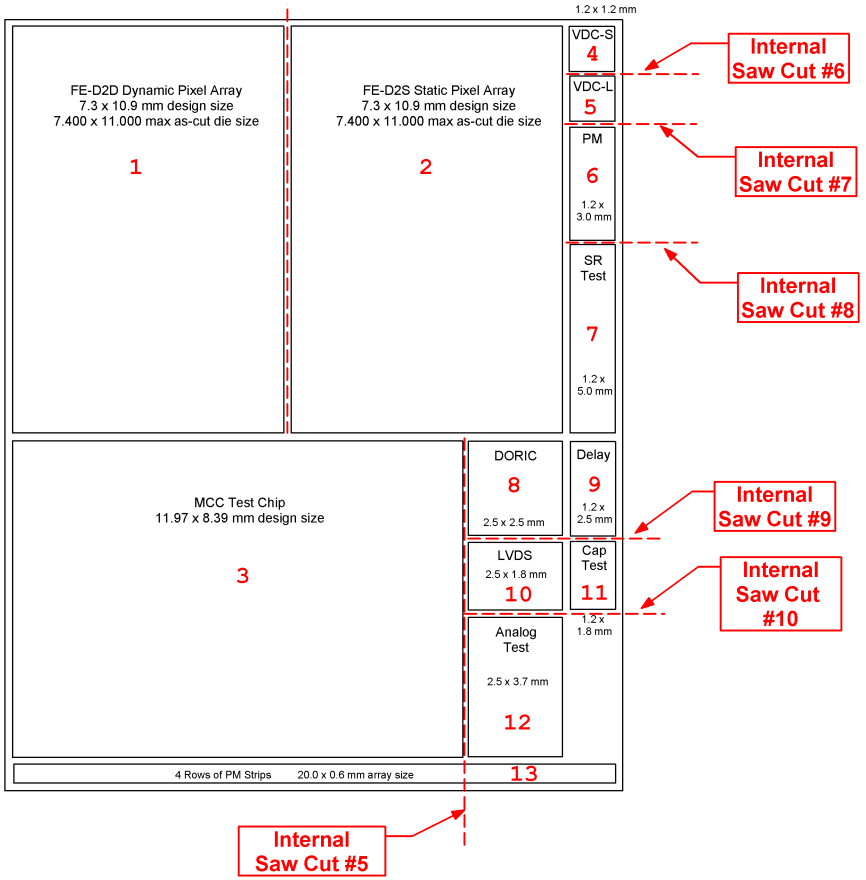




- Measurements of the state of the dynamic node (green trace) were made directly using FET probe (20fF load capacitance).
- Good pixels show stable logic high value over relevant timescale.
- Exponential slope for bad pixel corresponds to dynamic phase when logic value is “leaking” away.
- Depending on clock frequency for column readout, it is possible to produce a “digital oscillation”

Summary of FE-D2 Run

- Submitted second run to ATMEL for fabrication July 26 00. ATMEL agreed to fabricate a standard prototype run (8 wafers delivered), plus a special collection of 9 corner runs where three separate parameters were varied (Leff, poly etch, and contact etch). The goal was to look at yield correlations to understand the technology problems observed in the FE-D1 run.



- Run included two versions of the FE chip. One with same design but all known errors fixed (FE-D2D), and one with the two low-yield dynamic blocks (Hit Logic and Pixel Register) replaced with static versions but with threshold trim circuitry removed (FE-D2S).
- Included MCC-D2 as a complete design addressing the final pixel system needs. Also included second generation opto-chips, and several test chips.

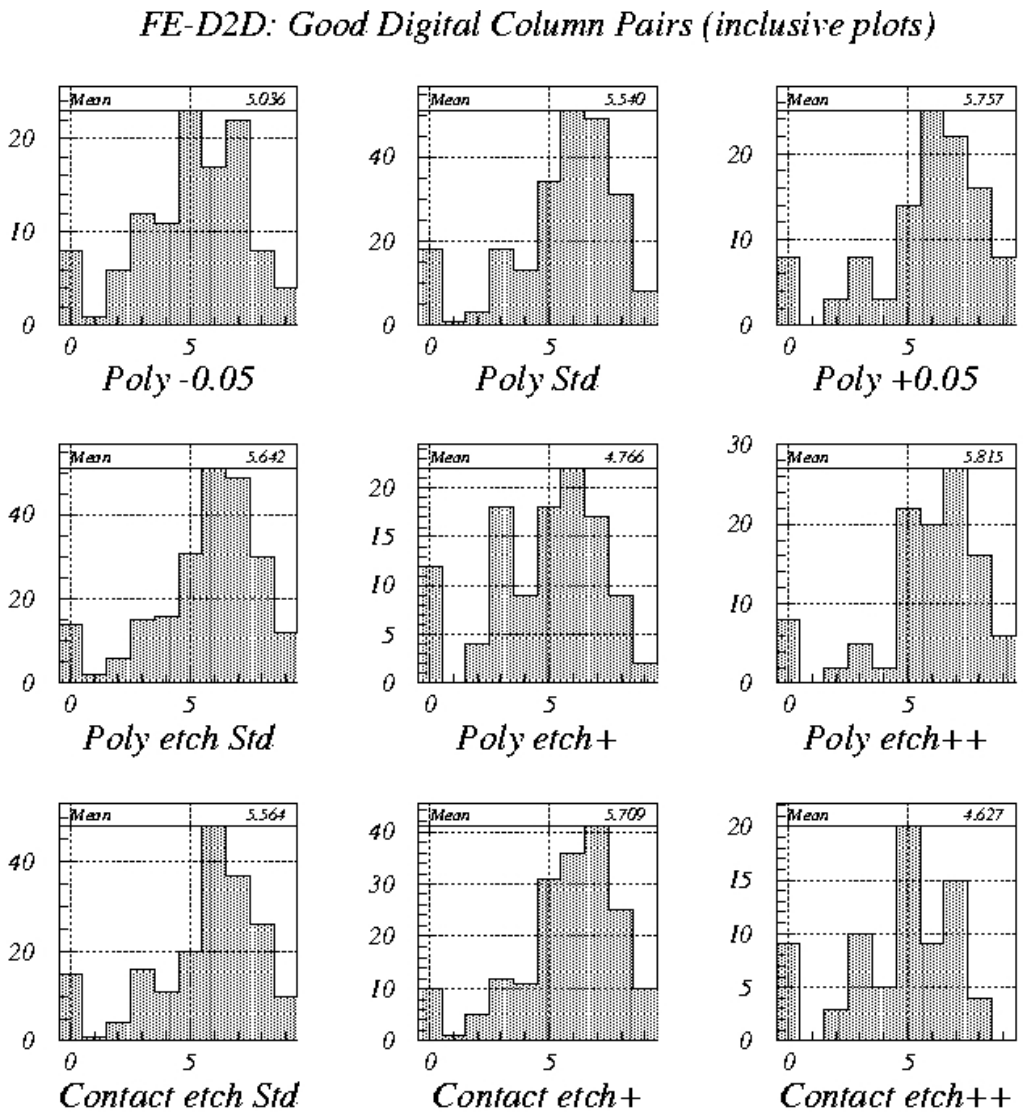
Results from FE-D2 Run

- Yield for original design (FE-D2D) was similar to the FE-D1 run, and still unacceptable:

FE-D2D (DYNAMIC IMPLEMENTATION) STANDARD WAFERS							
	GLOBAL REGISTER	PIXEL REGISTER		GOOD COLUMN PAIRS		PERFECT COLUMN PAIRS	
WAFER	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*
03	39/39 100%	334/351 95%	30/39 77%	155/334 45%	0/30 0%	47/334 14%	0/30 0%
04	38/39 97%	337/342 99%	33/38 87%	204/337 61%	0/33 0%	47/337 14%	0/33 0%
05	41/42 98%	348/369 94%	22/41 54%	154/348 44%	0/22 0%	66/348 19%	0/22 0%
06	41/42 98%	310/369 84%	27/41 66%	169/310 55%	0/27 0%	71/310 23%	0/27 0%
07	41/42 98%	329/369 89%	26/41 63%	161/329 49%	1/26 4%	57/329 17%	0/26 0%
08	41/42 98%	324/369 88%	25/41 61%	183/324 57%	0/25 0%	69/324 21%	0/25 0%
09	42/42 100%	348/378 92%	30/42 71%	200/348 57%	0/30 0%	75/348 22%	0/30 0%
10	33/42 79%	241/297 81%	16/33 48%	118/241 49%	0/16 0%	32/241 13%	0/16 0%

- Minimal digital test criteria are working Global and Pixel Register and nine Good Columnpairs. Only one chip in 8 wafers satisified these requirements !

- Comparison of yield distribution for each corner run parameter value does not show any correlation with the processing variations tried by ATMEL:



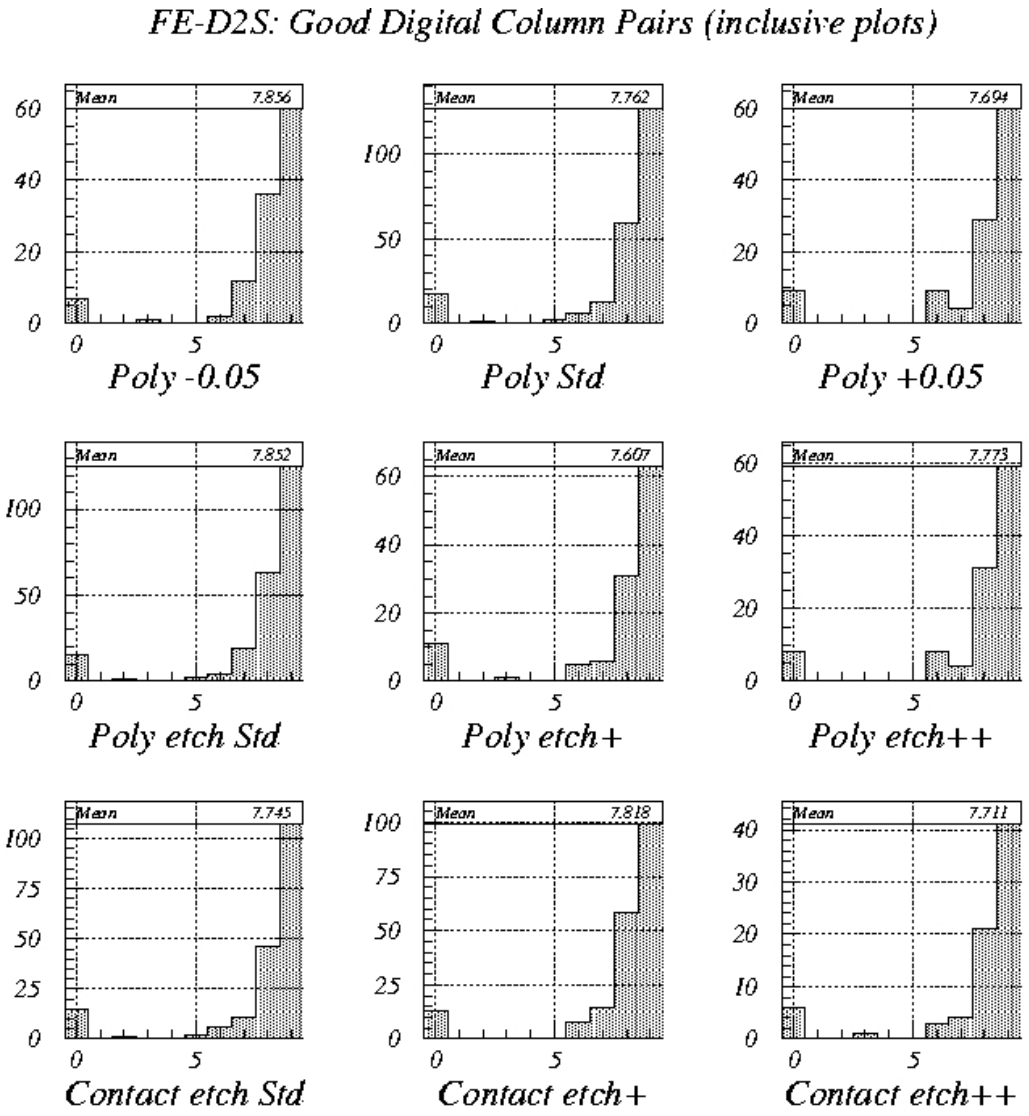
- Corner runs included 8 corners with 2 wafers each plus standard set with 6 wafers. We received a subset of 16 of these 22 wafers for evaluation.
- Bin data according to particular value for each of the three parameters (actual runs varied more than one parameter in some cases).
- No combination observed with improved yield.

- Yield for FE-D2S design looked much more promising:

FE-D2S (STATIC IMPLEMENTATION) STANDARD WAFERS								
	GLOBAL REGISTER	PIXEL REGISTER		GOOD COLUMN PAIRS		PERFECT COLUMN PAIRS		MEAN BAD PIXELS
WAFER	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER GOOD CHIP*
03	40/40 100%	349/360 97%	34/40 85%	299/349 86%	18/34 53%	244/349 70%	3/34 9%	101/18 = 5.6
04	40/40 100%	356/360 99%	37/40 93%	319/356 90%	23/37 62%	282/356 79%	12/37 32%	33/23 = 1.4
05	40/40 100%	355/360 99%	36/40 90%	324/355 91%	29/36 80%	279/355 79%	6/36 17%	88/29 = 3.0
06	43/43 100%	327/387 85%	29/43 67%	274/327 84%	16/29 55%	190/327 58%	2/29 7%	135/16 = 8.4
07	41/43 95%	336/369 91%	32/41 78%	284/336 85%	22/32 69%	238/336 71%	8/32 25%	49/22 = 2.2
08	41/43 95%	325/369 88%	30/41 73%	298/325 92%	21/30 70%	247/325 76%	6/30 20%	56/21 = 2.7
09	42/43 98%	371/378 98%	38/42 92%	297/371 80%	15/38 39%	235/371 63%	2/38 5%	94/15 = 6.3
10	40/43 93%	298/360 83%	26/40 65%	224/298 75%	11/26 42%	181/298 61%	1/26 4%	54/11 = 4.9

- Observe decent yield for simple digital tests (about 50%), but almost all chips had some bad pixels.

- Small correlations with corner runs were observed for Pixel Register yield and single bad pixel fraction. No other global yield correlations seen:



- FE-D2S chips looked sufficiently promising that decided to pursue a complete evaluation program for them.
- Large threshold dispersion with no TDACs makes operation and characterization of the chips more challenging.

Status of Rad-Hard Developments in 0.8μ

Continuing to evaluate chips from FE-D2 run:

- FE-D2S wafers being bump-bonded into single-chip and 16-chip module assemblies using 6 wafers at two vendors (AMS and IZM) for further study.
- FE-D2S single die have been irradiated recently at LBL 88" Cyclotron. First results show some circuit elements survive to 50MRad, and others do not:

FE-D2S being tested at 88" Cyclotron using N_2 coldbox to irradiate at about -5 C.

- Irradiations taking place using opto-chips (VDC-D2 and DORIC-D2) in the April PS run. Further irradiations of FE-D2S could be performed at the PS in May, and irradiations of MCC-D2 could be performed in July.
- Further testing of MCC-D2 continuing. However, low yield (less than 10%) makes the testing difficult. Problems in event building still being studied.
- ATMEL presently running new experimental lots using different epi deposition vendor for wafer preparation. Should get wafers for evaluation in late May.

Factors driving us to suspend design work on FE-D/MCC-D:

- Design short-cuts required to fit into available space. Process density lower than expected, dynamic logic used in several blocks poses SEU and yield problems.
- Experience with yield and technology quality. Even for FE-D2S, observe significant number of isolated defects (bad channels, both digital and analog).
- Problems with radiation hardness for our application. Device parameter shifts very large, and often seem to observe “mysterious” circuit failures in large chips.
- Relatively high cost (given low and erratic yields) and lack of future for process.
- Honeywell SOI work suspended as of July 2000 due to large cost increases.

Present direction:

- All design effort is being directed to the use of commercial 0.25μ processes with radiation tolerant layout rules.

Deep Sub-micron Approach:

- One of dominant effects of irradiation of CMOS devices is creation of trapped charge in the critical gate oxide layers. Below about 10nm oxide thickness, the charge trapping largely vanishes due to quantum tunneling effects. Modern 0.25μ processes are the first to operate fully in this regime (they have 5-6nm oxides).
- The RD-49 collaboration has studied details, confirming that if one controls leakage paths using layout, then a commercial 0.25μ process can be very rad-hard (circuits tested to 30MRad). Many technical concerns addressed, but basically little experience with full-scale devices, so some concerns still remain.
- All experience so far with analog and digital designs suggests that the silicon behaves almost exactly like the SPICE BSIM3 simulations. Nevertheless, given our lack of experience with these processes, we are making several prototypes.
- CERN has negotiated a frame contract for LHC with IBM for their CMOS6 0.25μ process which extends through 2004. This fixes prices and terms for engineering and production runs, and would provide the basis for our production procurement. We can also access the TSMC 0.25μ process in production quantities via the MOSIS consortium as a back-up should problems arise.
- This path places us into commercial mainstream, where we can be assured of low prices and availability in the future. Depending on R&D in 0.18μ and smaller feature sizes, it provides a technology path for upgrades to the B-layer. By 2005, roadmaps suggest “baseline” process would be 0.10μ 9-metal, operating at 1.0V.

Test System for FE Chips and Modules

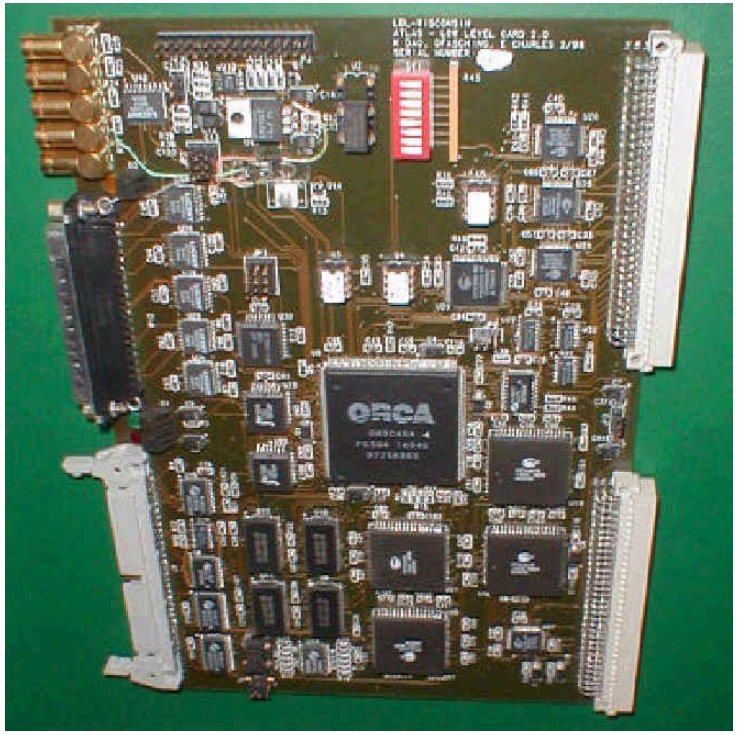
History:

- LBL/Wisconsin developed original test system in 97/98 for use with initial rad-soft pixel “demonstrator” prototypes.
- This system has been successfully used for wafer probing, and characterizing single chips and modules in the lab and in the testbeam.
- A total of 16 such systems are presently in use throughout the pixel collaboration. They are the standard with which all chips and modules are evaluated.
- The use of a common, high-performance test system for this full range of activities has allowed greater efficiency and easier comparison of results.

Overview:

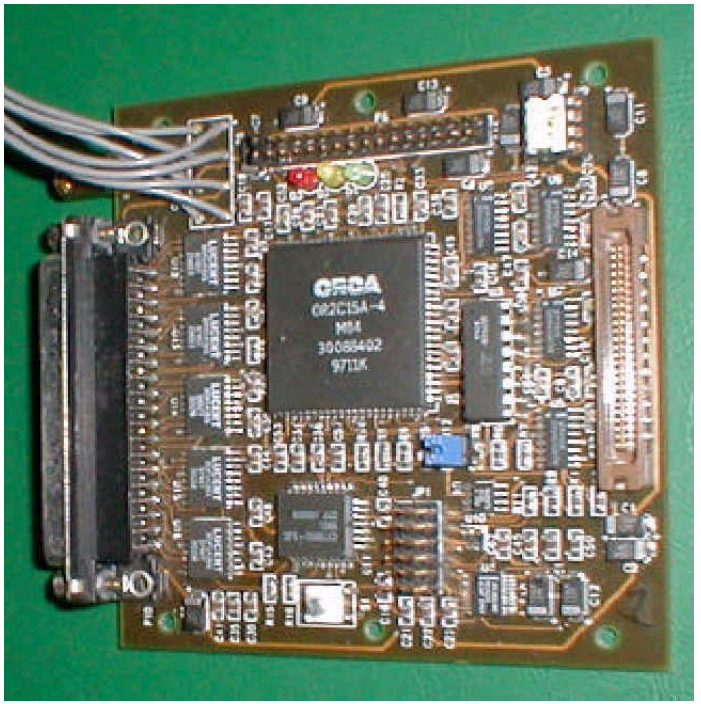
- The system consists of a PC host running National Instruments software environment and one or more VME boards (so-called PLL).
- Each VME board drives a local control card (PCC) over a long cable (20m), which in turn drives the individual test cards (support cards) over a short cable (1m).
- There are now several generations of test cards supporting the different applications from wafer probing to single chip testing to bare module testing and the first two generations of Flex modules.

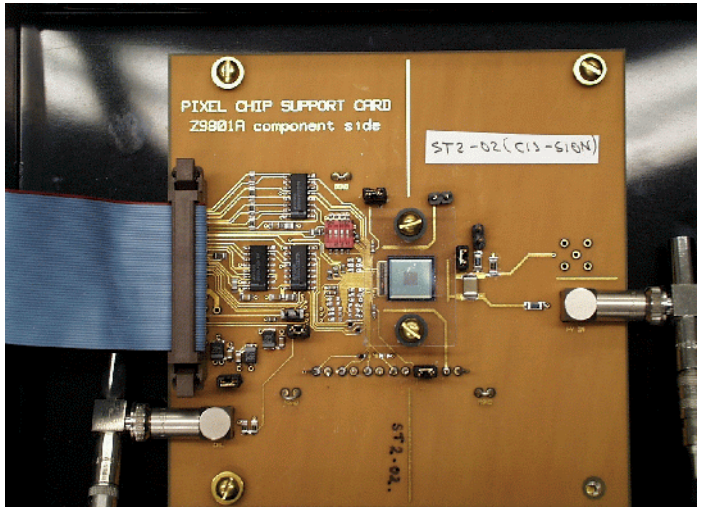
Components of Current Test System:

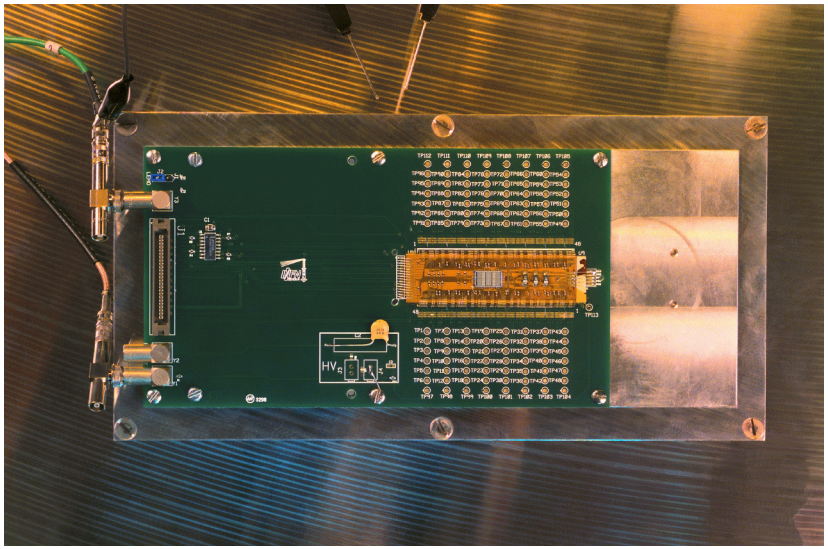


PLL

PCC





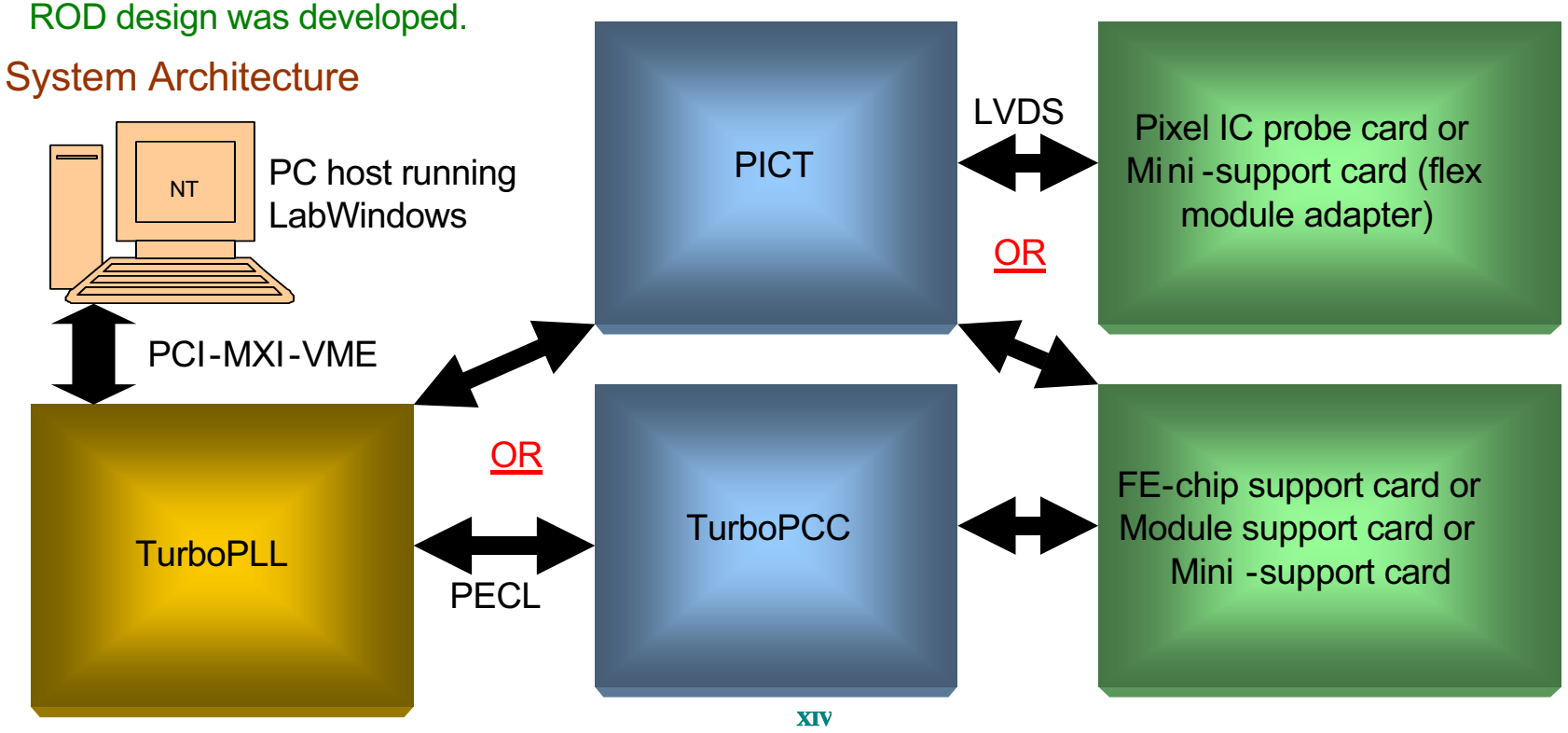


Upgraded Test System

- New generation under design. Incorporate experience with present system, and optimize to cover complete range of production needs with one modular set of hardware and software, keeping same basic interfaces to provide flexibility.
- Includes upgrades for greater range of test capability (vary amplitudes and timing), plus optimized buffering and variable frequency testing:

Architecture is directly based upon the original PLL approach, which had proven so ideally tailored to our needs and which represents the model upon which the ATLAS ROD design was developed.

System Architecture



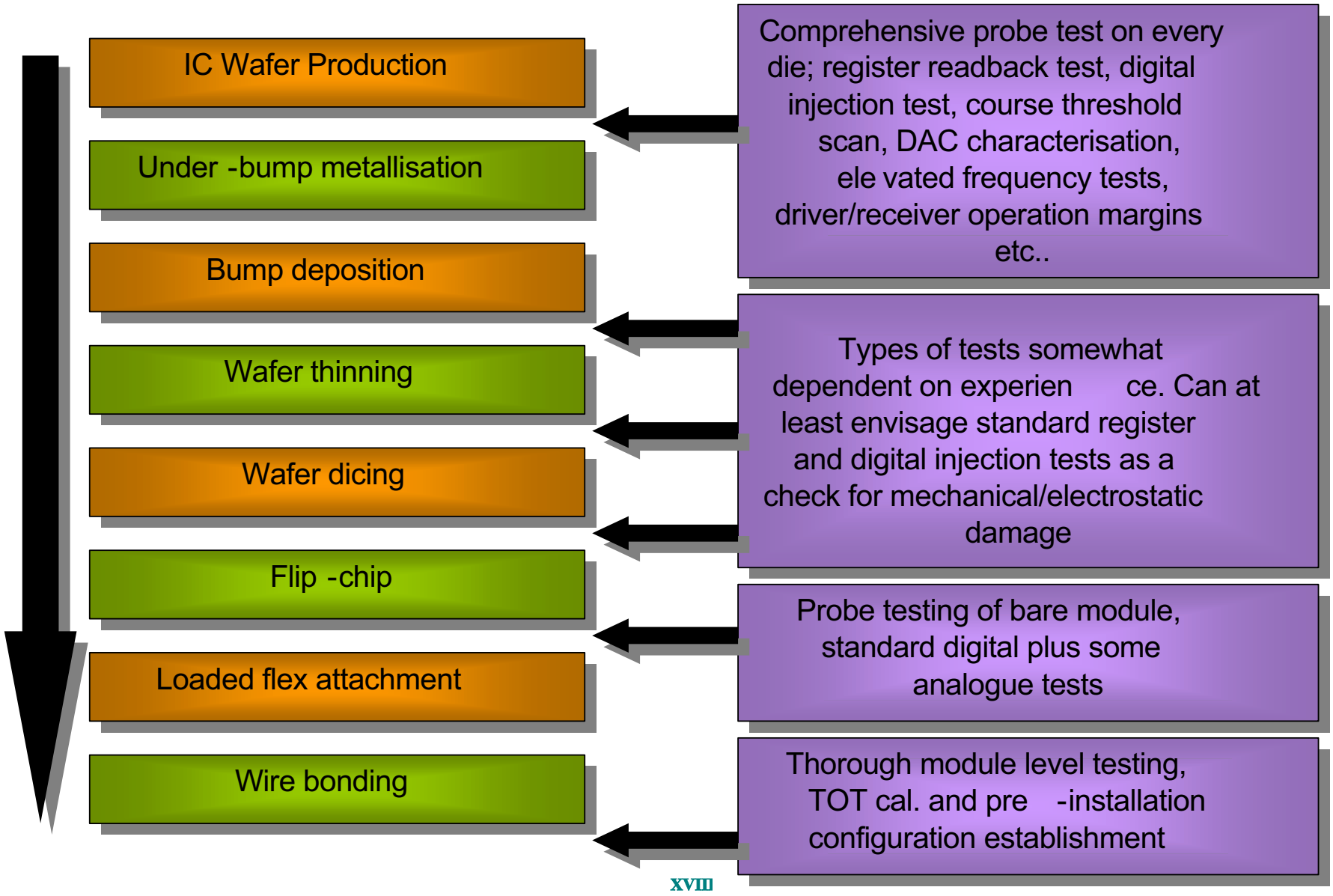
Design Goals:

- New system allows complete evaluation of operating margin available in each chip. Optimized cuts can then be used to select die and modules that should continue to work properly after full lifetime radiation doses.
- Cover wider range of needs, including parametric testing at all stages from initial wafer probing, to module testing, and module burn-in.
- System designed to allow operation over wide range of supply voltages, from a minimum of 1.6V up to 4V, to cover testing of 0.8µ and 0.25µ (and below) chips.
- New system will be operating in time for complete characterization of 0.25µ FE-I chips described in next talk.

Schedule:

- TurboPLL design is complete. Transfer of VHDL from previous system is complete, almost all upgrades now defined and written. Board layout is complete, but optimizing routing of critical high-speed paths. Should go out for fabrication within next month. Components purchased for first 10 cards.
- PICT/TurboPCC schematics are complete, board layout starting in April. Most components in hand for initial construction of 5 PICT cards.
- Higher performance probe card designed and simulated.
- On schedule to deliver total of 15 PLL/PCC systems and 5 PLL/PICT systems to the pixel collaboration this calendar year.

Production Testing Plans



- New system addresses range of needs from wafer probing to module burn-in.

Deliverables:

US Responsibilities include:

- FE chip design, testing and production (LBL): Contribute roughly 20% towards the common procurement of the series production. Test roughly 50% of FE ICs.
- Opto-link chip design, testing and production (OSU): Contribute approximately 50% towards the common procurement of the series production.
- Design and provide hardware/software for lab/testbeam single chip and module testing, production FE wafer probing, production module testing/burn-in (LBL).

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.3	Electronics	0	0	0	0	0	615	621	354	26	0	1616
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	446	161	0	0	989
1.1.1.3.1.1	IC design	0	0	0	0	0	189	269	11	0	0	469
1.1.1.3.1.2	Test design	0	0	0	0	0	140	75	0	0	0	216
1.1.1.3.1.3	Systems Engineering	0	0	0	0	0	52	101	151	0	0	304
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	234	133	0	0	0	367
1.1.1.3.2.1	Atmel/DMILL prototypes	0	0	0	0	0	130	0	0	0	0	130
1.1.1.3.2.2	Honeywell	0	0	0	0	0	10	0	0	0	0	10
1.1.1.3.2.3	0.25 Micron	0	0	0	0	0	0	54	0	0	0	54
1.1.1.3.2.4	Test	0	0	0	0	0	94	79	0	0	0	173
1.1.1.3.3	Production	0	0	0	0	0	0	42	193	26	0	261
1.1.1.3.3.1	Front-end ICs	0	0	0	0	0	0	19	140	26	0	185
1.1.1.3.3.2	Optoelectronics	0	0	0	0	0	0	23	53	0	0	76

Summary and Conclusions

Sensors:

- Extensive design and prototype program now complete. Prototype performance, including operation after lifetime radiation doses, is acceptable.
- Oxygenated material provides significant increase in operating margins (lifetime dose and access scenarios) and will be used for production sensors.
- Pre-production with two final vendors completed and under evaluation.
- Would be ready to proceed with production order later this year.

Opto-links:

- Second generation of opto-chips in DMILL are working relatively well. System-level evaluations will continue using complete opto-card with 6 opto-links.
- Improved design submitted in 0.25μ. Both DMILL and 0.25μ processes remain candidates for opto-chip production.
- Expect to select package in June 01, and proceed to finalize opto-card design.

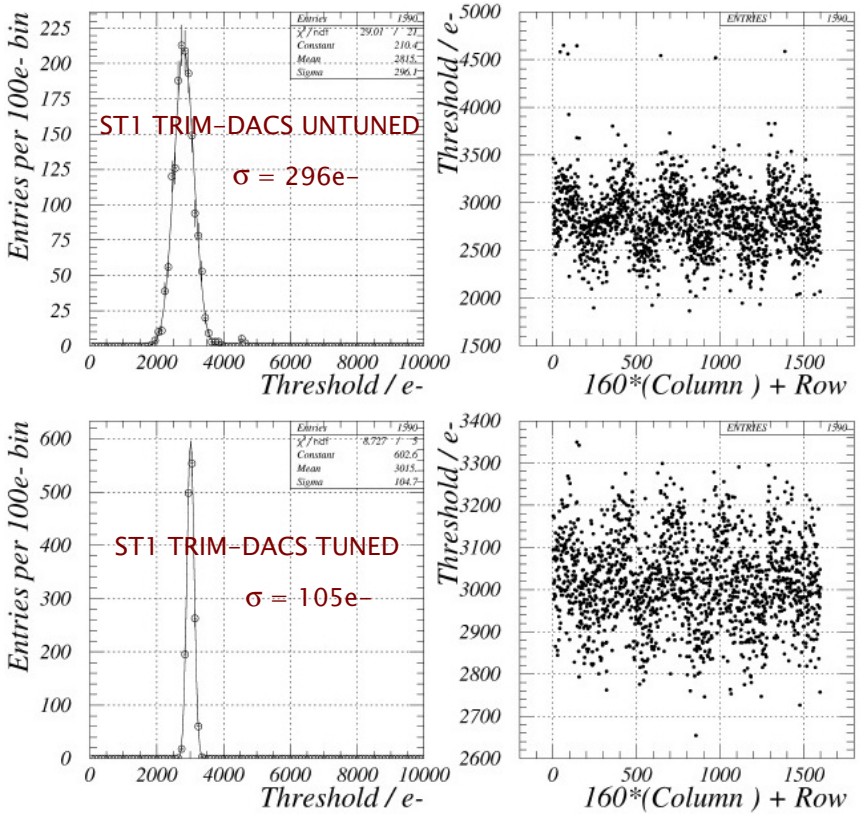
On-Detector Electronics:

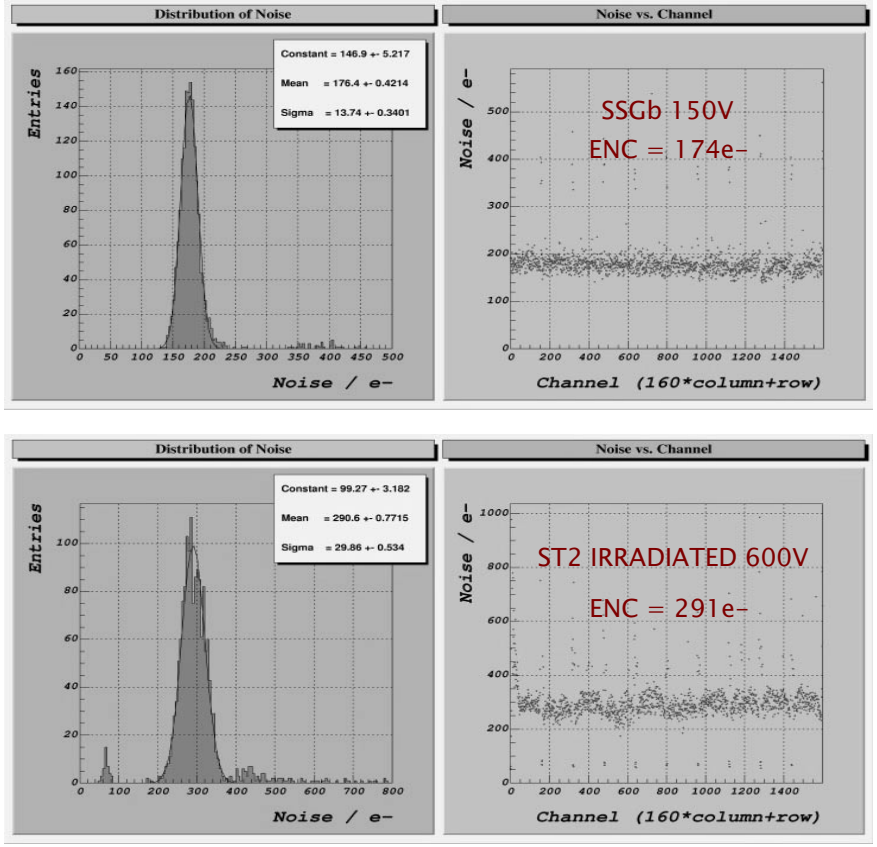
- Prototypes built using rad-soft electronics have been extensively tested in lab and testbeam, Present designs basically meet all ATLAS requirements.

- Honeywell SOI design for FE chips has been abandoned due to catastrophic cost increases from vendor.
- Transfer of FE chip design to DMILL has basically failed for technology reasons. Will continue to evaluate FE-D2S design over next months to look for generic problems and to develop and refine test methods. Have suspended all design work towards a production DMILL FE.
- Opto-chip designs in DMILL appear to be working, and are undergoing further evaluation. First prototype opto-packages and opto-cards appear to work, and intensive characterization is now beginning.
- Design of production version of test system is almost complete, and is on schedule for delivery to the collaboration by the end of this year.
- All on-detector design activity and cost/schedule definitions have now been focussed on 0.25µ versions of electronics (see next talk).

Lab Measurements using Rad-soft Prototypes

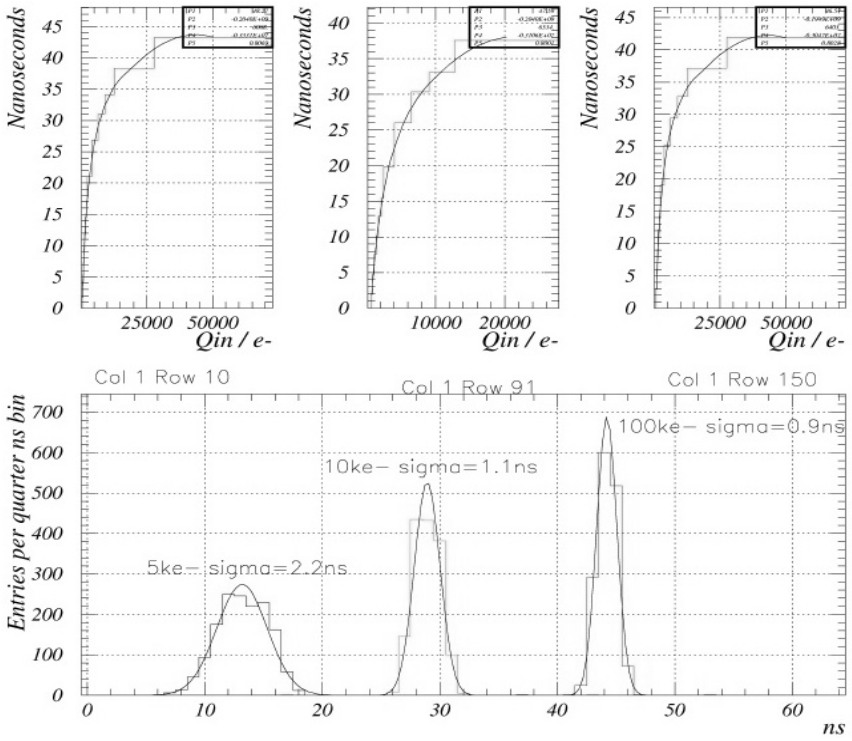
Examples of threshold and noise behavior in single chips:



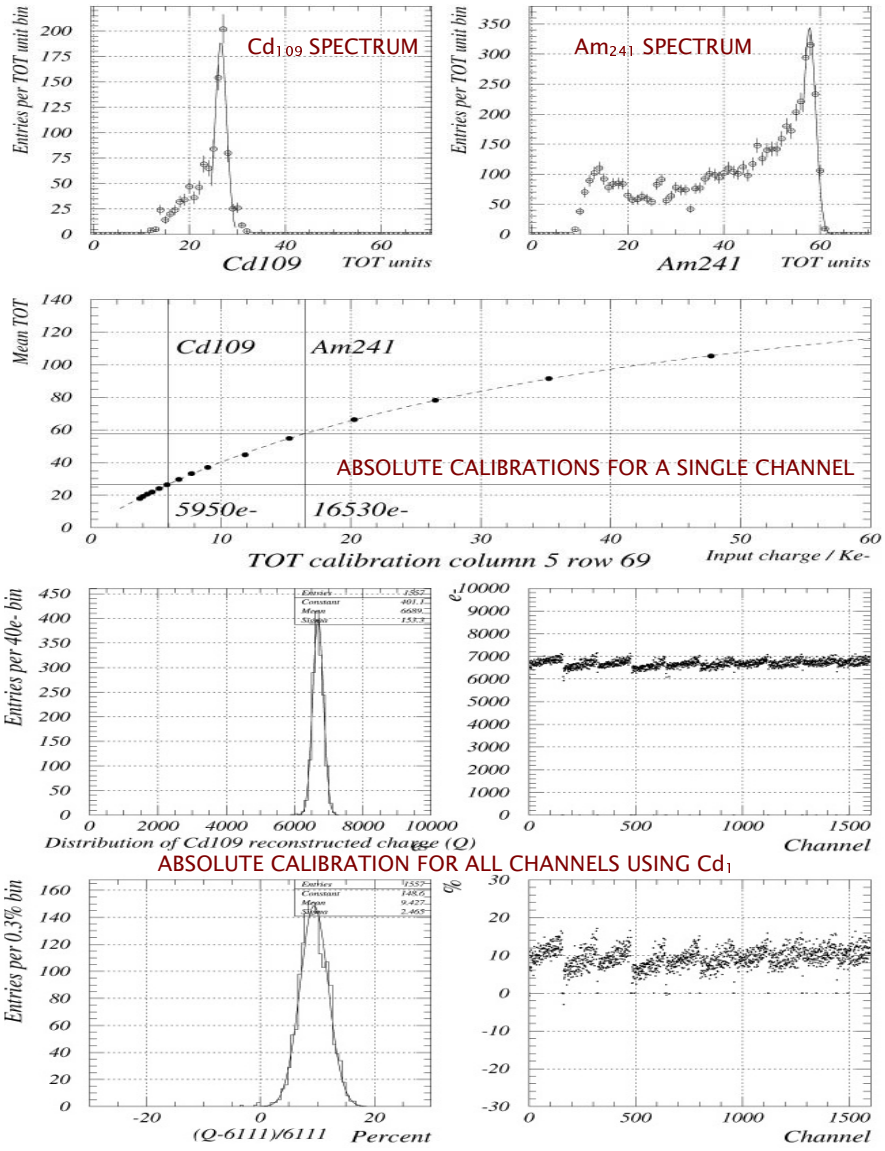


- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

Examples of timing and charge measurements:

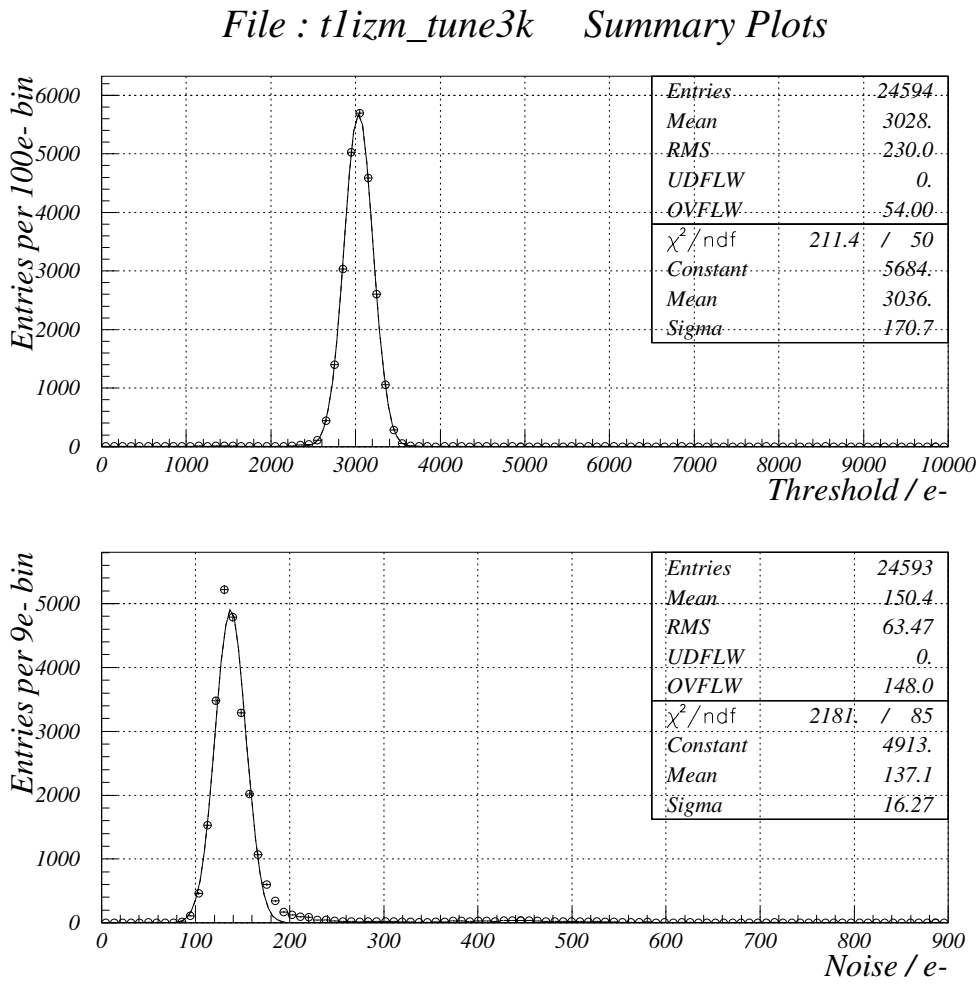


- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.



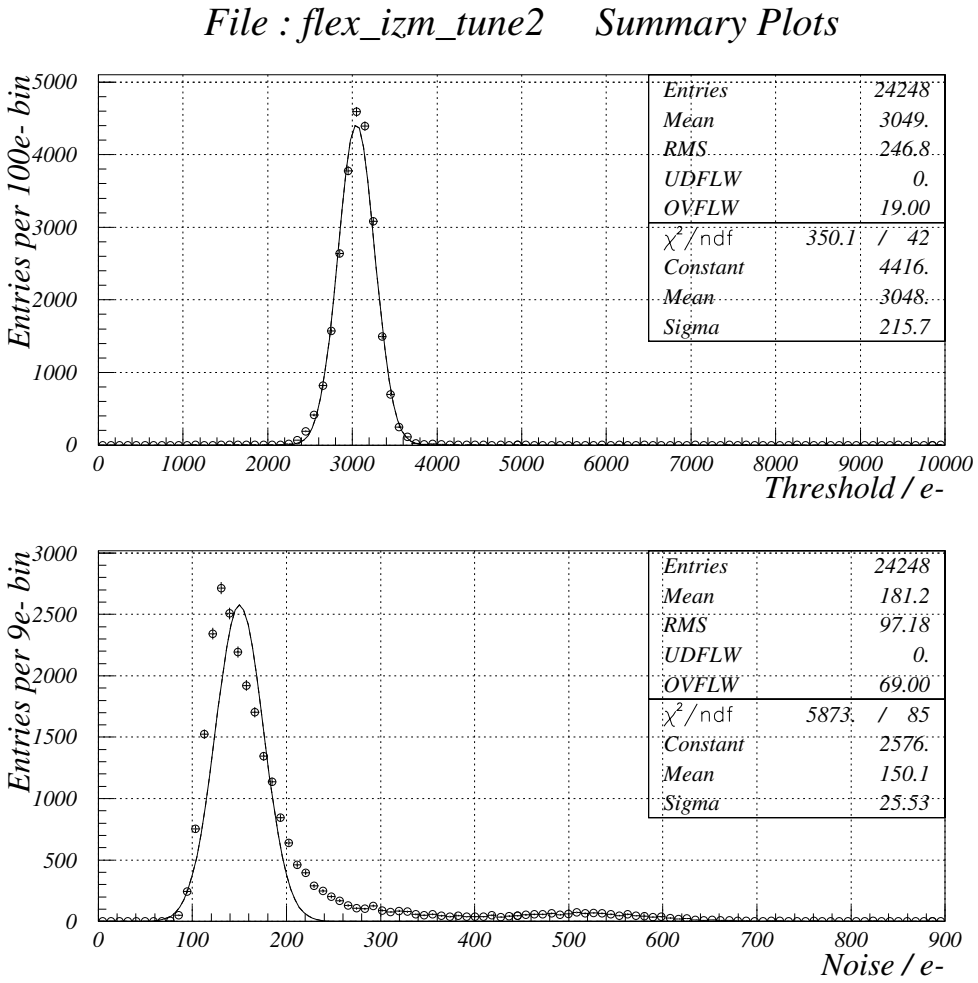
Examples of Module Results:

Bare Module (FE chips wire-bonded to PC board):



- Module has excellent threshold and noise behavior. For FE-B module should be only 16x1600 = 25600 good channels. Dead channels here are apparently all from bump-bonding problems (shorts).
- Threshold dispersion (230e) and noise (150e) for whole module are about same as for single chips.
- Module was operated in self-trigger mode at 70 KHz with excellent performance.

Performance of best Flex module is not as good:



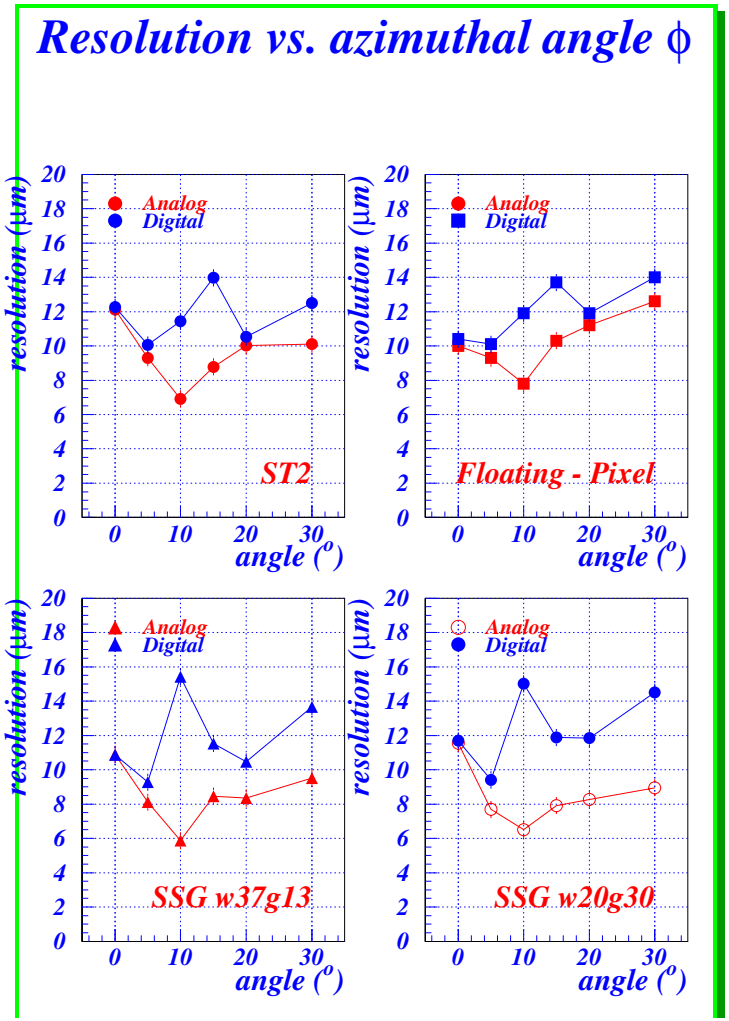
- Threshold dispersion is the same as for bare module.
- Noise distribution has a long tail. The origin of these noisy channels in this module is not clear.
- These results are from Spring 99, and have not been improved due to subsequent bumping problems with IZM which are still under study.

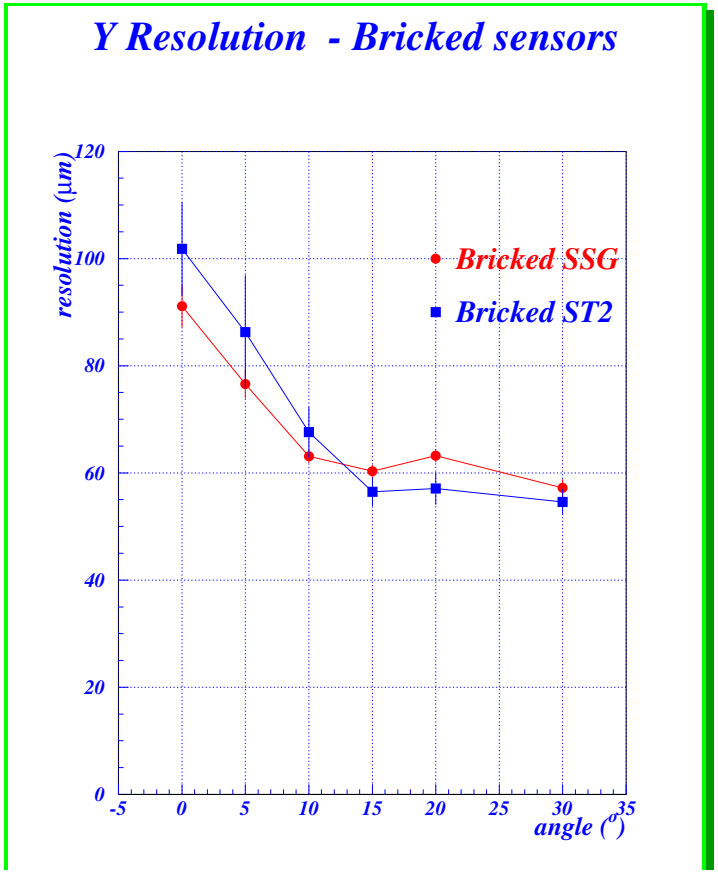
- Many impressive results from first prototype modules, but much larger statistics needed to check whether high quality modules can be built in a reproducible manner. Lab and testbeam characterization ability is now well-developed.

Sensor+Rad-soft Electronics Prototype Testbeam Results

Measure resolution versus incident track angle:

- Compare digital (binary) and analog algorithms for different sensor types, and also compare effect of "bricking" (half-pixel stagger) in long direction of pixel:



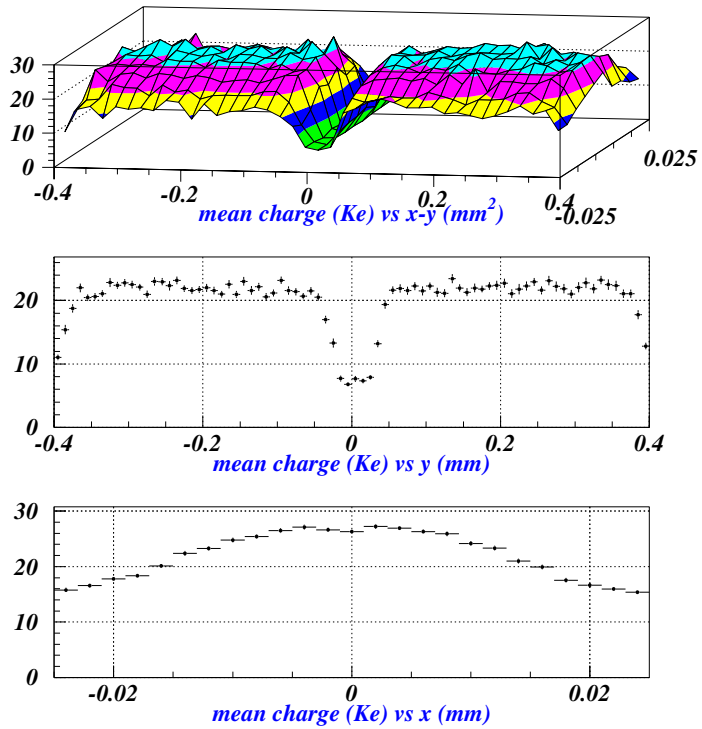


Could achieve perhaps 8-10μ in narrow and 60-80μ in wide direction for best case in barrel

Measure charge collection versus track location in pixel:

- Original n-ring design has serious charge loss problems, while new small-gap design is much better, with only small loss at bias dot location:

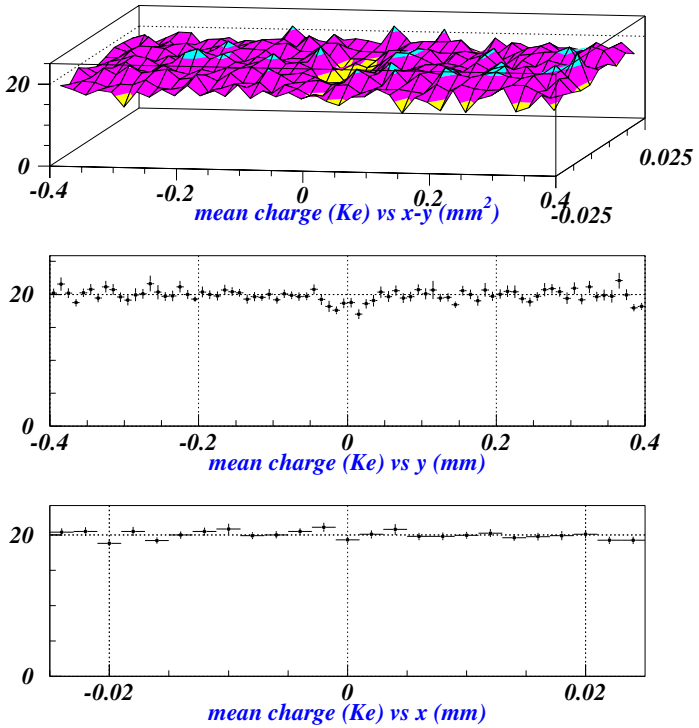
Tile 2 Design Threshold 2 Ke



large loss (0.7) near the grid
loss located ± 30 μm around the grid
losses at the pixel edges

Design 1.b:

- *p-spray insulation*
- *no floating atoll*
- *modified bias grid*



Measure efficiency as a function of track arrival time:

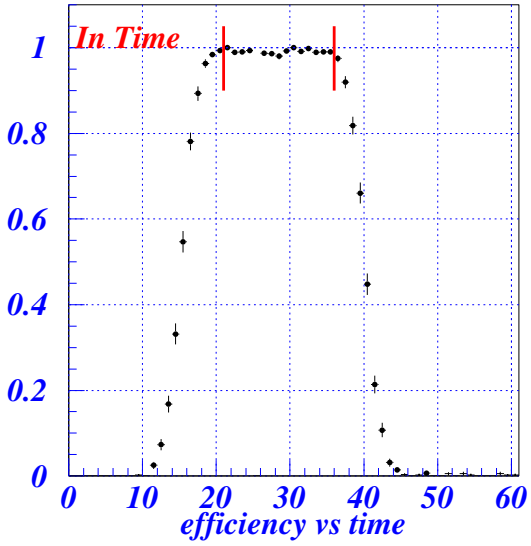
- Behavior of new design (pre-rad) is excellent, and behavior of old design (post-rad) is very good, provided that poor charge collection regions are removed:

Efficiency 'In Time'

Detector Tile 2 new design (with bias grid)

not Irradiated - Thr. 3 Ke

efficiency	*99.1*	*Losses*	*0.9*
1 hit	*81.8*	*0 hits*	*0.4*
2 hits	*15.6*	*not matched*	*0.1*
>2 hits	*1.7*	*not in time*	*0.4*

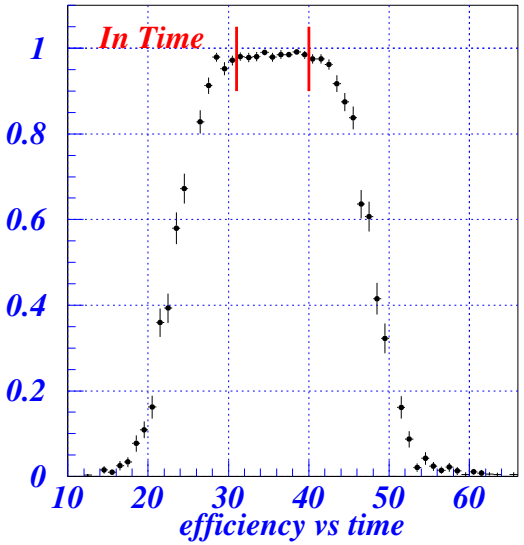


Efficiency 'In Time'

Detector Tile 2 - Irradiated V_{bias} = 600 V

Fluence 10^{15} n/cm^2 - Thr. 3 Ke

efficiency	*98.4*	*Losses*	*1.6*
1 hit	*94.2*	*0 hits*	*0.4*
2 hits	*3.1*	*not matched*	*0.0*
>2 hits	*1.1*	*not in time*	*1.2*



|xloc| < 0.01

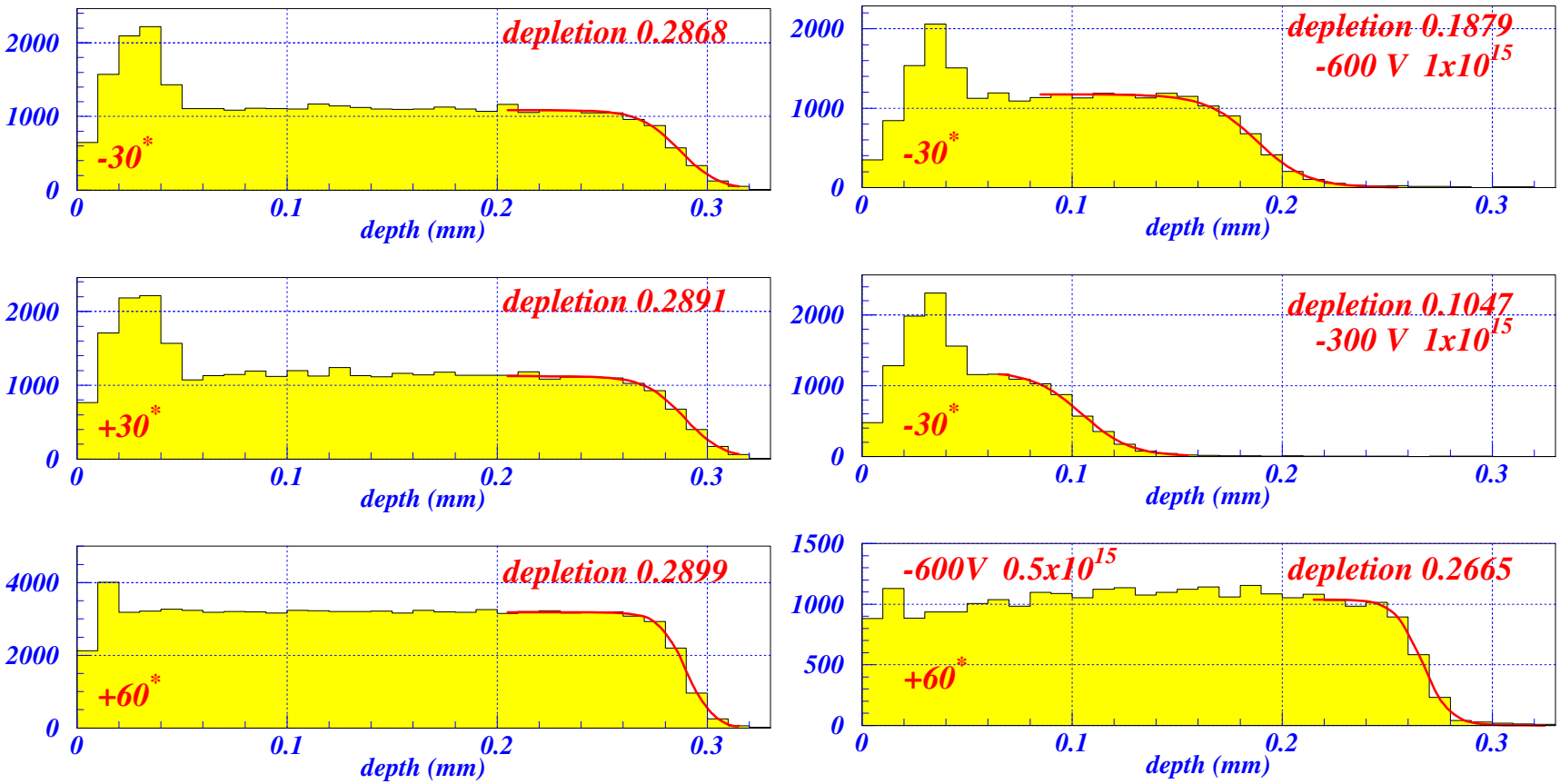
|yloc| < 0.15

Measure depletion depth in sensors:

- Look at cluster width for highly inclined tracks and use this to measure uniformity and depth of charge collection inside of sensor:

Not irradiated - depletion depth

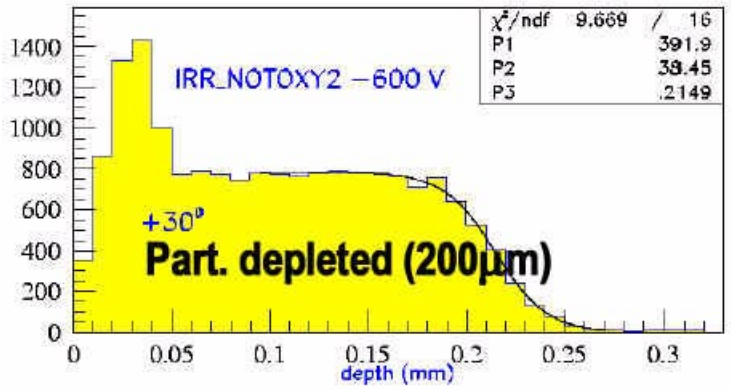
Irradiated - depletion depth



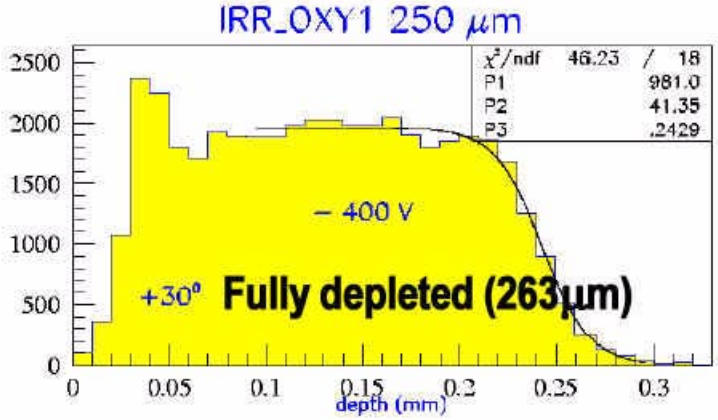
- Pre-rad result agrees with 280μ thickness. At 600V bias, lose full depletion at about half the lifetime dose, and still collect from about 180μ after lifetime dose.

Test Beam Results for Oxygenated Silicon

- First tests with irradiated single chip sensors in CERN testbeam in June 00.
- Additional tests, including single chips with full lifetime dose, completed in July 00.



Not-Oxy



Oxy

Comparison of oxygenated and non-oxygenated after 5.6 10^{14} n/equiv.

- Measure depletion depth by using tracks at large incidence angle to extract cluster length.
- Compare two sensor types after irradiation to about 6x10^{14} n-equiv. (lifetime dose for outer layers).
- As expected, get significantly better performance with oxygenated sensors, with full depletion at 400V bias, compared to partial depletion at 600V bias for standard sensor.
- More detailed analysis shows no efficiency losses or other negative effects of oxygenation.