ATLAS Lehman Review, Silicon ROD

March 20 to March 22, 2001

Wisconsin

Khang Dao, Damon Fasching,

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Sriram Sivasubramaniyan and

Will Wang

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Material Covered

Major Events

ROD Overview

Current Status

ROD Schedule

ROD Cost

May 25, 2000 ROD Schematic Review

July 31, 2000 BOC, ROD, TIM Review

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Major Events

1. May 25, 2000 ROD Schematic Review

"Extraordinary amount of good work was carried out since the Dec. 99 review. There is progress on all fronts, and well-organized team now functioning on both hardware and software."

2. July 31, 2000 BOC, ROD, TIM Review

"The two-day review of the entire Off Detector Electronics System was very informative and provided an excellent opportunity for interaction among the developers, a small subset of the users and the outside reviewers. The developers come from four institutions from the UK and the US and have demonstrated a very satisfactory working relationship in spite of their large geographical separation. The team has the technical expertise to complete the development work and deliver the needed equipment. The presentations and the documentation made available show a good understanding of the requirements and much effort in designing the necessary hardware and software. The review board was impressed by the quantity and quality of the work presented. The presenters are to be commended for their good work. The summary following will concentrate on the concerns and recommendation of the review board. It should not be detract from the good work done."

3. The ROD card infrastructure is tested and functional.

4. The initial test stand software is working.

5. SCT and pixel off detector electronic workshops (4)

6. Test plan is fully developed, necessary Hardware is fabricated and necessary VHDL and software is near completion.

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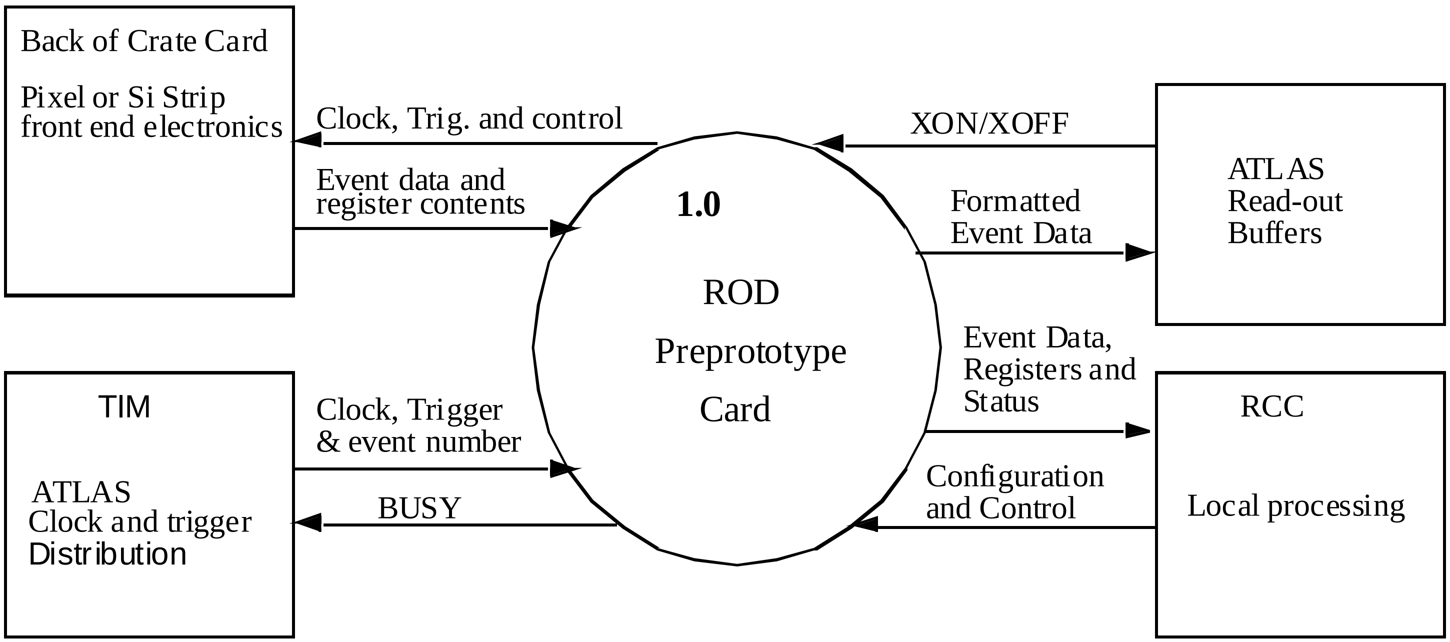
ROD Overview



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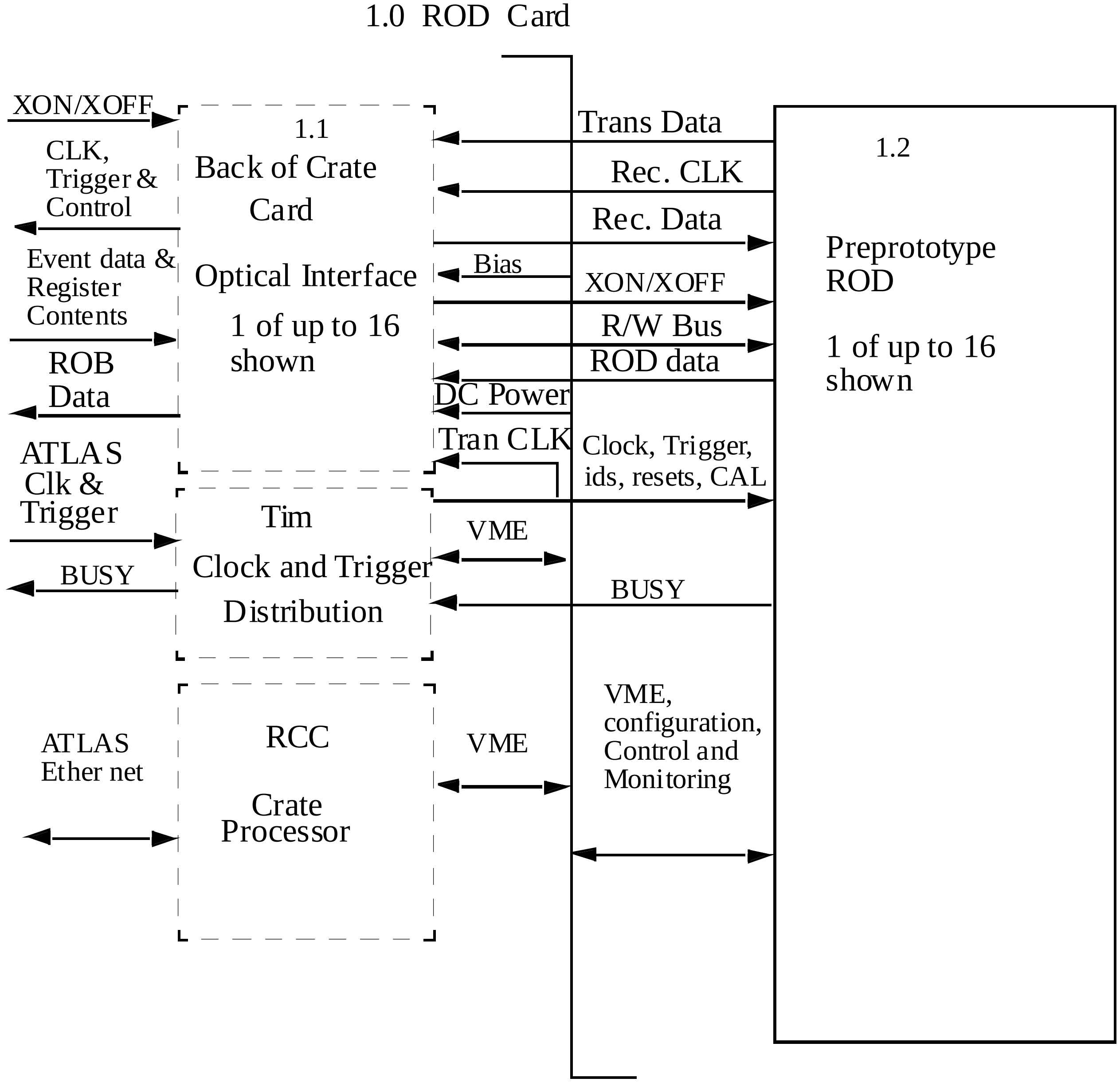

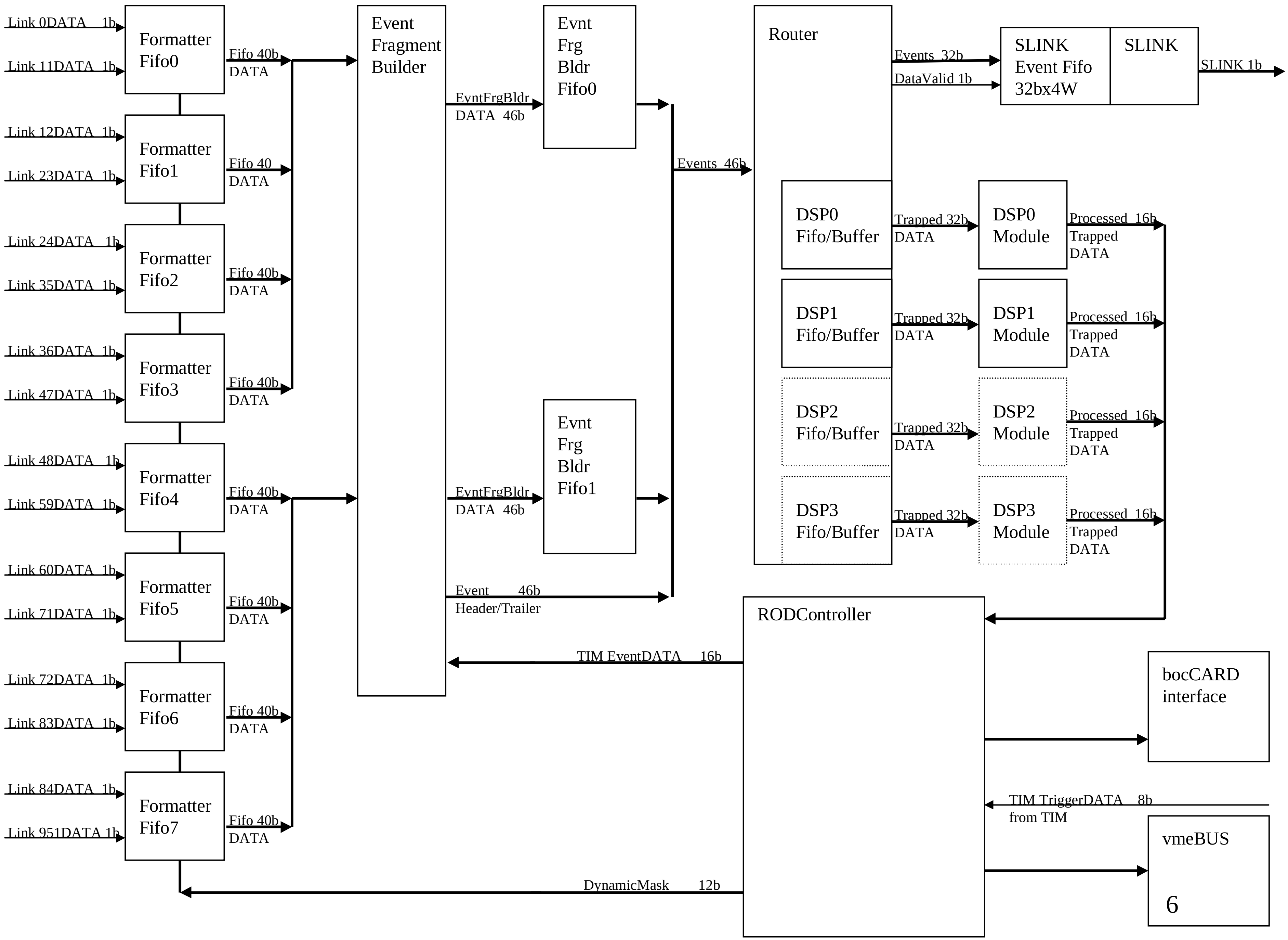
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Fifo 40b DATA
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Fifo 40 DATA
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Link 35DATA 1b
Formatter Fifo2
Fifo 40b DATA
Link 36DATA 1b
Link 47DATA 1b
Formatter Fifo3
Fifo 40b DATA
Link 48DATA 1b
Link 59DATA 1b
Formatter Fifo4
Fifo 40b DATA
Link 60DATA 1b
Link 71DATA 1b
Formatter Fifo5
Fifo 40b DATA
Link 72DATA 1b
Link 83DATA 1b
Formatter Fifo6
Fifo 40b DATA
Link 84DATA 1b
Link 951DATA 1b
Formatter Fifo7
Fifo 40b DATA
Event Fragment Builder
EvntFrgBldr DATA 46b
Evnt Frg Bldr Fifo0
EvntFrgBldr DATA 46b
Evnt Frg Bldr Fifo1
Event 46b Header/Trailer
Events 46b
Router
Events 32b
DataValid 1b
SLINK Event Fifo 32bx4W
SLINK
SLINK 1b
DSP0 Fifo/Buffer
Trapped 32b DATA
DSP0 Module
Processed 16b Trapped DATA
DSP1 Fifo/Buffer
Trapped 32b DATA
DSP1 Module
Processed 16b Trapped DATA
DSP2 Fifo/Buffer
Trapped 32b DATA
DSP2 Module
Processed 16b Trapped DATA
DSP3 Fifo/Buffer
Trapped 32b DATA
DSP3 Module
Processed 16b Trapped DATA
RODController
TIM EventDATA 16b
bocCARD interface
TIM TriggerDATA 8b from TIM
vmeBUS
DynamicMask 12b

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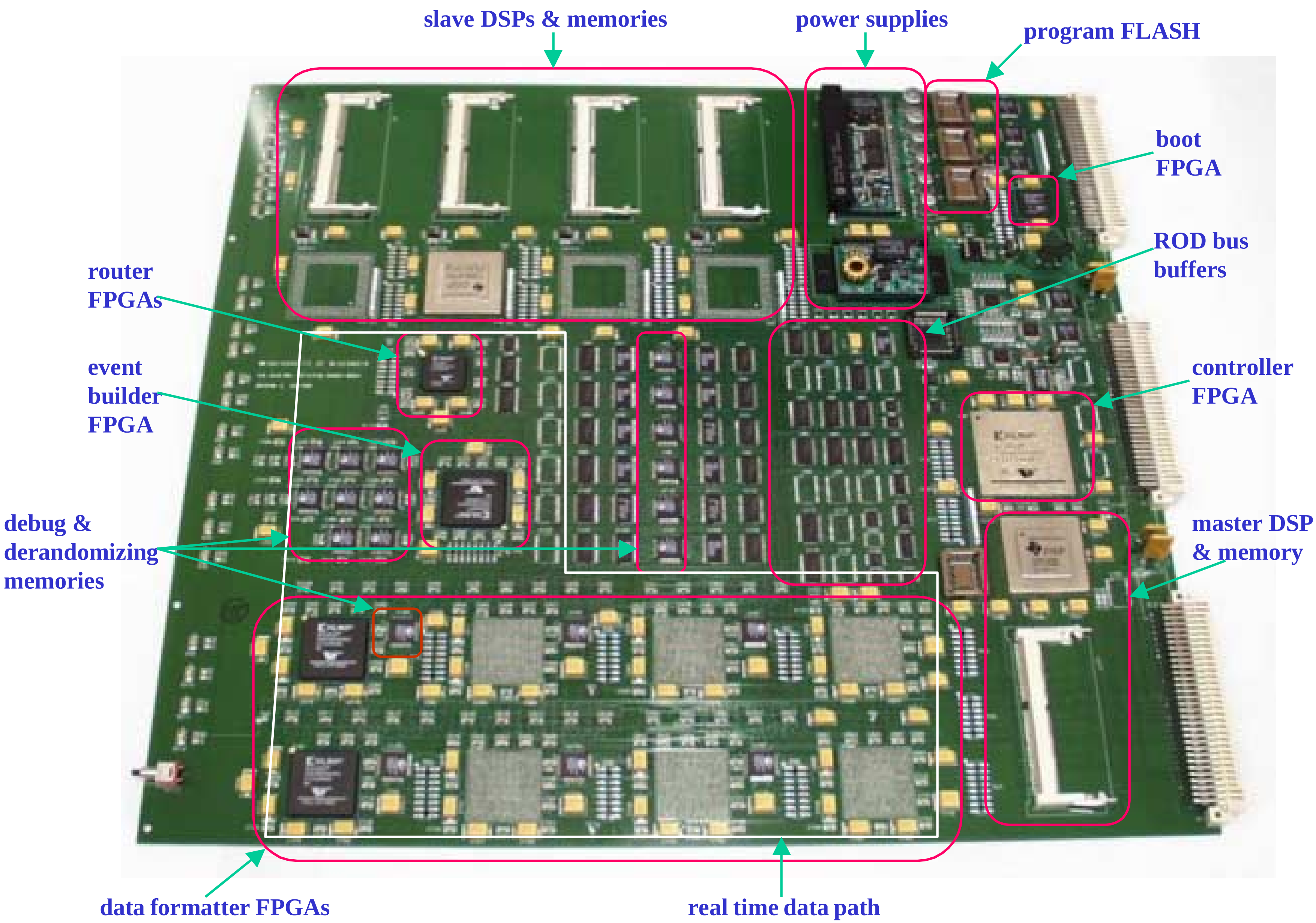

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Current Status (ROD hardware)

The design of the ROD has been completed.
Simulation of the ROD is complete with the exception of the controller FPGA that is only 90% complete.
Three ROD PC cards have been fabricated.
One ROD card have been partially loaded.
One ROD card have been fully loaded.
Three crates have been delivered.
The fabrication of the ROD test cards that loop outputs to inputs have been fabricated.
Booting of FPGAs and DSPs is working
VME r/w to the program manager works.
VME Read/write via the DSP host port interface to/from DSP program memory, data memory, flash memory, SDRAM memory and controller FPGA is working.
Controller FPGA read/write to ROD bus is working.
The ROD bus communicates to the BOC card, Formatter FPGAs, event fragment builder FPGA, router FPGA and slave DSPs.
The data path has been simulated is being debugged

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Current Status (ROD software)

Master DSP infrastructure code has been written:

memory map (.h), initialization, process list from RCC state machine, master process list from slave state machine, primitive list handler, interface between master and slave, error diagnostic buffers, transfer text buffer to RCC state machine, readout of slave text buffer state machine, error handling.

The master DSP code for maintaining communication to the RCC when the slave is processing a primitive has being written.

The DSP infrastructure code is complete.

Primitives code has been written:

Echo (diagnostic), R/W field of register or single r/w, r/w block of data, configure slave DSP (on, off and type (error checking, etc.)).

Echo has been tested successfully with the ROD.

Only primitive code needs to be written.

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Current Status (ROD test stand)

The ROD test stand software for initial testing has been written.

Windows have been tested that support the following:

> **VME r/w block (supports create and or store for later use) or single register, Master DSP r/w block (supports create and or store for later use), command and status register r/w, Flash memory r/w, Primitive generation (supports create and or store for later use) and r/w data to the ROD locations.**

These windows communicate to the following tested modules:

> **Buffer handler communicates to ROD(regular r/w, list transfer to DSP, poles and transfers text buffers), Primitive list formatter (format list for transfer to ROD), Reply list processor (check sum, converts data and store/distribute data), Host control (initialization, etc), Text buffer processing (formats data, adds headers and place text in files).**

The test stand software is functional. It will be refined and improved in the future.

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Current Status (current work)

The testing of the ROD is ongoing. It is estimated that the ROD will be functional in 4 weeks.

Current work is debugging of the data path.

Concerns:

The ROD is complex. This complexity could result in schedule slippage during the debugging stage.

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ROD Schedule

Comparison of Old and New Schedule

Task Name	Old Dates	New End Dates
Design ROD Cards	12/99- 8/00	3/01
ROD Prototypes	4/00- 6/01	8/01
ROD Fabrication	3/01- 5/02	6/03
ROD Installation	9/01- 2/05	2/05

In general there has been about a 5 month slip of the early delivery items.

The project delivery of SCT ROD is about one month late.

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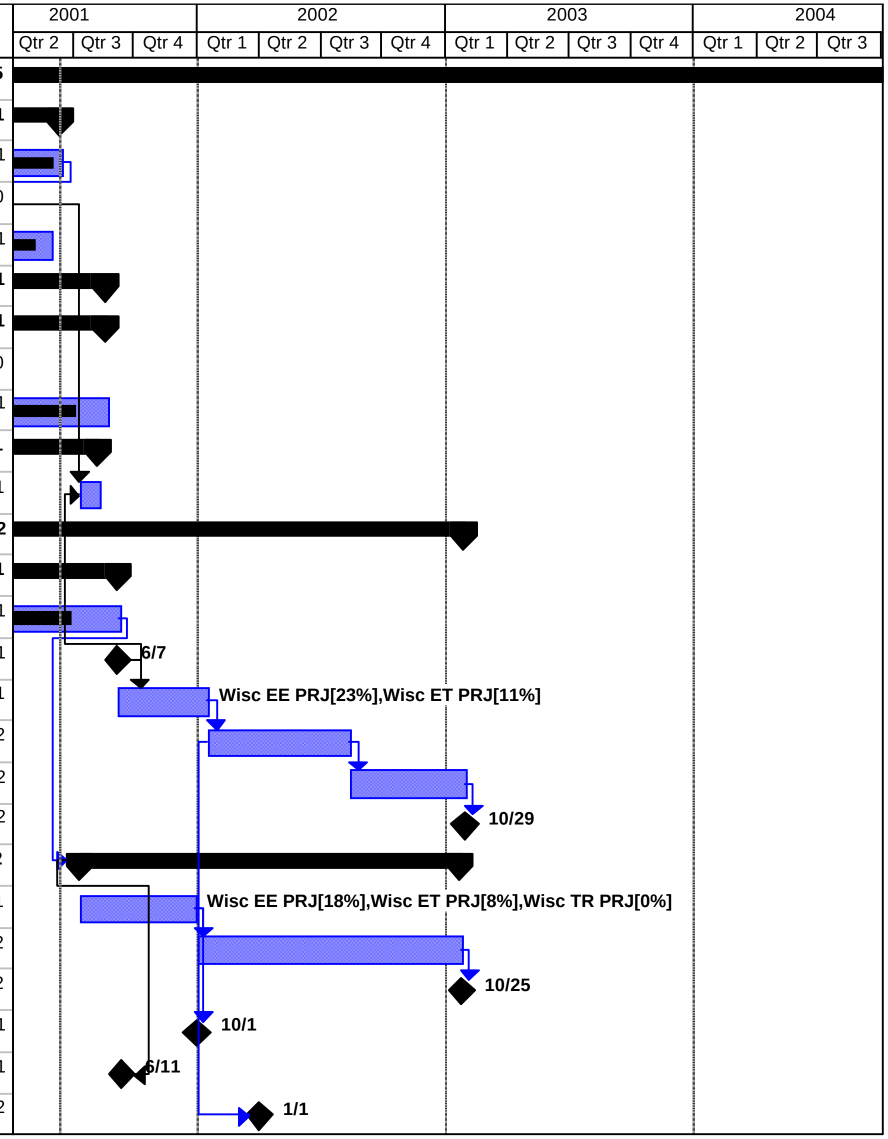
ROD Schedule

ID	WBS	Task Name	Start	Finish
1	**1.1.3**	**ROD Design & Fabrication**	**Sun 10/1/95**	**Wed 2/2/05**
10	**1.1.3.3**	**Design ROD Cards**	**Thu 12/3/98**	**Thu 3/15/01**
16	1.1.3.3.6	Board Level Simulation	Mon 4/3/00	Thu 3/15/01
17		ROD Prototype Design Review	Fri 5/26/00	Fri 5/26/00
18	1.1.3.3.7	Pixel specific Formater VHDL	Fri 5/26/00	Thu 3/1/01
21	**1.1.3.4**	**ROD Test Stand**	**Mon 12/20/99**	**Mon 5/21/01**
24	**1.1.3.4.3**	**SCT/Pixel Test Stand Software**	**Thu 6/1/00**	**Mon 5/21/01**
26		Production Diagnostic Test Sta	Fri 9/29/00	Fri 9/29/00
27		SCT Pix T.Std S/W FY01 Mat'l/	Mon 10/2/00	Mon 5/21/01
28	**1.1.3.5**	**ROD Prototypes**	**Thu 1/13/00**	**Wed 5/9/01**
32		ROD Prototype PC Loading(7 each)	Thu 4/12/01	Wed 5/9/01
33	**1.1.3.6**	**ROD Prototype Evaluation**	**Mon 7/17/00**	**Tue 10/29/02**
34	**1.1.3.6.1**	**SCT Prototype Testing**	**Mon 7/17/00**	**Thu 6/7/01**
36		SCT Proto Test FY01 Mat'l/Lab	Mon 10/2/00	Thu 6/7/01
37		SCT Complete ROD Proto Testing	Thu 6/7/01	Thu 6/7/01
38	1.1.3.6.2	Pixel Prototype Testing	Thu 6/7/01	Wed 10/17/01
39		Pixel User Evaluation	Thu 10/18/01	Tue 5/14/02
40		Pixel User Evaluation Phase II	Wed 5/15/02	Tue 10/29/02
41		Update Pixel DAQ from User Evalua	Tue 10/29/02	Tue 10/29/02
42	**1.1.3.6.3**	**User Evaluation of ROD in Europe**	**Fri 4/13/01**	**Fri 10/25/02**
43		User Eval of ROD FY01 Mat'l/L	Fri 4/13/01	Fri 9/28/01
44		User Evaluation of ROD Phase	Mon 10/1/01	Fri 10/25/02
45		Update SCT DAQ from User Ev	Fri 10/25/02	Fri 10/25/02
46		SCT ROD User Evaluation Complete	Mon 10/1/01	Mon 10/1/01
47		SCT ATLAS Final Design Review	Mon 6/11/01	Mon 6/11/01
48		Pixel ATLAS Final Design Review	Tue 1/1/02	Tue 1/1/02



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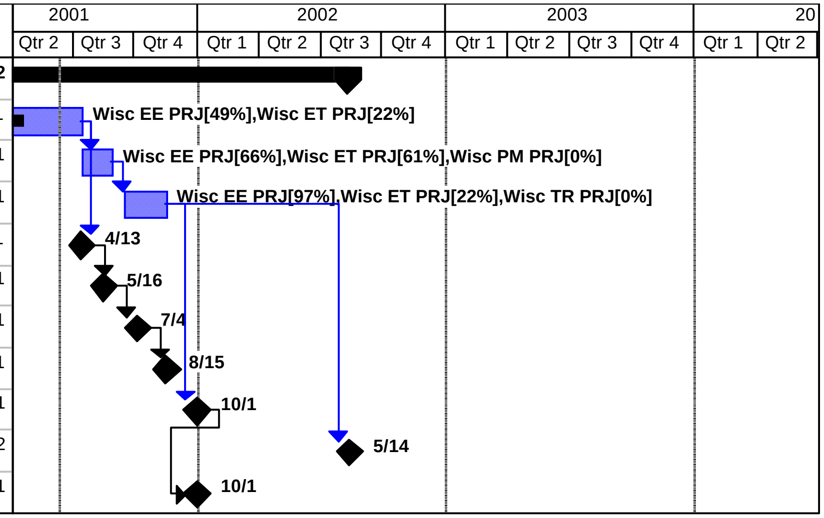
ROD Schedule

ID	WBS	Task Name	Start	Finish
49	**1.1.3.7**	**Rod Production Model**	**Thu 11/30/00**	**Tue 5/14/02**
50	1.1.3.7.1	Udating of ROD to Production Mode	Thu 11/30/00	Fri 4/13/01
51	1.1.3.7.2	Fabrication of Production Model	Mon 4/16/01	Wed 5/30/01
52	1.1.3.7.3	Evaluation of Production Model	Thu 6/14/01	Wed 8/15/01
53		Start Production Procurements	Fri 4/13/01	Fri 4/13/01
54		Release Production Dwg/Specs	Wed 5/16/01	Wed 5/16/01
55		Release Production Bids	Wed 7/4/01	Wed 7/4/01
56		Bid Evaluation Complete	Wed 8/15/01	Wed 8/15/01
57		SCT ATLAS ROD PRR	Mon 10/1/01	Mon 10/1/01
58		Pixel ATLAS ROD PRR	Tue 5/14/02	Tue 5/14/02
59	**Sil L2/3**	**SCT ROD Design complete**	Mon 10/1/01	Mon 10/1/01



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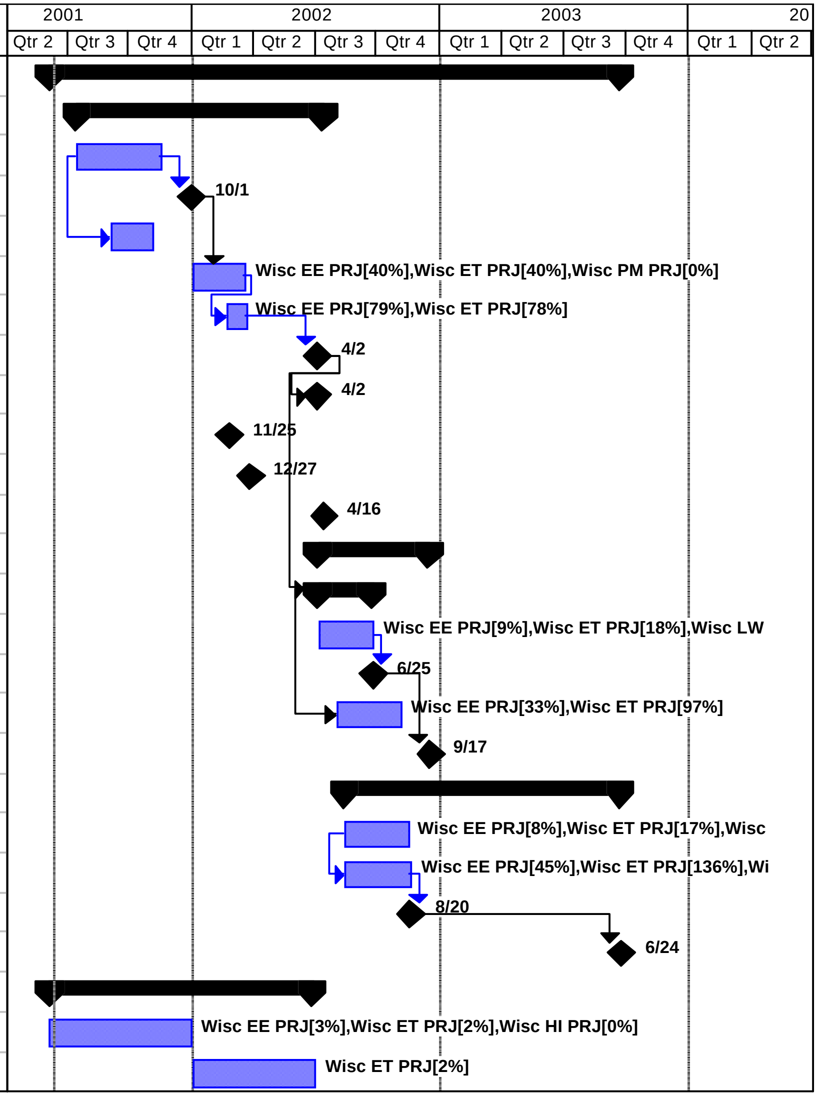
ROD Schedule

ID	WBS	Task Name	Start	Finish
61	**1.1.3.8**	**ROD Fabrication**	**Tue 3/6/01**	**Tue 6/24/03**
62	**1.1.3.8.1**	**ROD 5% Production**	**Mon 4/16/01**	**Tue 4/16/02**
63		ROD 5% Contract Negotiations	Mon 4/16/01	Wed 8/15/01
64		Project Managers Approval 5%	Mon 10/1/01	Mon 10/1/01
65		ROD SCT & 5% Production Pa	Mon 6/4/01	Thu 8/2/01
66	1.1.3.8.1.1	ROD 5% Production Fabricatio	Tue 10/2/01	Mon 12/17/01
67	1.1.3.8.1.2	ROD 5% Production Debuggin	Mon 11/19/01	Tue 12/18/01
68		ROD 5% Production complete	Tue 4/2/02	Tue 4/2/02
69		Release Management Continge	Tue 4/2/02	Tue 4/2/02
70		Begin First End Cap SCT Modu	Sun 11/25/01	Sun 11/25/01
71		Begin First Barrel SCT Module	Thu 12/27/01	Thu 12/27/01
72		First SCT Full Assembly Test S	Tue 4/16/02	Tue 4/16/02
73	**1.1.3.8.2**	**SCT ROD Production**	**Wed 4/3/02**	**Tue 9/17/02**
74	**1.1.3.8.2.1**	**SCT ROD Production Fabrica**	**Wed 4/3/02**	**Tue 6/25/02**
75		SCT ROD Prod Fabr FY0	Wed 4/3/02	Tue 6/25/02
76		SCT ROD Production Complete	Tue 6/25/02	Tue 6/25/02
77	1.1.3.8.2.2	SCT ROD Production Debuggin	Wed 5/1/02	Fri 8/2/02
78	**SIL L4/2**	Baseline Scope Complete	Tue 9/17/02	Tue 9/17/02
79	**1.1.3.8.3**	**Pixel ROD Production**	**Wed 5/15/02**	**Tue 6/24/03**
80	1.1.3.8.3.1	Pixel ROD Production Fabricati	Wed 5/15/02	Tue 8/13/02
81	1.1.3.8.3.2	Pixel ROD Production Debuggi	Wed 5/15/02	Tue 8/20/02
82		Pixel ROD Production Complet	Tue 8/20/02	Tue 8/20/02
83	**Sil L2/5**	**Pixel ROD Production/Testing**	Tue 6/24/03	Tue 6/24/03
84	**1.1.3.8.4**	**Purchase ROD Crates**	**Tue 3/6/01**	**Thu 3/28/02**
85		Purchase ROD Crates FY01 M	Tue 3/6/01	Fri 9/28/01
86		Purchase ROD Crates FY02 M	Mon 10/1/01	Thu 3/28/02



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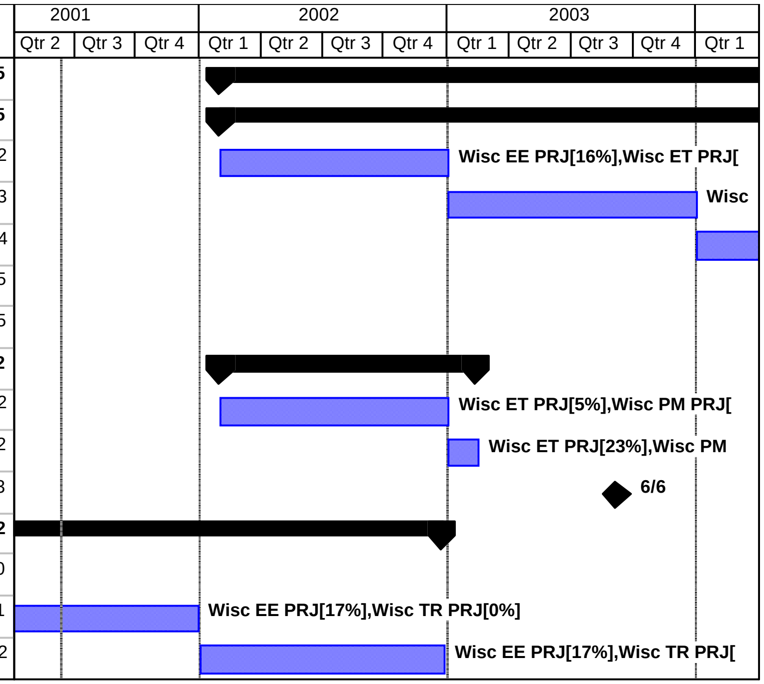
ROD Schedule

ID	WBS	Task Name	Start	Finish
87	**1.1.3.9**	**ROD Shipping, Installation and Repair**	**Fri 11/2/01**	**Wed 2/2/05**
88	**1.1.3.9.1**	**ROD Installation and Repair**	**Fri 11/2/01**	**Wed 2/2/05**
89		ROD Install & Repair FY02 Mat	Fri 11/2/01	Mon 9/30/02
90		ROD Install & Repair FY03 Mat	Tue 10/1/02	Tue 9/30/03
91		ROD Install & Repair FY04 Mat	Wed 10/1/03	Thu 9/30/04
92		ROD Install & Repair FY05 Mat	Fri 10/1/04	Wed 2/2/05
93		ROD Installation/Final commiss	Wed 2/2/05	Wed 2/2/05
94	**1.1.3.9.2**	**ROD Shipping**	**Fri 11/2/01**	**Wed 11/13/02**
95		ROD Shipping FY02 Mat'l/Labo	Fri 11/2/01	Mon 9/30/02
96		ROD Shipping FY03 Mat'l/Labo	Tue 10/1/02	Wed 11/13/02
97		Begin SCT all barrel test at CERN	Fri 6/6/03	Fri 6/6/03
98	**1.1.3.10**	**Project Management**	**Fri 10/1/99**	**Thu 9/26/02**
99		Proj Mgmt FY00 Mat'l/Labor $s	Fri 10/1/99	Fri 9/29/00
100		Proj Mgmt FY01 Mat'l/Labor $s	Mon 10/2/00	Fri 9/28/01
101		Proj Mgmt FY02 Mat'l/Labor $s	Mon 10/1/01	Thu 9/26/02



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ROD Cost Comparison of Costs

No calls on contingency

No changes in estimate except inflation

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May 25. 2000 Schematic Review Report

Summary of the May 25, 2000 ROD Schematic Review Report:

Review Board: Gil Gilchrese, Kevin Einweiler, Alex Grillo, Chris Bebek,
Bob Minor, and John fox

ROD Schematic Review
Date: May 25, 2000
Location: LBNL

The purpose of the review is to have permission to fabricate the PC board.

Extraordinary amount of good work was carried out since the Dec. 99 review. There is progress on all fronts, and well-organized team now functioning on both hardware and software.

Status Summary:

The design has now been completed. There is a complete schematic, with all parts and interconnects defined. For the major FPGA blocks, the initial pass through the VHDL is either complete, or estimated to be within a few percent of completion. An initial parts placement was made, and the board has been successfully routed at better than 99% level.

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The near-term schedule has the following goals:

* Completing all parts orders for a total of 12 boards. This is essentially done now, but some parts have longer lead times than desired. All parts should be available by middle to late July.

* Loading of first three boards by August 1.

Completion of board level simulations by August 1. There are presently some technical problems in integrating tools from Mentor, Synopsis, and Xilinx, that prevent the board-level simulations from working. This makes it difficult to commit to a schedule.

6/5/00 Note: The current status is that the Mentor, Synopsis, and Xilinx tool are working but the FPGA utilization is 10% higher than the PC based tools. The new version of the Synopsis sysnithesizer will be loaded to see if the utilization will be compatible with the PC tools (new version of Synopsis).
7/17/00 Note: The tools are now working and the board level simulation in progressing on all VHDL code.

Comments on implementation:

A short summary of two areas which were not yet designed in the previous review, and whose implementation is now much clearer:

The board initialization (upon power up) is complex. It is initiated by power-on reset circuits holding off start-up of the Reset Manager FPGA until after all the relevant power supplies have stabilized. Then, the Reset Manager FPGA is configured using standard serial PROMs. This FPGA then configures the other FPGAs by converting the configuration data stored in FlashRAM into the appropriate serial data stream, and emulating the serial PROM protocol to load each FPGA. Similarly, the Master DSP has a FlashRAM available containing the relevant boot code to get itself started.

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The VME interface is physically connected to three major objects. Two are FPGAs (the Reset Manager FPGA and the Resource Manager FPGA). The principle connection is to the Host Port of the Master DSP. The paths through the two FPGA are control/status paths. The path through the Reset Manager can be used to re-write the FlashRAM which stores the configurations for all FPGA on the board (except the Reset Manager), and initiate the reconfiguration of FPGAs and DSPs. The real data flow occurs over the Host Port path through the Master DSP. For the present generation of C60 used (C6201), this is a 16-bit port, connected to the DMA engine inside the DSP, which can operate at the same speed as the SDRAM that is being accessed (but only transferring 16 bits each cycle). This VME interface is somewhat complex, but should provide good bandwidth, while automatically resolving contention issues with the DSP CPU, and using the built-in SDRAM controller in the DSP to access the memory.

Concerns:

1) **Initialization of the ROD FPGAs**: A complex sequence of events required to initialize the board has been defined. This begins with a Reset manager FPGA that is initialized from a serial PROM. This FPGA then directs the loading of the configuration data into all of the other FPGA on the ROD. This procedure will take some hundreds of ms, and it is critical to verify that, during this extended time period, there are no major conflicts between bus driver chips, and that all chips are in suitable "default" states. Although the design team has clearly thought through these issues carefully, given the complexity of the ROD design, we recommend that these issues be carefully checked once more.

6/5/00 Note: The FPGA initialization has been reevaluated with no problems found. The tri-state buses have also been reevaluated. No problems with bus contention were found in the schematic. There may be some minor changes to the VHDL code to insure that the tri-state busses are break before make. All control lines will be pulled up with resistors to protect the tri-state drivers during initialization.

2) **Spare Connection Between Parts on the ROD**: The present technique used to map from VHDL to a physical part for placement on the PC board is such that all presently unused pins are left unconnected (in fact, no via is generated, so no access to the FPGA pin would be possible after board assembly). It was felt that, given the aggressive schedule in which board fabrication and board-level simulation will proceed in parallel, this was risky. It is strongly suggested that someone familiar with the detailed data and control flow between the different FPGAs should add an appropriate number of spare pins and wires to allow additional handshakes or data bits that could conceivably be required after completion of all detailed design and simulation. In addition, control pins on auxiliary chips, which might possibly need to be changed from a default ground or VDD setting, should be connected by pull-up or pull-down resistors, so that modifications could be possible. These techniques will significantly add to the range of improvements that could be made after board fabrication.

6/5/00 Note: This area has been reevaluated. The chosen solution is to bring out all unused pins to through hole vias. When connections are need. Wires will be added. This solution was chosen because it is very hard or next to impossible to determine where signals need to be connected. A few dedicated lines were also added.

3) **DSPs in the Real Time Path**: During discussions, it was stated that the present role for the Master DSP included processing real-time interrupts for each L1 trigger (100KHz maximum rate). Although some latency is tolerable here, this was still felt to be a somewhat riskier approach. In addition, it includes the DSP as a critical element in the ROD data path. This means that the board-level simulations which are needed to determine the ability of the ROD to meet the critical rate and bandwidth requirements will also have to include some fairly detailed model for the DSP (technically, it is not clear how to implement such a model). A lower risk approach would involve attributing this critical task to the ROD Resource FPGA, which the Master DSP could influence in a "non-realtime" manner by for example making a request to drop an event on some links to restore synchronization.

6/5/00 Note: The plan is to take the real-time path out of the DSP. The resource manger will contain the code in VHDL.

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4) **Diagnostic Capabilities**: The present ROD design has extensive diagnostic capability, in many cases implemented using a large number of bidirectional buffers and latches to direct data flow between special memories. This allows injecting test data before each major circuit block, and then capturing it after each block. We would like to see a more detailed investigation of what fraction of faults on a board (PC fabrication faults, and/or component faults) can be detected by the types of algorithms that would be used in the test system. Typically, data paths are easy to test, but there are often many miscellaneous control lines that are equally critical, but harder to test. What fraction of the connectivity and functionality of the board can be easily checked?

6/5/00 Note: This will be studied.

5) **Library Parts Verification**: There was a concern (based on previous experience) about the number of parts in the parts database which were generated for this board at LBL Error-free entry of all pins is difficult, and finding minor errors, etc. can be difficult. We urge careful cross-checking of these parts before submission of the PC board for fabrication.

6/5/00 Note: A check of the parts has been made. No errors were found. A further check will be made in the next week with two people checking each others work.

6) **Selection on Pins on FPGAs**: The description of how the assignment of signals in the VHDL to FPGA pins was made raised some issues. One issue was whether the placement of complete busses of 30-40 pins within a particular I/O bank on the Xilinx parts exceeded recommendations on the number of simultaneous transitions. In addition, there was a concern about how much flexibility was left to the place and route tools for the future. The concern was that by freezing the pin assignment in a (possibly) somewhat unnatural configuration it would become increasingly difficult to successfully route the parts as VHDL changes occurred in the future. Careful attention should be given to the internal constraints on connecting CLB's and I/O pads to try to minimize the possibility of the chosen pin assignments causing such "getting trapped into a corner" routing problems as the ROD firmware evolves.

6/5/00 Note: The pins on the router have been released to be selected by the Synopsis tool. This was the only FPGA that had forced pins for busses. The I/O bank on the Xilinx part have been checked for over current. No problems were found.

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7) **Verification of Printed Circuit Board Connections**: The proposed PC board is very complex, and manufacturer test is a concern. We urge the design team to explore whatever techniques the board vendors have at their disposal to try to assure a high-quality board. Beyond the usual flying-probe continuity test, it is not clear what options exist. This concern involves both the debug time of the initial small number of PC boards, and the production risks for larger numbers of cards (since the cards can only be tested once all components are loaded).

6/5/00 Note: Holmes is contacting venders to find alternatives that will check the ROD PC card.

8) **Protection of the ROD from Over Temperature**: We were presented with a first power analysis on the board, which did not look unreasonable (85W). Given the high power densities on the card, it could be useful to investigate some type of thermal monitoring to detect over-temperature conditions.

6/5/00 Note: A thermal switchs will be added to the ROD. These switchs on over temperature will place all FPGAs and DSPs in the initialization mode (standby power state). This will reduce the power on the card to a minimal value. The crate over temperature sensor (normal part of the crate) will be relied on to turn off crate power in extreme circumstances. The status of the ROD temperature sensor will be displayed on the front panel.

9) **Development of a Testing Plan**: The general issue of a test plan was. It is not clear whether it will be easily possible to debug a complete card, or whether it would be useful to begin with a partial loading of at least some cards. This raises issues of BGA loading and replacement capabilities needed during testing (for example, can additional BGA be easily added to a partially loaded board). Also, the DSP debug environment will be critical. Presently, the JTAG interface required to connect the development system is provided for each DSP on a separate connector. We strongly encourage the design team to be thinking through some of these issues during the period of board fabrication, so they can "hit the ground running" once the first boards are fabricated.

6/5/00 Note: A testing plane will be developed.

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10**) Design Rule Checking**: There is some concerned about the amount of design-rule checking that has been done as part of the Mentor schematic editor. I think the design group should confirm that the fanouts and electrical loading of the I/O ports on the EPLDs, and of the other parts on the board is OK. We worry a little bit about the timing of the various 3-stated multiplexed busses, because without any timing verification. Were concerned that skews or delay variations are going to have possible bus contention problems as slow drivers stay on a little bit while fast drivers turn on, leading to high-current transients in the bus structures.

6/5/00 Note: The design has been changed to have all I/O to/from the ROD going through buffers with the exception of the VME interface that is designed to be connected directly to the VME bus.

Concerns from previous review revisited:

1) **ESD Protection for the ROD**: Concern was expressed on the question of physical I/O protection. The board will contain many low-voltage complex parts which will be very sensitive to static. Particularly for FPGA's which power on with their I/O pins configured in a sensitive mode, there was concern that the basic interface to the BOC through the backplane would be very sensitive to grounding. Given that these boards will surely not be handled with full ESD precautions over their full lifetime, it would be worthwhile to study all I/O lines connected to the outside, and make sure that they have adequate protection against ESD, perhaps only in the form of pull-up or pull-down resistors to ensure that a low impedance is always defined.

6/5/00 Note: The design has been changed to have all I/O to the ROD go through buffers with the exception of the VME interface that is designed to be connected directly to the VME bus.

Conclusions:

We propose that the group should go ahead and fabricate PC boards based on schematics which would be very similar to the ones we were shown during the review. The risk of errors (due to the lack of completion of the board-level simulation effort), seems to be more than balanced by the need to get boards into the hands of users for evaluation as soon as possible. However, we feel strongly that the ROD prototype would benefit from the completion of the board-level simulation effort on the earliest possible time scale, preferably before loaded boards enter the initial test phase.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

BOC, ROD, TIM Review July 31 to August 1, 2000

Review Board:
Murdock Gilchriese, John Fox, Bob Minor , Abe Seiden, Larry Premisler, Alex Grillo, Kevin Einsweiler and Paul Keener

Participants:
John Lane. (TIM), Martin Postranecky (TIM), Dominic Hayes (TIM)
Eli Rosenberg (Pixel DAQ)
Maurice Goodrick (BOC)
John Hill (SCT DAQ)
Mark Nagel (ROD) , Damon Fasching (ROD), Lukas Tomasek (ROD),
Richard Jared (ROD) and John Joseph (ROD)

Summary Off-Detector Electronics Review 31-Jul/1-Aug-2000

The two-day review of the entire Off Detector Electronics System was very informative and provided an excellent opportunity for interaction among the developers, a small subset of the users and the outside reviewers. The developers come from four institutions from the UK and the US and have demonstrated a very satisfactory working relationship in spite of their large geographical separation. The team has the technical expertise to compete the development work and deliver the needed equipment. The presentations and the documentation made available show a good understanding of the requirements and much effort in designing the necessary hardware and software. The review board was impressed by the quantity and quality of the work presented. The presenters are to be commended for their good work. The summary following will concentrate on the concerns and recommendation of the review board. It should not be detract from the good work done.

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Key global items that should be addressed:

1. The BOC-ROD-TIM team should plan on an integrated ATLAS FDR by February 2001. An integrated schedule should be part of this review, and thus should be available for internal review in the US and UK by early December at the latest.
Note9/15/00: The Off Detector Electronics (ODE) group will try and meet the review date. Jared will coordinate producing an integrated schedule by Oct 1, 2000.

2. Having test results from all of the BOC-ROD-TIM, particularly together, was deemed very aggressive to meet the February FDR schedule. An integrated test plan, with responsibilities assigned, should be developed immediately so that it can be reviewed by the appropriate SCT, Pixel, UK and US entities by the end of September.
Note9/15/00: A plan has been developed by Cambridge (J. Hill) for the testing of the ODE crate and cards.

3. The SCT need for BOC-ROD-TIMs is substantially in advance of the current Pixel schedule and there is some risk that freezing the design too early, necessary for the SCT, may cause problems for the Pixels. This needs to be addressed directly in the integrated schedule, by a combination of sufficient design flexibility and/or phased fabrication.

4. Finally, the goal to complete the fabrication and testing of the RODs and probably the BOC and TIM (need integrated schedules) by early 2003, practically guarantees that some parts for these items will be obsolete by the time of commissioning in 2005 or so. There should be a clear proposal how to handle this situation for the February FDR with a final proposal to be ready by the ATLAS PRR.

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July 31, 2000 BOC, ROD,TIM Review

Global Issue:

L1 Latency:

There is a time budget for each component. The design of TIM, BOC and ROD indicate that they will meet their budget maximum. It will be important to confirm the time budgets in the system test at Cambridge in the November-December 2000 test.

SCT Module Reconfiguration:

Single Event Upsets (SEU) measurements are starting to be made on the FE ASICs. As expected the rate is non-zero. A plan needs to be developed between FEE group and Off-Detector Group to handle the to be measured rate of SEUs. This plan should include the possible use of the periodic reset.

Note9/15/00: When the rates are understood a plan will be developed.

Module Testing:

It became clear during the review that it will not be an easy task to test all of the components in the ROD crate in fully realistic conditions. One ROD crate services such a large number of detector modules that there will not be enough detector modules in existence to connect a full complement of modules to a ROD crate, not even a full complement for one ROD/BOC card, until much later than the planned FDR. The group is encouraged to look at alternatives which could test all the requirements of the ROD crate in a more piecewise fashion.

Note9/15/00: Three cards are being fabricated that will provide testing of I/O pins between the ROD and BOC. In addition partially loaded ROD in memories (play or record) will be used with a optical to electrical and electrical to optical being designed at Cambridge to test optical fiber inputs and outputs.

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Spare Pins:
There should be an effort to try to increase the number of spare pins on each connector to allow for future changes. There were some connectors that have 0 spare pins.
Note9/15/00:This item will need to be evaluated in detail in November 00.

ROD Crate Testing:
A plan should be developed that outlines how each element of the combined TIM/BOC/ROD requirements can be demonstrated prior to the PRR. This could specify a different test for each element of the requirements even though no one test set up emulated the entire SCT or Pixel environment.
Note9/15/00: Each cards test plan will measure the requirements compliance prior to the Cambridge test. The Cambridge test plan will measure system performance.

Integrated Schedule:
An integrated schedule for all components of the Off Detector Electronics showing activities through the completion of production units is needed.
Note9/15/00: An integrated schedule draft will be produced by Oct 1, 00.

SLINK Interface:
It should be made clear to the ATLAS DAQ Group that we plan to use the mezzanine SLINK card and that the electrical interface, connector and form factor of that card must be frozen at the time of the Off Detector FDR (i.e. Feb-2001). There must be sign-off by someone in ATLAS-DAQ for that.

Pixel Module Interface:
A formal interface document describing the Pixel data stream is needed.
Note9/15/00: We will attempt to have the pixel module people write the interface specification.

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Back Of Crate (BOC) (Optical Interface) Items:

Requirements:
BOC requirements need to be more quantitative. Such as detailed information of the command delay range.
Note9/15/00: The requirements are being updated.

BOC without ROD:
A check should be made if the BOC “idles” in the right state if its corresponding ROD is unplugged.
Note9/15/00: This will be investigated by Oct 30, 00. Future BOC designs will have a local clock that will maintain clocking to the modules when other components/cards fail.

BOC laser interlock:
There was much discussion of the interlock mechanism whereby fibers from the on-detector electronics are disabled if unplugged at the BOC. The interlock system must be understood and implemented.

BOC schedule:
The short term schedule is understood but the long term schedule needs to be developed.

BPM12 and VCSELS12 Parts:
The availability of BPM12 and VCSEL12 parts must be monitored. The time they are needed should be clearly marked on the integrated schedule so it can be tracked with the Links Group.

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Read Out Drivers (ROD) Items:

Temperature of ROD PCB
Temperature sensors on the ROD PCB will trip at over temperature. Not clear what temperature the "hot" ICs will be at that point. Need to measure IC package temperatures at PCB trip point and make sure this is below spec limit for packaged ICs. ROD card over temperature monitor needs to be read out remotely- not
just as an led on the card.
Note9/15/00: The trip state of the temperature sensor readout is still open. The temperature of the ICs and board will be measured.

ROD Cost:
The parts cost are stable at the 10% level. The new pricing from Xylinx seems to indicate they are favoring their new products and discouraging older ones. We should determine if some of these older products which are designed into the ROD are going to obsoleted soon. If so, we need to plan accordingly with larger/earlier buys or designing in another part.
Note9/15/00: This will be evaluated in early 2001 after the system test is running.

ROD Simulation:
Simulation of the data path is 75% complete. Simulation of the logically more complex controller section has not begun. This is unfortunate since this section of the board is required to function early in the debugging process. The simulation must be completed to aid in debugging.
Note9/15/00: Simulation of the data path is complete. The controller simulation is starting.

Requirements:
The requirements document is stable.

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DSP Software:
This seems to be well advanced. The host-masterDSP and masterDSP-slaveDSP communication protocol is done and in fact is done very symmetrically. I like the attention paid to communicating error messages to the host. How to handle these error reports is still in development.

Test Stand:
Software is impressive. It is hard to anticipate if it will meet the demands of the board debuggers, ie, how flexible and easy is it execute new sequences of commands.

ROD Test Plan:
A sequence of steps for commissioning the first ROD board was presented. It seemed to progress logically from the VME interface to greater board depths such as booting FPGA's and testing memories and data paths. The plan is in the early stage of development. A detailed test plan needs to be developed that determines if the requirements have been meet.
Note9/15/00: A detailed test plan has been generated. This plan compares requirements to test.

Pixel anxiety

No pixel specific VHDL code exists to "prove" that ROD can deal with pixel issues. Einsweiler asked how can ROD get through a February FDR without this crucial input. In the end, the answer seems to be, "Too bad. If a different ROD is needed by the pixels it will be developed when the pixel system is stable."
Note9/15/00: Pixel ROD VHDL has been almost completed. Board level simulation needs to be performed after the SCT prototype ROD is functional. It is planned to use the test card that generate input patterns to fully test the known front end operations. This will help with understanding of the ROD performance for pixels.

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Timing Interface Module (TIM) Items:

Requirements: TIM requirements need to be more quantitative.
Note9/15/00: The requirements have been updated and are in review.

TIM Simulation:
TIM is designed and in fabrication. The implementation is smallish CPLD's which can be individually simulated but their interaction cannot. The commissioning may take some time as the IC interaction are not simulated.

TIM Design Changes:
There is discussion about future incorporation of deadtime statistic accumulation per ROD. Fox pointed out that this might be doable with unused resources on each ROD. Another future change to the design is to mount the TTRx logic directly on the PCB instead of continuing with an "ATLAS standard" daughter board. There is concern that changes as the board is being fabricated may lead to schedule slippage.

VME Addressing:
It was stated that a switch is used to set the board base address. From the discussion that followed it, seems that the ROD used the nGA lines on the backplane to establish the board base address. It did not sound to be strictly VME64x compliant, but it will work fine. The TIM should do what the ROD does so that there is no confusion later on with TIM encroaching on ROD address space due to a mis-set switch.

TIM Schedule:
7 October - Two TIM boards are thought to be available.

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ROD Crate Controller (RCC)

RCC Software:

It is not clear what software is need in order for the Off Detector PRR to be completed. The RCC Software development should be included on the Integrated Schedule. It appears that there may be a manpower shortage in this area. Some estimates should be made of what is needed and then discussed with the SCT Steering Group if there is not sufficient manpower within the Off Detector Electronics Group.

Note9/15/00: The ROD test stand software will be initially used for testing. This software will be expanded to meet the system test needs. Cambridge and Wisconsin are in close communication on the design of the test stand software.