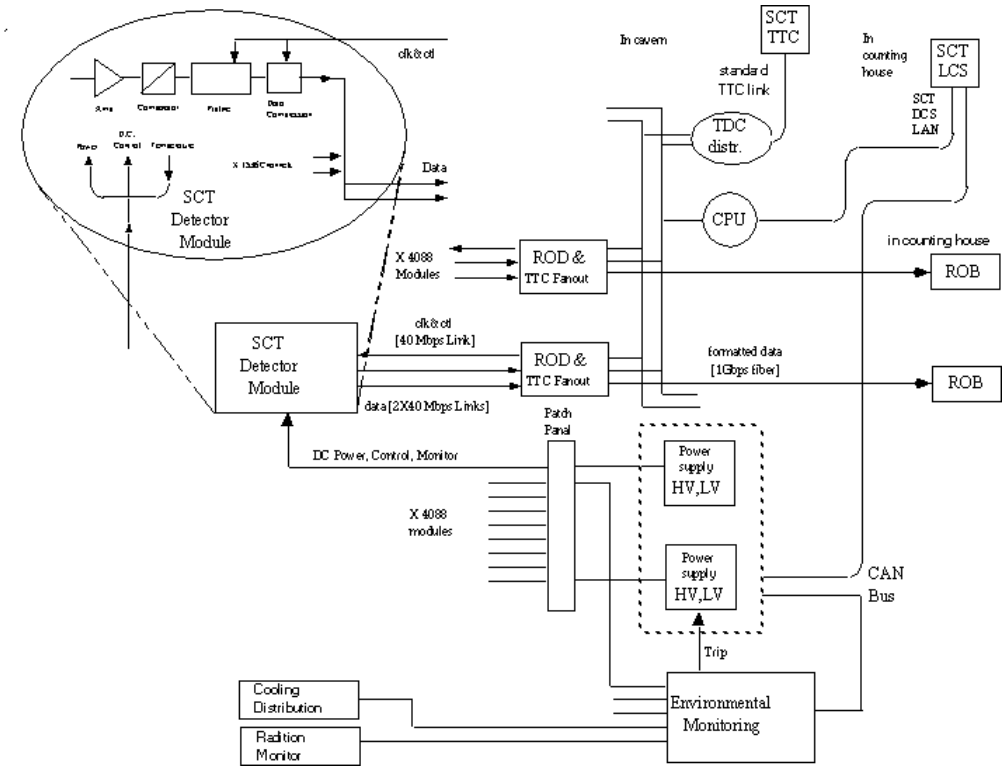
WBS 1.1.2.1
ATLAS SCT Electronics

US ATLAS DoE/NSF Review
20/23-Mar-2001

Alex Grillo

A Bit of History

The ATLAS-SCT electronics system has the following architecture:



The US deliverables include partial amounts of:

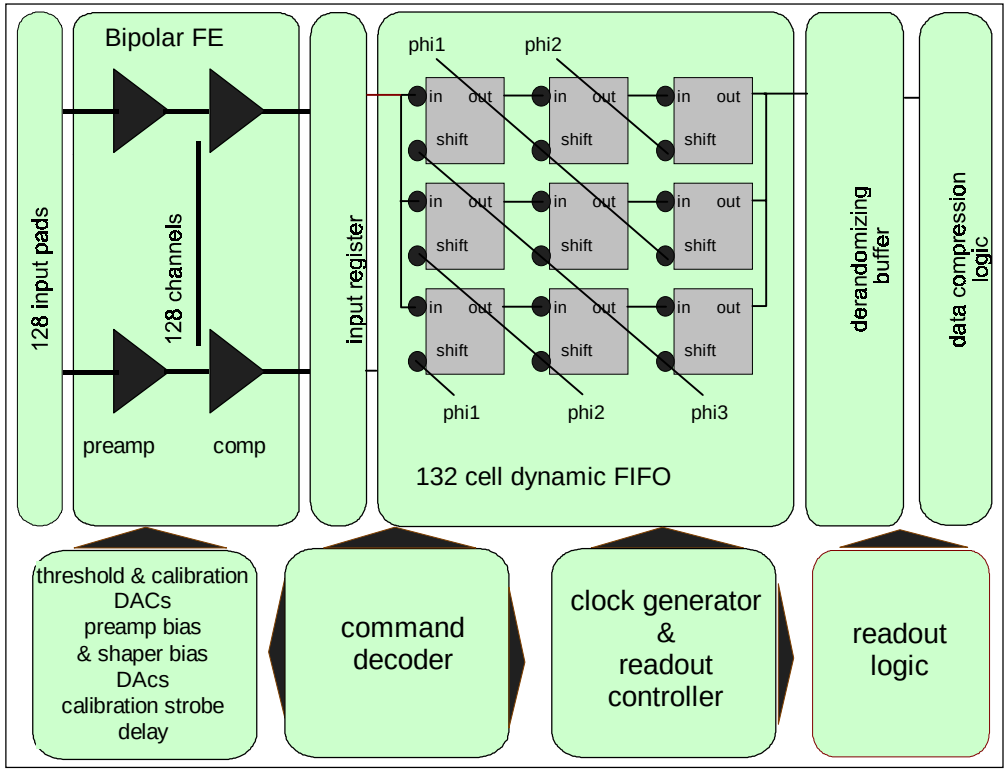
Front-end ASICs	**1.1.2.1 (This presentation)**
Detector Hybrids & Modules	**1.1.2.2 & 1.1.2.3 (Carl Haber's presentation)**
RODs	**1.1.3 (Dick Jared's Presentation)**

The US is also contributing to the electronics system engineering

The Front-End ASIC (Named ABCD)

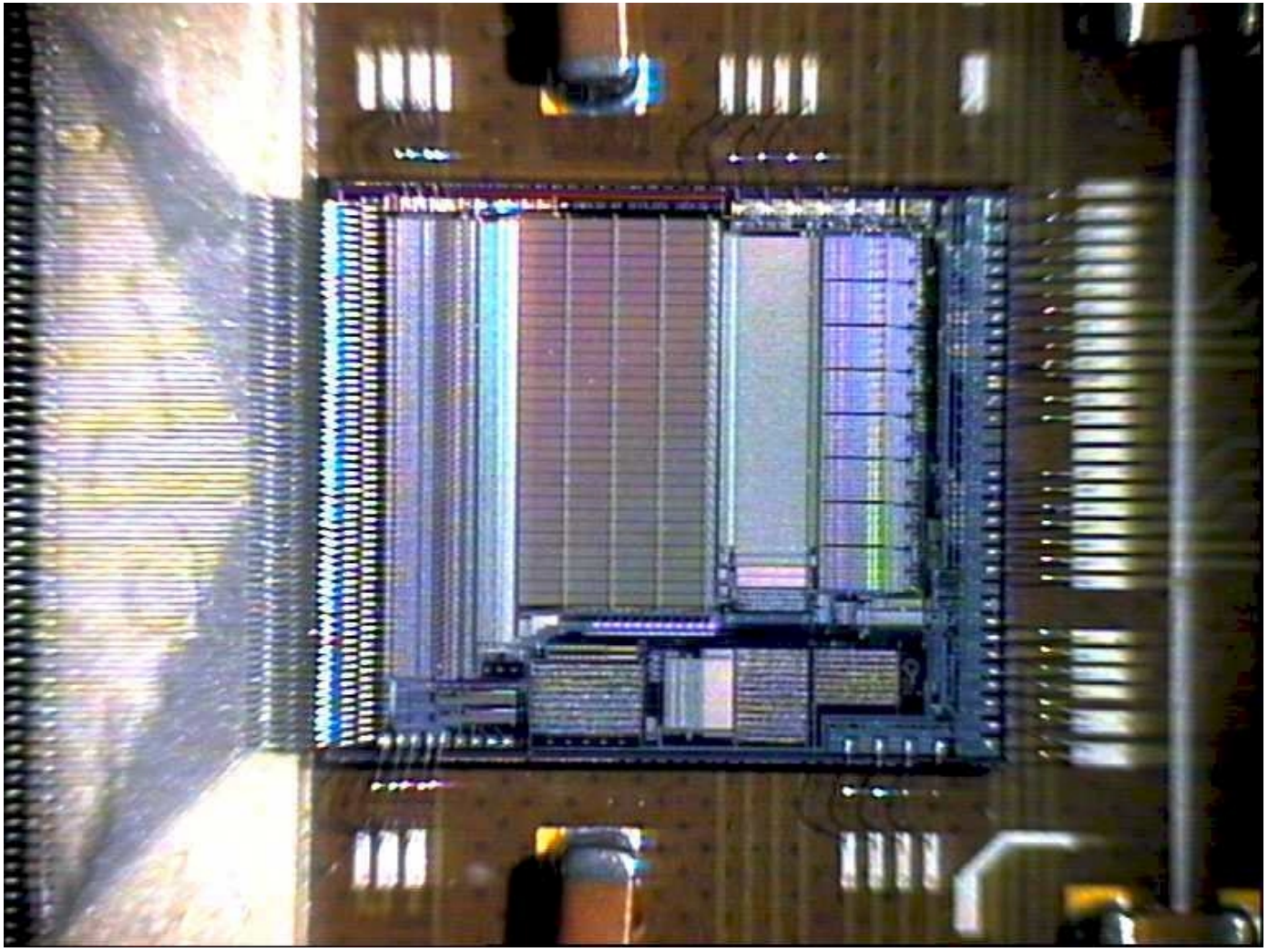
Several years ago the SCT Collaboration selected "Binary Readout" as its baseline.

After parallel developments of two technologies, the ABCD chip fabricated with the DMILL technology was selected last year as the best choice for final production.



This is a biCMOS IC that incorporates bipolar front-end amplifier and shaper circuits, a comparator with programmable threshold (each channel trimable), a pipeline, de-randomizing output buffer, data compression and output serializing circuits.

The ABCD in Silicon



A.A. Grillo
SCIPP - UCSC

Pre-Production Phase

Following the ABCD Final Design Review in March-2000, an order was placed for 40 wafers to be fabricated in 5 mini-lots of 8 wafers each.

The objective was to sample the DMILL fabrication line at 5 points in time and also to give the vendor (Atmel) the financial incentive to operate their DMILL line in a more continuous manner.

- **Atmel runs the DMILL process on the same line with several commercial CMOS processes.**
- **While a few hundred wafers have been processed as part of their qualification of the process after transferring the license and recipe from the French CEA lab, there are currently no designs in production with the technology. The ABCD may be the first.**
- **Yield has been lower than expected on prototype lots and remains a concern.**

A Frame Contract has been negotiated and is in place between CERN and Atmel which fixes the price per wafer (in Euros) and a minimum yield based upon die size (26% for the ABCD). This contract is the basis of our cost estimate and our assurance against disastrous yield.

Due to various delays in the fab line, some caused by an Atmel subcontractor, the delivery of wafers was more sporadic than expected. The last 3 mini-lots were delivered together at the very end of the planned period and were really processed all together. The last lot had an oxide thickness out of spec and has not been officially accepted by SCT pending test results.

Pre-Production Yield (so far)

The yield results for the wafers tested so far are:

	Date Received	# of wafers tested	Yield (perfect)	Yield (incl. 1 bad channel)	Comments
1st	Jul-00	8	10.6%	21.4%	
2nd	Nov-00	8	16.5%	31.0%	Process "Corner" Run
3rd	Feb-01	4	24.7%	42.4%	New inspection instituted
4th	Feb-01	3	8.1%	18.4%	High sheet resistance flagged
5th	Feb-01	2	12.1%	26.7%	Thin oxide flagged

As you can see, the yields for perfect chips do not meet the minimum guarantee.

The process "corner" run showed very little correlation of yield to process variations.
This shows that the design is robust against process variation.

The results of the "corner" run and the significantly higher yield when including one bad channel indicate that the primary yield limiter is defects.

Also, wafers demonstrate a non-random pattern of areas with 0% yield, again indicating a cause of defects.

Of the 25 wafers tested, 6 wafers had yields $\geq$ 26%.

Searching for the Key to High Yield

Analysis by Atmel of areas of 0% yield on a few wafers from the first lot found a correlation with defects in the oxide before first metal deposition. A new inspection was instituted prior to fabrication of the third lot. This may explain its improved yield.

The cause of the low yield on the last two lots is still being examined. All the wafers from the last three lots have not yet been tested.

Atmel now believes that their subcontractor used to deposit the epitaxial layer is introducing a large number of defects, especially defects that affect the bipolar devices.

This is supported by the fact that an alternate vendor was used for a test lot in 1999 and those wafers yield much better (38.2% with the worst wafer at 27.3%).

Atmel is now in the process of qualifying this vendor for production and fabricating a split lot (old and new vendor) of ABCD wafers to determine if this yield improvement is real. These wafers are expected out in April.

Another possible downside is that we are still developing our test specification, reviewing IC performance on modules and after irradiations, in an attempt to improve overall quality. Adjustments to the test specification to improve module performance could result in lower yields. We believe, however, based upon the test results of the "corner" run that such a yield decrease should not be more than a few percent.

If the high yield key is not found before production starts, Atmel will have to reduce the price of the wafers in proportion to gain our acceptance of the wafers.

We have, as a back up, a plan to increase test capacity to cope with this possibility.

Irradiation Tests

Six full modules (12 chips on each) were assembled from the wafers received in July and irradiated in the CERN PS in October.

The modules were irradiated to a total fluence of $3x10^{14}$ protons/cm^2, which corresponds to the full 10-year lifetime at the inner most SCT radius with agreed safety factors.

All performance characteristics (e.g. noise, gain, time-walk) were found to meet requirements after the full irradiation.

Two problems did show up.

Problem 1: Trim-DAC Range Adjustment:

> **A new feature was added to the design prior to the pre-production submission to provide a global range adjustment to the 128 trim-DACs.**
>
> **After full irradiation, it was found that the 2-bit range adjustment could no longer be re-written. However, the trim-DACs continued to operate correctly at the range set prior to irradiation.**
>
> **The problem was quickly diagnosed and a fix found. The fix required a change the VIA mask. This was implemented and the new mask supplied to Atmel fab in time to be included in the last 3 lots which were still in fabrication.**
>
> **Pre-rad tests of the fix indicate that no new problem was introduced. Parts from the new design will be irradiated in April. The expectation, based upon careful simulation, is that the problem will not re-appear.**

The Remaining Nagging Problem

The Vdd Protocol Violation:

The second problem appeared at slightly past 50% of the full fluence.

The symptom is that data, which is serially passed from one chip to the next during readout on the way to the serial optical driver, is corrupted with a few 0s changed to 1s.

Since the chips are operated continuously during the irradiation we have indication when the problem started to occur.

The problem can be mitigated by raising Vdd (power to the digital portion of the chips).

Analysis at the present time:

Of the 72 chips irradiated, only ~20% show the problem.

All failing chips come from the same wafer, however, it was an unfortunate coincidence that most of the 72 irradiated chips came from that same wafer.

The failing chips will work correctly if Vdd is raised to approximately 4.8 V (4.0 V is nominal)

External signals between chips are good. Probing of internal signals indicates the problem is in the digital logic after the data receiver circuit on failing chips.

Curiously, lowering the temperature requires a higher Vdd. There is significant correlation between CMOS speed (as measured by on-chip delay generator) and minimum Vdd for acceptable performance.

Continuing Studies

Work is continuing to understand this problem:

Further analysis of wafer test data, looking for a correlation with failing chips

Studies of the post-receiver data processing circuit including simulations looking for a cause for the extra delays measured by probing the failing chips

More radiation studies of chips from different wafers and with different speeds as measured at wafer test

Several possible remedies are being considered:

A design fix once the cause has been identified

A new screen at wafer test to bin the parts into those most likely and most unlikely to show this problem. If continued irradiation studies show that the problem only appears late in the expected lifetime fluence, the weak parts could be used for modules at the outer radius.

Increase the operating voltage for modules at the inner radius, possibly up to 5.0 V.
This will increase the power consumption so it has implications for cooling and for issues related to over-voltage protection.

Plans

Planning optimistically to keep on the production schedule, we scheduled the ABCD "Production Readiness Review" (PRR) for 4-Jul of this year.

The target is to have a remedy (likely one of those mentioned above) for this last problem with the added expectation that the further radiation tests in April do not turn up any new problems.

With regard to the yield, we expect that the combination of the new epitaxy sub-contractor and much more careful attention to detail by the Atmel fabrication personnel will move the yield above the minimum guarantee point.

If the remedy to the Vdd Protocol Violation problem requires more time to implement (e.g. a mask change with follow-up fabrication) we could start production of approximately 50% of the ICs to be used on modules only at the outer radii. This could buy us approximately 6 months to execute a final solution but critically depends upon confirmation in the April radiation tests that the problem does not appear until the chips have been exposed to at least 50% of the total expected fluence.

We will make the final decision on whether to proceed with the PRR on 4-Jul or to delay it when the data is reviewed for the Module Final Design Review in late May.

If the PRR is delayed because we must first fully execute a fix to this last problem, the production schedule could be delayed by 6 months.

Systems Engineering

Alex Grillo has been the Electronics Coordinator for the SCT since 1995.

After several failed attempts to recruit an electronics system engineer for SCT at CERN or at one of the other European institutes, Ned Spencer, also from UCSC, has taken on that job.

A comprehensive plan for grounding and shielding has been developed.

This plan is being tested in the SCT System Test Lab at CERN. As of this time, only a small number of modules have been operated simultaneously due to the lack of assembled modules. This number is expected to grow this summer to 18 barrel modules and 18 forward modules.

There is a severe limitation on material inside the tracker volume. This means that each element of shielding must be justified and proven to work.

There is considerable concern about common mode noise injected by the power supplies (custom designed by another SCT collaborator) or picked up on the long cable runs. Work is now starting to analyze these effects and develop proper filtering.

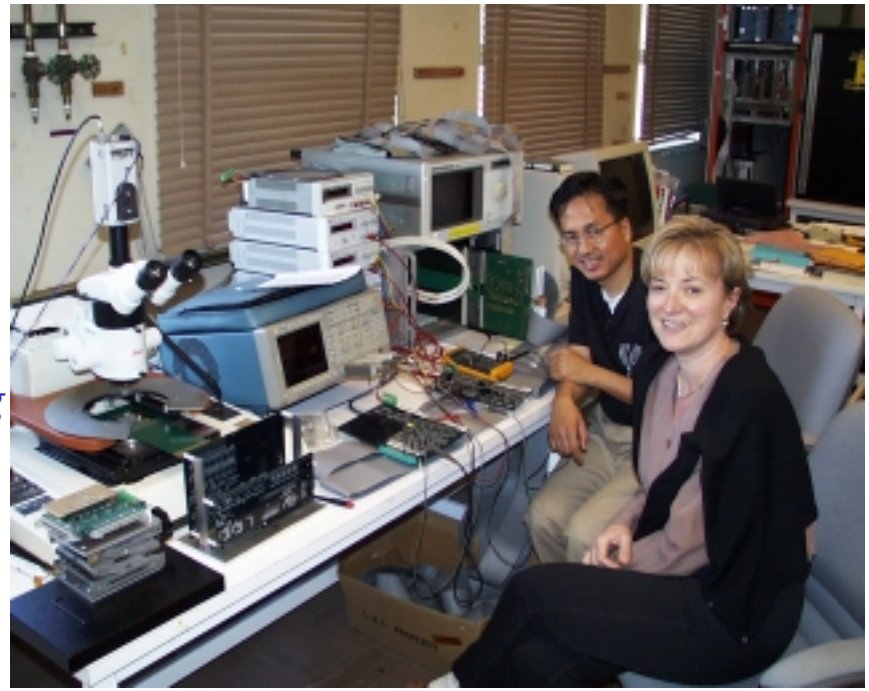
Adding to this challenge is the severely limited space for services exiting the tracker through the calorimeter and muon system.

A detailed power supply specification review was conducted last summer and a grounding safety review for all of ATLAS was held in December. Much work is left to be done but we are finally focused on a coherent plan.

SCT ASIC Tester Development

Original LBNL design (Hubert Niggli)

LBNL - design, hardware production, software
Alessandra Ciocio, Vitaliy Fadeyev,
Chinh Vu, Thorsten Stezelberger,
Gil Gilchriese, Carl Haber,
Francesco Zetti
George Zizka, Helen Chen, Co Tran
Rhonda Witharm



UC SantaCruz – implementation, debugging
Alex Grillo, Abe Seiden,
Max Wilder, Ned Spencer

CERN – Wafer production
and Software for control and analysis
Francis Anghinolfi, Jan Kaplon,
Wladek Dabrowski,
Wojciech Bialas, Carlos Lacasta (Valencia)

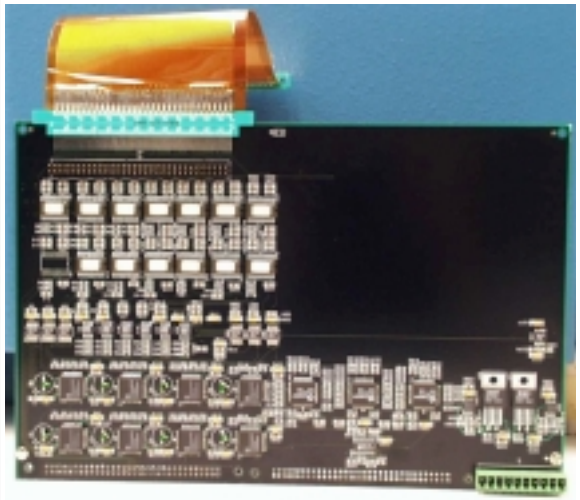
SCT ASIC Tester

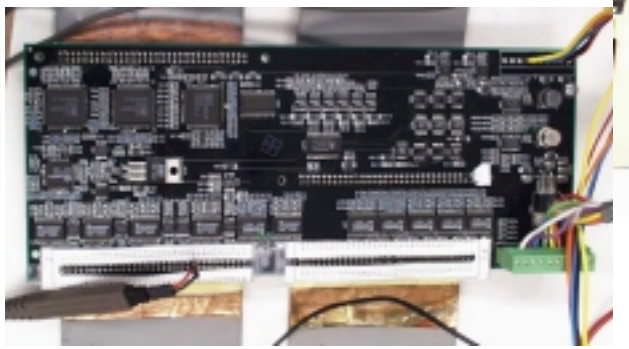
- **SCT DAQ electronics not sufficient to drive chips while under wafer probe**
- **LBL system was developed to allow high speed wafer testing and to scan signal and timing margins.**
- **The full production lot cannot be scanned without this system -> too much time**
- **First version of fully working systems delivered to CERN, RAL, and UCSC (January)**

SCT ASIC Tester

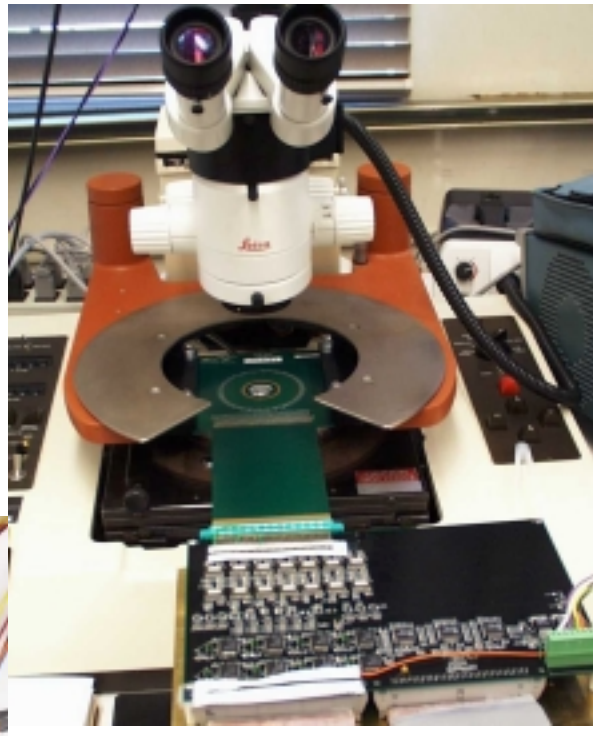
VME Board

Pindriver board(s)



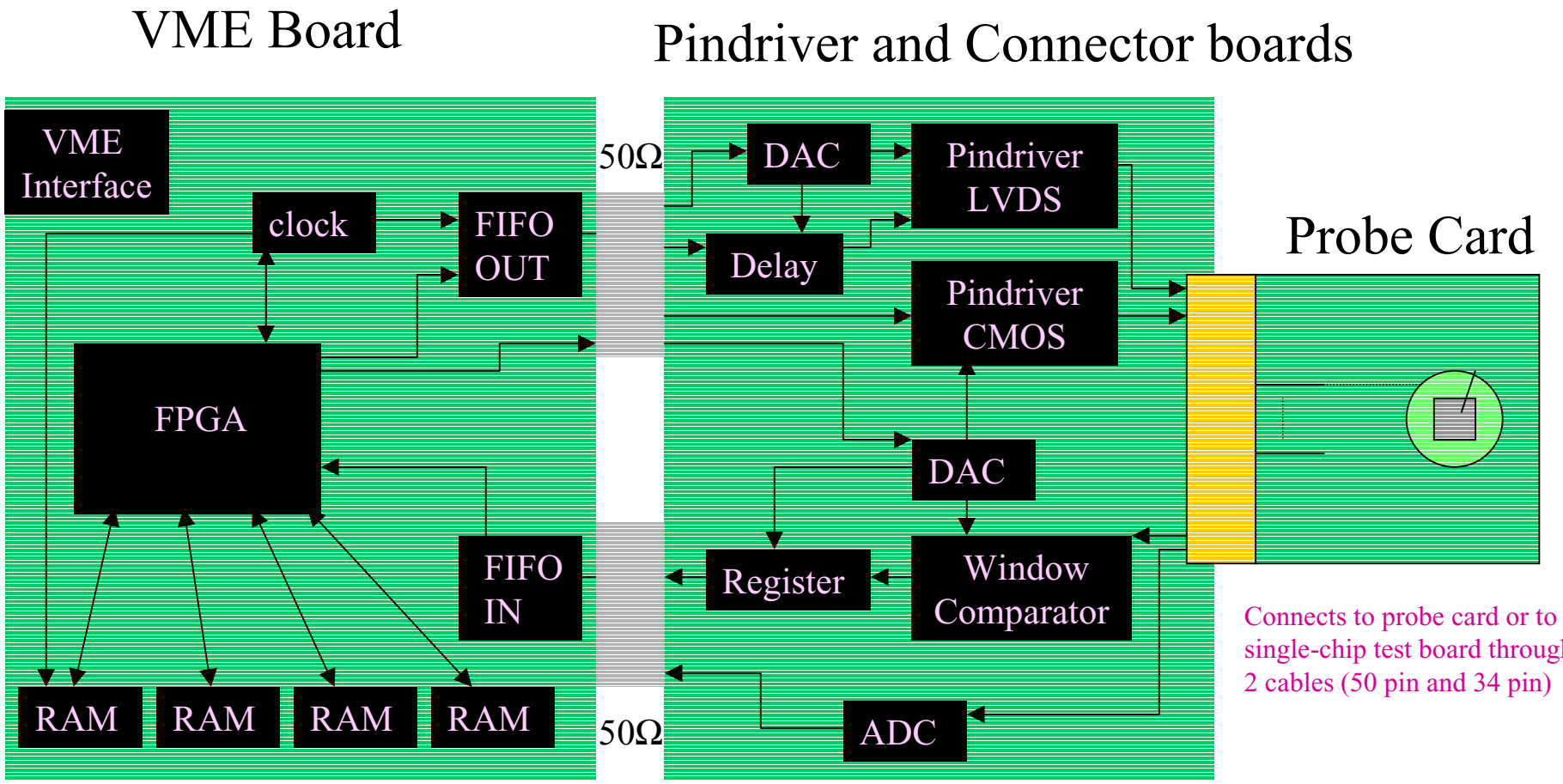


Probe Card



http://www-atlas.lbl.gov/strips/tester/

Overview



Connects to probe card or to a single-chip test board through 2 cables (50 pin and 34 pin)

All operations are programmed in the FPGA using VHDL
On-board comparison of chip response to testvectors with Verilog simulation. The simulation vector is stored in the sim vector memory. The result of the comparison is one bit in the FPGA status register. Frequency from 40-80 MHz

Allow to adjust amplitude and delay of the signals within a range to test functionality of ABCD by feeding signals through pindriver and delay chips. DACs allow varying parameters.
Signals from ABCD go through window comparators.

Status of the Hardware

Major steps for the past few months

- **During the summer 2000 we went through submission of new layout for all boards:**
  VME Board, Pindriver and Connector Boards
  - **We kept the original design but we fixed major bugs**
  - A50 pin and a 34 pin 3M connectors replaced the 128 pins edge connector on Connector Board
  - **We assembled Pindriver and Connector Board in a box with a built-in fan for cooling**

  Probe Card
  - **We designed a custom card to accommodate for different probe stations geometry**
    - Differential pair signals are layout in parallel and on the same trace layer
    - Low frequency filter is applied to the differential threshold lines (VT1, VT2) and Shaper+Preamp Current lines
    - 6 layers (50 ohm matched impedance ,full body gold) in the following order:
      Top traces, VDD, Digital and Analog layer spit plane, Analog ground, VCC, Bottom traces layer

  Single-chip test Board (see slide)
- **We sent one of two prototype systems to Carlos Lacasta (Valencia) to start developing software (July)**
- **Vitaliy Fadeyev (postdoc) joined the LBNL group in July**
- **New system was available at LBNL in September**
- **We sent a first prototype system to CERN (October)**

NEW fully operational systems installed at CERN, RAL, and UCSC in January

Status of the Software

- Stand-alone diagnostic software to perform Threshold Scan and Testvectors at LBNL running on PC/WNT, controlling VME using NI-MXI/PCI interface

- The new system functionality has been merged into CERN Online Control software (Visual C++ application, running on PC/W95 developed by Carlos) and Analogue + Digital tests have been implemented (Verilog simulation is provided by F. Anghinolfi/CERN)

- Beta release of Online Control Software (February 2001)
- Release of offline software for analysis of wafer screening data

- We need to define the additional tests that the new system makes possible, like signal phase and amplitude margins, and higher frequency clocking for a better screen of the IC's.
  The final test specification must be approved by Atmel in accordance with contract for yield guarantee.

- Documentation in progress
- UCSC and CERN have fully working system, RAL still developing integration of local probe station control software into Beta release.

In Progress

- New boards (pindriver and VME) under revision to clean up patches and jumpers. Completion by mid-summer.
- New design of single-chip test card for diagnostics (summer).

- A full comparison of the CERN old system and the LBNL systems will be performed first by testing wafers from current batch to verify same yield results.
- Comparison of new tester systems at CERN and UCSC with same wafers.

- Implementation of new tests (higher frequency, amplitudes and phases) in the control software (work to be done in collaboration with C. Lacasta/Valencia)

- Final version of offline software completed but under installation at different sites

- Getting ready for PRR in July