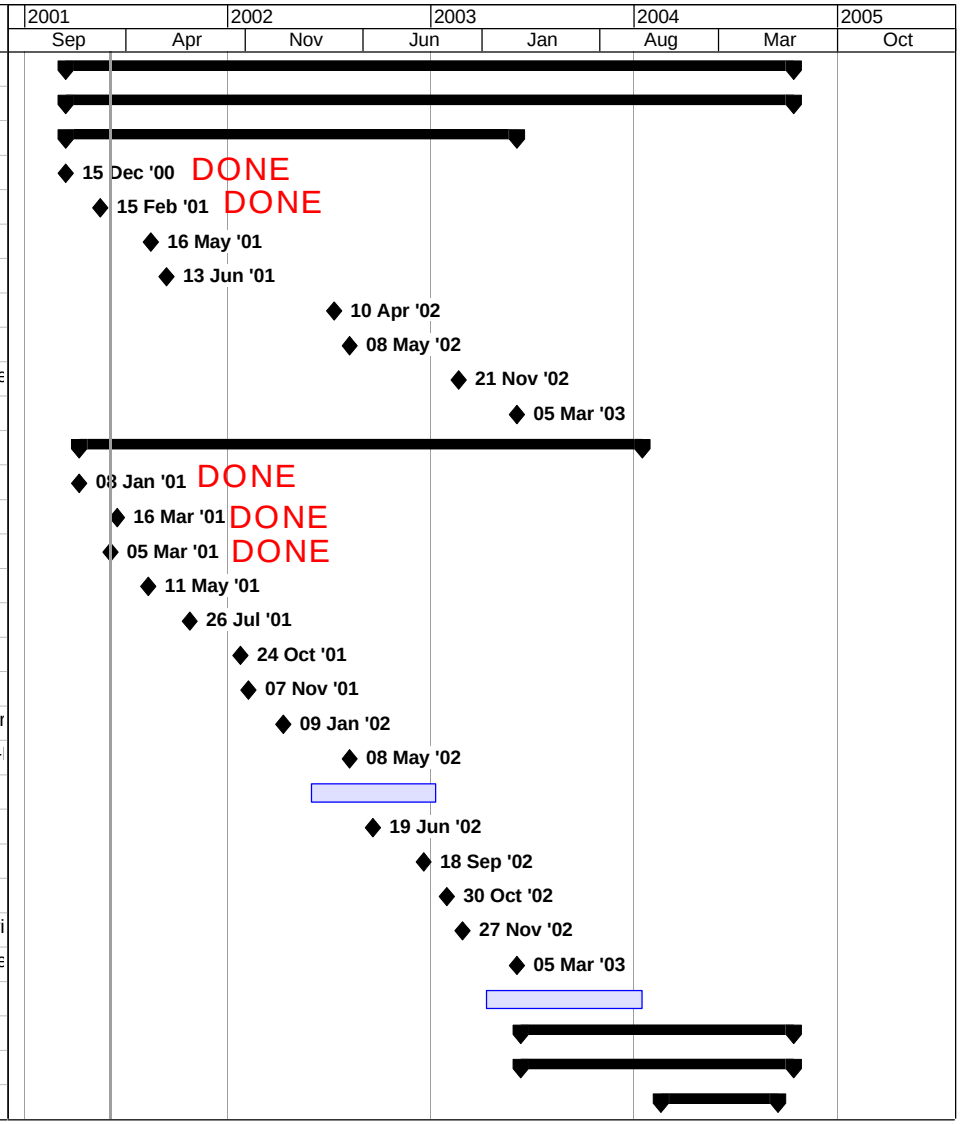
Pixel Frontend Electronics
in 0.25m CMOS

- Pixel → Radiation-tolerant CMOS design
  CERN RD-49, FPIX for BTeV, ...
  Smaller feature size has allowed design to become more conservative (*DMILL* design was space-constrained)

- Pixel FE-I Roadmap
  Technology/Design developments required
  Test chips
  Planning and status

Plan as Presented in Pixel Baseline Review (11 '00)

ID	WBS	Task Name
1	1.1.1	**US ATLAS Pixel Project**
2	1.1.1.1	**Electronics**
3	1.1.1.3.	**Design**
4		DMILL Review
5		DMILL decision(FE-D3 or not)
6		FE-I1 spec complete
7		FE-I1 FDR
8		FE-I2 spec complete
9		FE-I2 FDR
10		Compl. Spec forIBM production order re
11		IBM FE PRR
12	1.1.1.3.	**Development/Prototypes**
13		Submit TSMC digital test chip
14		Digital test chip delivered
15		Submit TSMC analog test chip
16		Analog test chip delivered
17		1st IBM prototype submitted(FE-I1)
18		1st IBM prototype delivered
19		Complete initial wafer probe FE-I1
20		First bump bonded FE-I1 assemblies arr
21		Complete initial lab/ irradiation tests FE-
22		Beam/system tests of FE-I1 assemblies
23		2nd IBM prototype submitted(FE-I2)
24		2nd IBM prototype wafers delivered
25		Complete initial wafer probe FE-I2
26		First bump bonded FE-I2assemblies arri
27		Complete initial lab/system/ irradiation te
28		Beam/system tests of FE-I2 assemblies
29	1.1.1.3.	**Production**
30		**Outer FE Production**
35		**B-Layer FE Production**



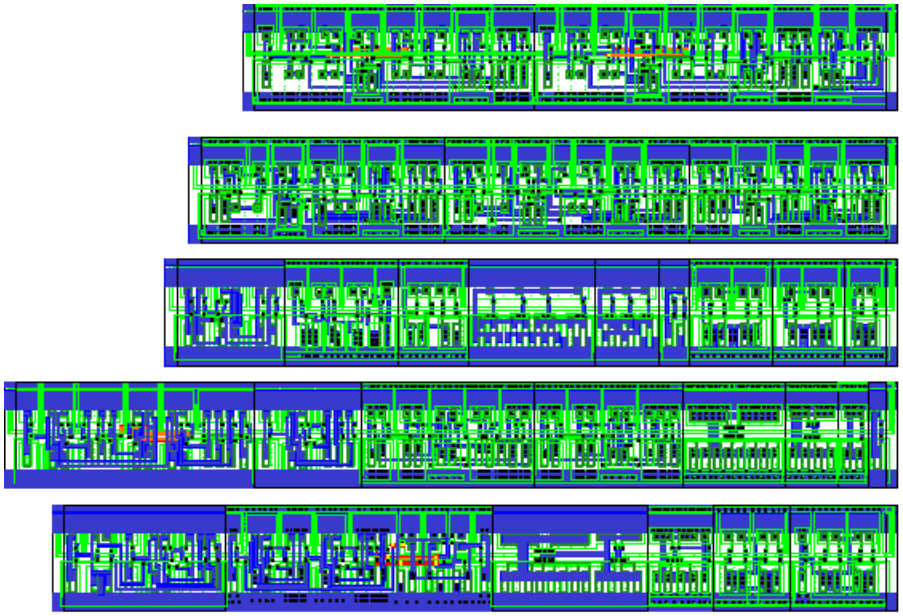
Roadmap

- Develop in two technologies
  Baseline: order via CERN frame contract, Backup: TSMC
- Insert test chip runs to cross-check (before full wafer run)
- Minimize layout time (Small feature size ⇒ extra space. Use synthesis + automated place-and-route wherever possible)
- Maximize verification time (2 000 000 transistor, mixed-mode chip)
- Submit 1st full-wafer run by end July '01

FE-I Design team

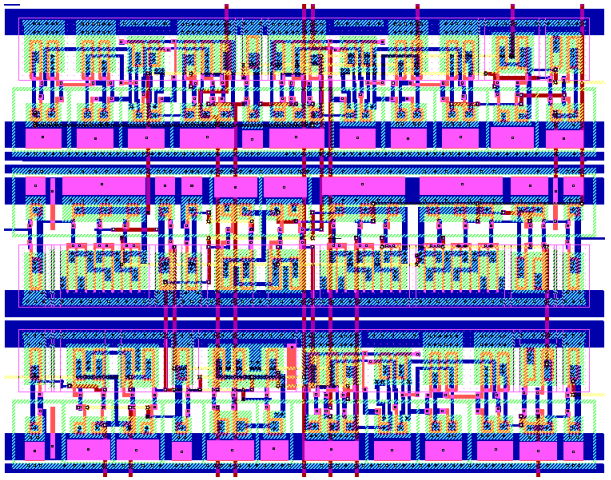
Mario Ackers - Bonn
Laurent Blanquart - Marseille
now LBL (from 28 Feb. 01)
Giacomo Comes - Bonn
Peter Denes - LBL
Kevin Einsweiler - LBL
Peter Fischer - Bonn
Ivan Peric - Bonn
Emanuele Mandelli - LBL
Roberto Marchesini - LBL (until 16 Jan 01)
Gerrit Meddeler - LBL

Technology / Design Developments



Mixed-mode standard cell library (Modification of CERN / RAL library - Bonn)

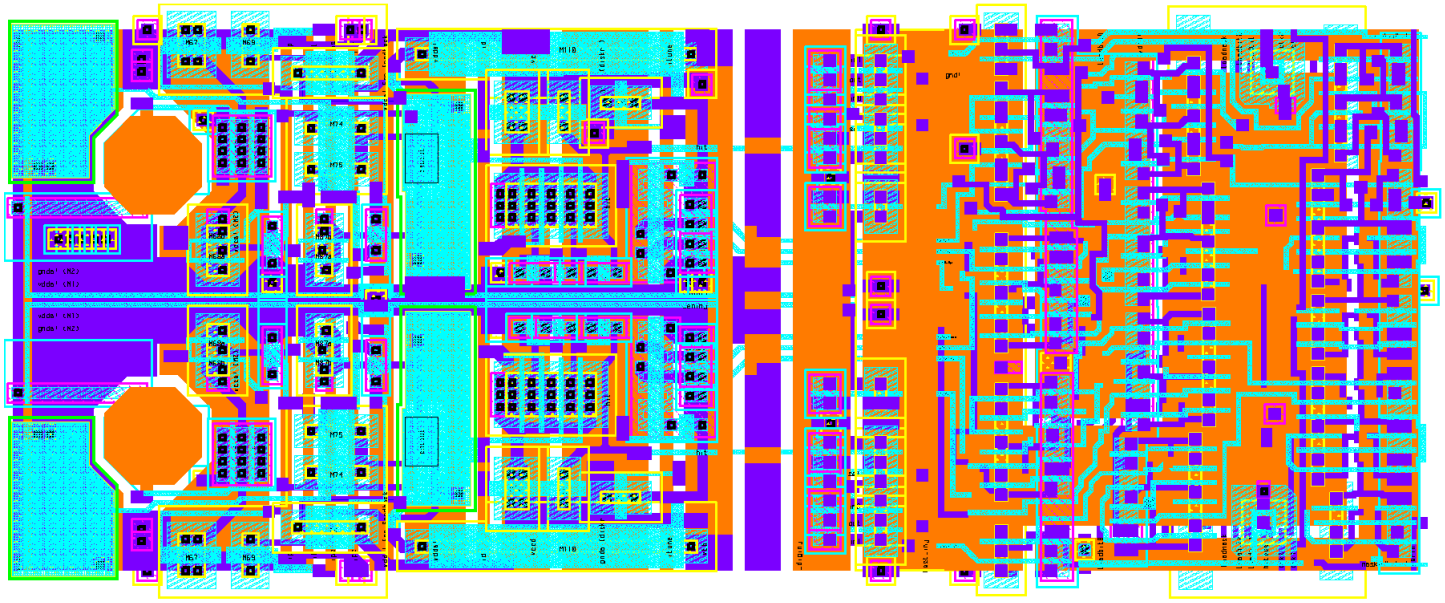
Implement Silicon Ensemble (to be able to autoroute standard cells - LBL)



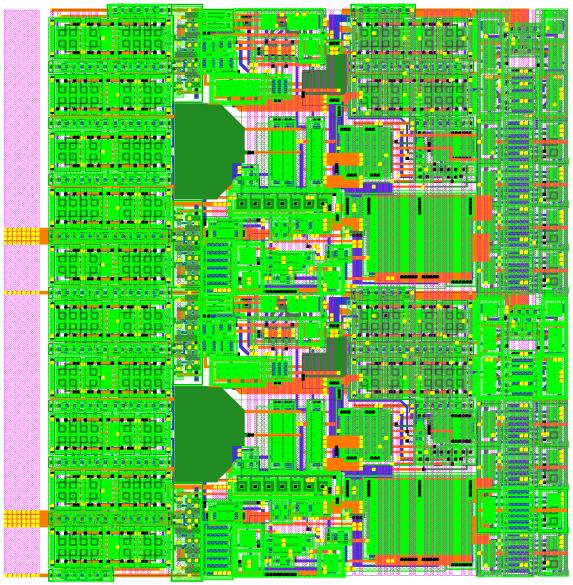
example - Pixel Logic

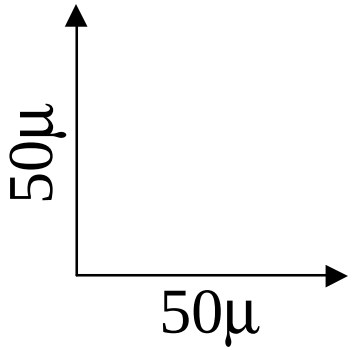
Comparative Size

Two pixels (analog) in *DMILL*

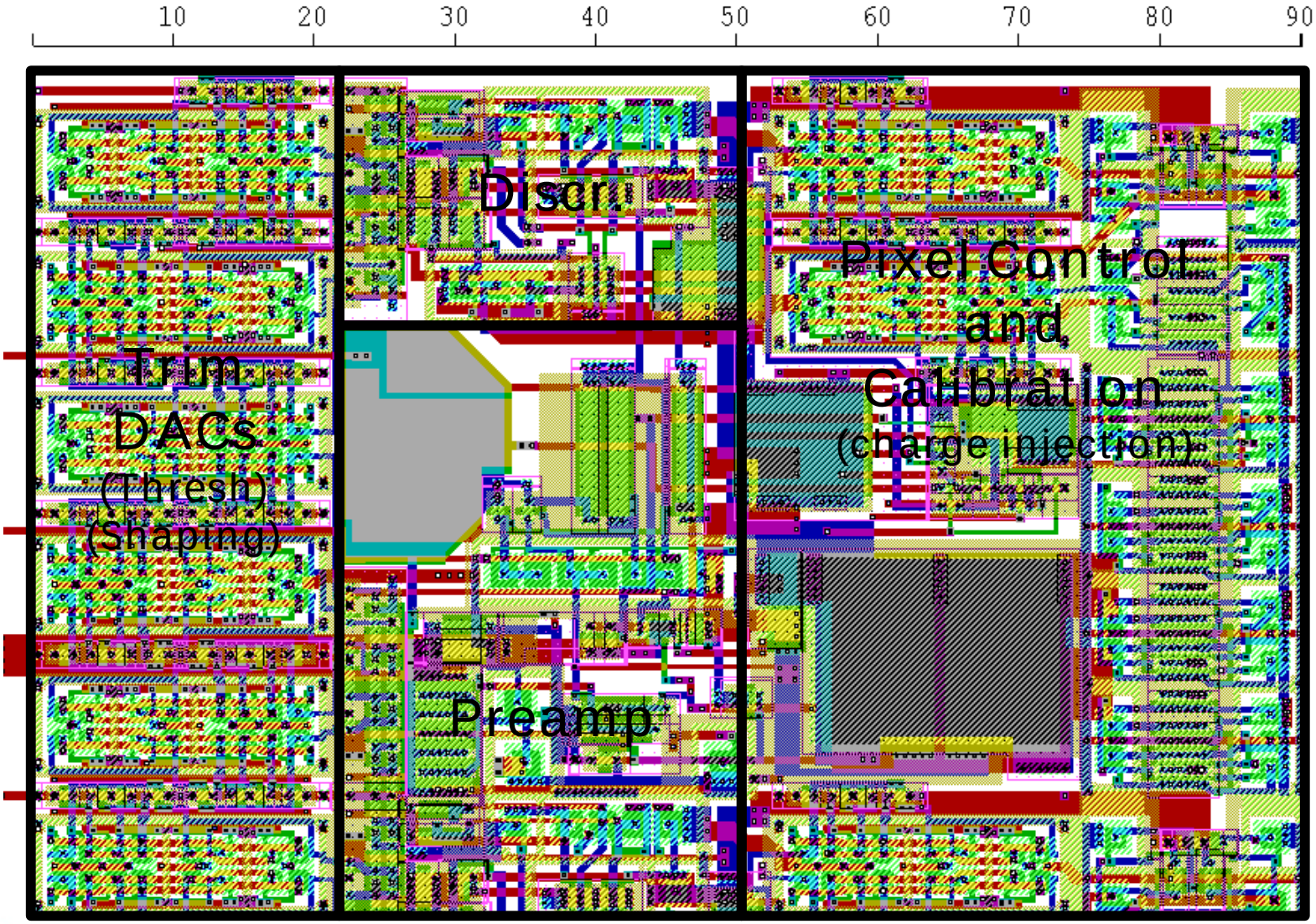


Two pixels in 0.25µ





In a Pixel

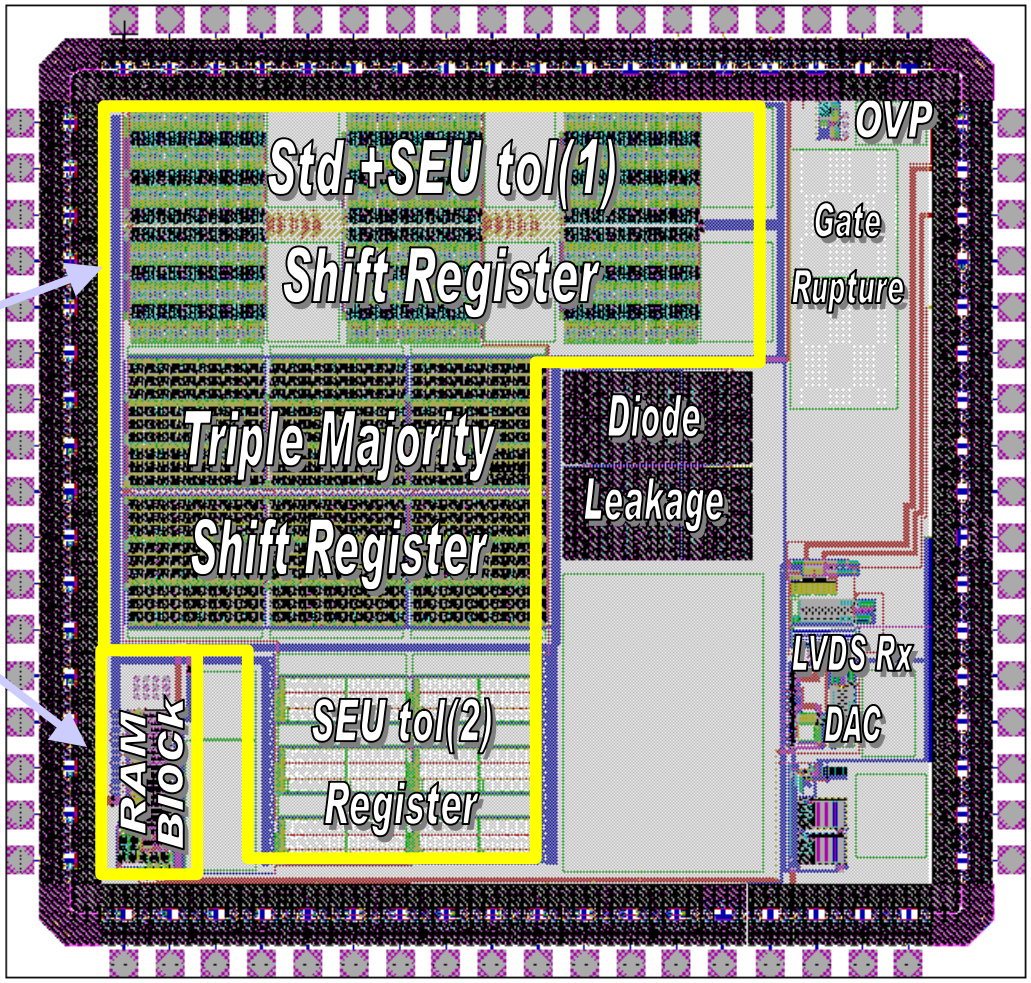

10
20
30
40
50
60
70
80
90
Trim
DACs
(Thresh)
(Shaping)
Discr.
Preamp
Pixel Control
and
Calibration
(charge injection)

Digital Test Chip

TSMC 0.25µ
Submitted 08 Jan ‘01

Structures to test SEU sensitivity of storage registers
Pixel RAM block

Irradiate Apr ‘01

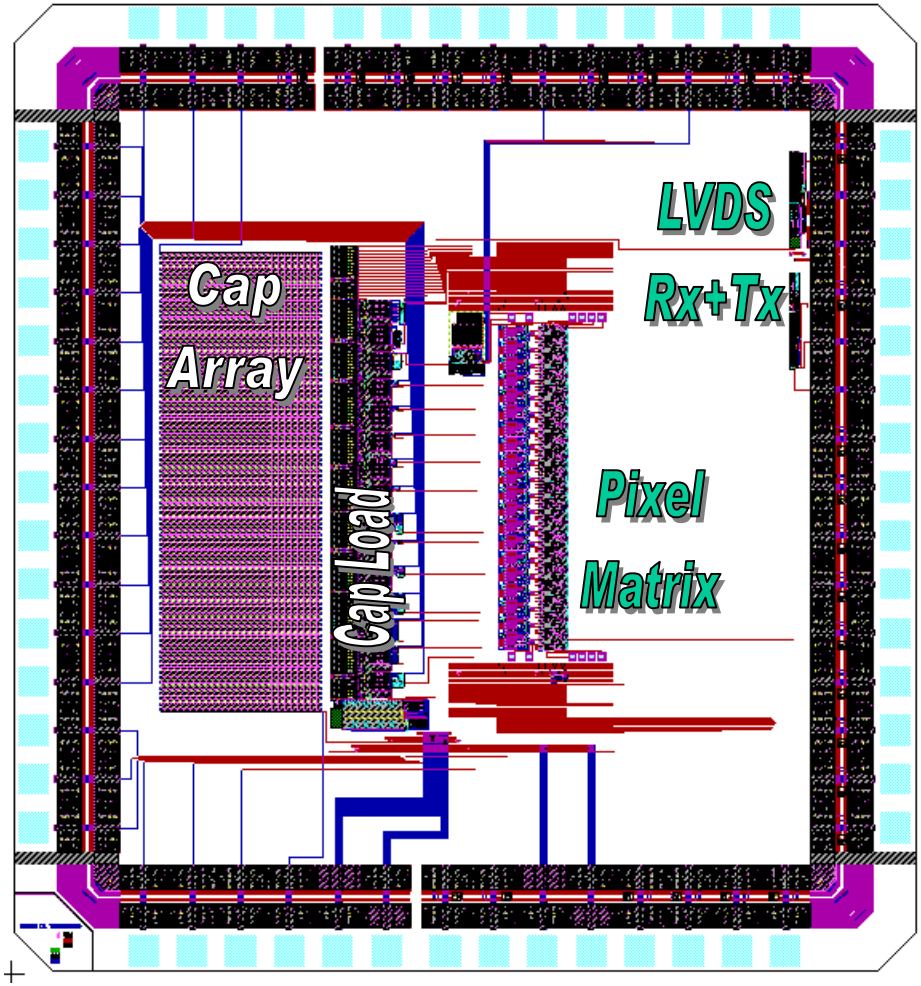


Analog Test Chip

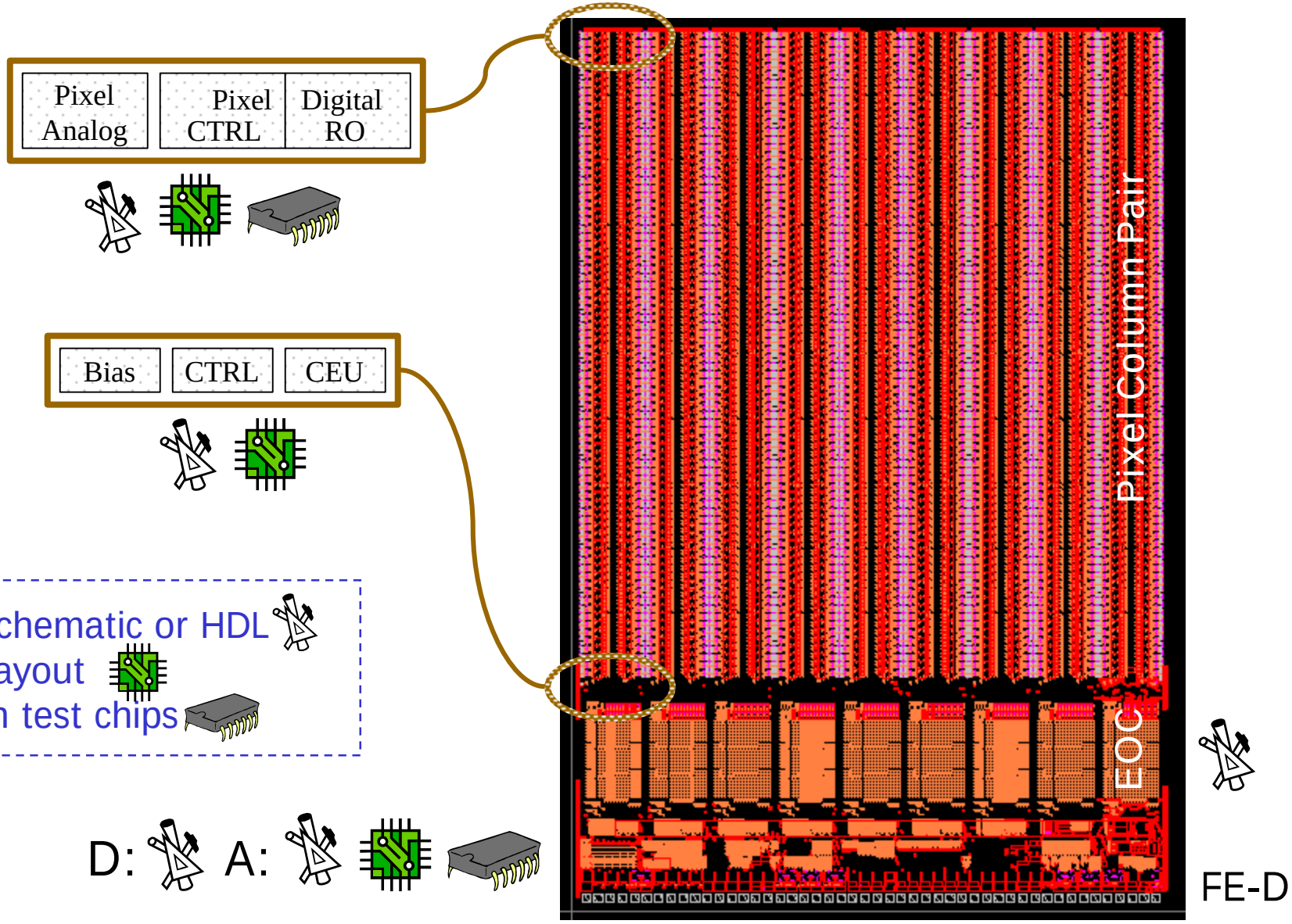
Submitted (CERN) 28 Feb 01
Submitted (TSMC) 6 Mar 01

Array of pixels along with other analog functions

- Preamp and discriminator
- Trim DACs
- Main DACs
- 50Ω output buffer
- Input capacitance test structure

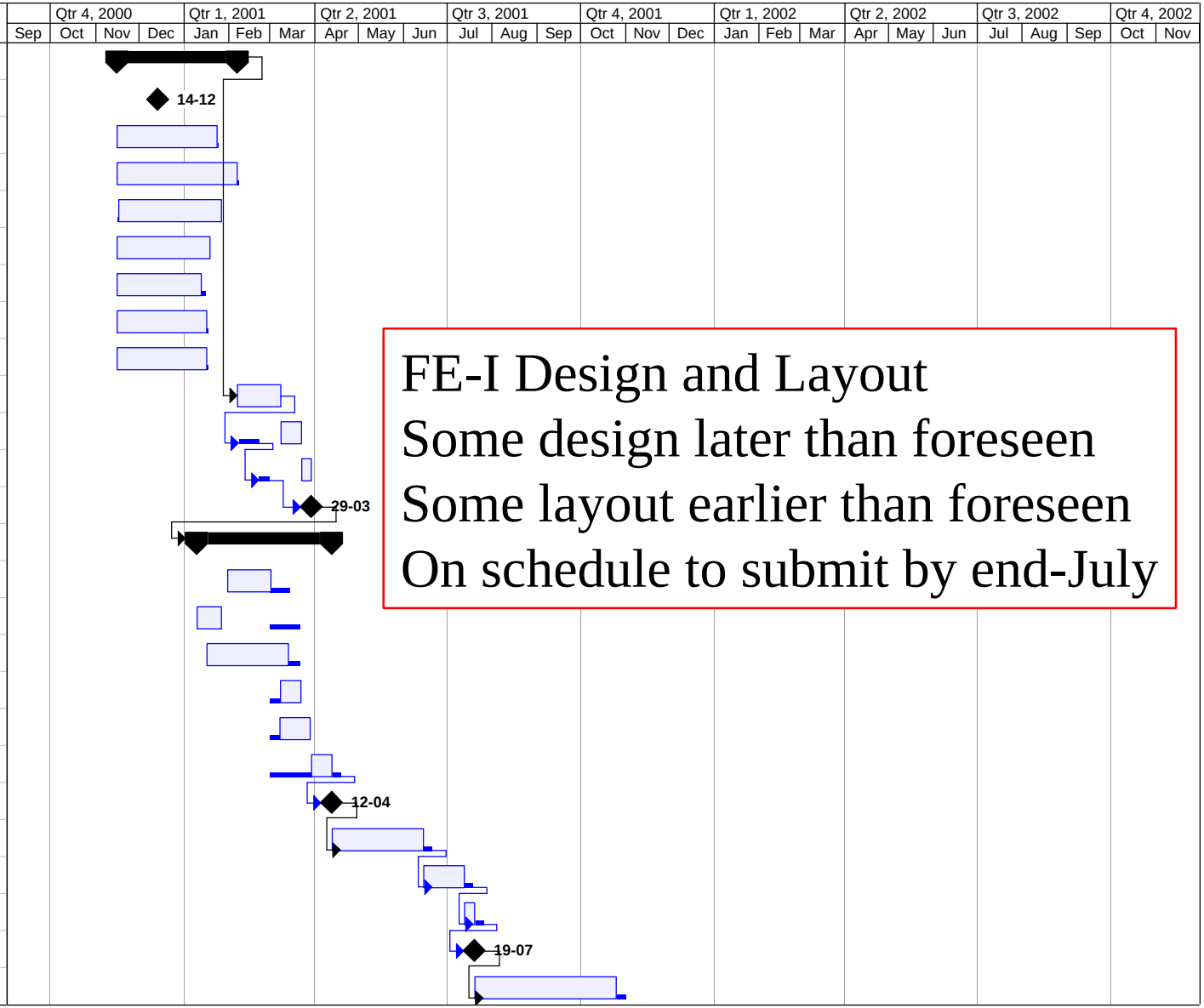


Status - Ready to Assemble Final Chip



Planning (1) - Design/Fabricate

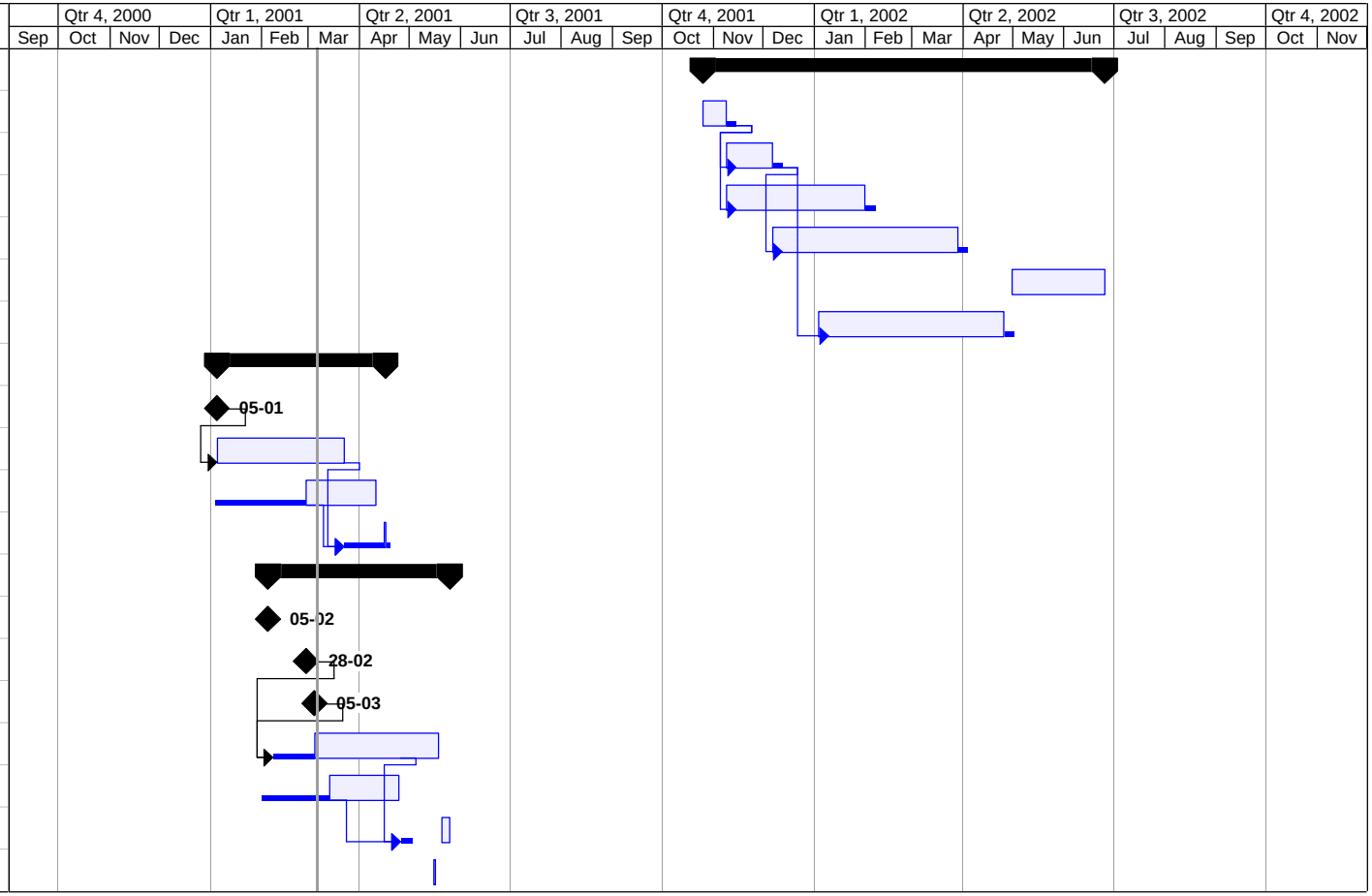
ID	Task Name
1	**Design**
2	Kickoff Meeting
3	Specification
4	Pixel analog
5	Pixel digital
6	EOC logic
7	Chip digital
8	Chip analog
9	Chip pad+ESD
10	Final Schematics
11	Top level sim (sch)
12	(Modifications)
13	PDR
14	**Layout**
15	Pixel analog
16	Pixel digital
17	EOC logic
18	Chip digital
19	Chip analog
20	Chip integration
21	Extract
22	Post-layout sim
23	(Modifications)
24	CDR
25	Submit
26	Fab



FE-I Design and Layout
Some design later than foreseen
Some layout earlier than foreseen
On schedule to submit by end-July

Planning (2) - Characterization

ID	Task Name
27	**Characterization**
28	Wafer Probe
29	Bump, thin, flip
30	Irradiate (chips)
31	Lab test of assemblies
32	Test Beam (modules)
33	Irradiate (modules)
34	**Digital Test Chip**
35	Submit
36	Fab
37	Test card
38	Irradiate
39	**Analog Test Chip**
40	Planned Submit
41	Submit Process 1
42	Submit Process 2
43	Fab
44	Test card
45	Test
46	Irradiate



US ATLAS E.T.C.

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.3	Electronics	0	0	0	0	0	615	621	354	26	0	1616
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	446	161	0	0	989
1.1.1.3.1.1	IC design	0	0	0	0	0	189	269	11	0	0	469
1.1.1.3.1.2	Test design	0	0	0	0	0	140	75	0	0	0	216
1.1.1.3.1.3	Systems Engineering	0	0	0	0	0	52	101	151	0	0	304
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	234	133	0	0	0	367
1.1.1.3.2.1	Atmel/DMILL prototypes	0	0	0	0	0	130	0	0	0	0	130
1.1.1.3.2.2	Honeywell	0	0	0	0	0	10	0	0	0	0	10
1.1.1.3.2.3	0.25 Micron	0	0	0	0	0	0	54	0	0	0	54
1.1.1.3.2.4	Test	0	0	0	0	0	94	79	0	0	0	173
1.1.1.3.3	Production	0	0	0	0	0	0	42	193	26	0	261
1.1.1.3.3.1	Front-end ICs	0	0	0	0	0	0	19	140	26	0	185
1.1.1.3.3.2	Optoelectronics	0	0	0	0	0	0	23	53	0	0	76