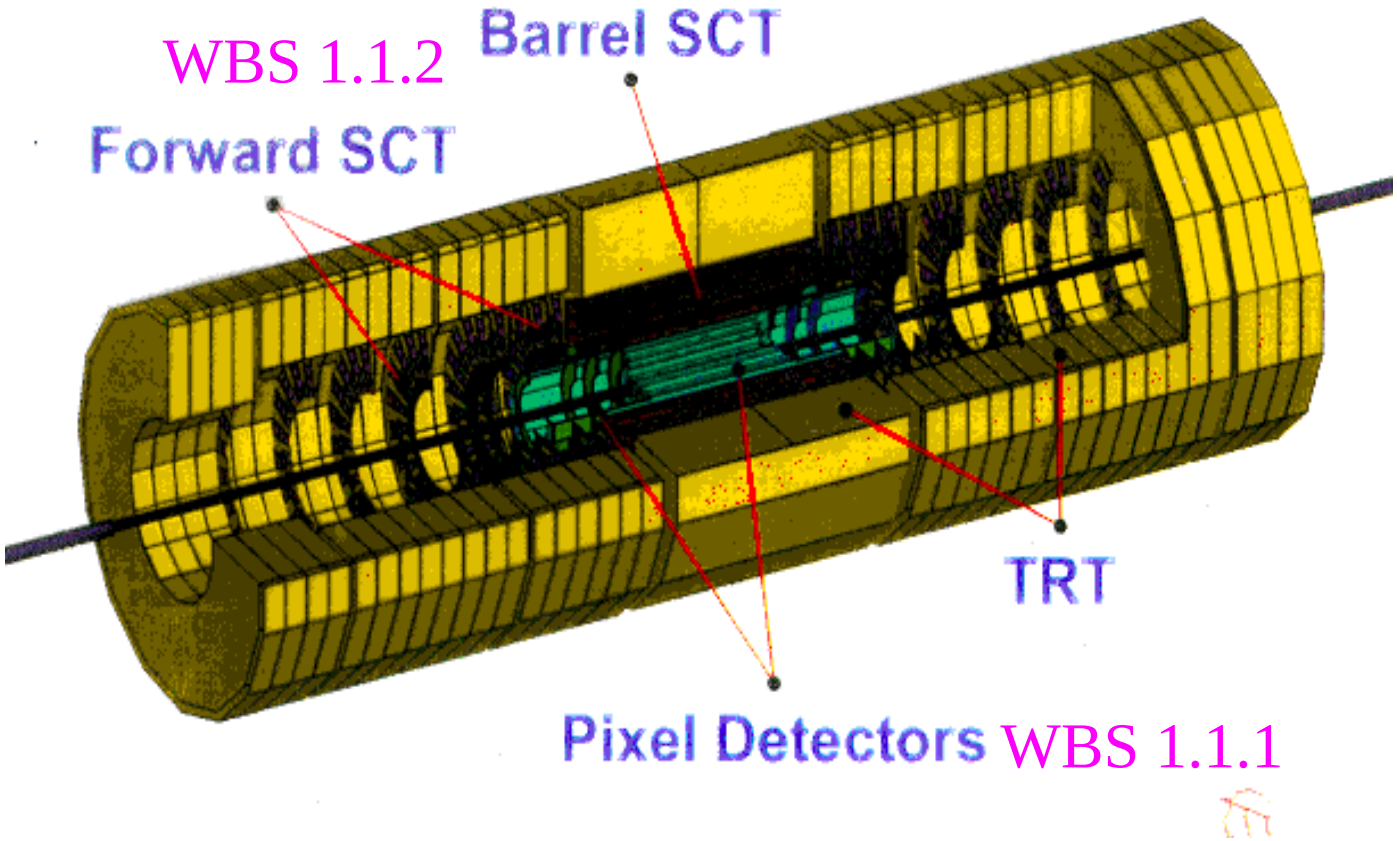
WBS 1.1 Silicon Subsystem

M. G. D. Gilchriese

Lawrence Berkeley Laboratory

Silicon Subsystem



ReadOut Drivers - WBS 1.1.3

Organization

- **Institutions and responsibilities - no changes**
- **Management**
  - **Senior physicist and engineer added to pixel team**
  - **Otherwise no changes at Level 4 or above**
- **Other personnel**
  - **Engineering added**
  - **Modest increase in technical staff**

Institutions

SUNY Albany
Iowa State University
UC Berkeley/LBNL
University of New Mexico
Ohio State University
University of Oklahoma/Langston Univ.
UC Santa Cruz
University of Wisconsin

Management

1.1.1 Pixels(Gilchriese)
1.1.1.1 Mechanics/Services(Gilchriese, Anderssen)
1.1.1.2 Sensors(Seidel, Hoeferkamp)
1.1.1.3 Electronics(Einsweiler, Denes)
1.1.1.4 Hybrids(Skubic, Boyd, Gan)
1.1.1.5 Modules(Garcia-Sciveres, Goozen)

1.1.2 Silicon Strips(Seiden)
1.1.2.1 IC Electronics(Grillo, Spencer)
1.1.2.2 Hybrids(Haber)
1.1.2.3 Modules(Haber, Senior Techs)

1.1.3 RODs(Jared, Fasching, Meyer)

(Physicist, Engineer or Senior Tech)

Highlights Since Last Review

- **Pixels**
  - Design of Pixels and Inner Detector changed to allow insertion or removal of Pixels without removing rest of Inner Detector => gain >1 year in pixel critical path schedule
  - Production baseline cost and schedule established
- **Silicon Strips**
  - Preproduction order of rad-hard front-end integrated circuits(40+ wafers) delivered
  - Baseline design of barrel modules established
- **ReadOut Drivers**
  - Prototype ROD fabricated and under test

Silicon Performance Data

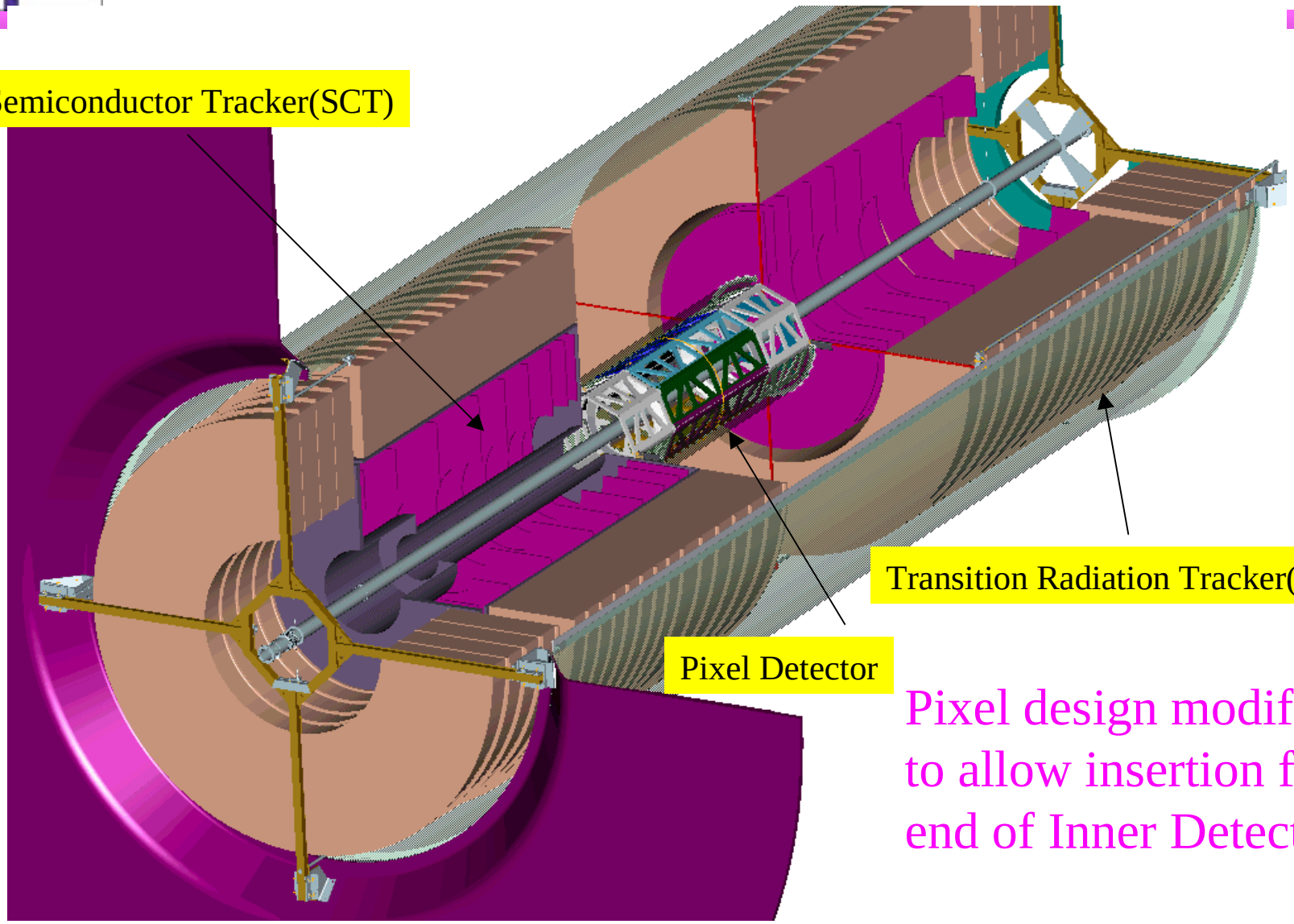
Comparison Against ETC00 Baseline

WBS Level 3 through 1/31/01

WBS	Description	BCWS	BCWP	ACWP	SV	CV
Silicon						
1.1.1	Pixels	2,787,269	2,787,269	2,185,800	-	601,469
1.1.2	Silicon Strip System	4,403,865	4,385,805	3,927,380	(18,060)	458,425
1.1.3	RODs	1,252,803	1,057,053	1,181,667	(195,750)	(124,614)
	Total	8,443,937	8,230,127	7,294,847	(213,810)	935,280

- **Some delay in silicon strip system(ICs)**
- **Delay in prototype ROD -> production delay**
- **Details to follow after technical status described**

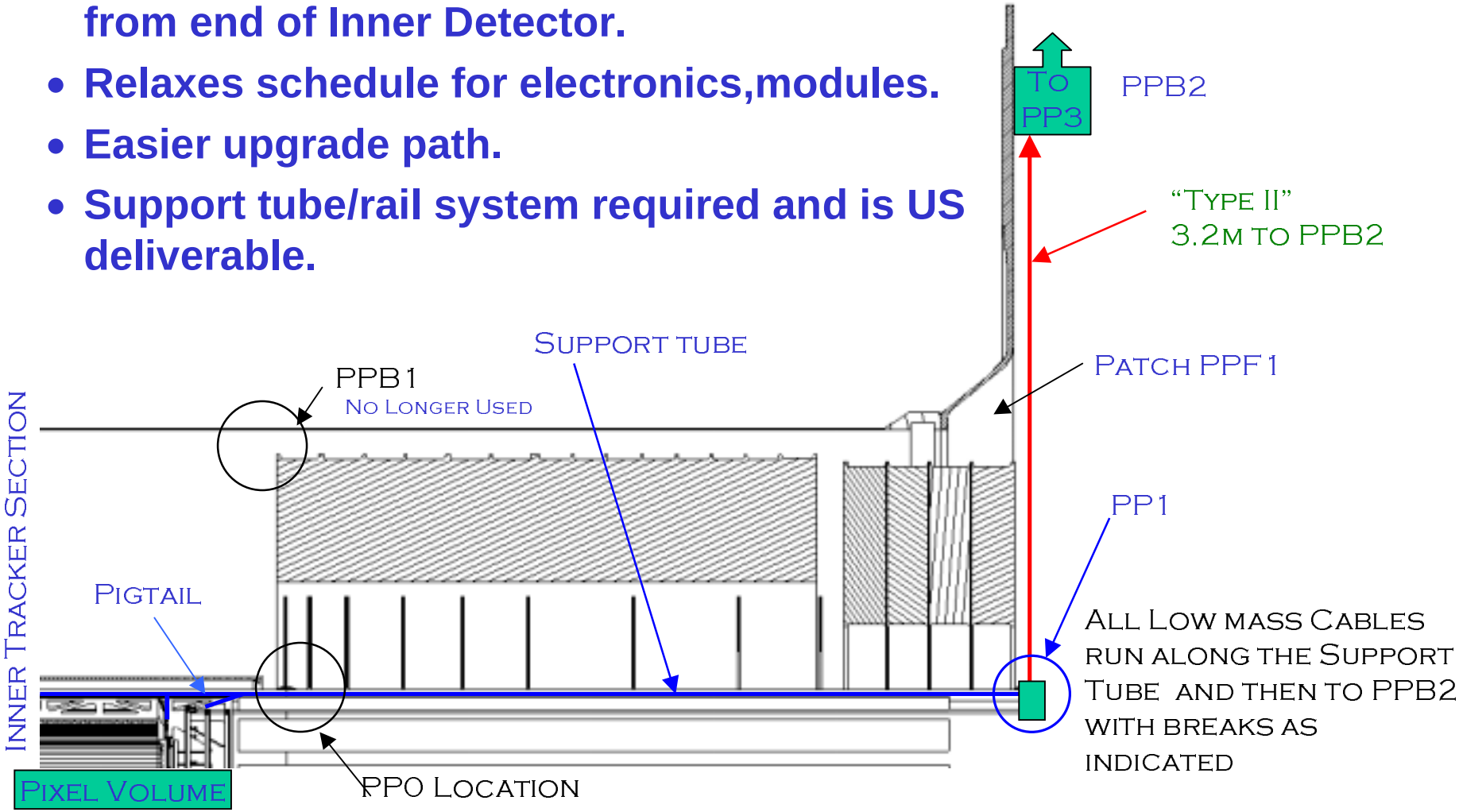
Technical Status - 1.1.1 Pixels



Pixel design modified to allow insertion from end of Inner Detector

Technical Status - 1.1.1 Pixels

- **Insertion/removal of complete Pixel System from end of Inner Detector.**
- **Relaxes schedule for electronics,modules.**
- **Easier upgrade path.**
- **Support tube/rail system required and is US deliverable.**



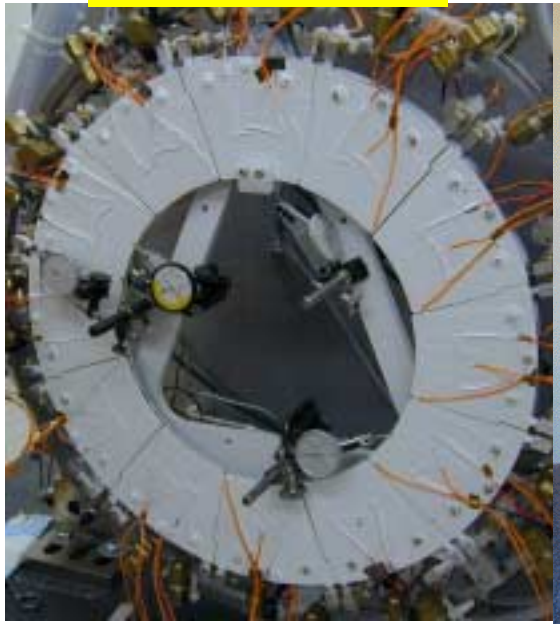
Technical Status - 1.1.1 Pixels

- Scope reduction(less active area) required to implement removable system. Pixel System gets smaller.
- A “3-hit” system is required to achieve full ATLAS performance goals. This requires three barrel layers and 2x3 disks.
- However, the performance of a “2-hit” system is judged to be adequate for the initial operation of ATLAS. This is based on simulations done already in 1997, new simulations underway.
- The US baseline is thus a “2-hit” system. This requires 2 barrel layers and 2x2 disks.
- Release of Management Contingency(currently 600K) is needed to achieve a “2-hit” system.

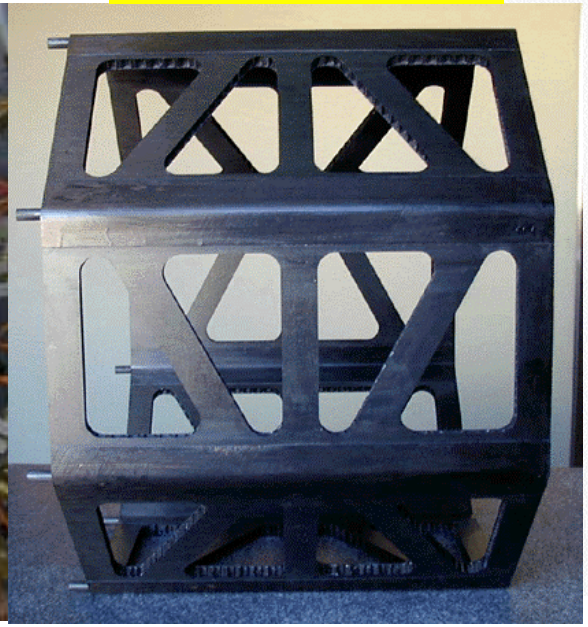
Technical Status - 1.1.1 Pixels

- **Prototypes of all US deliverables for mechanical structure either already built or to be fabricated within about next year.**
- **Design work advancing well**

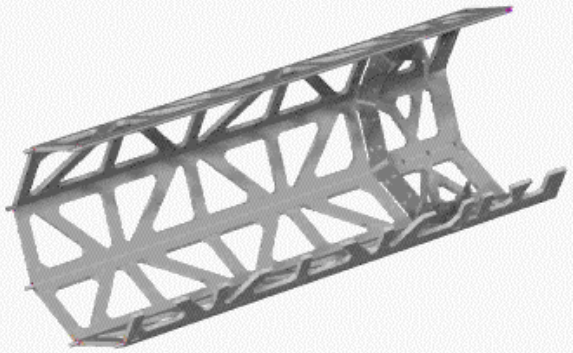
Disk Prototype



Frame Prototype

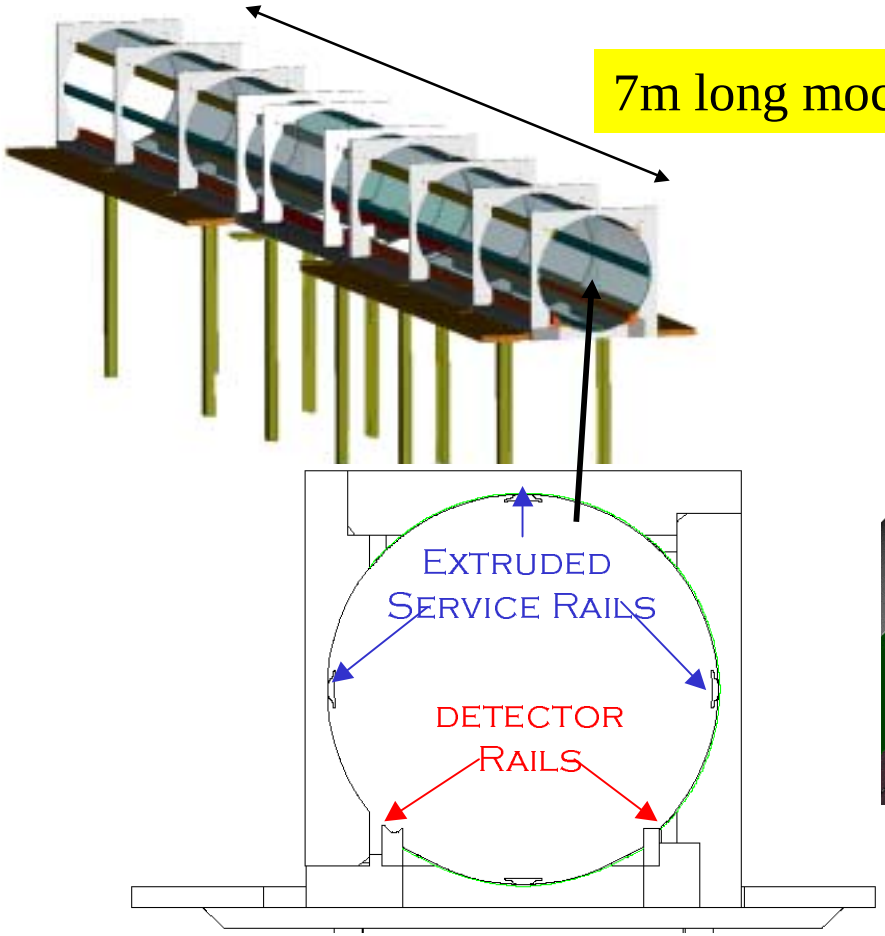


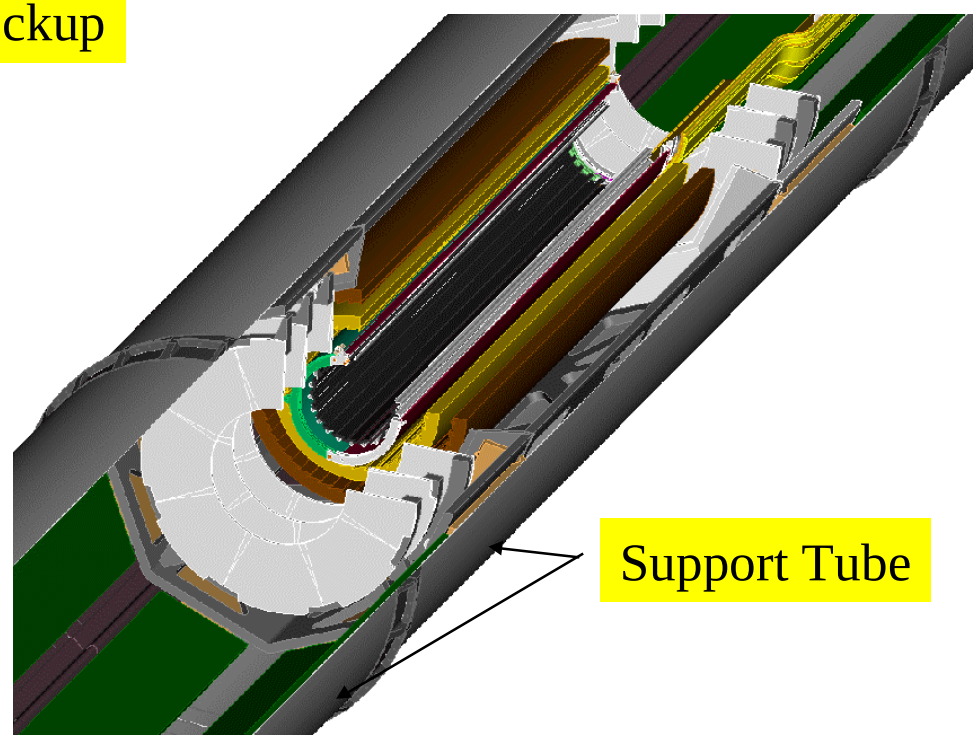
Support Frame



Technical Status - 1.1.1 Pixels

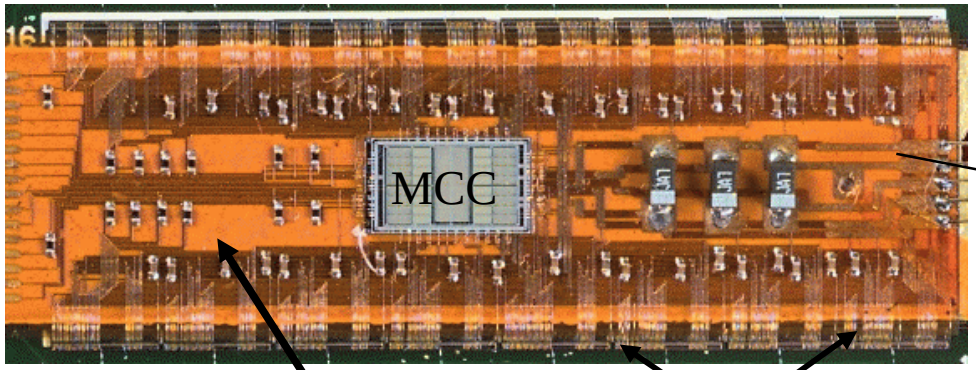
- **Full mockup of support tube under construction at LBNL to be ready for first studies next month.**
- **Design of support tube and interfaces underway.**





Technical Status - 1.1.1 Pixels

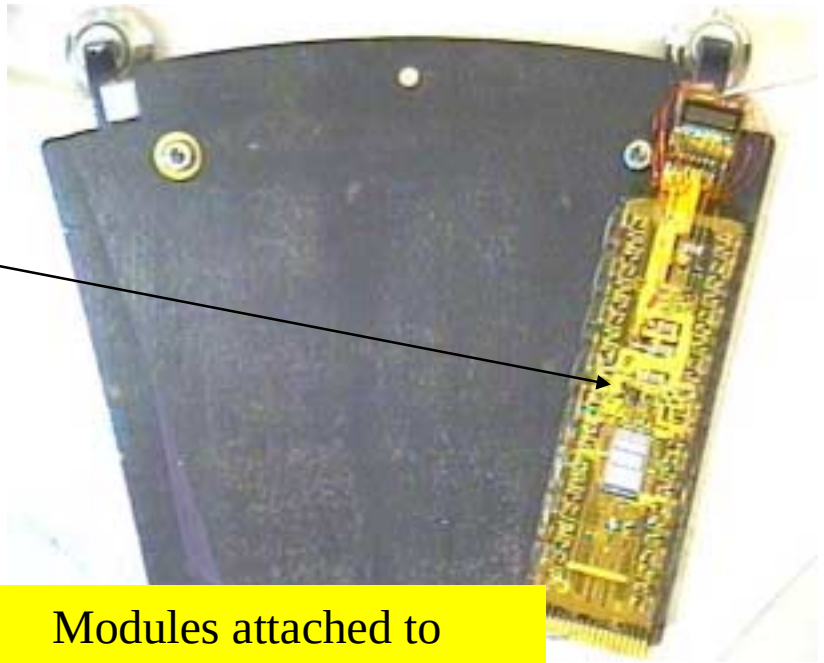
- **Module is basic building block of system.**
- **Module consists of silicon sensor, 16 front-end(FE) chips, flex hybrid with Module Control Chip(MCC) and passive components and interconnect(pigtail) to power and optical signal transmission.**
- **Connection between sensor and FE chips is made by Pb/Sn or In bump bonding.**



Kapton hybrid

Front-end chips

Kapton hybrid glued to sensor



Modules attached to mechanical/thermal structure

Technical Status - 1.1.1 Pixels

- **Sensors**
  - Production Readiness Review completed
  - Production contract between CERN and two vendors in place
  - First preproduction lots completed and under test, OK so far
- **Hybrids**
  - ATLAS Final Design Review of flex hybrids completed
  - Two generations of prototype flex hybrids made and used for module assembly, 3rd under design to be made this year
  - First prototypes of optical hybrids fabricated and under test
- **Module assembly**
  - ATLAS Final Design Review of bump bonding completed and prospective production vendors identified.
  - First generation of assembly tooling completed, dummy and active modules assembled, tested.

Technical Status - 1.1.1 Pixels

- Four rad-hard integrated circuits are required: front-end(FE), optical ICs(VDC and DORIC) and Module Control Chip(MCC).
- Development first in DMILL(Atmel) and then Honeywell began in late 1998.
- First DMILL run(FE-D1) - more than one year ago
  - Prototypes of all four chips included.
  - Major conclusion was that yield of FE chip was essentially zero.
  - Circuit elements(transistors) that were responsible for bad yield found, but root cause in production process not understood after extensive investigation by ATLAS, vendor and consultants.
- Honeywell(after merger with Allied Signal) eventually confirms large price increase - design started but dropped in Fall 2000.
- Collaboration immediate began ramp up of effort on 0.25 micron processes, IBM and TSMC(used by all other LHC expts)
- CERN completes Frame Contract with IBM.

Technical Status - 1.1.1 Pixels

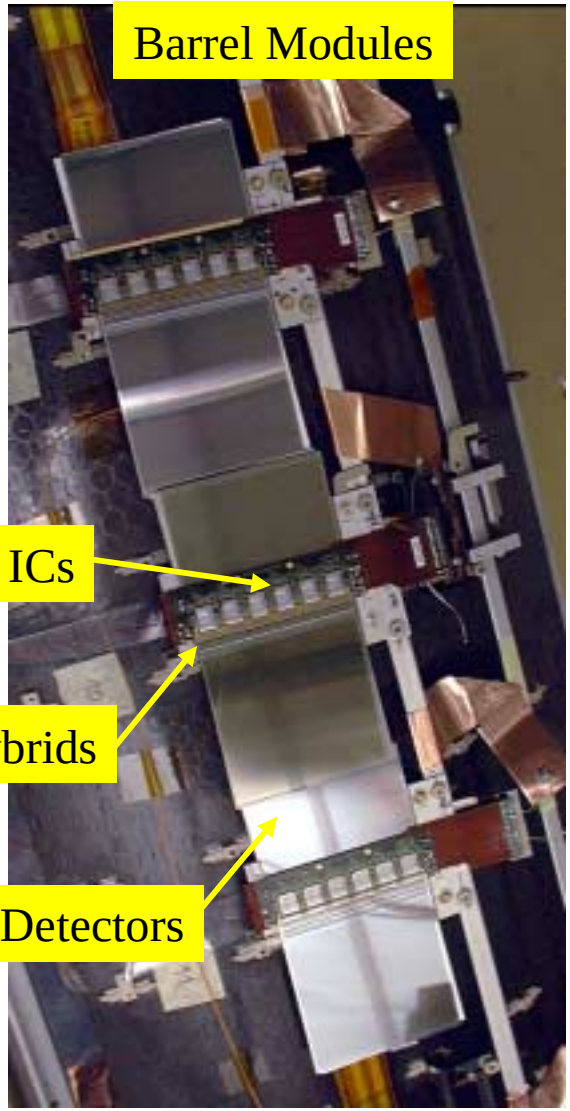
- **Second DMILL run(FE-D2) delivered in November 2000**
  - **Known design errors in FE from first run fixed successfully.**
  - **Two versions of FE chip made.**
    - **One with just fixes(yield still zero)**
    - **One with redesign to eliminate suspect circuit block but some other critical circuit blocks had to be eliminated in redesign to fit within existing 400 micron long pixel size. Yield of this chip good enough to continue testing program.**
  - **First irradiations(of FE with redesign) completed last month. Performance not acceptable so far. More irradiations to come.**
  - **Preliminary results on other chips indicate Atmel possible candidate for optical ICs. Yield of MCC prototype low(about 10%).**
  - **DMILL design work has been suspended in favor of 0.25 micron for now. Irradiations and testing are continuing. Gives information on design + irradiation methodology.**

Technical Status - 1.1.1 Pixels

- **0.25 micron processes**
  - Rapid progress on conversion of designs
  - Test chips submitted to TSMC in Jan and Mar this year. Also IBM in Feb.
  - On track for first multi-wafer engineering run(IBM) with all ICs by July
  - Taking maximum advantage of work by other experiments(CMS, BTeV, ALICE, LHCb…that all rely on this)
- **US baseline for ICs assumes**
  - 0.25 micron(IBM) for FE, TSMC backup vendor
  - DMILL(Atmel) for VDC and DORIC(small chips, total production is only a few wafers).
  - MCC is solely European cost responsibility, likely to be 0.25 micron.

Technical Status - 1.1.2 Silicon Strips

- US deliverables are front-end integrated circuits, test system for ICs and barrel modules.
- Front-end IC baseline chosen about one year ago(ABCD)
- Barrel module baseline established.



Technical Status - 1.1.2 Silicon Strips

- A Frame Contract with the ABCD vendor(Atmel) and CERN was established. It has a minimum yield guarantee.
- Five preproduction lots(8 wafer each) of ABCD3 have been delivered as of early February.
- The yield varies significantly from wafer-to-wafer and lot-to-lot. Yield is around 15%(perfect chips) and about twice this for chips with single bad channel.
- Minimum guaranteed yield from vendor is 26%. Will deliver additional wafers to meet minimum guarantee, trying to understand source of poor yield.
- A number of wafers had obvious defects(scratches, misalignments…) that can be eliminated. Even so the yield for perfect chips is below the minimum on average.

Technical Status - 1.1.2 Silicon Strips

- Atmel now suspects one of their subcontractors that provides wafers with epitaxial silicon. Is processing an additional 36 wafers(part with old vendor, part with new vendor) at their expense aimed at greater understanding of the yield. These will be delivered in the next two months.
- A design modification was made between the 2nd and 3rd preproduction lots to fix a problem seen after high-dose-rate irradiation. This will be tested in April.
- An additional problem after high-dose-rate irradiation at about 50% of lifetime dose was seen in about 20% of chips and continues to be investigated.
- Need for more irradiation testing and probing of 36 wafers is projected to delay start of electronics production from 4/01 to 7/01.

Technical Status - 1.1.2 Silicon Strips

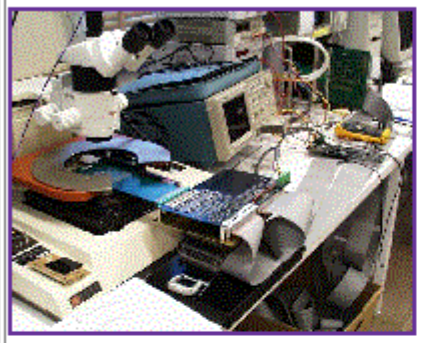
- New, high speed test system for IC wafer probing and verification designed and built by LBL is nearing completion. Needed to cope with production volume.
- Will be used at Santa Cruz, RAL and CERN for wafer probing and first systems are at all three sites.
- Detailed verification of test system in progress at all three sites.
- Plan to have two complete systems available at each site. Nominally one is spare to maintain high reliability but could be used with additional probe stations to increase probing rate, if needed(total volume assuming minimum guaranteed yield is about 1000 wafers in about one year). Have capacity to do more or go faster.

Technical Status - 1.1.2 Silicon Strips

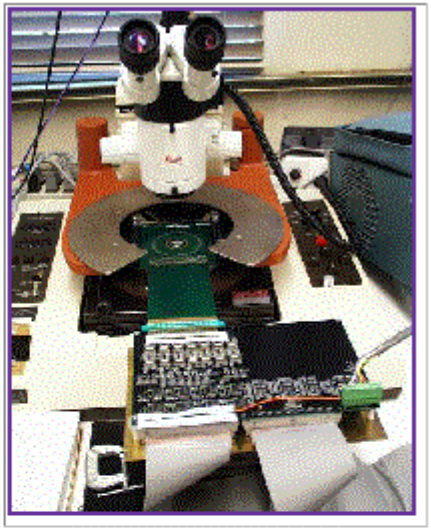
ABCD
Test System

Three boards
+ probe card

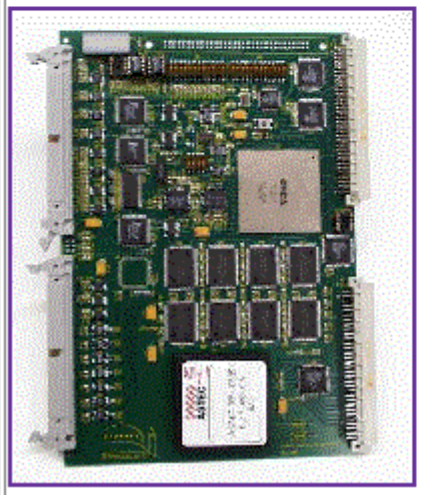
Setup



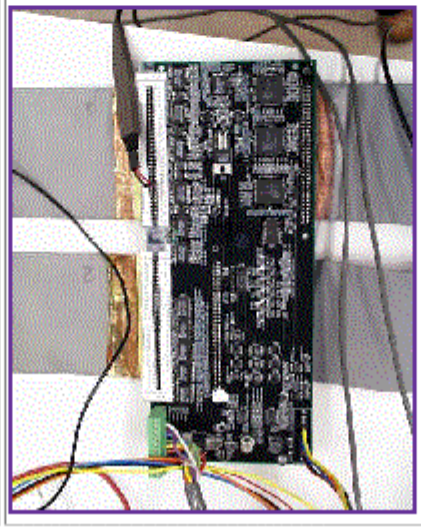
Probe station



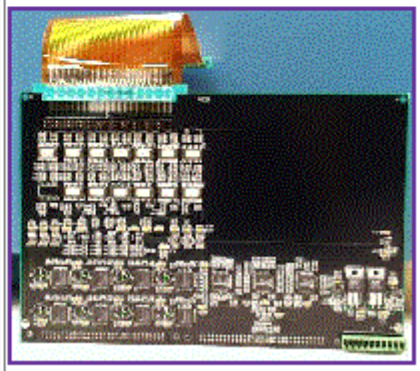
VME Board



Pindriver Board



Concard



Technical Status - 1.1.2 Silicon Strips

- Barrel module baseline design established
- Active modules constructed and tested in beam and in ongoing “system” test at CERN.
- Some production tooling remains to be fabricated
- Have removed some slack in schedule and slightly modified production sequence to cope with delays in electronics. End date for module completion same as last year.
- Lack of collaboration-wide, production planning raised last year is still a concern although progress made in last month or so.

Technical Status - 1.1.2 Silicon Strips

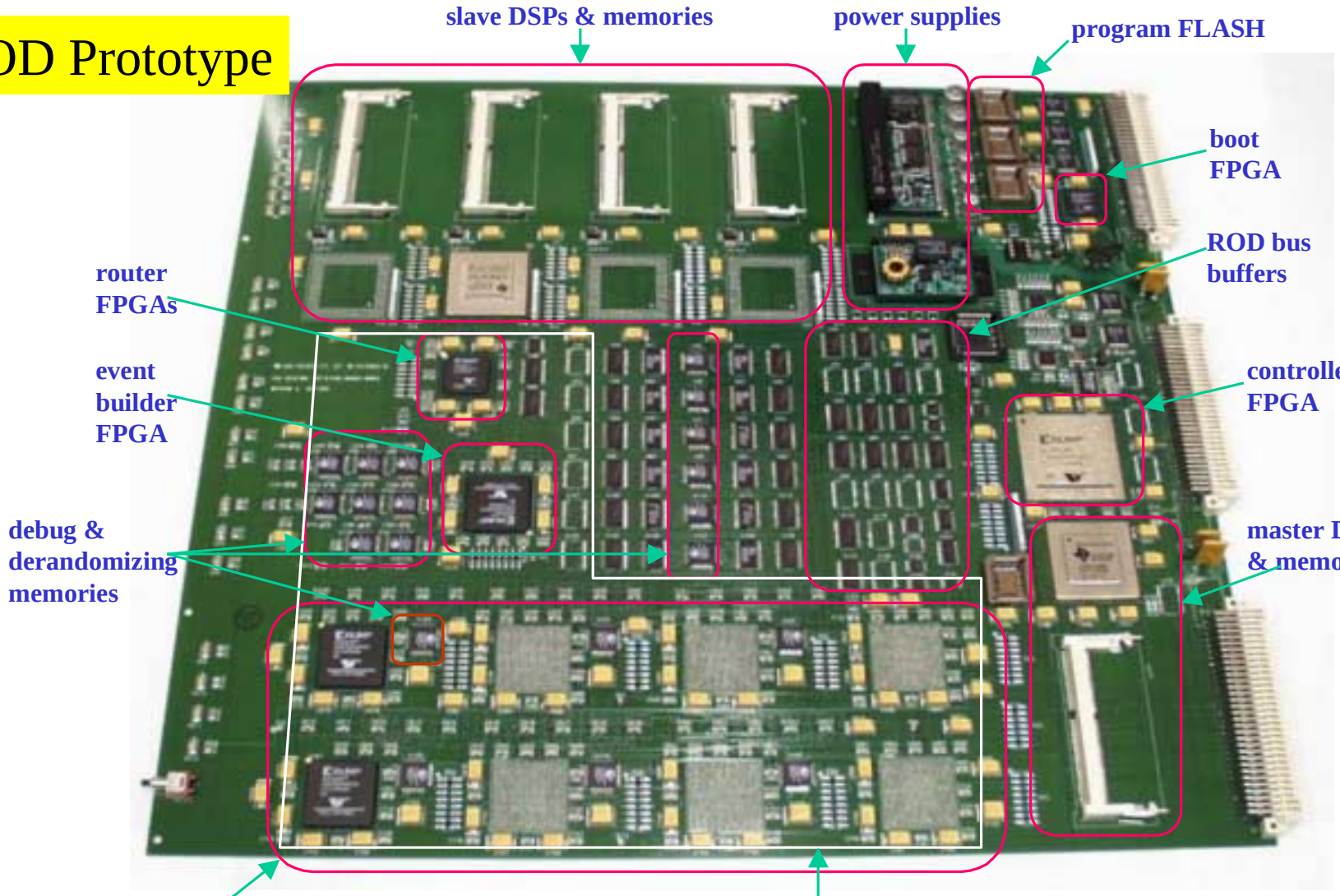
- **Basic module assembly equipment and facilities are largely complete but not yet in production status.**
- **Assembly and test procedures being debugged using dummy modules and few active modules. Staff being trained.**

Technical Status - 1.1.3 RODs

- Components of the Pixel/SCT Off Detector Electronics
  - Back Of Crate (BOC) card (optical interface), Cambridge
  - Read Out Driver (ROD), Wisconsin
  - Timing Interface Module (TIM), University College London
  - Crate Backplane, Oxford
  - SCT DAQ, Cambridge + others to join
  - Pixel DAQ, Iowa State + others to join
- First prototypes of components built and under test individually

Technical Status - 1.1.3 RODs

ROD Prototype



Technical Status - 1.1.3 RODs

- Preliminary Design Review of ROD complete
- Two, partially loaded, prototype boards received and debugging underway.
- Plan to fabricate 6 more with (hopefully) minor modifications after initial debugging complete.
- No showstoppers yet but also no demonstration all specs met according to documented test plan.
- Delays in fabrication and slower debugging + better understanding of need for system test of all components propagate directly into delay of ROD production start by about 4-5 months.
- Integrated test of BOC-ROD-TIM planned to start next month at Cambridge.

ETC01 vs ETC00

Silicon

WBS Level 3

Access Comparison (Silicon Level 3)
(Project FY00K$s)

	ETC 00			ETC 01			
WBS	ETC Access (in FY00 $s)	Actuals Thru FY99	TPC Access Plus Actuals	ETC 01 New Access (in FY00 $s)	Actuals Thru FY00	TPC 01 New Access Plus Actuals	Delta
111 Pixel System	8,256	1,005	9,261	6,382	1,910	8,291	970
112 Silicon Strip	4,996	911	5,907	4,612	1,414	6,026	(119)
113 Read-out Drivers	2,186	630	2,816	1,829	1,019	2,847	(31)
Total	15,439	2,546	17,985	12,822	4,343	17,165	820

Explanation of ETC01 Cost Changes

- **Pixels(1.1.1)**
  - TPC below original estimate.
  - Why? 0.25 micron ICs, scope cut, increased contingency + savings during development phase.
- **Silicon Strips(1.1.2)**
  - Increases in engineering + materials for high-speed IC tester(US responsibility) needed to cope with potential for low yield.
  - Decreases in IC costs(fixed in Euros, $ stronger than last year).
- **ReadOut Drivers(1.1.3)**
  - No change in estimate except for inflation
  - No calls on contingency yet

ETC01 Funding Profile

Silicon

WBS Level 3 Funding Profile

Silicon ETC 01 Access Profile (Project K$s)

WBS	FY01	FY02	FY03	FY04	FY05	FY06	Total
111 Pixel System	1,933	1,927	2,084	408	30	0	6,382
112 Silicon Strip	3,616	731	264	0	0	0	4,612
113 Read-out Drivers	1,081	604	52	45	46	0	1,829
1.1 Total (FY00$s)	6,630	3,263	2,401	454	76	0	12,822
1.1 Total (AY$s)	6,795	3,431	2,595	504	87	0	13,413

ETC01 Milestone Changes

Level 2 Milestones

Subsystem	Schedule Designator	Description	ETC Schedule Date	ETC 01 Schedule Date
Silicon	Sil L2/1	Start Full Silicon Strip Elec Prod	23-Apr-01	6-Jul-01
	Sil L2/2	Start Full Strip Module Production	26-Nov-01	7-Jan-02
	Sil L2/3	ROD Design Complete	14-Jun-01	1-Oct-01
	Sil L2/4	Compl Shipment of Silicon Strip Modules Prod	13-Oct-03	13-Oct-03
	Sil L2/5	ROD Production/Testing Complete	13-Mar-03	24-Jun-03
	Sil L2/6	Pixels 1st IBM Prototype Submitted	N/A	26-Jul-01
	Sil L2/7	Pixels Start IBM Production	N/A	13-Mar-03
	Sil L2/8	Pixels Start IBM Outer Bare Module Production	N/A	22-Oct-03
	Sil L2/9	Pixels 'Disk System at CERN'	N/A	13-Oct-04

Level 4 Milestones (Baseline Scope)

WBS	Schedule Designator	U.S. ATLAS Responsibility Completion Description	ETC Planned Completion Date	ETC 01 Planned Completion Date	ATLAS Required Date	ETC 01 Planned Float (Months)
Silicon						
1.1.2	Sil L4/1	Compl Shipping of Silicon Strip Prod Modules	10/03	10/03	4/03	**-6**
1.1.3	Sil L4/2	RODs 45% Production Compl	4/02	9/02	6/03	9
1.1.1	Sil L4/3	Pixels 'Disk System at CERN'	N/A	10/04	12/04	2

Explanation of ETC01 Milestone Changes

- **Pixels(1.1.1) - baseline established.**
- **Silicon Strips(1.1.2)**
  - **Delay in rad-hard qualification of front-end ICs by about 3 months**
  - **Full module construction start delayed, but can start without ICs for few months + have removed some slack => end date kept same.**
  - **Conflict with (old) ATLAS need date remains. Impact of new ATLAS schedule to be assessed.**
- **ReadOut Drivers(1.1.3)**
  - **Delay in fabrication and debugging of prototype.**
  - **Better understanding of full prototype system test needs(not just ROD)**
  - **Total delay 4-5 months in production**

Conclusions

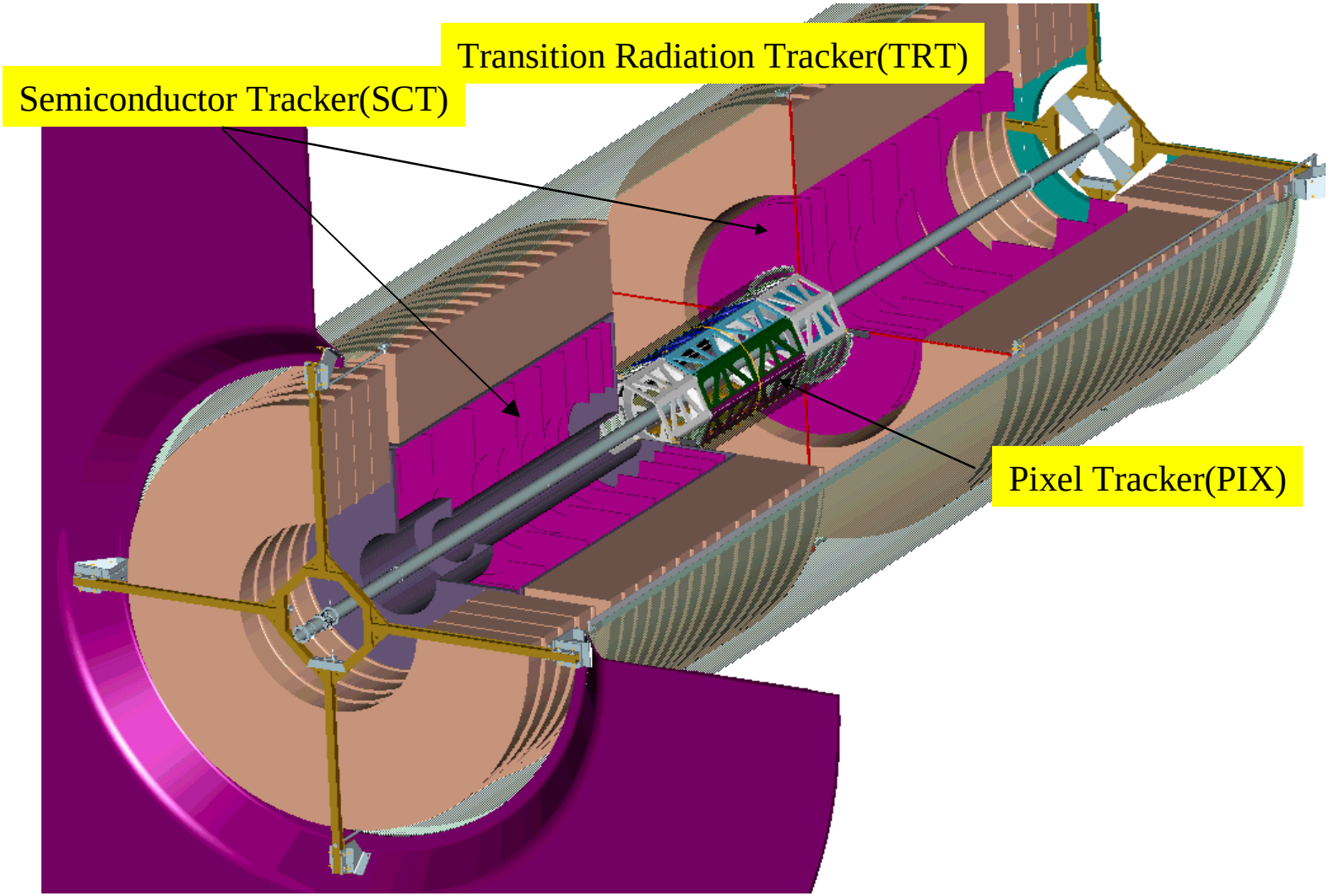
- **Pixels(1.1.1)**
  - **Production baseline established**
- **Silicon Strips(1.1.2)**
  - **TPC about same as last year**
  - **Few month delay in start of IC production projected**
  - **Completion date for modules same as last year**
- **ReadOut Drivers(1.1.3)**
  - **TPC same as last year**
  - **Delays in prototypes delay production**
  - **But significant float remains in schedule**

WBS 1.1.1 Pixel Overview and WBS 1.1.1.1 Pixel Mechanics

M. G. D. Gilchriese

Lawrence Berkeley Laboratory

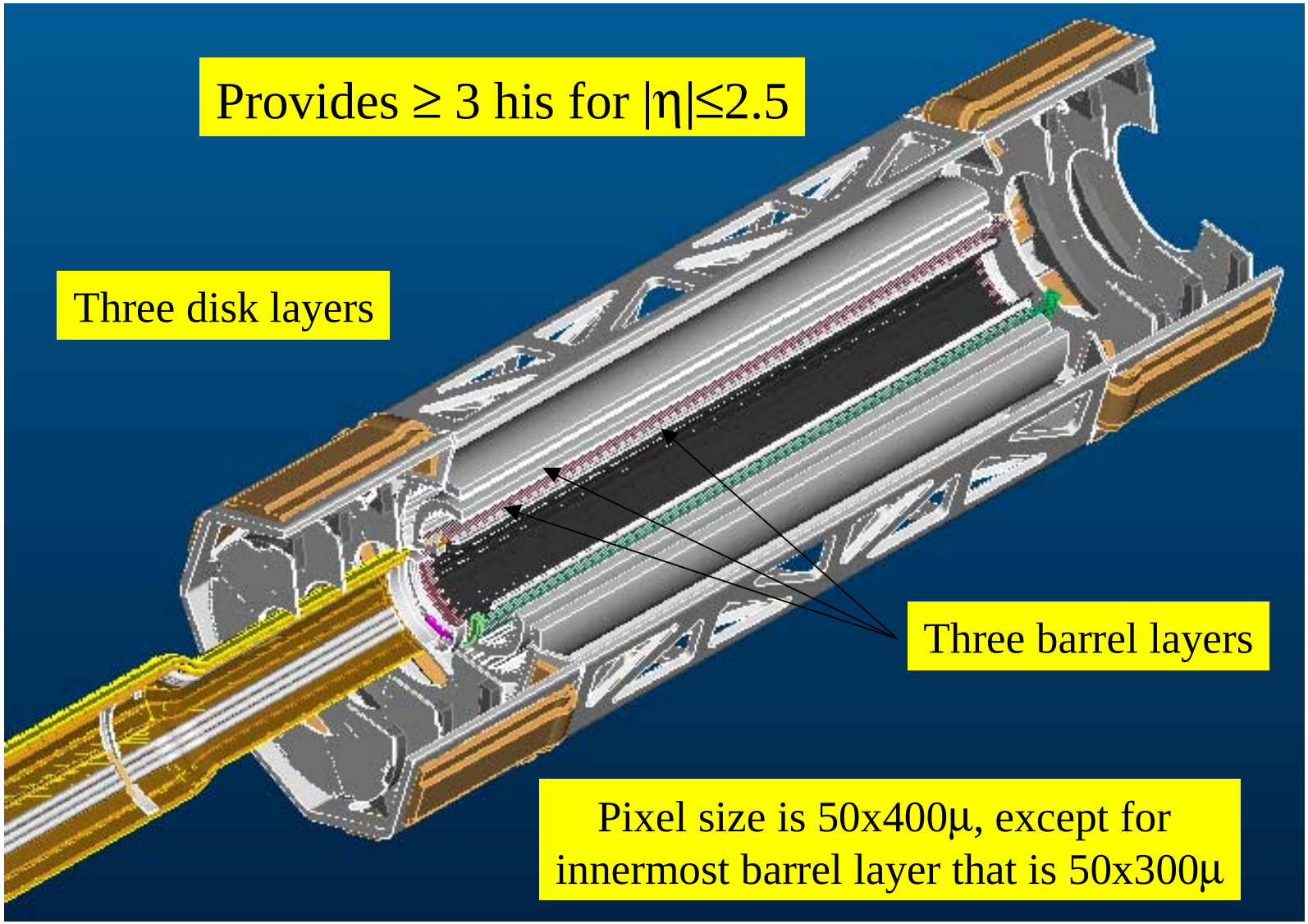
ATLAS Pixel System



Overview

- **Pixel system in ATLAS**
  - **Provides critical pattern recognition**
  - **Determines ability to find secondary vertices eg. for identifying b-quarks**
  - **Part of Level 2 trigger**
- **Countries involved are Canada, Czech Republic, France, Germany, Italy and US.**
- **The US is roughly 20% of the project.**

ATLAS Pixel Baseline



US Pixel Baseline Scope

- The US baseline scope corresponds to a 2-hit system.
- The innermost(B-layer) and outermost barrel layers are retained.
- 2x2 disks are retained.
- This corresponds to the current concept for the ATLAS initial detector
- Upgrade path to full 3-hit system

Pixel Parameters

Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer	50.5	22	286	4576	1.76E+07	0.28	-20
Layer 1	88.5	38	494	7904	3.04E+07	0.48	-20
Layer 2	122.5	52	676	10816	4.15E+07	0.65	-20
Subtotal(3 hits)		112	1456	23296	8.95E+07	1.41	
Subtotal(2 hits)		74	962	15392	5.91E+07	0.93	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
495	88.1	148.9	48	768	2.21E+06	0.04	8
580	88.1	148.9	48	768	2.21E+06	0.04	8
650	88.1	148.9	48	768	2.21E+06	0.04	8
Subtotal(Both Sides - 3 hits)			288	4608	1.33E+07	0.27	48
Subtotal(Both Sides - 2 hits)			192	3072	8.85E+06	0.18	32
GRAND TOTALS(3 hits)			1744	27904	1.0E+08	1.68	
GRAND TOTALS(2 hits)			1154	18464	6.8E+07	1.11	

US Institutions and Management

	ALB	LBL	UNM	UOK	OSU
1.1.1 Pixels(Gilchriese)					
1.1.1.1 Mechanics(Gilchriese, Anderssen)		x	x		
1.1.1.2 Sensors(Seidel, Hoeferkamp)			x	x	
1.1.1.3 Electronics(Einsweiler, Denes)		x			x
1.1.1.4 Hybrids(Skubic, Boyd, Gan)	x	x		x	x
1.1.1.5 Modules(Garcia-Sciveres, Goozen)		x	x	x	x
1.1.1.6 Test Support(Gilchriese)		x			

(Physicist, Engineer)

SUNY Albany, LBL, New Mexico, Oklahoma, Ohio State

In addition, off-detector electronics(ReadOut Drivers for both pixels and SCT) are separate project(Wisconsin, Iowa State and LBL).

2-Hit System - US Deliverables[1]

- **Mechanics(1.1.1.1)**
  - Support tube and plugs at end of support tube
  - Overall pixel support structure(frame)
  - Disks
  - Coolant pipes(shared with Europe)
  - Power and other cables(shared with Europe)
  - Tooling for final assembly of system(shared with Europe)
- **Sensors(1.1.1.2)**
  - About 20% of production procurement and testing
- **Electronics(1.1.1.3)**
  - About 20% production procurement, 50% of testing of front-end ICs
  - About 50% production procurement and testing of optical ICs
  - Common test systems for all collaboration for front-end ICs, modules
- **Hybrids(1.1.1.4)**
  - All flex hybrids
  - Optical components and hybrids for disk region
- **Modules(1.1.1.5)**
  - Thinning, dicing of FE and die sort
  - Assemble and test about 25% of modules
- **Test Support(1.1.1.6)**
  - About 20% of support for system tests and beam tests at CERN

[1]Assumes release of 600K of management contingency

US Baseline Cost

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1	Pixels	0	0	0	0	0	1932	1989	2023	408	30	6382
1.1.1.1	Mechanics and Final Assembly	0	0	0	0	0	923	917	1032	177	19	3067
1.1.1.1.1	Design	0	0	0	0	0	571	447	262	83	12	1375
1.1.1.1.2	Development and Prototypes	0	0	0	0	0	152	105	0	0	0	257
1.1.1.1.3	Production	0	0	0	0	0	199	365	770	94	7	1435
1.1.1.2	Sensors	0	0	0	0	0	97	35	0	0	0	133
1.1.1.2.1	Design/Engineering	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.3	Production	0	0	0	0	0	62	0	0	0	0	62
1.1.1.3	Electronics	0	0	0	0	0	615	621	354	26	0	1616
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	446	161	0	0	989
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	234	133	0	0	0	367
1.1.1.3.3	Production	0	0	0	0	0	0	42	193	26	0	261
1.1.1.4	Flex Hybrids/Optical Hybrids	0	0	0	0	0	110	138	273	4	0	525
1.1.1.4.1	Design/Engineering	0	0	0	0	0	18	50	9	0	0	77
1.1.1.4.2	Development and Prototypes	0	0	0	0	0	92	62	0	0	0	154
1.1.1.4.3	Production	0	0	0	0	0	0	26	264	4	0	294
1.1.1.5	Module Assembly/Test	0	0	0	0	0	159	244	330	190	0	924
1.1.1.5.1	Design/Engineering	0	0	0	0	0	79	47	0	0	0	126
1.1.1.5.2	Development and Prototypes	0	0	0	0	0	80	135	46	0	0	261
1.1.1.5.3	Production	0	0	0	0	0	0	61	285	190	0	536
1.1.1.6	Beam/System Test Support	0	0	0	0	0	28	33	33	11	11	117
1.1.1.6.1	Test Beam Support	0	0	0	0	0	11	17	17	0	0	45
1.1.1.6.2	System test support	0	0	0	0	0	17	17	17	11	11	72

Management Contingency

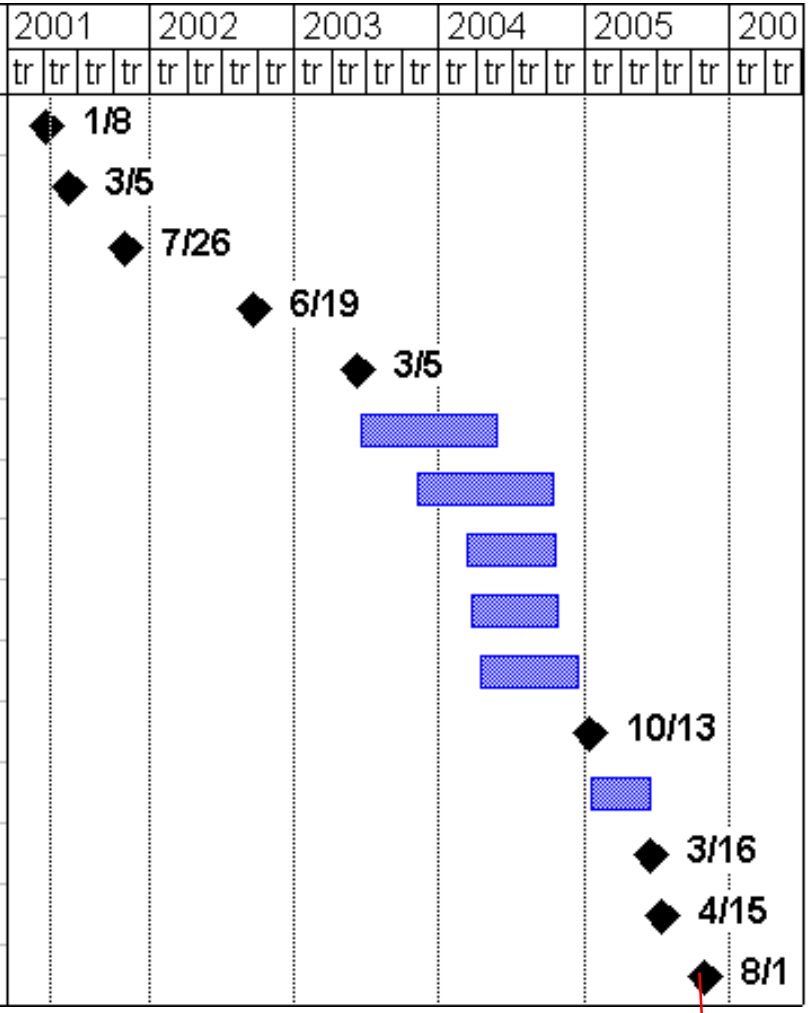
- Management contingency for pixels in two parts.
- High priority(600K)to complete 2-hit system. See below.

WBS	Description	Scope-$s (FY00 $s)	Decision Date	FY01	FY02	FY03	FY04
1.1.1.2.3.1.2	Pixels Sensor	92,873	9/30/01		92,873		
1.1.1.2.3.1.3	Pixel Sensor testing (FY02 on)	78,000	7/1/01		39,000	39,000	
1.1.1.4.3.1.1	Bare Flex Hybrid Production	144,075	7/1/02		144,075		
1.1.1.4.3.1.2	Flex Components & Assembly	67,487	7/1/02			67,487	
1.1.1.3.3.1.1.2	FE IBM Production	60,549	3/1/03			60,549	
1.1.1.4.3.3.2	Optical Hybrids	32,621	3/1/03			32,621	
1.1.1.4.3.3.1	Optical Package & Component	13,538	3/1/03			13,538	
1.1.1.3.3.2.1	Optoelectronics Production	26,460	3/1/03			26,460	
1.1.1.3.3.1.2	B-Layer Production	28,345	11/1/03			28,345	
1.1.1.5.3.3	FE IC die sort	58,080	6/1/03			54,000	4,080

- Lower priority - to complete 3 hit system.
- Note all structural mechanics in baseline, so if more. money found(even from outside US) chance to complete 3-hit system.

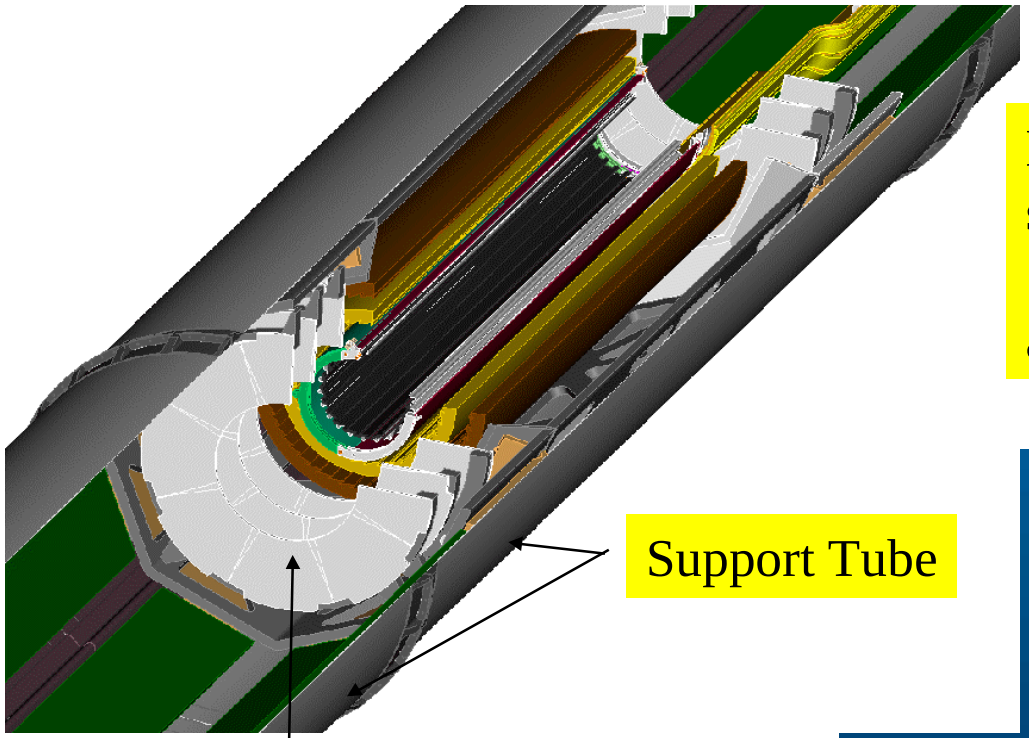
US Baseline - Critical Path

ID	Task Name
1	Submit TSMC digital test chip
2	Submit TSMC analog test chip
3	1st IBM prototype submitted(FE-I1)
4	2nd IBM prototype submitted(FE-I2)
5	IBM FE PRR
6	Outer FE IBM Production
7	Test outer FE IBM wafers
8	IBM outer module assembly/test(US)
9	Module attach to disk sectors
10	Disk Assembly/Test
11	Disk System at CERN
12	Outer System Assembly/Test at CERN
13	Outer System Ready for Installation
14	ATLAS need date for pixel system install
15	ATLAS first beam



US Baseline schedule established before recent change to LHC/ATLAS schedule. More float?

Mechanics(1.1.1.1)



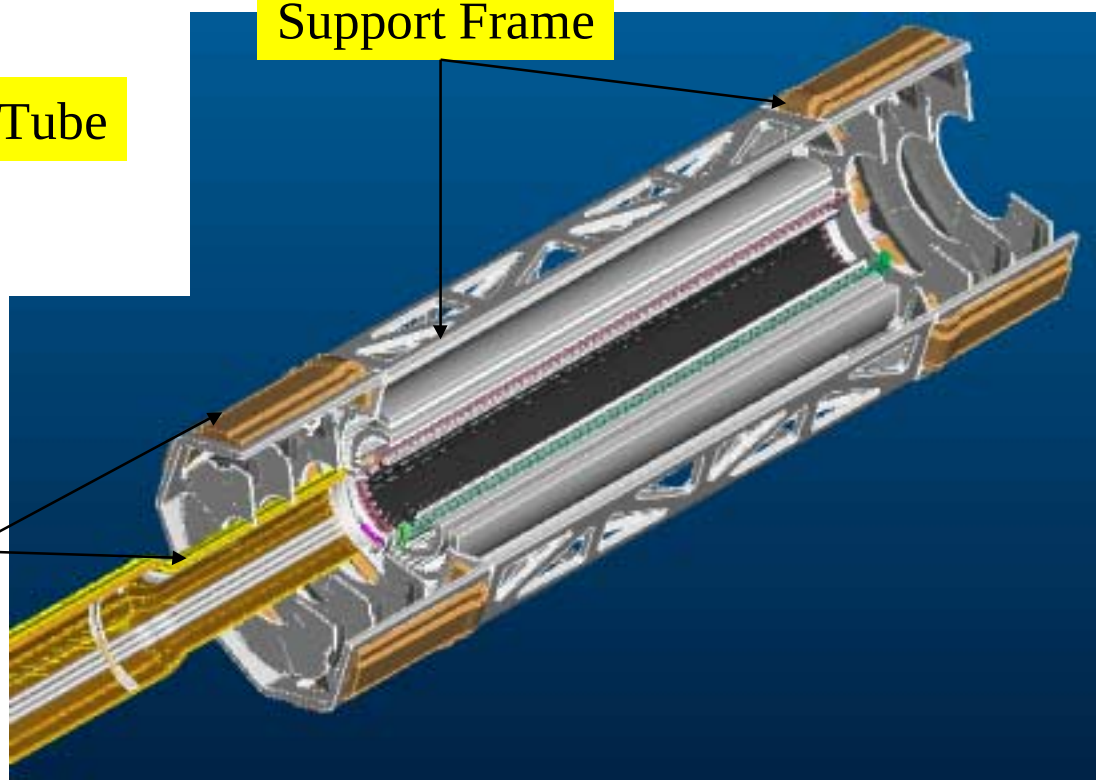
Barrel supporting./cooling structures are European responsibilities. Services and final assembly/installation are shared with US.

Support Frame

Support Tube

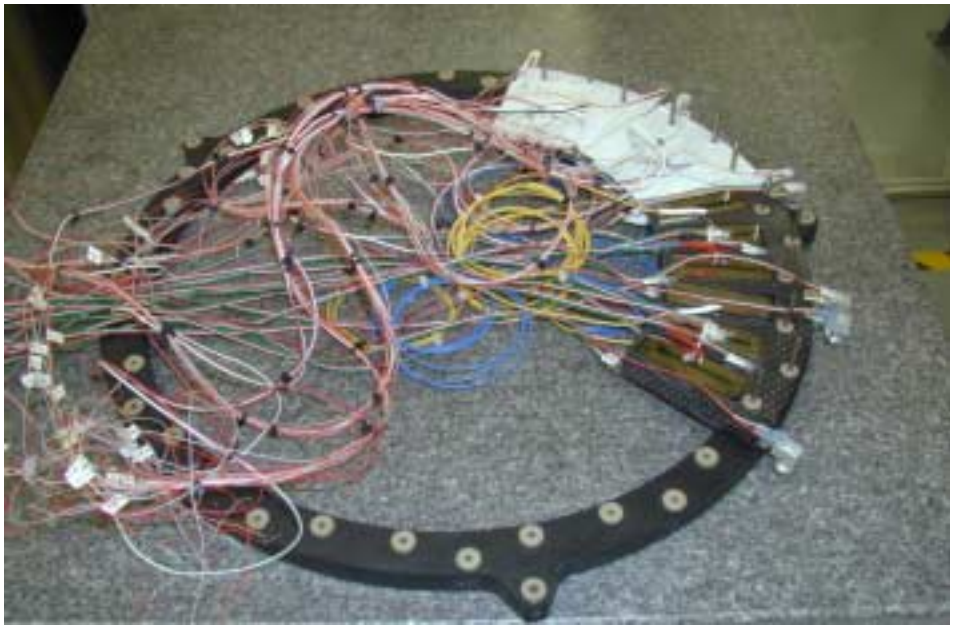
Disks

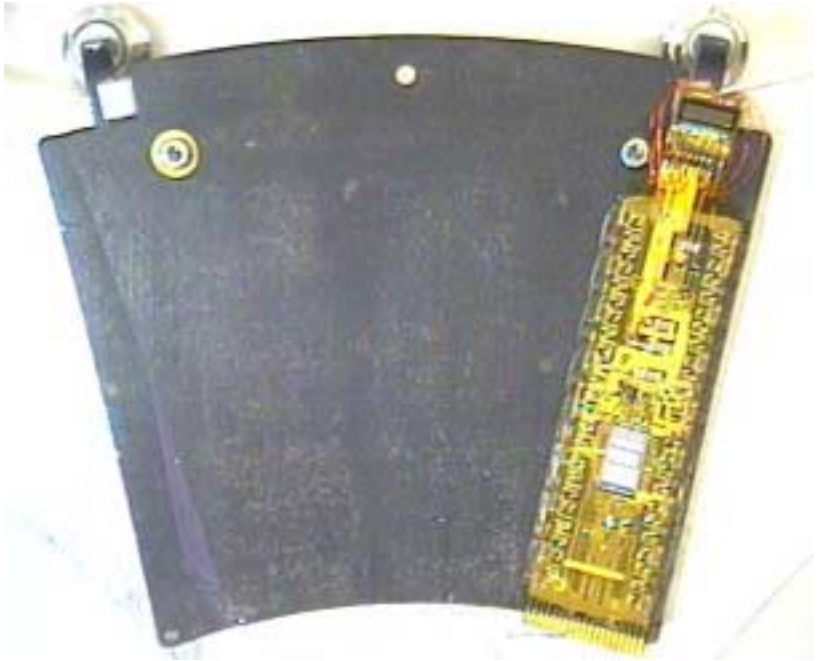
Services



Disk Structures

- Disks are composed of sectors(8 per disk) that provide mechanical support and cooling and support rings.
- Six modules are mounted on each sector.
- Sectors are attached to disk support ring at outer radius.
- Disk support ring is mounted in support frame.





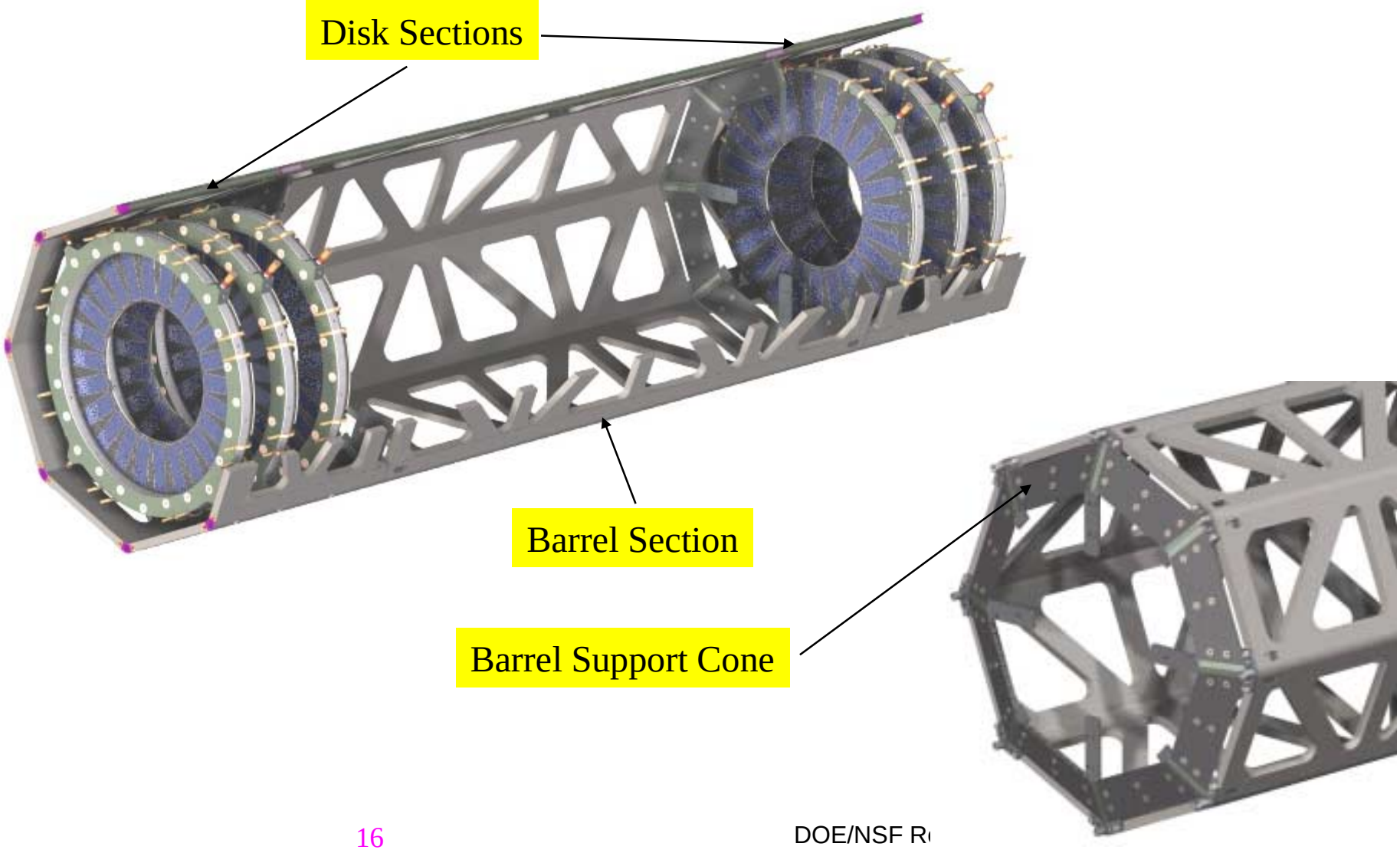
Baseline Sector Concept

- Combined structural support with cooling.
- Carbon-carbon faceplates. Front and back faceplates offset in phi to provide full coverage(minimal gaps).
- Aluminum coolant tube between faceplates.
- Three precision support points to disk ring.
- Modules mounted on both sides.

Disks - Status

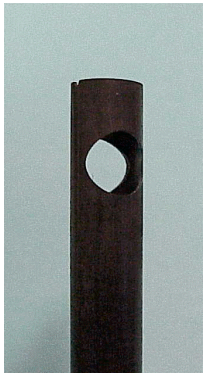
- Two complete mechanical/thermal disks have been made and tested.
- In addition, about one dozen prototypes of sectors along baseline design have been made and tested.
- Baseline design of sectors is under configuration control.
- Final design of support rings is almost complete, but not yet under configuration control. Need to verify mount concept to frame - see next pages.
- Requirements and interface documents for sectors exist and Final Design Review completed.
- Production Readiness Review for sectors(and corresponding barrel element - staves) scheduled for June 19.
- On track to make a preproduction disk(8 sectors + 1 ring) starting in July.
- On or ahead of schedule, costs OK so far but still very early - production ahead.

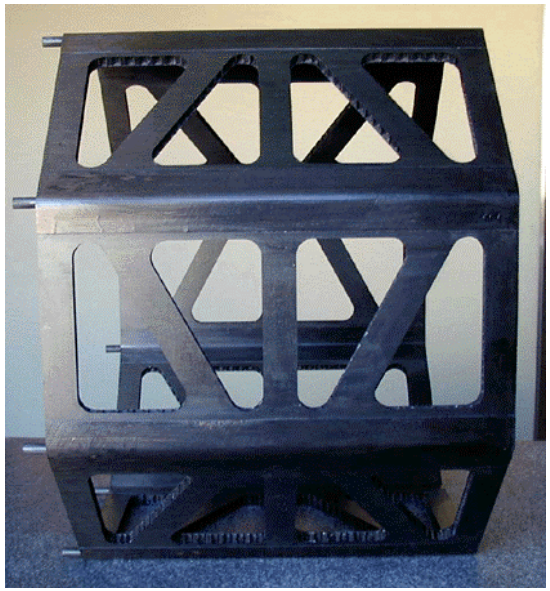
Support Frame



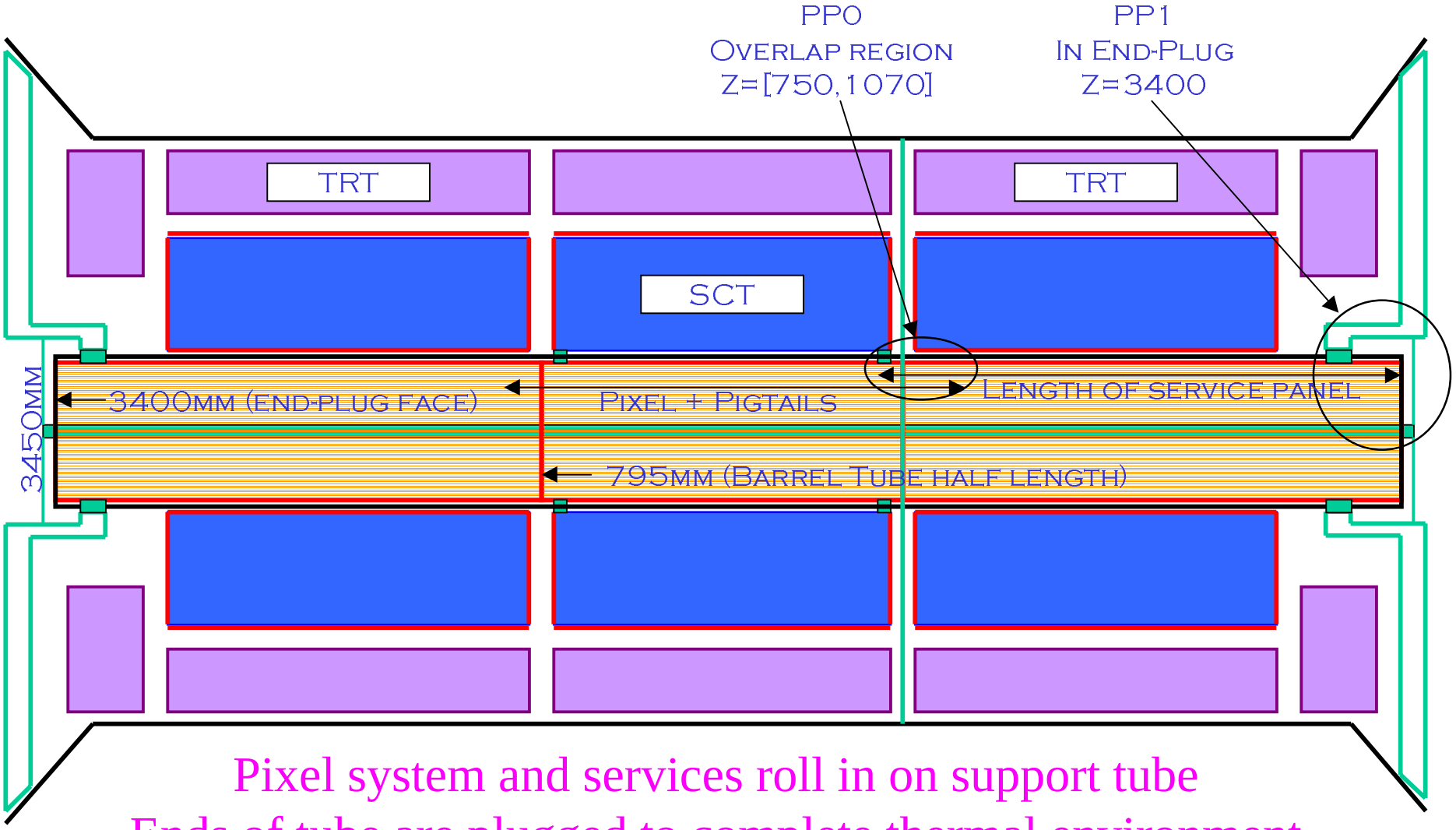
Support Frame Status

- Full-size disk portion of frame made and tested. Looks good.
- Prototype endcone under construction. Tests complete by July.
- Prototype disk ring mounts made, preliminary tests complete.
- Final location of disks made by drilling in frame. Fixture to do this under fabrication, prototype ring modified to accept prototype mounts, procedure, including insertion, will be tested by Sept.
- Interfaces(to barrel region, services and support tube) now design drivers.





Support Tube

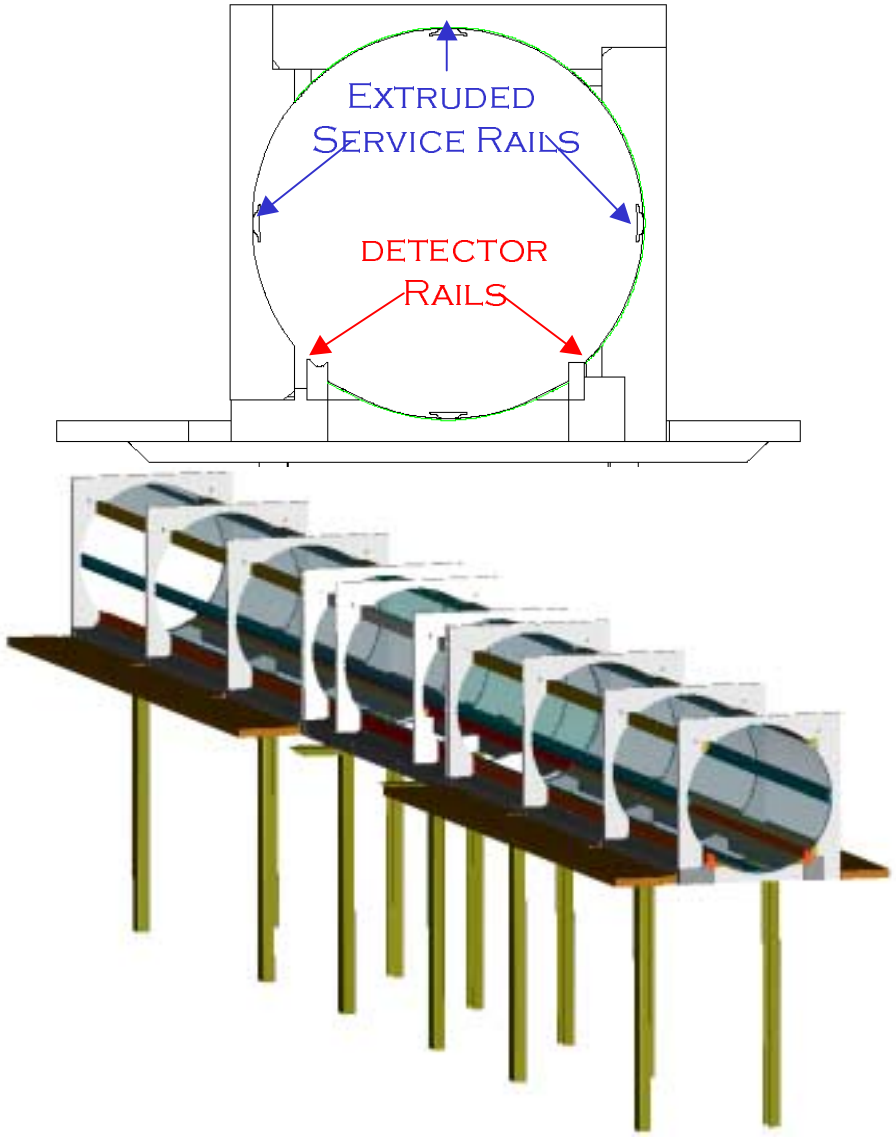


Pixel system and services roll in on support tube

Ends of tube are plugged to complete thermal environment

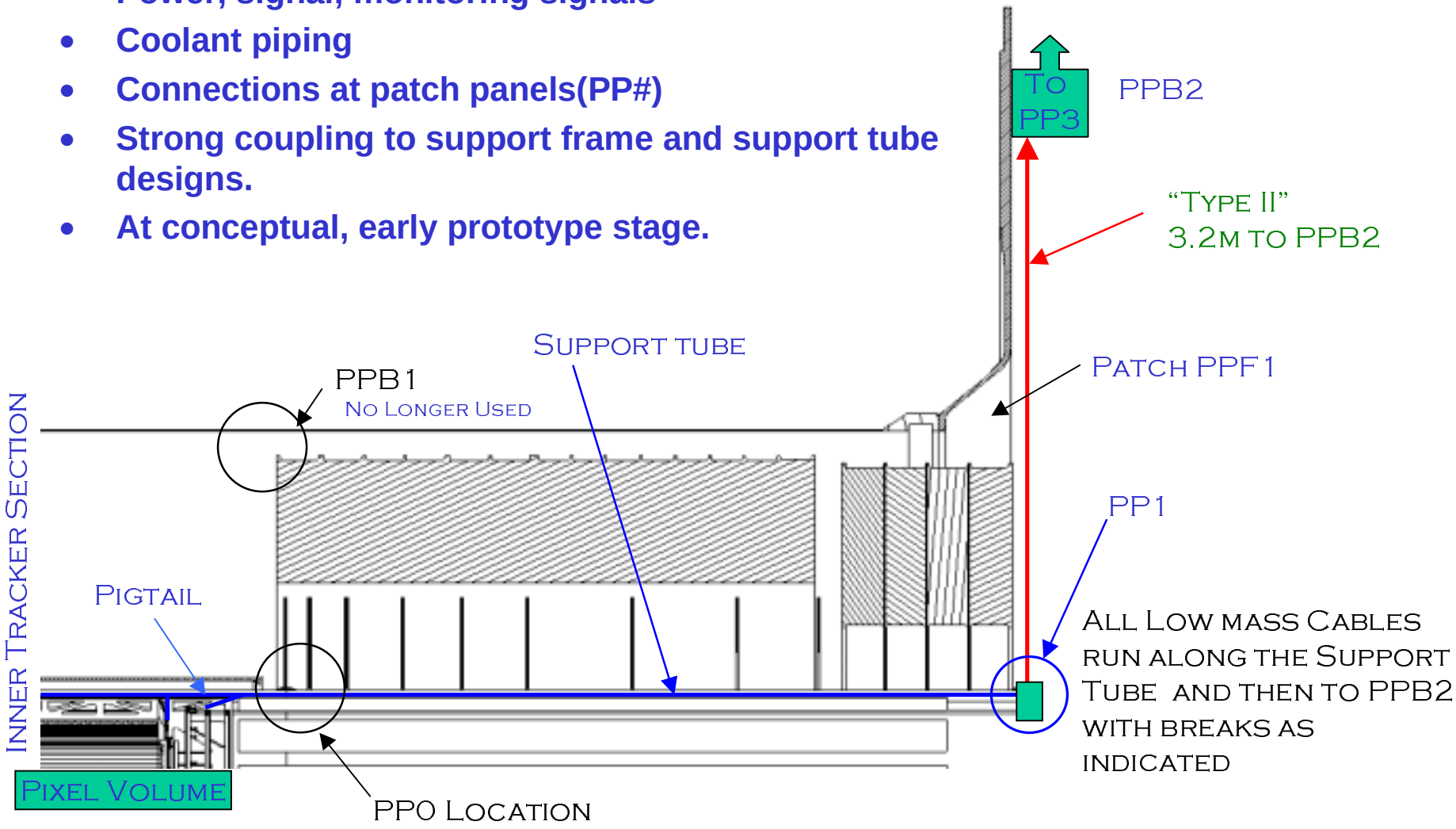
Support Tube Status

- Conceptual design phase
- Full-scale mockup under construction at LBL
- Test insertion and services support schemes
- Will fabricate prototype of center section by next year.

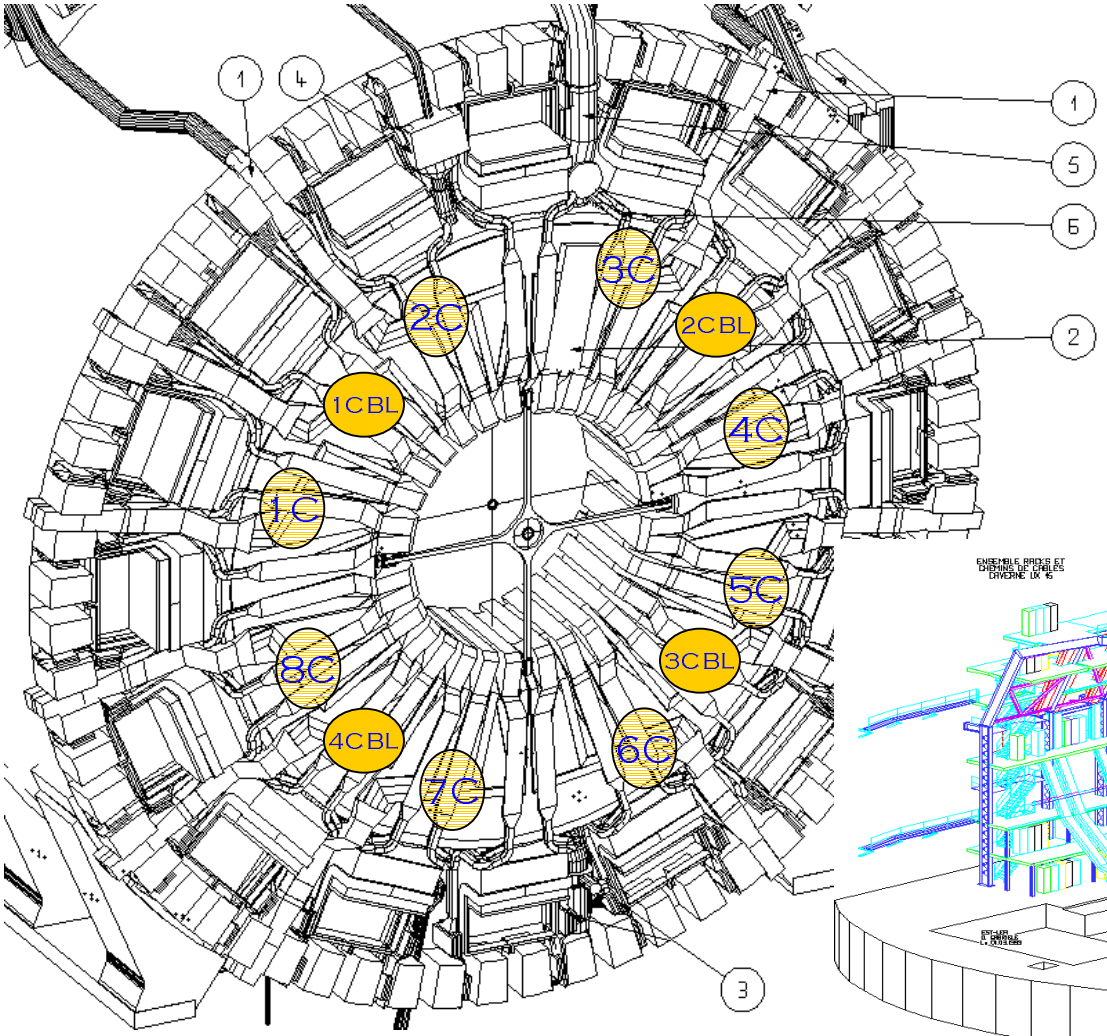


Services - Inner Detector Region

- Power, signal, monitoring signals
- Coolant piping
- Connections at patch panels(PP#)
- Strong coupling to support frame and support tube designs.
- At conceptual, early prototype stage.

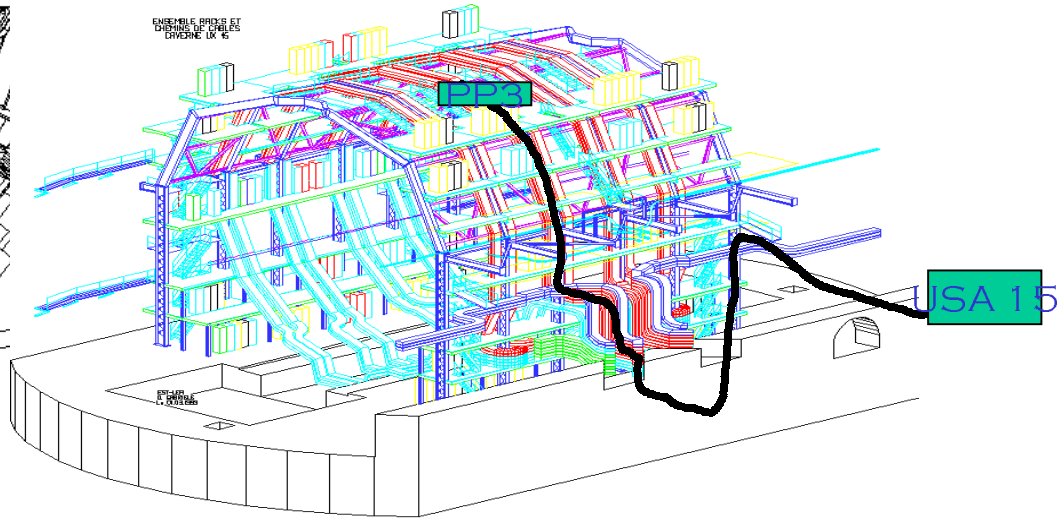


Services - Outside Inner Detector



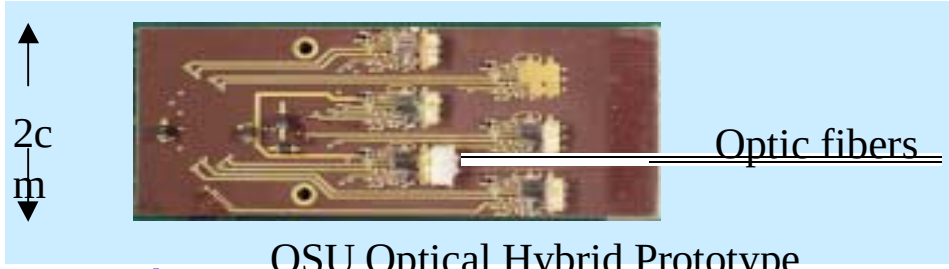
PP2 region

- PP2
- PP2 -> PP3
- PP3 -> underground caverns
- Also conceptual, early prototype phase.

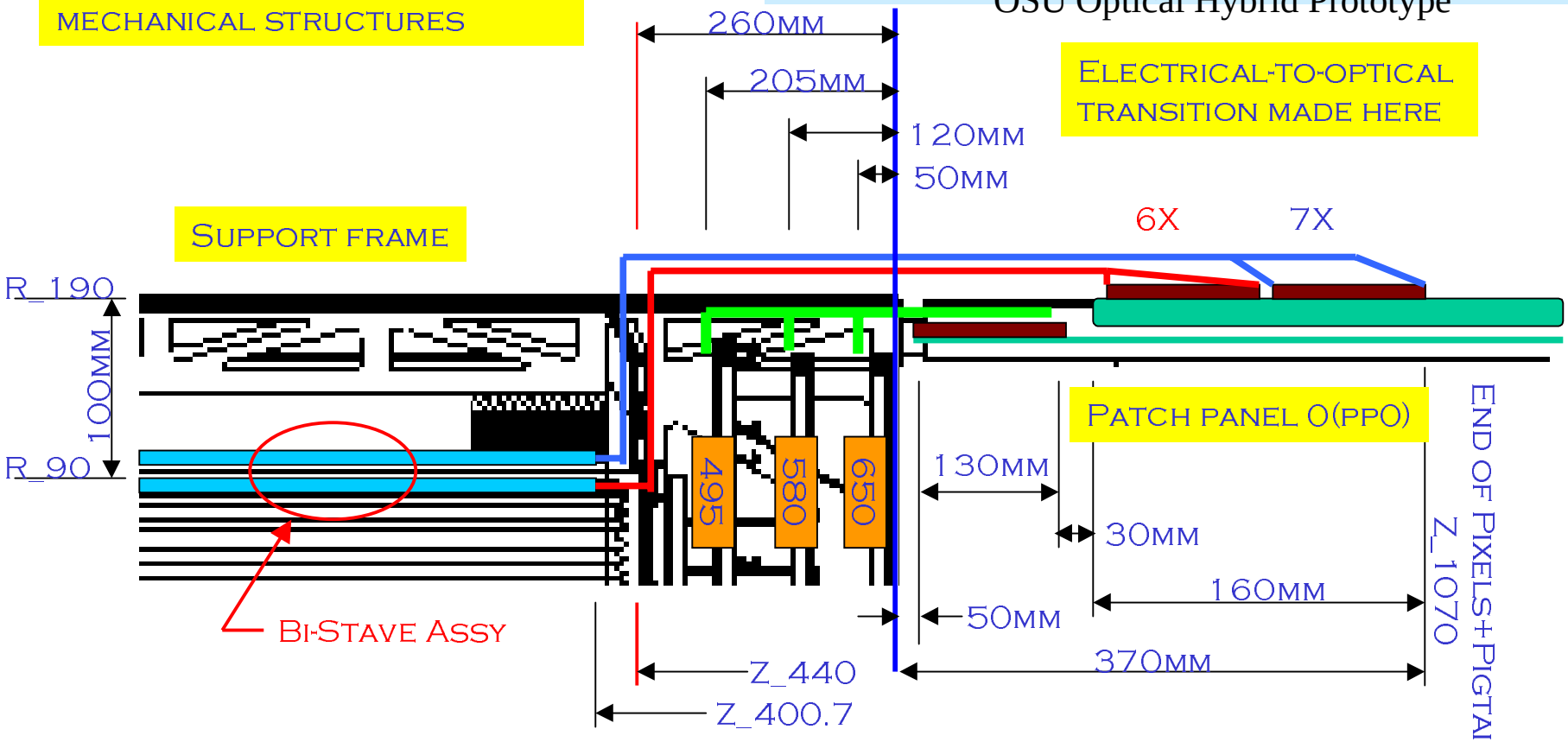


Services I

Integration of services
-cooling, power, signal-
is now major design driver
for support frame and other
mechanical structures

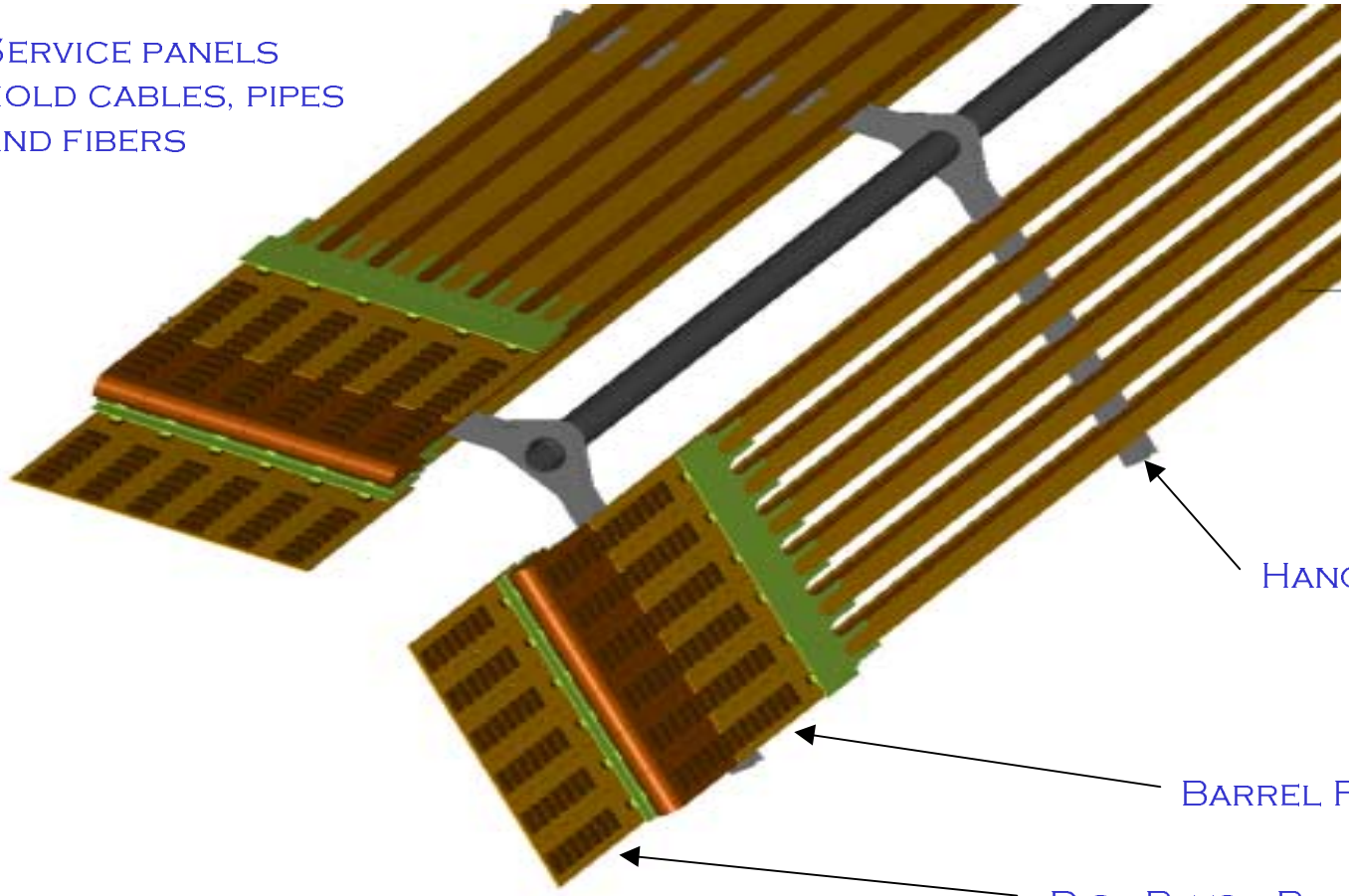


OSU Optical Hybrid Prototype



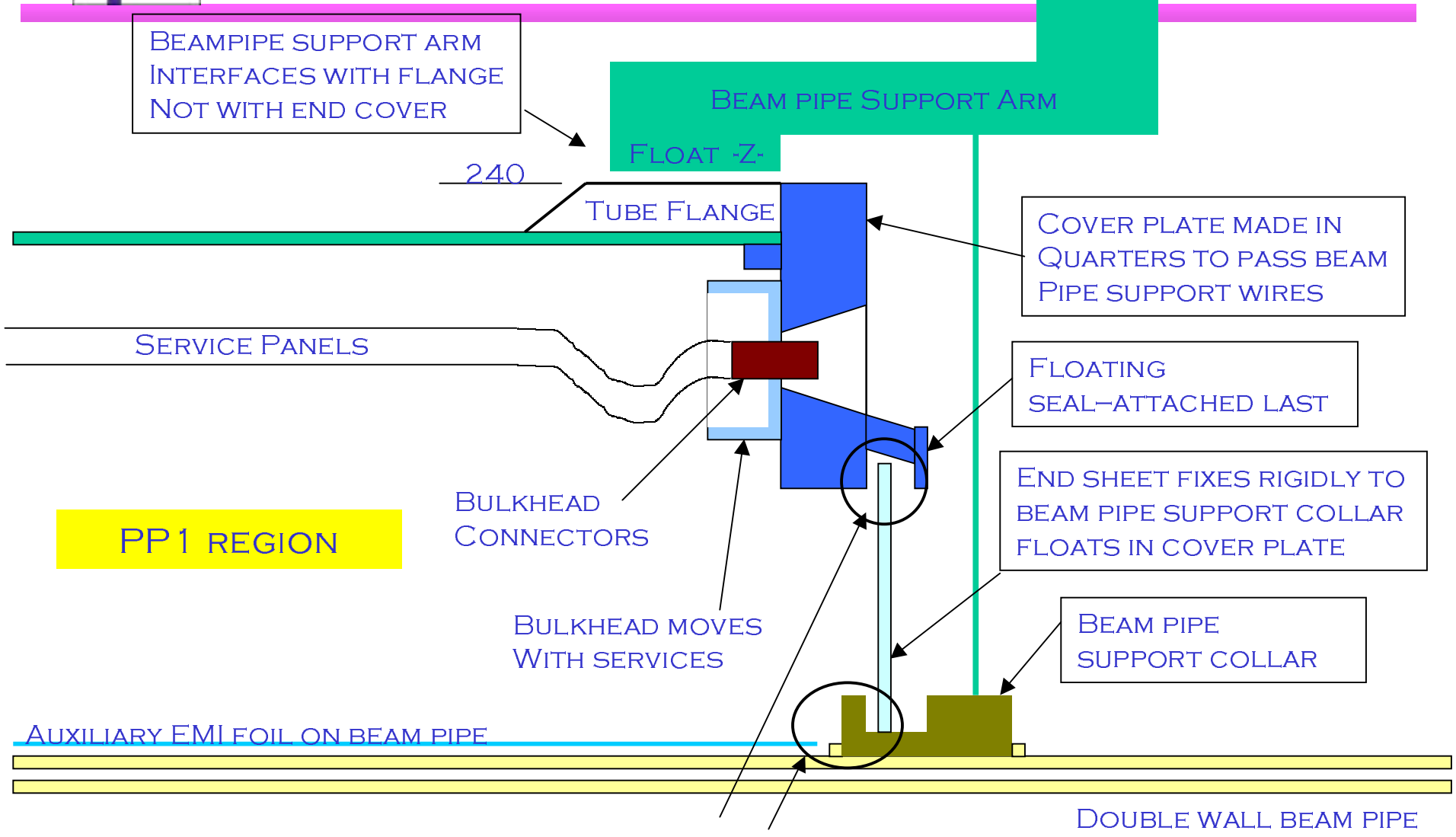
Services - II

Service panels hold cables, pipes and fibers



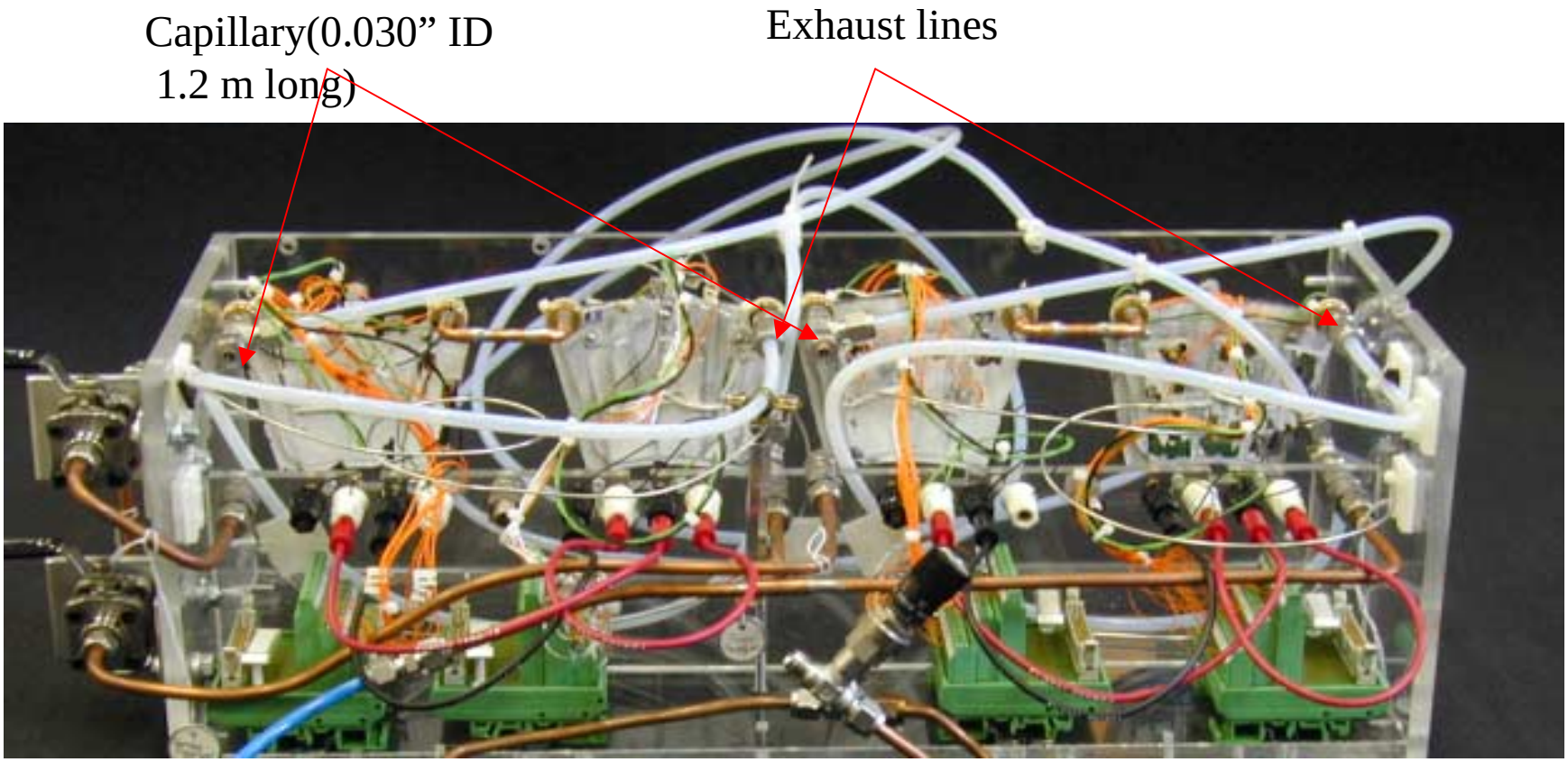
Structure necessary to support services during installation. These slide along rails in support tube

Services - III



Cooling

- **Evaporative C_3F_8 is baseline.**
- **Sectors tested - test setup below. Substantial headroom to maintain temperature of silicon at or below 0°C.**

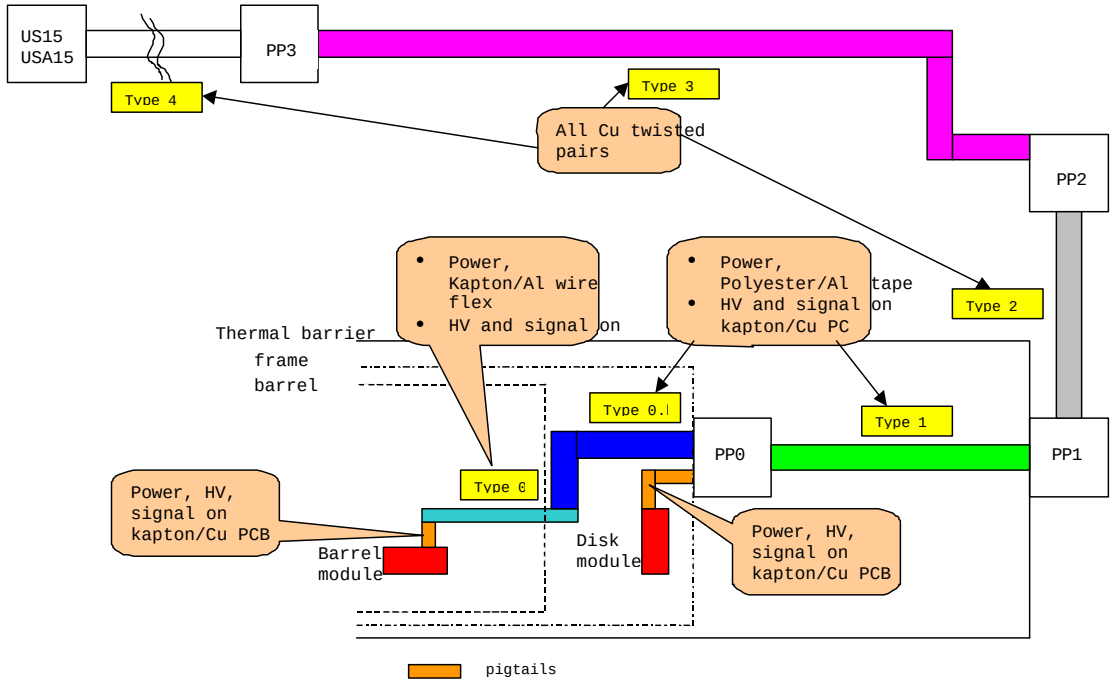


Cooling Connections

- Advanced prototype stage.
- Joint US/Europe program with multiple options for joining tubes and connectors.
- Brazing, gluing and e-beam welding under study.
- Connector types under study and test.
- Corrosion of aluminum under radiation in C_3F_8 studied - not a problem.
- Baseline choice for connection to sector(or stave) in time for June PRR.

Cables and Connections

- Conceptual framework documented(eg. for ATLAS-wide power supply review this month).
- Prototypes built for
  - module -> PP0 ->PP1
  - evaluating prototype power supplies(simulate full length)



Final Assembly/Installation

- Full “trial assembly” of structures in schedule.
- Disk regions assembled at LBNL.
- Shipped(as units or pieces) to CERN for integration with barrel. Barrel assembly will be done at CERN.
- Conceptual installation sequence in support tube exists.
- Still in conceptual design phase but mockup will allow test of some concepts(not all).
- Close integration with ongoing overall re-baselining of ATLAS installation plan and access scenarios.

US Mechanics/Services Team

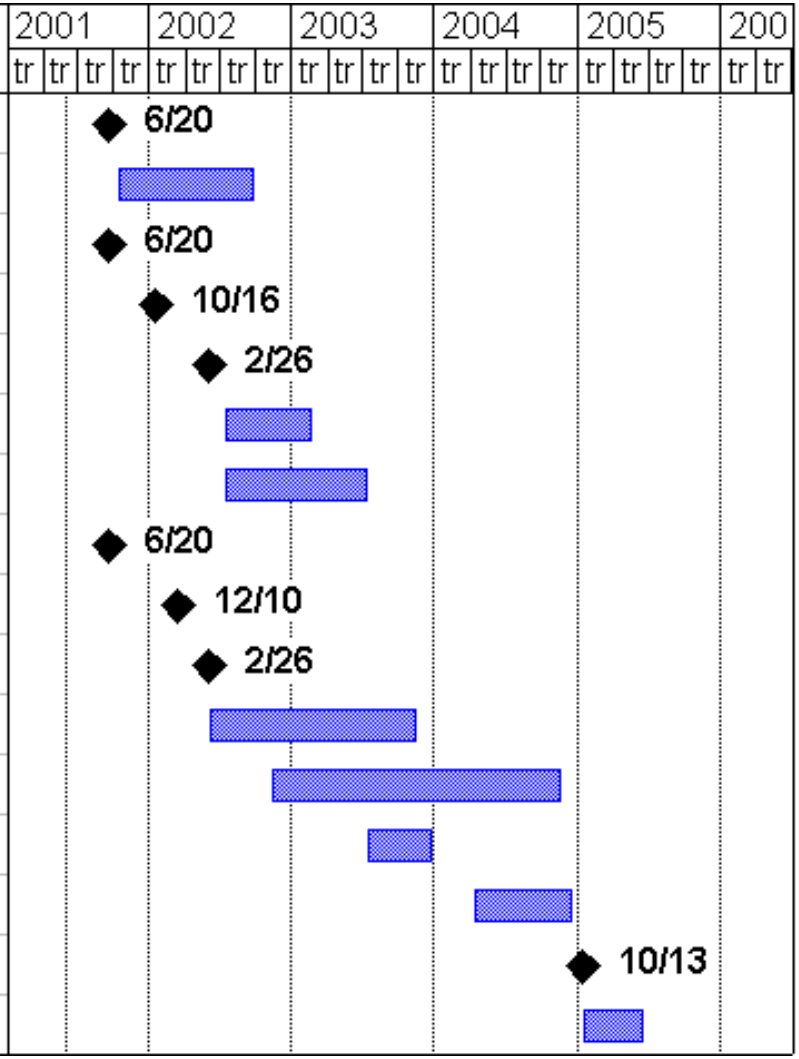
- Almost all at LBL or under contract to LBL(Hytec, Inc).
- Engineers[Anderssen, Goozen, Hartman, Hoeferkamp(EE - UNM), Miller(Hytec), Miller(Hytec)]
- Designers(Taylor, Uken, Hytec team)
- Techs(Johnson, McCormack, Weber, Wirth, Witharm)
- Shops, special services + students.
- Physicists[Gilchriese + Einsweiler/Garcia-Sciveres on services]

Funding Profile - Base Cost

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.1	Mechanics and Final Assembly	0	0	0	0	0	923	917	1032	177	19	3067
1.1.1.1.1	Design	0	0	0	0	0	571	447	262	83	12	1375
1.1.1.1.1.1	Prototype Design	0	0	0	0	0	136	0	0	0	0	136
1.1.1.1.1.2	Production Design	0	0	0	0	0	435	447	262	83	12	1239
1.1.1.1.2	Development and Prototypes	0	0	0	0	0	152	105	0	0	0	257
1.1.1.1.2.1	Disk Sectors	0	0	0	0	0	17	0	0	0	0	17
1.1.1.1.2.2	Disk Support Rings	0	0	0	0	0	8	0	0	0	0	8
1.1.1.1.2.3	Support Frame	0	0	0	0	0	20	0	0	0	0	20
1.1.1.1.2.4	Support Tube	0	0	0	0	0	44	21	0	0	0	65
1.1.1.1.2.5	Services	0	0	0	0	0	64	84	0	0	0	148
1.1.1.1.2.6	Disk Assembly	0	0	0	0	0	0	0	0	0	0	0
1.1.1.1.2.7	Final Assembly and	0	0	0	0	0	0	0	0	0	0	0
1.1.1.1.2.8	Test Equipment	0	0	0	0	0	0	0	0	0	0	0
1.1.1.1.3	Production	0	0	0	0	0	199	365	770	94	7	1435
1.1.1.1.3.1	Disk Sectors	0	0	0	0	0	117	28	0	0	0	145
1.1.1.1.3.2	Disk Support Rings	0	0	0	0	0	0	126	0	0	0	126
1.1.1.1.3.3	Support Frame	0	0	0	0	0	0	122	122	0	0	243
1.1.1.1.3.4	B-layer Support	0	0	0	0	0	0	0	26	37	0	64
1.1.1.1.3.5	Support Tube	0	0	0	0	0	0	56	156	0	0	211
1.1.1.1.3.6	Endplug Thermal Barrier	0	0	0	0	0	0	0	41	0	0	41
1.1.1.1.3.7	Services	0	0	0	0	0	0	21	290	0	0	311
1.1.1.1.3.8	Disk Assembly	0	0	0	0	0	0	11	91	0	0	102
1.1.1.1.3.9	Disk Region Final Assembly	0	0	0	0	0	0	0	42	50	0	92
1.1.1.1.3.10	Test Equipment	0	0	0	0	0	82	2	2	7	7	100
1.1.1.1.3.11	Installation	0	0	0	0	0	0	0	0	0	0	0

1.1.1.1 Mechanics -Schedule Flow

ID	Task Name
1	Disk Sector PRR
2	Disk Sector Fab/Test
3	Global Support CDR
4	Global Support FDR
5	Global Support PRR
6	Disk Support Ring Fab/Test
7	Support Frame Fab/Test
8	Support tube CDR
9	Support tube FDR
10	Support tube PRR
11	Support tubes Fab/Test
12	Outer Services Fab/Test
13	Trial Outer Structure Assembly
14	Disk Assembly/Test
15	Disk System at CERN
16	Outer System Assembly/Test at CERN

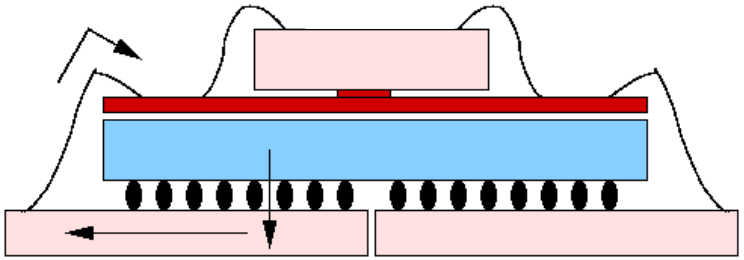


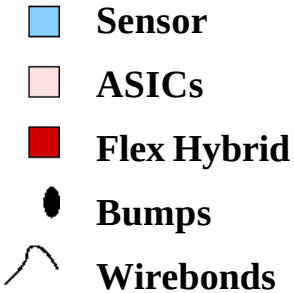
Hybrids
WBS 1.1.1.4
&
Module Assembly
WBS 1.1.1.5

M. Garcia-Sciveres

LBNL

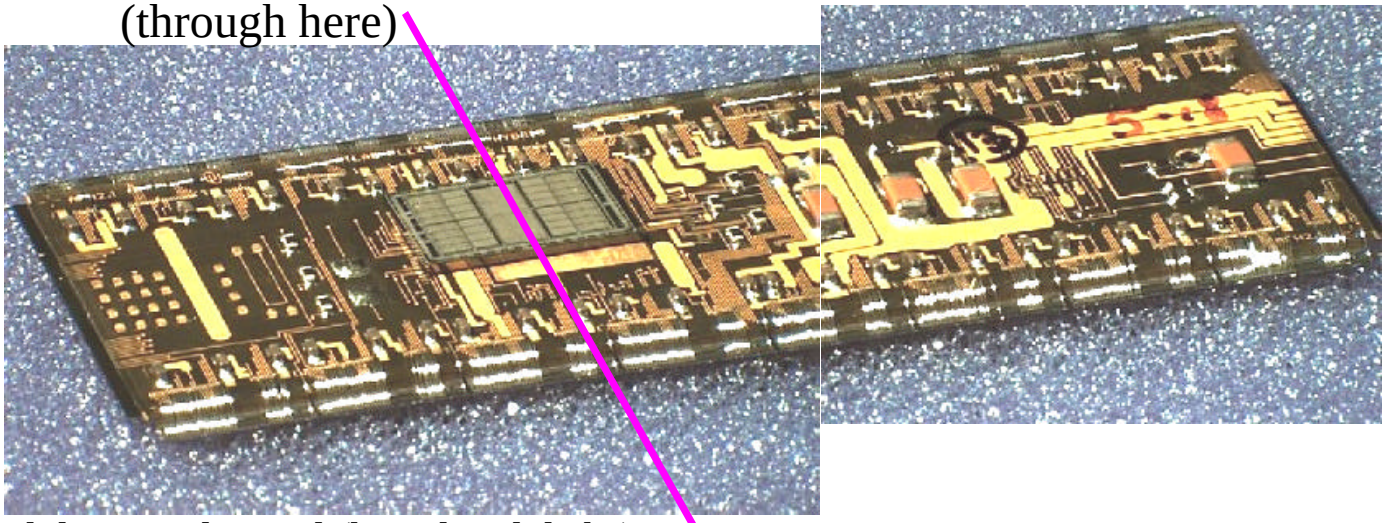
The Pixel Module





Schematic Cross Section

(through here)



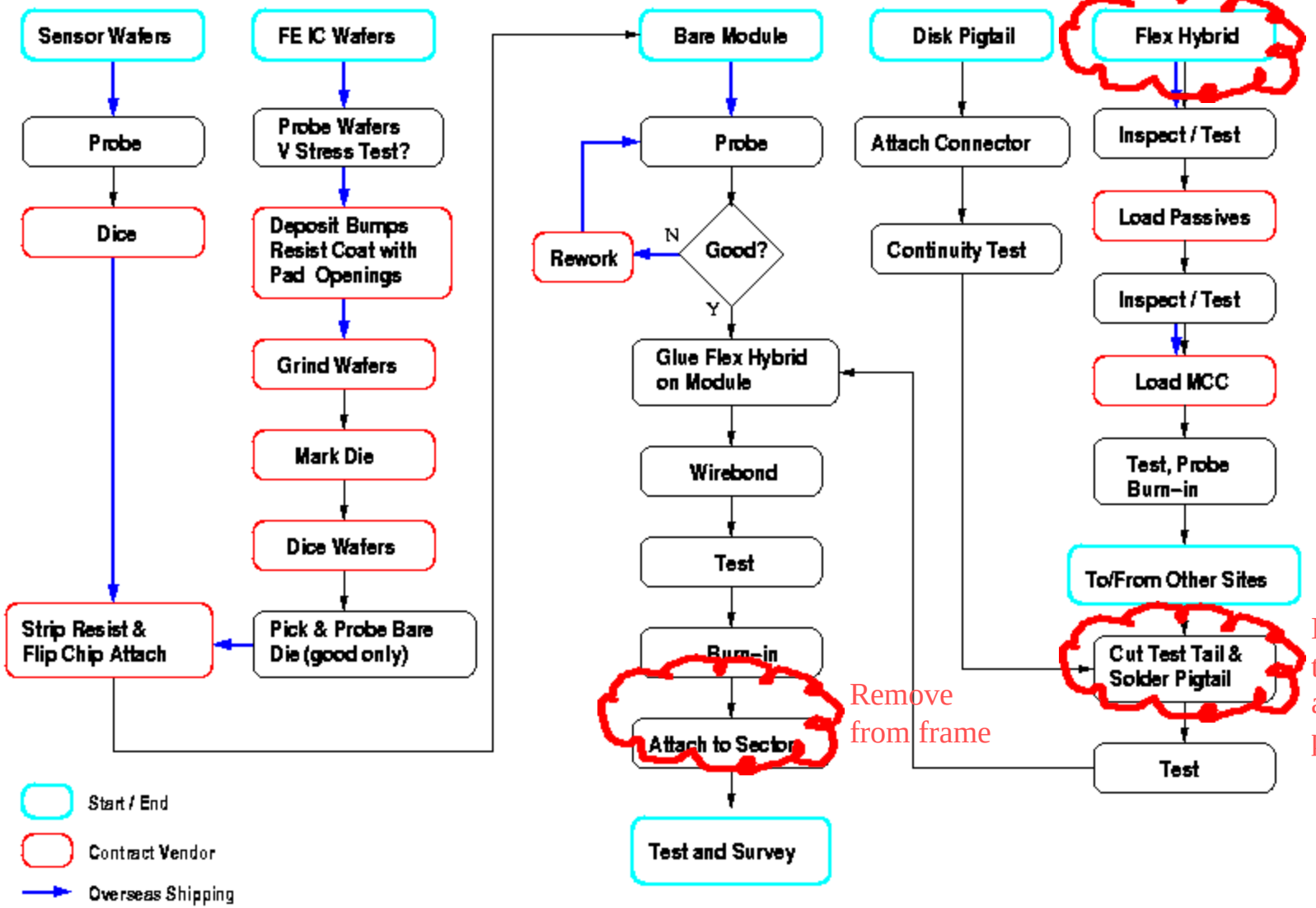
•All modules are identical (barrel and disks)

•"Pigtails" of different varieties are attached in assembly depending on use location

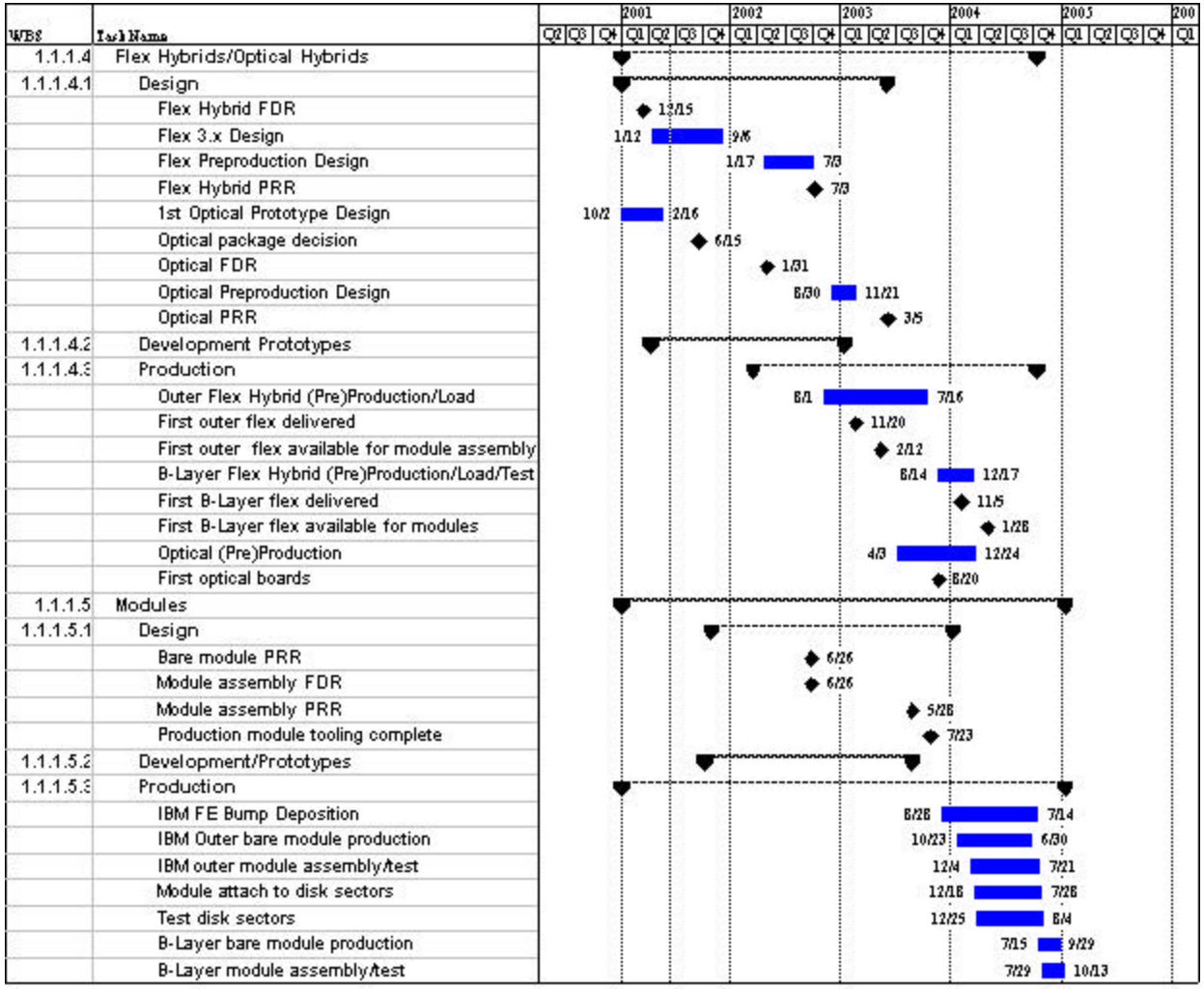
Module Production

COMPONENTS	US RESPONSIBILITY	INSTITUTIONS
Bumped 8" FE Wafers	Probe Thin and Dice	LBNL
Sensors	Probe	New Mexico, Oklahoma
Bare modules	Probe (no flip-chip in US)	LBNL
Flex Hybrids	Fabricate Component load & Test Load MCC chip & test	Oklahoma Oklahoma, Albany Oklahoma, Albany
Full Modules	Assemble, Wirebond, Test, Burn-In	LBNL TBD
Disk Pigtails	Fabricate, Test, Assemble	LBNL

U.S. Atlas Pixel Module Assembly Flow, Nov. 2, 2000



1.1.1.4 & 1.1.1.5 Schedule Summary



WBS	Task Name
1.1.1.4	Flex Hybrids/Optical Hybrids
1.1.1.4.1	Design
	Flex Hybrid FDR
	Flex 3.x Design
	Flex Preproduction Design
	Flex Hybrid PRR
	1st Optical Prototype Design
	Optical package decision
	Optical FDR
	Optical Preproduction Design
	Optical PRR
1.1.1.4.2	Development Prototypes
1.1.1.4.3	Production
	Outer Flex Hybrid (Pre)Production/Load
	First outer flex delivered
	First outer flex available for module assembly
	B-Layer Flex Hybrid (Pre)Production/Load/Test
	First B-Layer flex delivered
	First B-Layer flex available for modules
	Optical (Pre)Production
	First optical boards
1.1.1.5	Modules
1.1.1.5.1	Design
	Bare module PRR
	Module assembly FDR
	Module assembly PRR
	Production module tooling complete
1.1.1.5.2	Development/Prototypes
1.1.1.5.3	Production
	IBM FE Bump Deposition
	IBM Outer bare module production
	IBM outer module assembly/test
	Module attach to disk sectors
	Test disk sectors
	B-Layer bare module production
	B-Layer module assembly/test

Flex Hybrids

- Development has so far gone through **two design cycles**
- Version **1.x** (x=0,1,3,4)
  - 80 Fabricated by CERN and Compunetics between 1998 and 1999.
  - Used to make "proof of principle" working modules with rad-soft electronics
- Version **2.x** (x=1,2)
  - 150 Fabricated by CERN and Compunetics in 2000
  - Detailed performance characterization & system tests have not been possible due to lack of rad-hard electronics
  - Used to debug manufacturing & assembly process & to investigate mass production issues.
- **F**inal **D**esign **R**eview during December '00 Pixel Week
  - "Early" in design terms to derive max. technical benefit

Flex Hybrids (continued)

- Goals for Version 3 Flex design (in progress):
  - **Qualify more vendors**
    - Increasing ease of manufacture through interaction with designs of new FE chip and services.
  - **Test bed for first IBM FE chip run (FE-I) – to submit July 01**
    - Accelerating design cycle and avoiding un-proven features so hybrids will be ready ahead of FE-I delivery
    - Making compatible with existing (obsolete) controller chip
  - **Compatible with mass assembly, testing, and handling**
    - Apply lessons learned from V2.x prototypes
  - **Address system integration**
    - Work closely with parallel development of service connections
- Preliminary layout to be ready for bidding in April
- Expected fabrication June-Aug. 2001.

WBS 1.1.1.4 Funding Profile

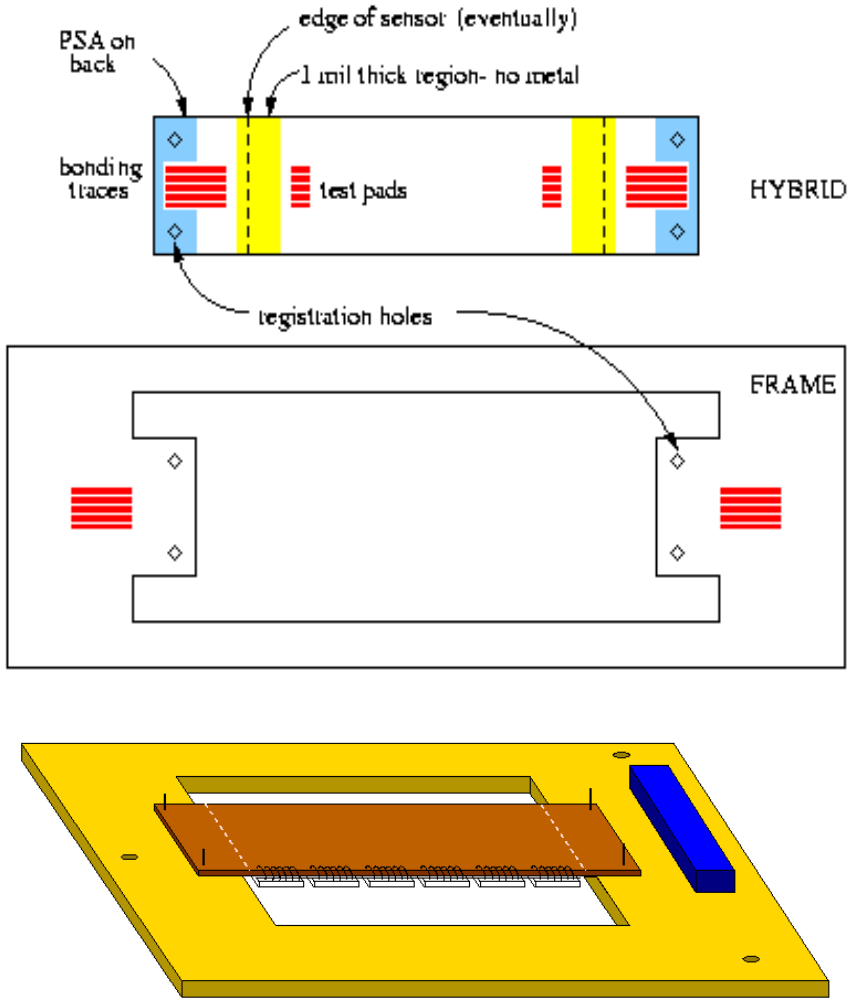
U.S. ATLAS E.T.C.
WBS Profile Estimates

Funding Source: All **Funding Type:** Project

WBS Number	Description	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.4	**Flex Hybrids/Optical Hybrids**	**0**	**0**	**110**	**138**	**273**	**4**	**0**	**525**
1.1.1.4.1	Design/Engineering	0	0	18	50	9	0	0	77
1.1.1.4.1.1	Prototype design	0	0	18	0	0	0	0	18
1.1.1.4.1.2	Production design	0	0	0	50	9	0	0	59
1.1.1.4.2	Development and Prototypes	0	0	92	62	0	0	0	154
1.1.1.4.2.1	Flex hybrids	0	0	35	10	0	0	0	45
1.1.1.4.2.2	Optical prototypes	0	0	41	41	0	0	0	82
1.1.1.4.2.3	Pigtails prototypes	0	0	16	11	0	0	0	27
1.1.1.4.3	Production	0	0	0	26	264	4	0	294
1.1.1.4.3.1	Flex hybrid	0	0	0	16	158	1	0	175
1.1.1.4.3.2	Pigtails	0	0	0	0	33	0	0	33
1.1.1.4.3.3	Optical hybrids	0	0	0	10	73	3	0	86

Carrier Frame

- New development for Flex V.3
- Needed for reliable mass production, handling, & shipping of hybrids & modules
- Based on module assembly and test experience with Flex V.2

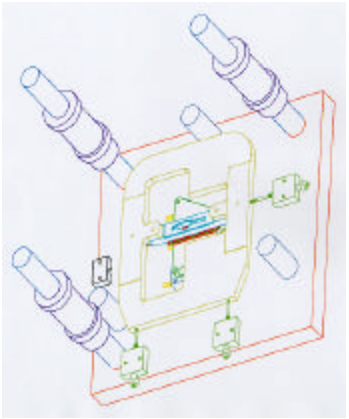
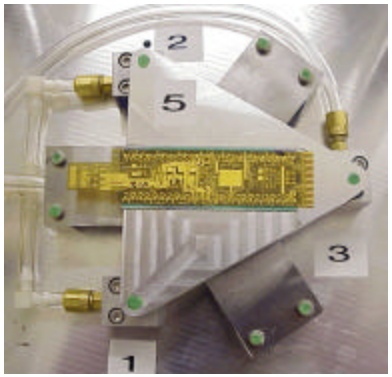


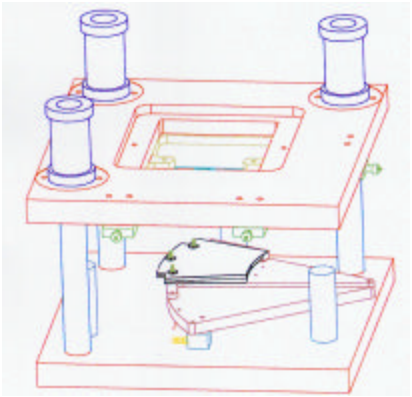
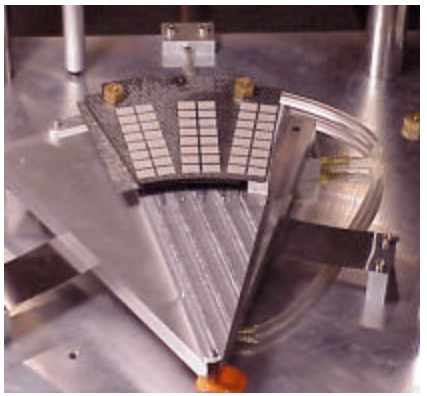
Pre-Production Module Work

		Parts Used
Validate Design	Electrical	**"Hot" Modules**
	Envelope	Mechanical Dummies
Debug Production Process	Assembly	Mechanical Dummies
	Handling	Mechanical Dummies
	Test	———

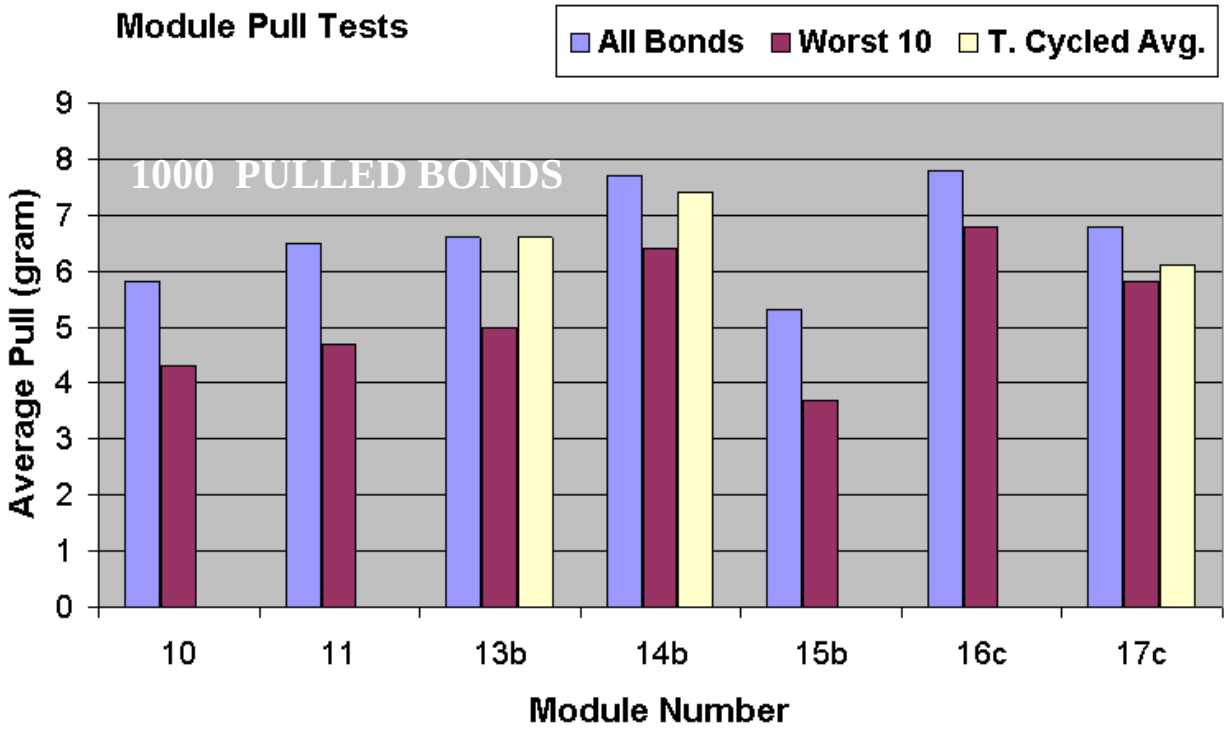
Modules Produced To Date in FY01

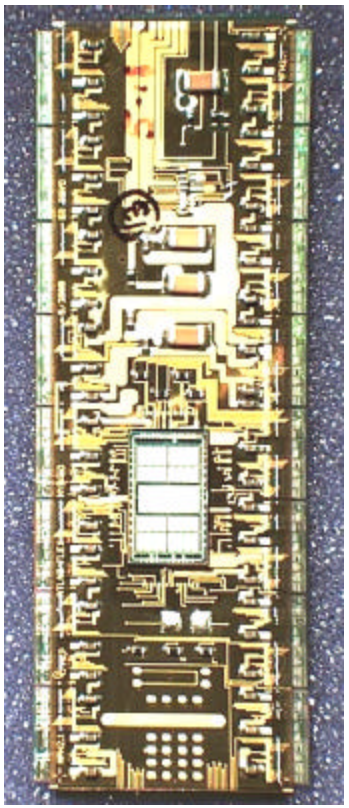
- 23 Mechanical Dummies
- 1 Hot Module (limited by FE chip availability)
- All Use Version 2 Flex Hybrid
- Built by Operators on Version 1 Production Tooling following assembly line procedures

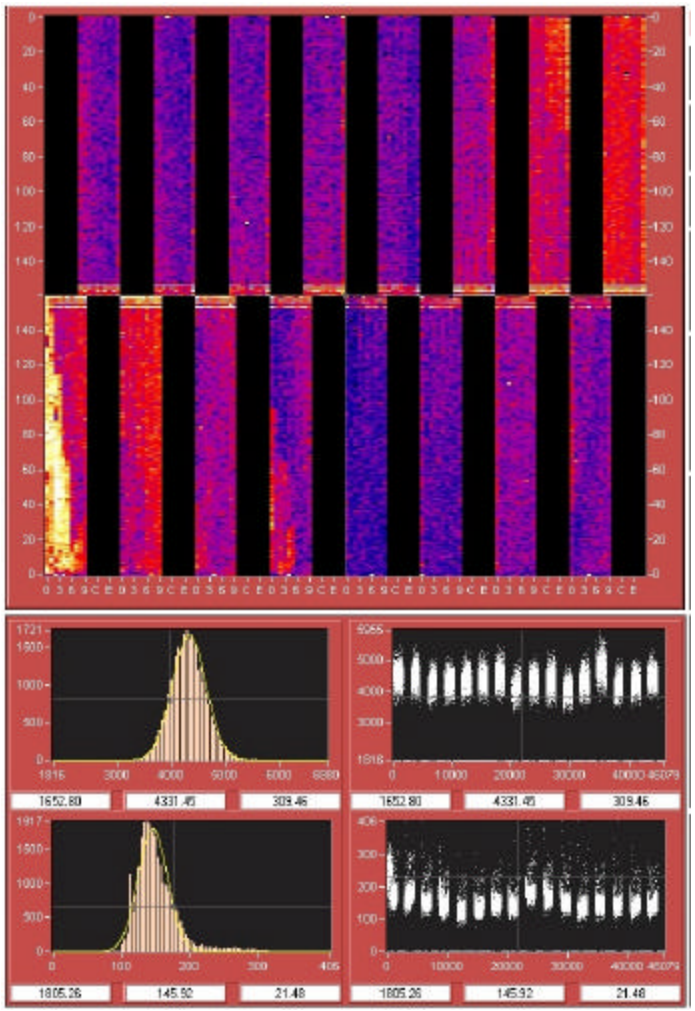
Mechanical Dummy Results

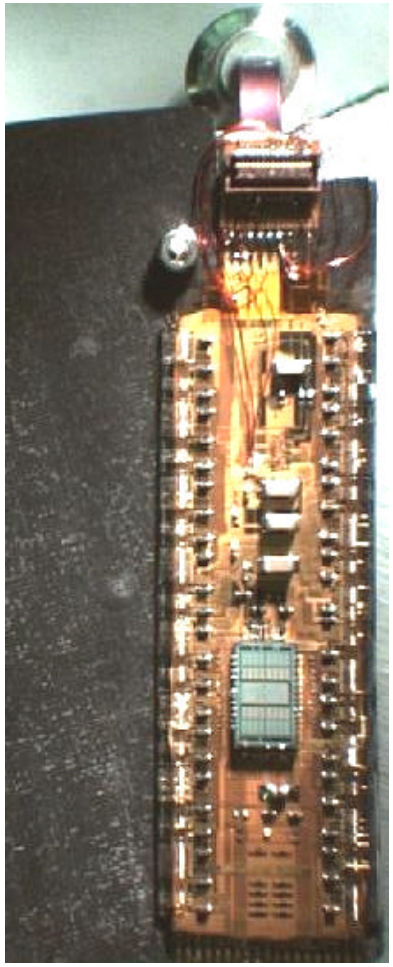




- Assembly tooling works
- Automatic wirebonding is feasible
- Adhesion and uniformity need improvement for production => better metalization
- Hybrids are fragile => need frame to control handling

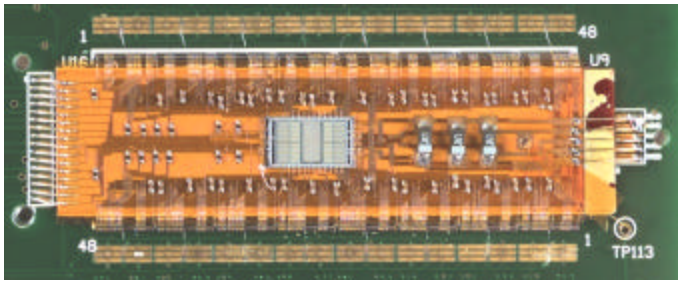
FY01 “Hot” Module Results





- Full digital funtionality
- Excessive IR drops => need better metalization
- Analog performance needs more study. 150e^- noise achieved but dependence on supply voltages not understood.
- Flex Circuitry is fragile => No tabs or soldered pigtail. Use Frame for test connections.

Global Summary of Hot Module Tests

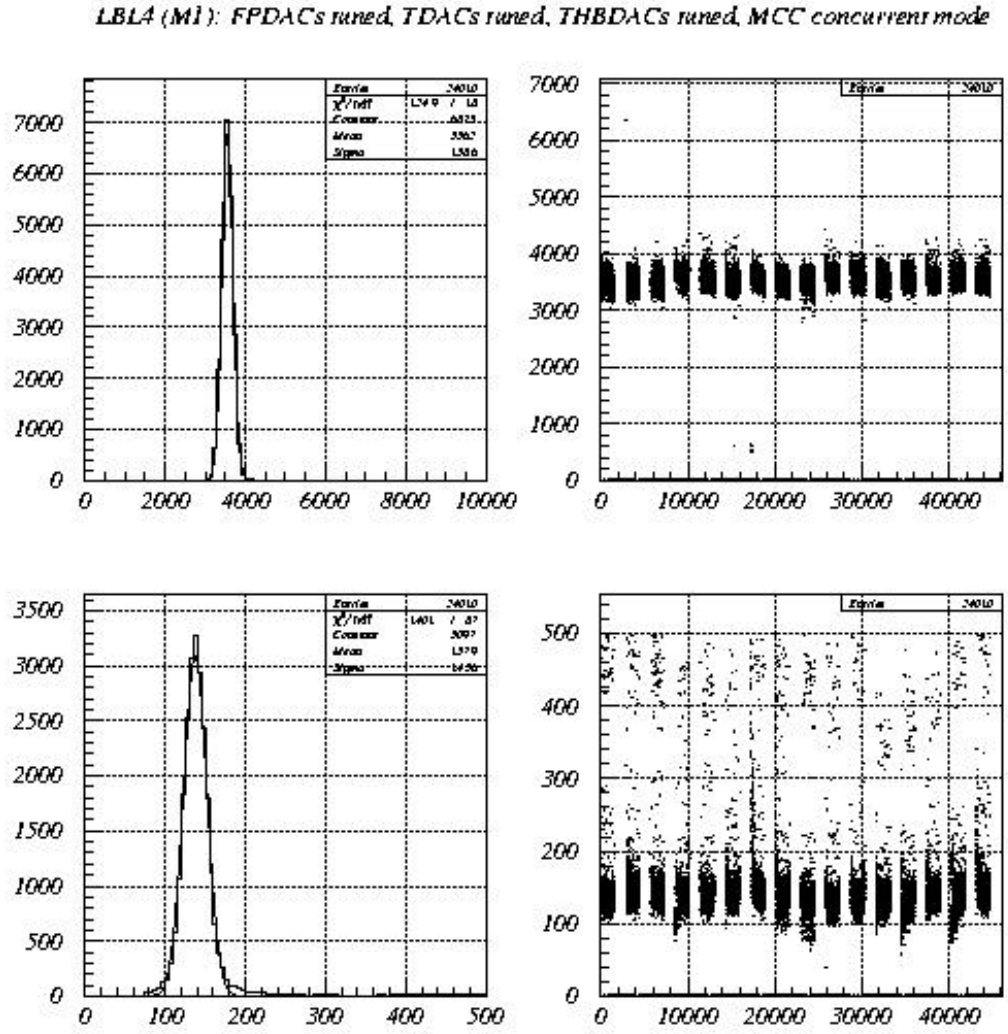


- First full modules operated in 1998
  - Rad-soft FE chips
  - Assemblies bump-bonded by Boeing
  - Version 1 Flex hybrid on support card
  - Full digital functionality. Some coherent noise issues.
- Hot modules with various bump technology and sensor combinations tested in 1999
  - Still Rad-soft electronics
  - “Ideal” analog performance achieved
  - Many assembly problems identified
- In 2000 fewer hot modules built due to lack of FE chips
  - Aim of electrical test is to validate assembly and hybrids
- To do once FE-I chips are available
  - Reproduce “ideal” performance with new chips and new flex hybrids
  - Move on to multi-module system tests

“Ideal” Module Performance

Threshold
s = 139e⁻

ENC = 138e⁻



Mechanical Dummy Program

- The 23 FY01 modules have no bumps- FE chips are glued to blank silicon
- Fabrication of 8” FE chip dummy wafers and 4” sensor dummies is under way – Expected delivery Apr. 5
- Enough parts for 300 bump-bonded dummies to test:
  - Thinning of bumped 8” wafers
  - Rate capability of flip-chip vendors
  - Electrical continuity of bumps through module assembly
  - Uniformity and rate of production line module assembly
- Will use remaining V.2 flex and assemble modules with V.3 flex ahead of FE-I delivery.
- Assembly period Jun. – Nov. 2001

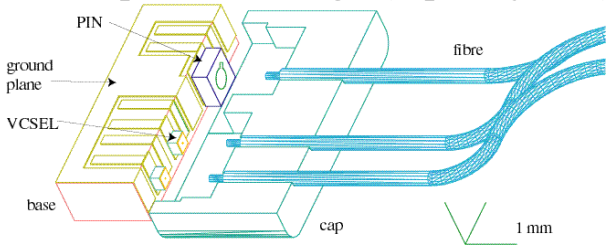
WBS 1.1.1.5 Funding Profile

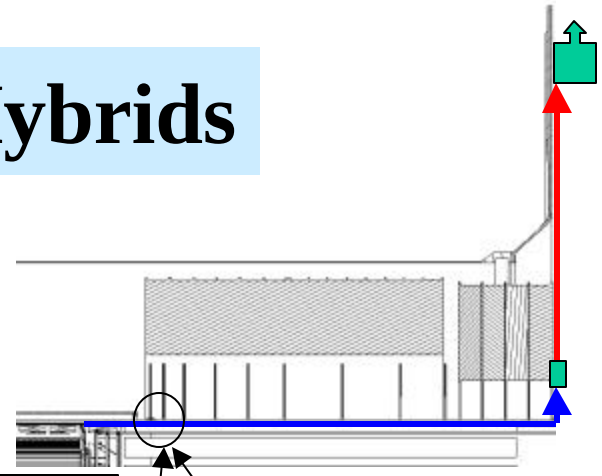
Funding Source: All **Funding Type:** Project

WBS Number	Description	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.5	Module Assembly/Test	0	0	159	244	330	190	0	924
1.1.1.5.1	Design/Engineering	0	0	79	47	0	0	0	126
1.1.1.5.1.1	Prototype Design	0	0	0	0	0	0	0	0
1.1.1.5.1.2	Production Design	0	0	0	0	0	0	0	0
1.1.1.5.1.3	Testing Design	0	0	79	47	0	0	0	126
1.1.1.5.2	Development and Prototypes	0	0	80	135	46	0	0	261
1.1.1.5.2.1	X-ray Inspection	0	0	6	6	6	0	0	17
1.1.1.5.2.2	Wafer Thinning	0	0	0	0	0	0	0	1
1.1.1.5.2.3	Wafer Dicing and Die Sort	0	0	1	3	2	0	0	6
1.1.1.5.2.4	Dummy wafers	0	0	15	13	0	0	0	28
1.1.1.5.2.5	Module Assembly and	0	0	54	83	30	0	0	166
1.1.1.5.2.6	Module Attachment	0	0	5	30	8	0	0	43
1.1.1.5.3	Production	0	0	0	61	285	190	0	536
1.1.1.5.3.1	IC Wafer Thinning	0	0	0	0	2	2	0	3
1.1.1.5.3.2	Dicing of IC Wafers	0	0	0	0	12	12	0	25
1.1.1.5.3.3	IC Die Sort	0	0	0	0	0	0	0	0
1.1.1.5.3.4	Module Assembly	0	0	0	17	108	48	0	173
1.1.1.5.3.5	Module Testing	0	0	0	45	113	51	0	209
1.1.1.5.3.6	Module Attachment	0	0	0	0	12	39	0	51
1.1.1.5.3.7	Sector Electrical Testing	0	0	0	0	25	35	0	60
1.1.1.5.3.8	Production database	0	0	0	0	12	3	0	16

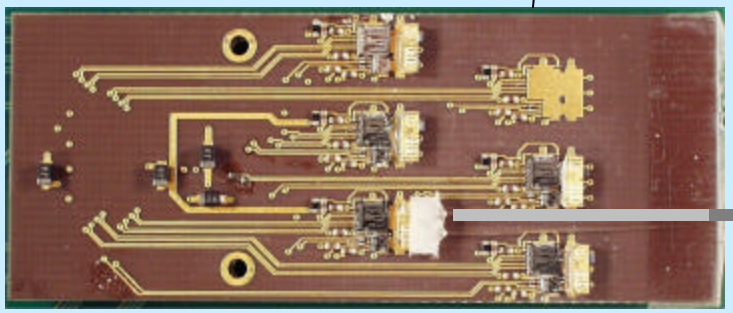
Optical Hybrids

OSU Optical Package (6 per hybrid)





2cm



Optic fibers

OSU Optical Hybrid Prototype

PP0 Printed Flex Prototype

2cm

Optical Hybrids (continued)

- US to produce and test optical hybrids for disks
- Parallel Hybrid development in progress at Ohio State and Wuppertal
- Parallel optical package development at Ohio State and Taiwan
- Choice of a baseline optical package scheduled for June 01
- First full hybrid p^+ irradiations scheduled for April 2001
- Initial γ irradiations of optical packages done in FY00

Conclsions

- Flex Hybrids on track towards production design.
- Issues being addressed: more vendors, FE-I schedule, service integration, production assembly, handling and testing.
- Module production being addressed with mechanical dummy program ahead of availability of final electronics.
  - Mechanical integration and manufacturing issues should not depend on details of readout chip.
- It is understood that design choices made now are contingent on results of system tests with final electronics.
- Optical hybrids designs advancing toward baseline selection date of June 2001.

WBS 1.1.1 Pixel System

Sensors, Opto-links, and On-detector Electronics

Major Topics:

- Sensors (WBS 1.1.1.2): Status and Issues
- Opto-links (WBS 1.1.1.3 and 1.1.1.4): Status and Issues
- On-Detector Electronics and Test System (WBS 1.1.1.3): Status and Issues

Details of our 0.25μ electronics program and schedule will follow in the talk of P. Denes

Summary and Conclusions

Prototype Results in Appendix

Sensor Concepts

Basic requirement is operation after 10^{15} NIEL fluence:

- Requires partially depleted operation. Chosen n^+ pixels in n-bulk material as basic configuration (does require double-sided processing).
- Two isolation techniques studied for the n^+ pixel implants. Selected low dose p-implantation over the whole wafer (so-called p-spray) approach. With p-spray technique, observe only bulk leakage in I/V curve after full dose. Does not require critical high-dose p implantation between n^+ implants, so yield should be high.

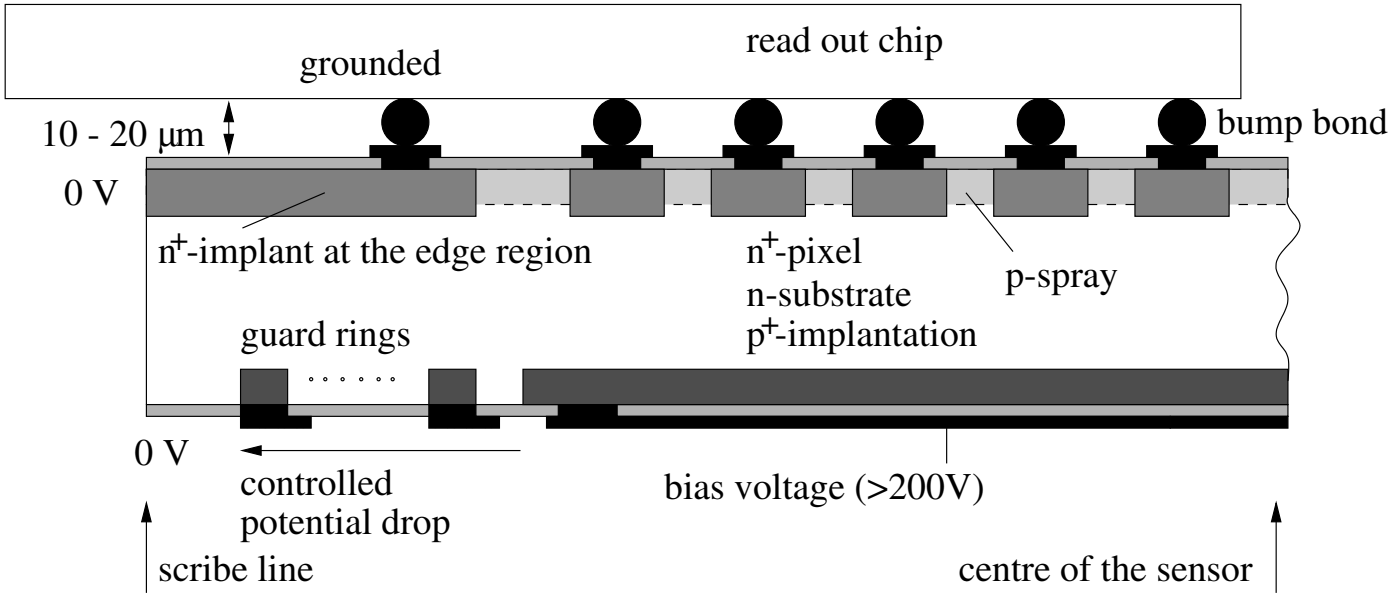


Diagram showing guard geometry near edges of module, designed to operate safely with bias voltages of beyond 700V.

Final Sensor Design (Sensor 2)

- Final design is based on small gap, and includes bias grid to allow testing (hold all pixel implants at ground for I/V characterization) and to keep unconnected pixels from floating to large potential in case of bump-bonding defects. It uses "moderated" p-spray to improve pre-rad breakdown voltage (better yield).
- Sensor 2 wafer layout had 3 module tile designs ("no dot", "small dot", and "large dot" bias structures). SMD (small dot) chosen based on yield and performance:

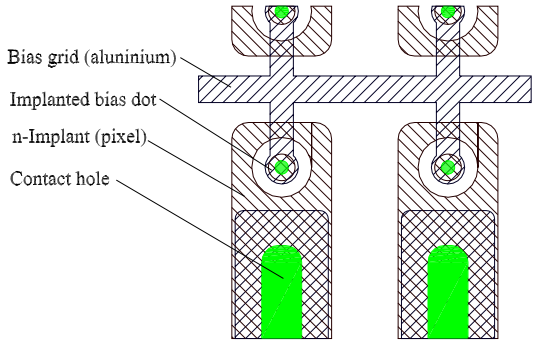
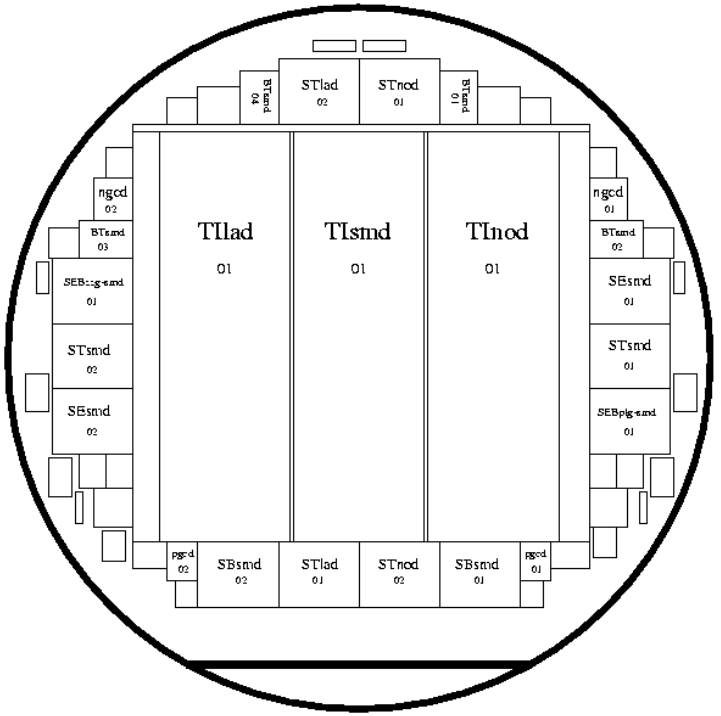
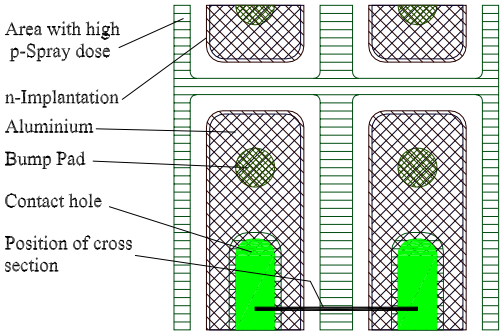
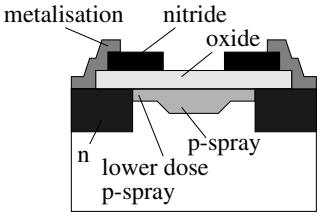


Fig. 10. Design detail of the bias grid in the second sensor prototype.



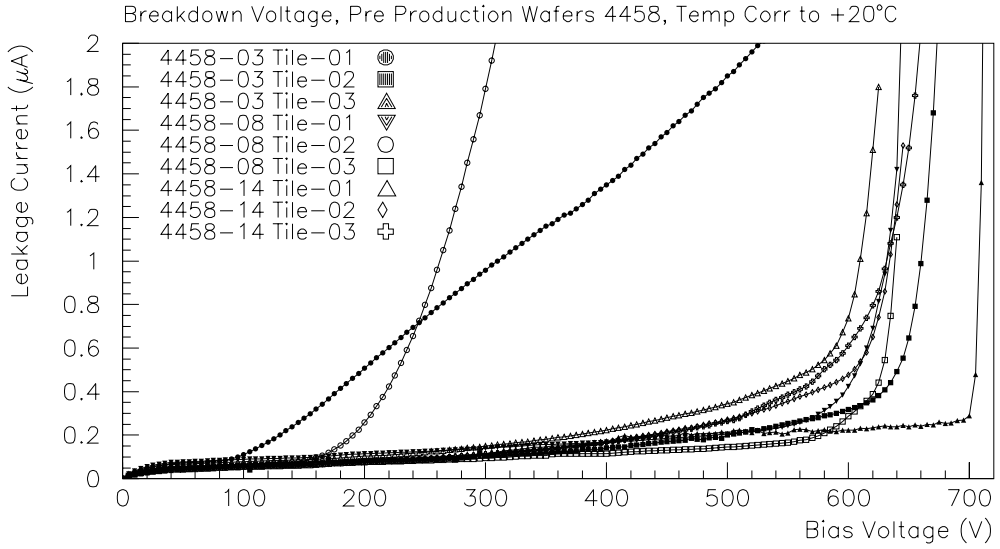


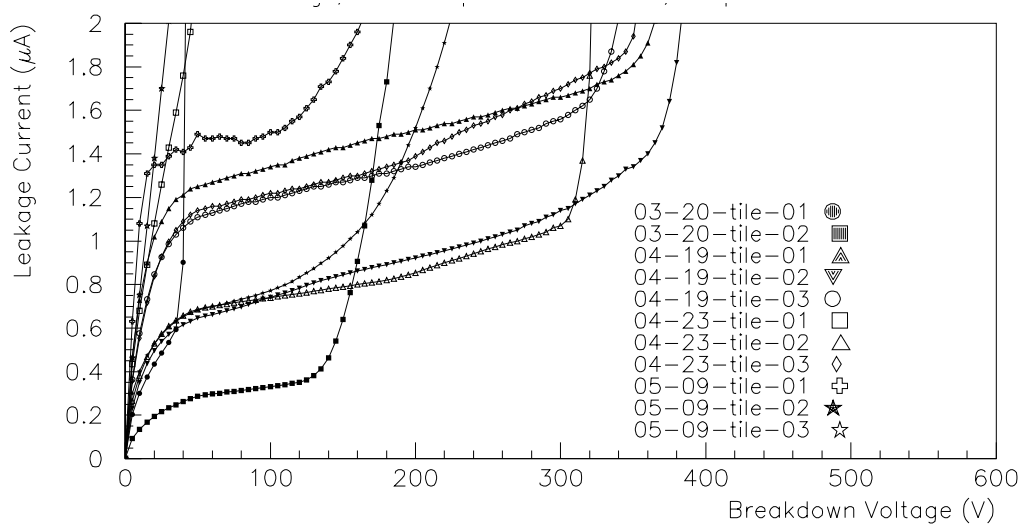


Prototype History:

- **Sensor 1 designs:** Initial designs from 1997 covering a wide range of concepts with CIS and Seiko. Extensively tested in the lab and testbeam in 1998, including irradiation of single chips and subsequent flip-chip to rad-soft electronics.
- **Sensor 1b designs:** Evolution of p-spray designs to include version very close to final production concept (SSGb). Only CIS was a vendor. Extensively tested in lab and beam in 1999. A second identical run (sensor 1c) was used to compare yield for standard and moderated p-spray.
- **Sensor 2 designs:** Emphasis on final wafer layout, significant orders to exercise vendors and allow us to build a large number of modules. Uses latest technology, including moderated p-spray and 50% of wafers oxygenated using ROSE recipe.
- **Oxygenation:** Technique involves diffusion into wafers for 16 hours at 1150 C in O atmosphere. Only useful when irradiation is predominantly charged particles (neutron damage un-affected). Two major effects (other properties unchanged):
- Modification of reverse annealing behavior by “saturating” the total reverse annealing. This gives about half depletion voltage for a fixed large dose. For B-layer, roughly doubles lifetime dose (ignoring trapping effects).
- Increase of reverse annealing time constant by about 4. This gives reduced effect of room temperature exposure on irradiated sensors, and considerably relaxes access scenarios. Largely understood in terms of defect phenomenology.
- FDR (Dec 3 99) and PRR (Feb 2 00) successfully completed.

- Pre-production order launched with two vendors: CIS and Tesla
- First wafers received from CIS in Jan and Tesla in Feb of this year:





- First plot shows I/V results for CiS module tiles. Breakdown is excellent, leakage is low, and yield is good.
- Second plot is for Tesla. Leakage and breakdown are not as good, but still acceptable on most tiles.
- Foundry does I/V characterization too, and only delivers wafers with 2 or 3 good tiles. Agreement with lab measurements is good.

US Roles:

- There are four active testing sites in pixels (Dortmund, New Mexico, Prague, and Udine). Test procedures and acceptance criteria are defined in great detail.
- UNM has performed US share of wafer probing up to the present, and has necessary equipment set up.
- Team is led by Seidel (physicist) and Hoeferkamp (engineer).
- University of Oklahoma could operate as a second site for testing if necessary.

Next Steps and Remaining Issues:

- Complete evaluation of pre-production prototypes from two vendors. Assemblies are in the process of being bump-bonded using FE-D2S chips.
- Pre-production wafer quality looks good to excellent, so all indications are that the two vendors are ready to fabricate production wafers.
- US schedule has procurement occuring in FY02. There appear to be no obstacles to keeping this schedule.

Deliverables:

US Responsibilities include the following:

- Participate in the design and testing of the sensors.
- Contribute roughly 20% towards the common procurement of prototype and production sensor wafers.
- Cost estimate for production is based on tender quotes. Funding is included in the Management Contingency category with high priority for release.

U.S. ATLAS E.T.C.
WBS Profile Estimates

Funding Source: All **Funding Type:** Project 3/6/01 12:17:25 PM

Institutions: All

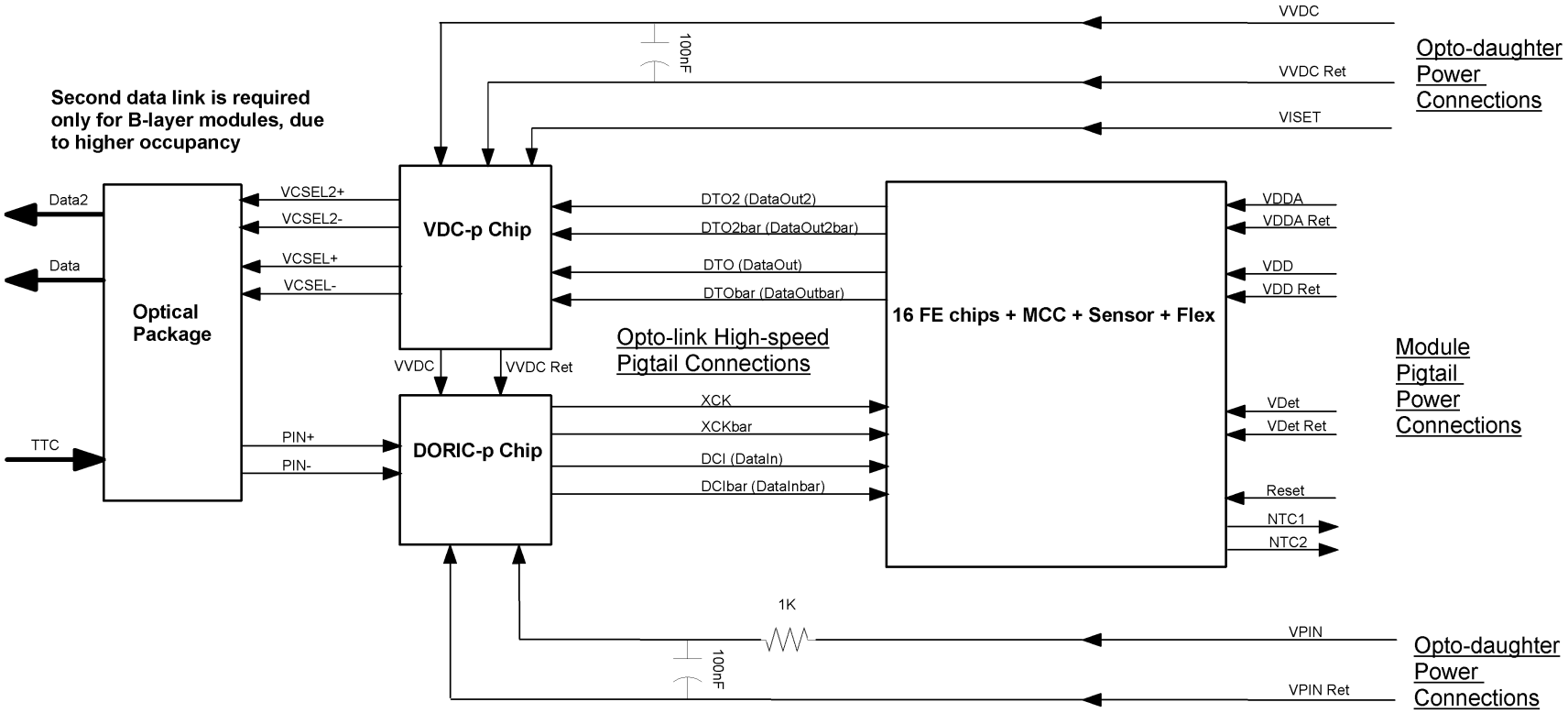
WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.2	Sensors	0	0	0	0	0	97	35	0	0	0	133
1.1.1.2.1	Design/Engineering	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.1.1	Test design	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.1.1.1	Design - New Mexico	0	0	0	0	0	35	35	0	0	0	70
1.1.1.2.3	Production	0	0	0	0	0	62	0	0	0	0	62
1.1.1.2.3.1	Barrels, Disks and B-layer(s	0	0	0	0	0	62	0	0	0	0	62
1.1.1.2.3.1.1	Preproduction	0	0	0	0	0	16	0	0	0	0	16
1.1.1.2.3.1.2	Production	0	0	0	0	0	0	0	0	0	0	0
1.1.1.2.3.1.3	Testing	0	0	0	0	0	46	0	0	0	0	46

On-Detector Electronics, Opto-links, Power Distribution

System Design:

- **Pixel Array (Bonn/CPPM/LBL):** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is “requested” by sending LVL1 signal with correct latency. FE chip then transmits corresponding digital hits autonomously.
- **Module Controller (Genova):** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command/control. The 16 FE chips on module connect to MCC in star topology to eliminate bottlenecks and increase fault tolerance.
- **Opto-link (OSU/Siegen/Wuppertal):** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Basic link is 5x5x1.5mm package, and there are two additional small optolink chips with LVDS interfaces. The fibers are rad-hard silica-core stepped-index multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling on module. Low-mass power tapes used to reach patch panels at end of support (PP0, 1m) followed by Al round cable to transition on cryostat wall (PP2, 7m), then conventional cables to USA15 cavern. Filtering, transient protection, and possibly local voltage regulation would be performed on intermediate patch panels.

Summarize all connections required for module operation:



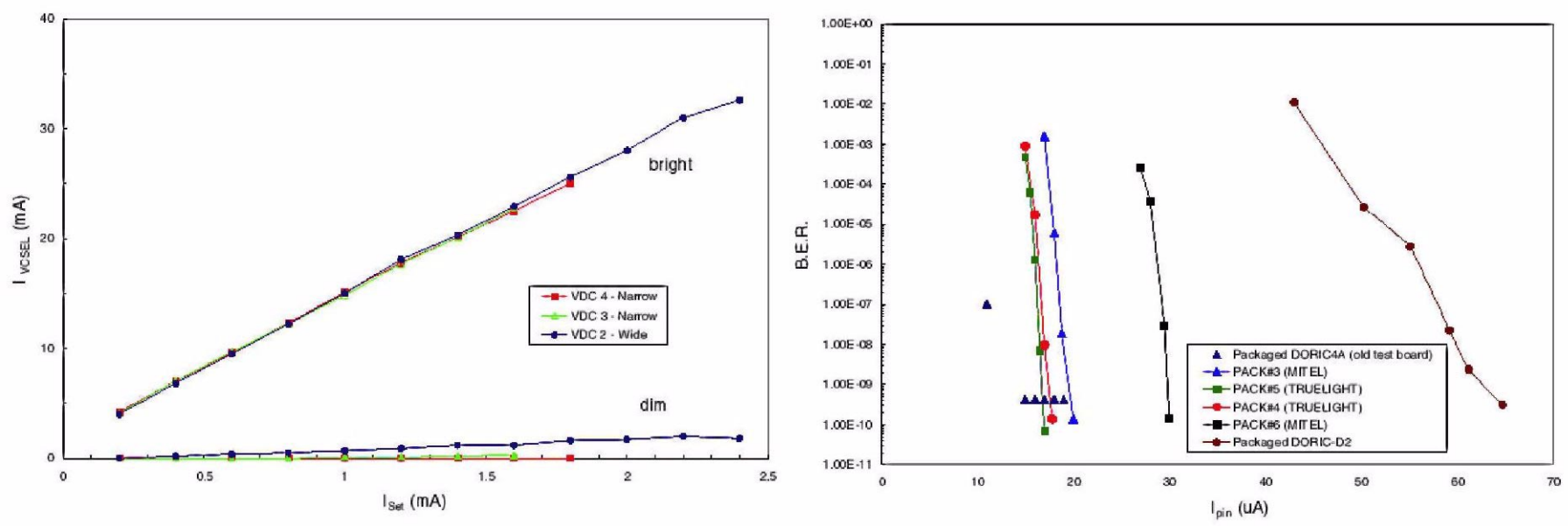
- There are five power supply voltages with their separate returns, and one control voltage that uses VVDCRet as a reference.
- VVDC powers both the DORIC and the VDC, and VPIN may connect directly to the opto-package instead of routing through the DORIC.
- Present concept is that DORIC, VDC and their passive components, plus the Opto-package are placed on Opto-card. Interface requires 3-4 LVDS signal pairs.

Pixel Opto-links:

- All AC signals (clock/commands/data) are transmitted optically to modules:
- **Receiver:** Fiber output is converted using an epitaxial Silicon PIN diode. The output (small current signal) is sent to the DORIC chip, which receives the 40 MHz crossing clock and a bi-phase mark encoded command stream as a single 40 Mbit/s serial stream. It uses a delay-locked loop to extract the clock (providing a high quality 50% duty-cycle clock) and decode the command stream. Note the command stream includes the synchronous LVL1 trigger commands, plus other synchronous commands, and slow configuration commands. An LVDS electrical interface is used to the MCC chip.
- **Driver:** The VDC chip converts LVDS data output streams from the MCC into current pulses suitable for driving the VCSELs chosen for data transmission. For pixel applications, the outer layers plan to use a single 80 Mbit/s output stream (provides roughly a factor 4 of safety), and the B-layer will use two 80 Mbit/s data streams. The format is NRZ, so the 80 Mbit/s link consists of sending a bit on each 40 MHz clock edge. The VCSEL drive current is adjustable using a remotely-controlled voltage. This allows in situ I/L curves, and also periodic operation at high bias to force rapid annealing of radiation damage.
- SCT groups (RAL/Oxford collaboration) have designed and produced two basic chips in pure bipolar AMS design. They work well, but do not withstand pixel doses. For several reasons, pixels have converted designs to rad-hard CMOS.

Status of Pixel DORIC and VDC:

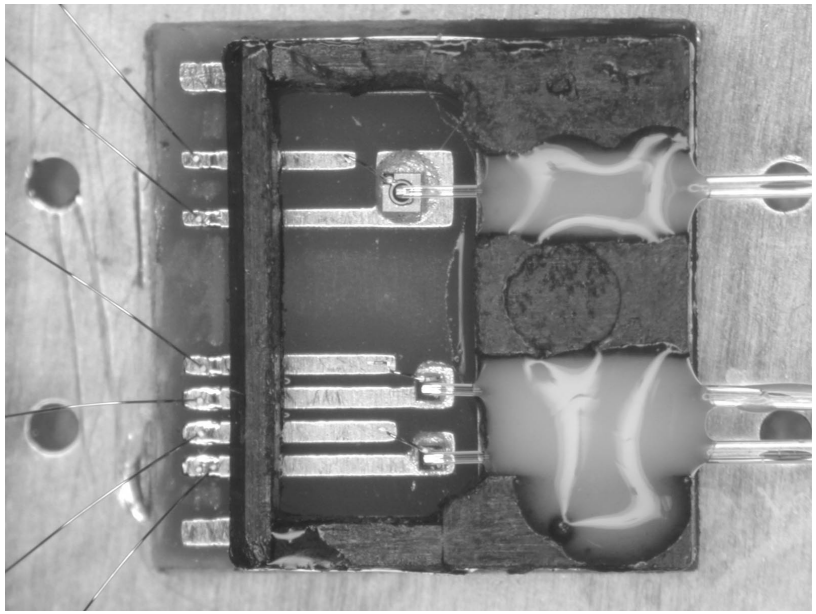
- OSU and Siegen converted SCT design from AMS bipolar to DMILL CMOS. Chips included in FE-D1 submission. VDC-D1 worked fairly well, DORIC-D1 had several design errors related to poor modeling of parasitics.
- Second generation fabricated in FE-D2 submission. DORIC-D2 now works fairly well, but only when used as a bare die very close to opto-package:

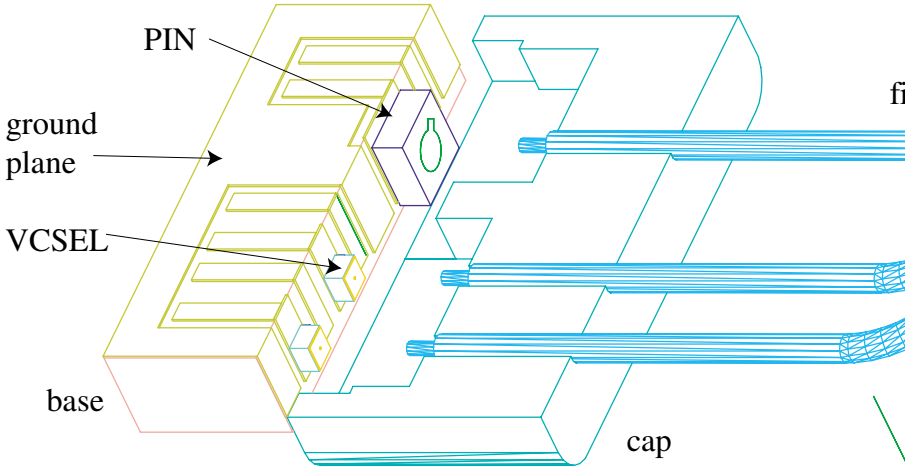


- VDC-D2 shows problem with behavior of dim current (should be constant 1mA).
- DORIC-D2 suffers from preamp DC offsets, and general has a somewhat higher error rate than the SCT DORIC-4A chip. However, it appears to meet specs.
- In Feb, submitted 0.25µ prototype VDC-I and DORIC-I with fixes for these errors. For now, treat both DMILL and 0.25µ as candidate technologies for opto-chips.

Status of Opto-package development:

- Original SCT development was done with Marconi. Package design appeared very expensive and complex. Idea was to develop a cheap and simple package.
- Both Taiwan and OSU have worked on different approaches to this problem.
- Agree to use SCT-qualified PIN (Centronics) and VCSEL (Mitel). These elements have been evaluated in neutron, gamma, and proton beams up to pixel fluences.

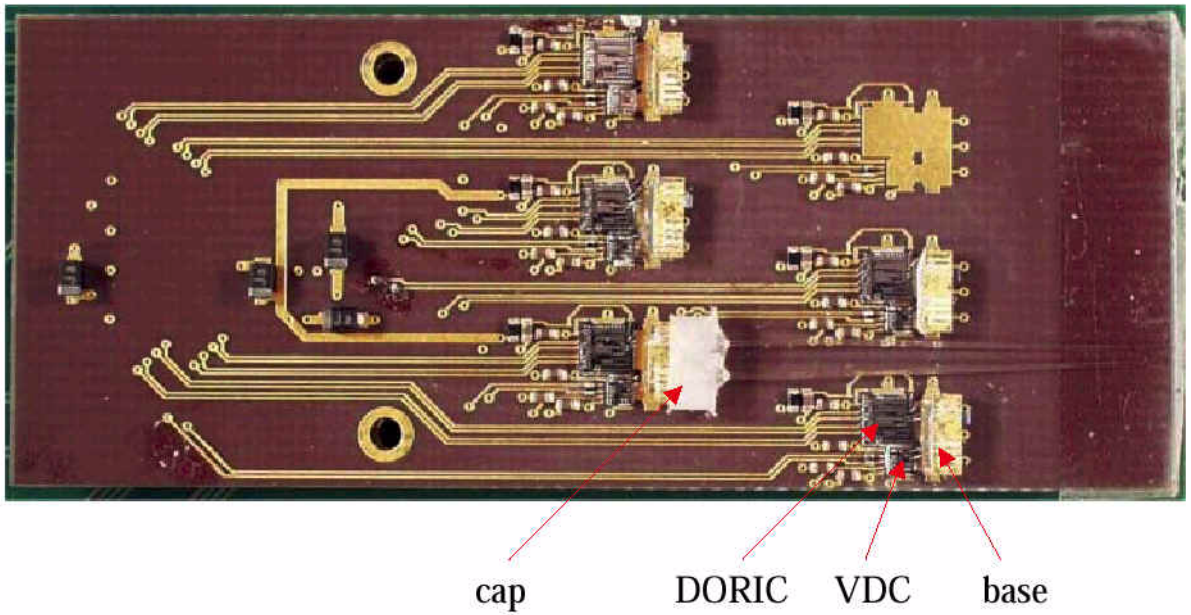




- Taiwan package (left) uses layered PCB, special 45 degree fiber cleaving, and active alignment to achieve good performance.
- OSU package (right) uses molded components and precise tooling to build in performance at low cost, but with larger dispersion in output power.

Opto-Card Concept for Mounting Opto-links

- Original concept was to keep fast timing signals in optical form until very close to the pixel module. Given the very challenging services integration in the pixel detector, especially the barrel, this has proven to be difficult.
- Present concept involves grouping opto-links at the ends of the Global Support structure (attaching them to PP0). This consolidates fiber interface and opto-packages onto a single card with electrical connection to PP0. This separate unit can be fully tested and burned in prior to installation. In addition, all opto-links are at a radius of 15cm, decreasing problems due to SEU effects at smaller radii. This does require high quality electrical pigtails to pixel modules to avoid EMI.

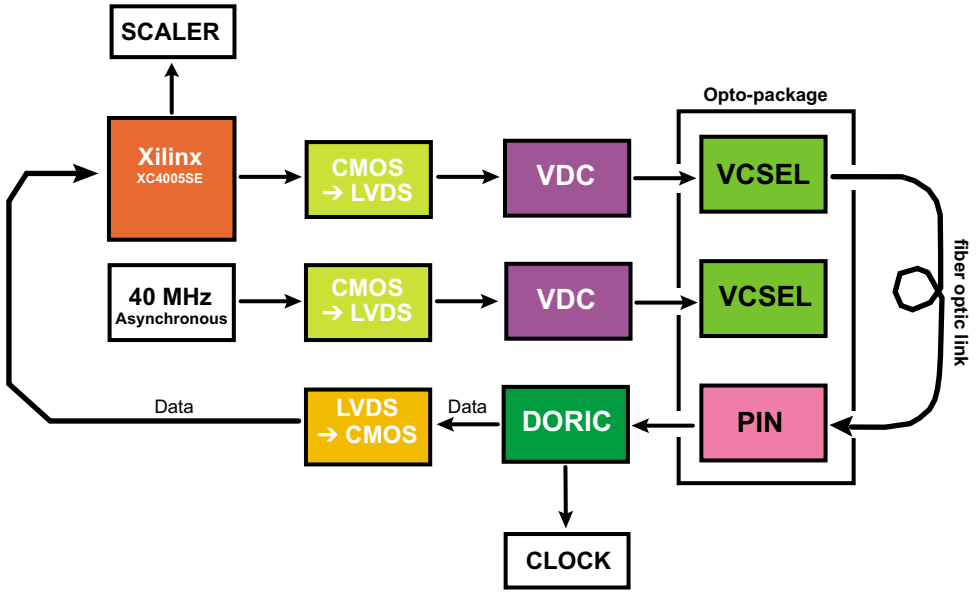


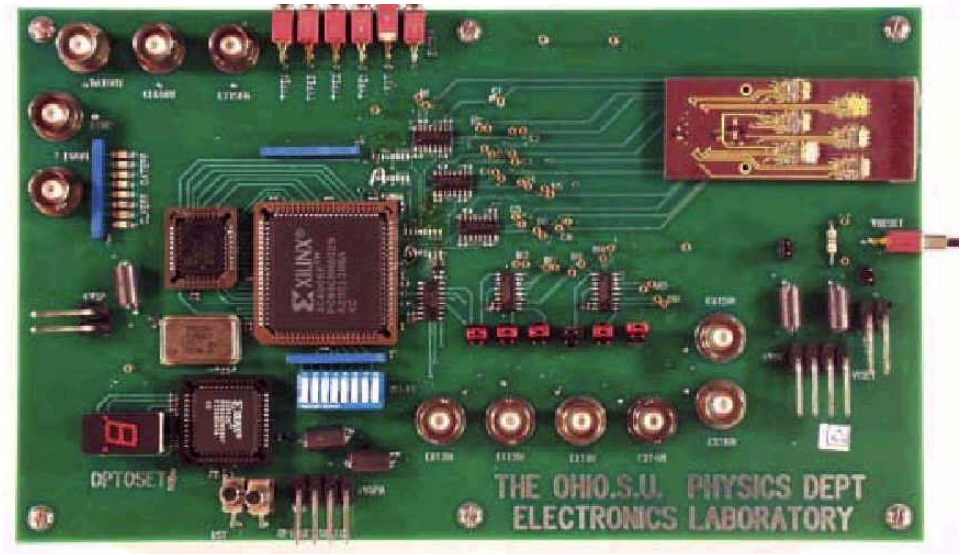
Prototype OSU opto-card.

Final version would be more compact, use BeO ceramic for support, and would use more optimal opto-package design with separate PIN and VCSEL packages.

Test System for Opto-chips and Opto-links

- OSU has built a first prototype of a high-performance opto-link tester, designed to be used for testing a complete opto-card.





- Use VDC and VCSELs as data source, and DORIC and PIN as data decoder/receiver.
- Can loop-back within the same opto-package for now since opto-packages are rare.
- Final system would use off-detector elements coupled by realistic fiber ribbon to opto-card under test.
- This means using a BPM chip and VCSEL array to generate input data, and a DRX chip and PIN array for receiving output data.

Irradiation qualification:

- Collaborative effort of SCT and pixels (Wuppertal from pixels) have performed systematic irradiation studies of optical fibers and opto-elements (PINs and VCSELs) up to pixel fluences. Results show no significant risks, provided PIN is operated with adequate bias voltage (up to about 7V), and provided VCSELs are operated with sufficient bias current (up to about 20mA).
- Only known issue at this time is single event upsets caused by interactions in the very thin epitaxial layer of the PIN diode. Irradiations at PSI showed a significant effect, but at the new radius of the opto-cards, this should not produce a BER of more than about 10^{-9}.
- Pixels has recently significantly upgraded the MCC command set to be highly fault tolerant. Critical commands (particularly LVL1) are successfully decoded under any single bit error, and are only mis-interpreted under double bit error.

Next Steps:

- During April 01 PS run, a complete opto-card will be irradiated, and evaluated during the irradiation using OSU opto-link test system.
- New 0.25µ versions of opto-chips submitted in Feb, expected back by end May.
- Have scheduled ATLAS review to decide on opto-package supplier in June 01.
- Finalizing design of opto-package and opto-card to match requirements of services layout for Insertable Pixel design.

Deliverables

US Roles

- Contribute to design of opto-chips (VDC and DORIC) in DMILL and 0.25μ processes.
- Contribute 50% towards opto-chip fabrication. Baseline in cost estimate is conservatively assumed to be DMILL.
- Probe 50% of opto-chips.
- Supply fraction of opto-cards corresponding to number of modules in the disks.

Electronics Challenges and Requirements

Main challenges are in FE chips:

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an “in-time” threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 300e) and low noise (about 300e).
- Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- Meet specifications with nominal analog power of 40μW/channel and nominal total power for FE chip of 200mW (worst case budget is 70μW and 350mW).

Status of MCC chip:

- First version fabricated by Genova in AMS technology. Chip is roughly 70 mm^2, and 400K transistors. Other than a few very minor errors, it works well.
- Second generation (final design) fabricated in DMILL process. Chip is 100 mm^2. Observed yield is poor (less than 10%), so now working on 0.25μ version.

FE Electronics Prototypes

Several generations of prototypes have been built:

- First “proof of principle” chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C). These were 18 column, 160 row chips with 50μ x 400μ pixels.
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Initial rad-hard activity focussed on common design DMILL chip (FE-D), followed by common design Honeywell chip (FE-H).

Features of initial rad-hard FE design:

- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

Initial Radiation Hard Strategy

Pursued essentially identical designs with two vendors:

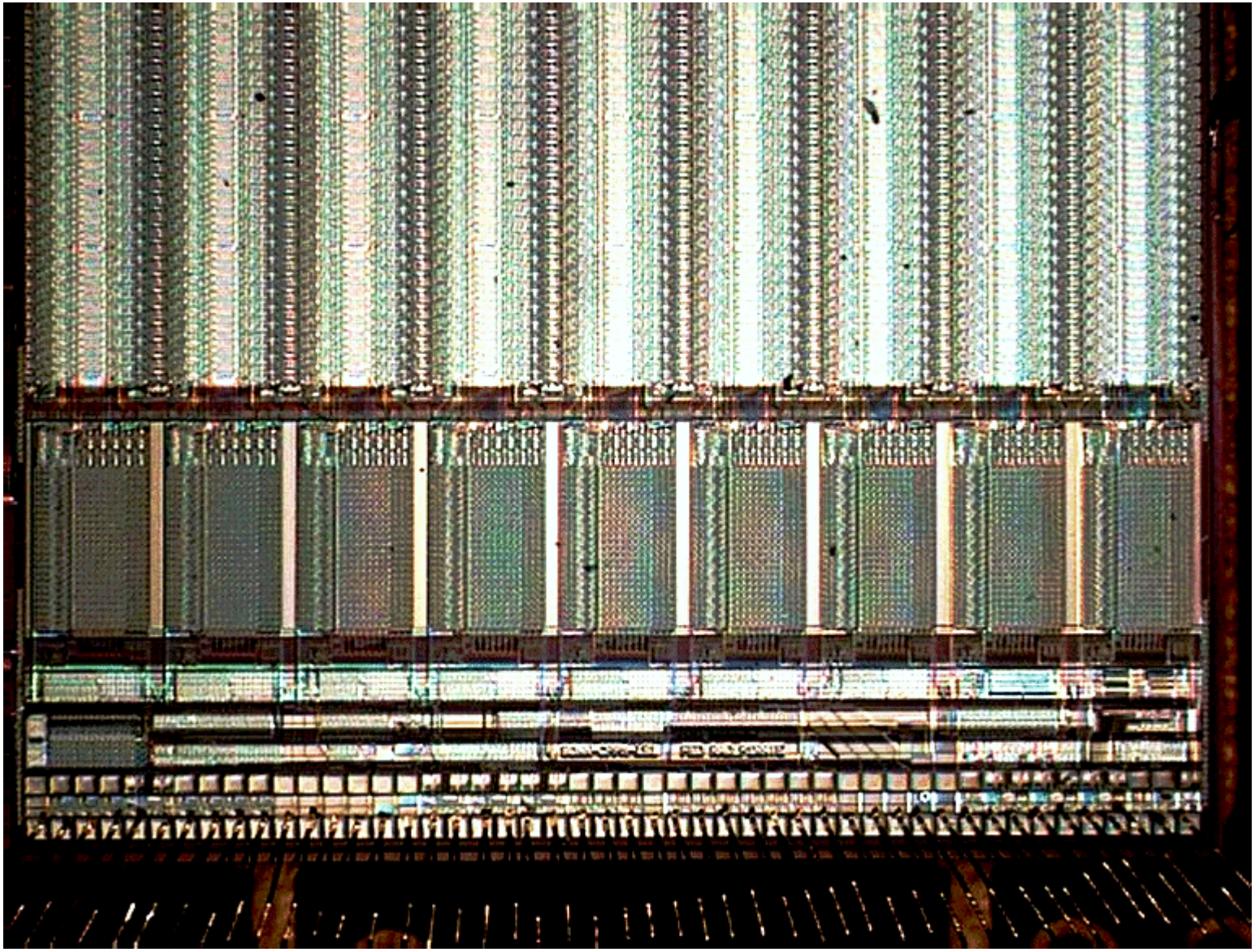
- **ATMEL/DMILL:** Began first work on FE-D in Summer of 98. FE-D1 run was submitted to TEMIC on Aug 10 99. Design contained some “simplifications” in digital readout from FE-B design to fit into DMILL constraints, as well as some improvements. Performance targeted at outer layers, with 400μ pixel and 24 EOC buffers per column pair.
- Comments: Initial version of front-end chip (FE-D1) showed very poor yield, concentrated in two circuit blocks. Second set of wafers for initial run were processed (FE-D1b), and showed same behavior. Extensive testing pointed towards technology problems. Second run was made, with two versions and many minor bug fixes (FE-D2). Will summarize these results.
- **Honeywell/SOI:** Began serious work on FE-H in Fall 99. At this time, only LBL and CERN had TAA agreements in place to do design. In addition, Honeywell was in process of revising Layout Rules, which caused significant delays. A number of minor improvements relative to FE-D, taking advantage of better device density and third metal layer. Design was made more robust, and performance was targeted at B-layer as well (400μ pixel with 32 EOC buffers).
- Comments: Had completed almost all layout work and were just starting verification in July 00, when we learned of cost increase to $20K$/wafer in large quantities. This made continued work impractical, and this path was abandoned.

Summary of FE-D1 DMILL Run

Reticle included many die (10 in total):

- Two pixel FE chips (FE-D). Several errors were found and reproduced in simulation. Two significant yield problems are believed to originate in TEMIC fabrication problems, and made operation of the chips very difficult.
- Prototype MCC chip. A prototype of several key elements of final MCC, about 20mm^2 core size. Included FIFO block for final chip, plus large synthesized command decoder block. Observed yield of about 80% for small die. Irradiations of 8 packaged die to 30MRad carried out at PS in Oct 00. All die survived irradiation, but many no longer function correctly after several months. Problems under investigation.
- Prototype CMOS opto-link chips (one DORIC-p and three VDC-p). Results discussed previously.
- Additional test chips: LVDS buffer for rad-hard test board, PM bar with W/L arrays and special pixel transistors, Analog Test chip with all critical FE-D analog elements. All work well, and transistor parameter measurements suggest run is slightly faster than typical. Many detailed characterizations of Analog Test Chip.
- Second half-lot (FE-D1b) processed several months later with minor metal layer changes, and observed same poor yield results for FE-D chips.

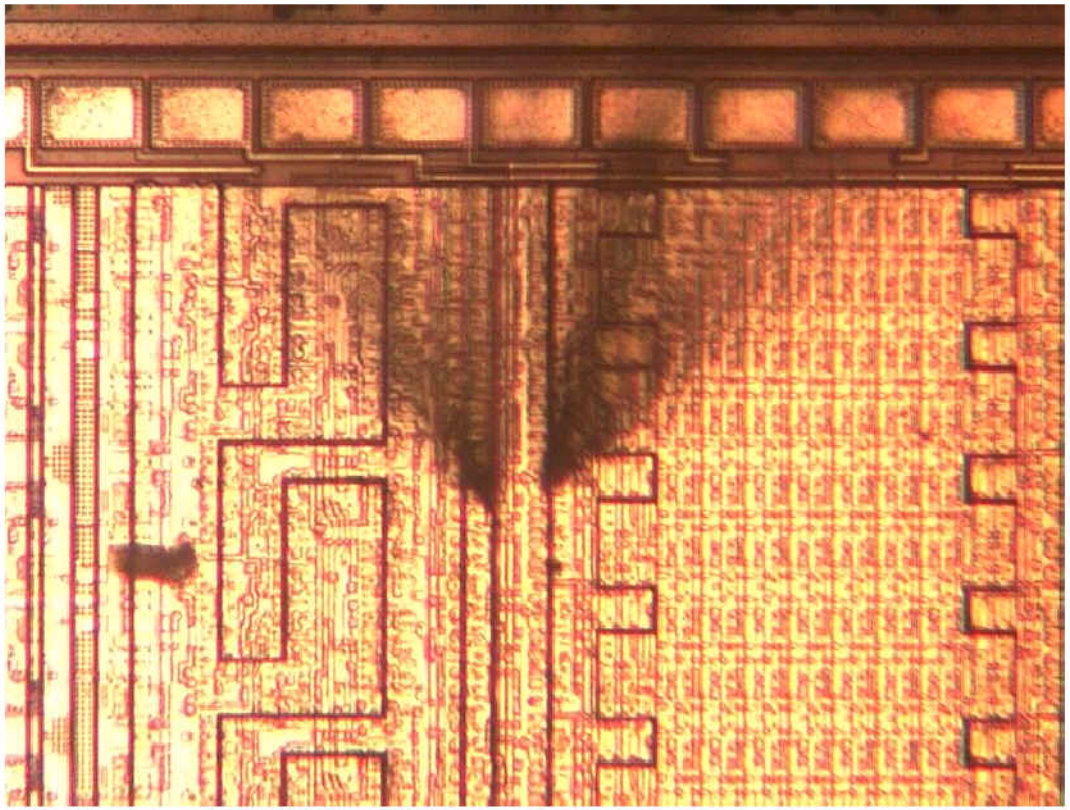
Details of Bottom of Chip:



- Layout is very dense, with 400μ pixel and overall die completely full of circuitry.

Example of Defect Analysis in Yield Studies

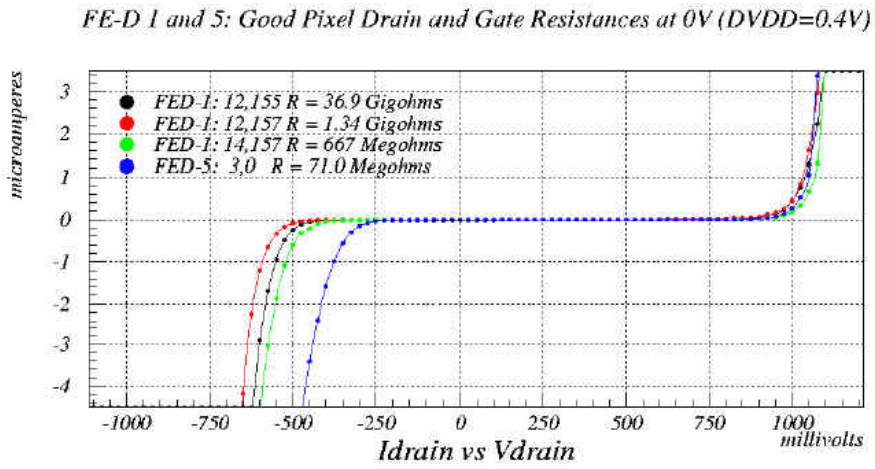
- Two chips which had been characterized in the lab had series of 20 small (8μx8μ) pads deposited by FIB surgery to allow probing of suspect “leaky NMOS”.
- Measurements were made of DC performance of the suspect device (somewhat complex to interpret since they are done in situ), as well as the dynamic performance (using an FET Picoprobe) of waveforms during operation.

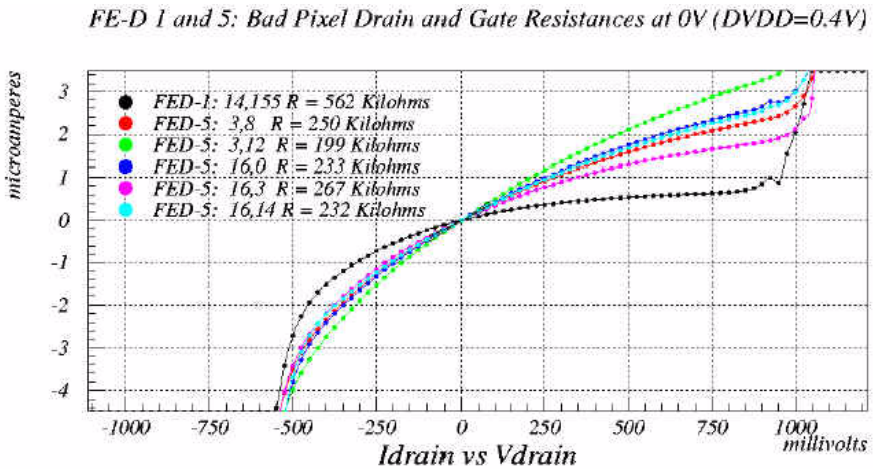


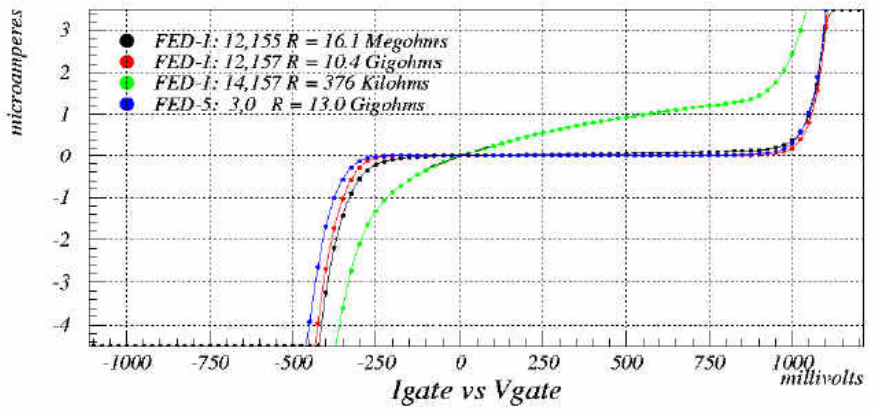
- Two 10μ probe needles place on pads. One pad was on the drain, the second on the gate of the suspect NMOS.

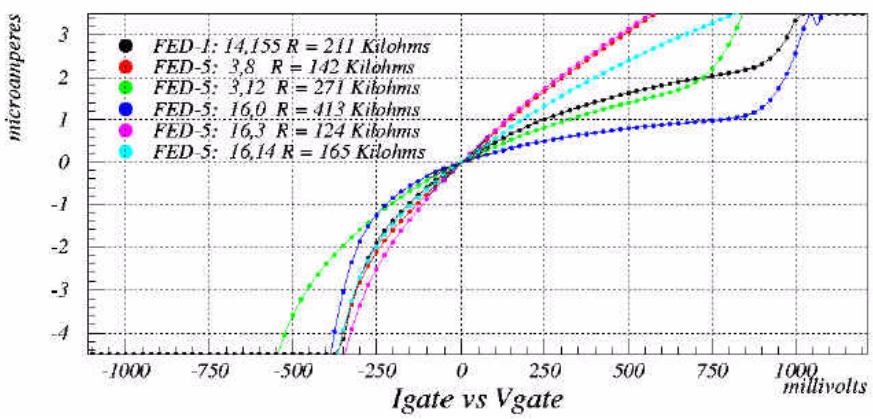
- Both DC and dynamic measurments confirm existence of defective NMOS’s.

DC curves for pixels previously classified good/bad:



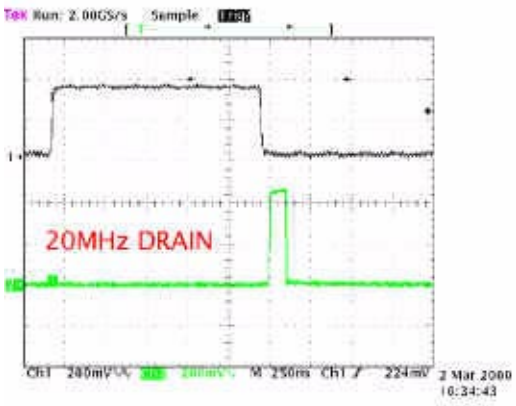


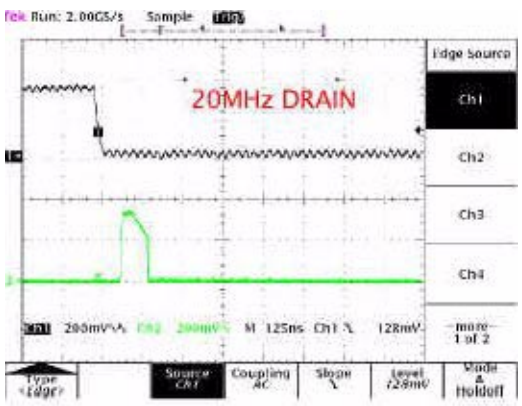


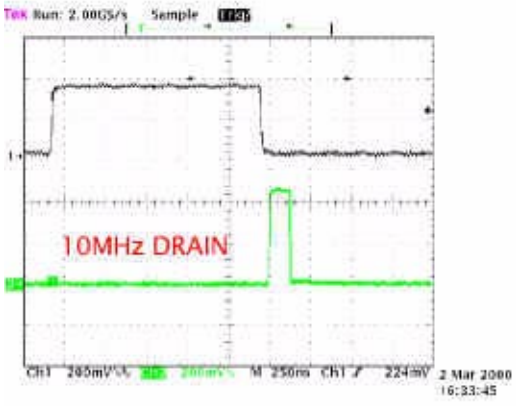


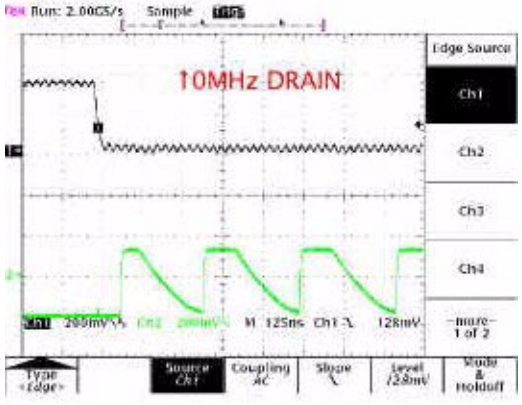
- Bad pixels consistently show apparent drain-source resistance in off state of a few 100's of KOhms. Good pixels show resistance of many orders of magnitude larger, with actual value most likely limited by Tungsten residue after FIB pad deposition.

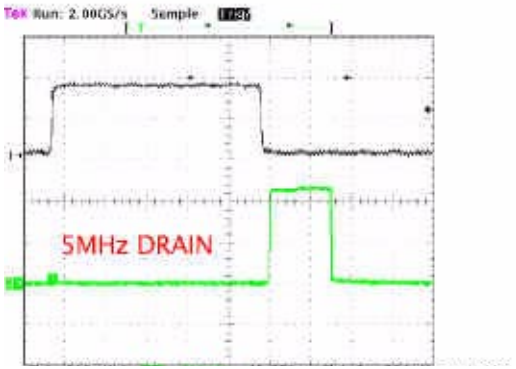
Dynamic measurements of a good and a bad pixel:

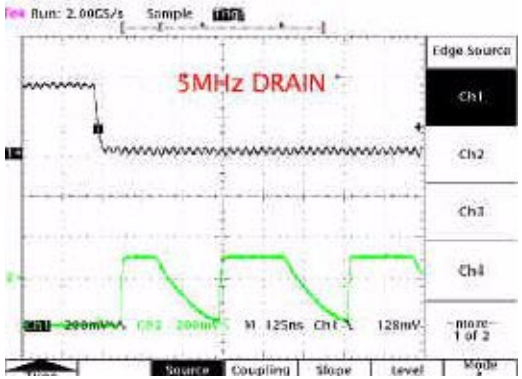








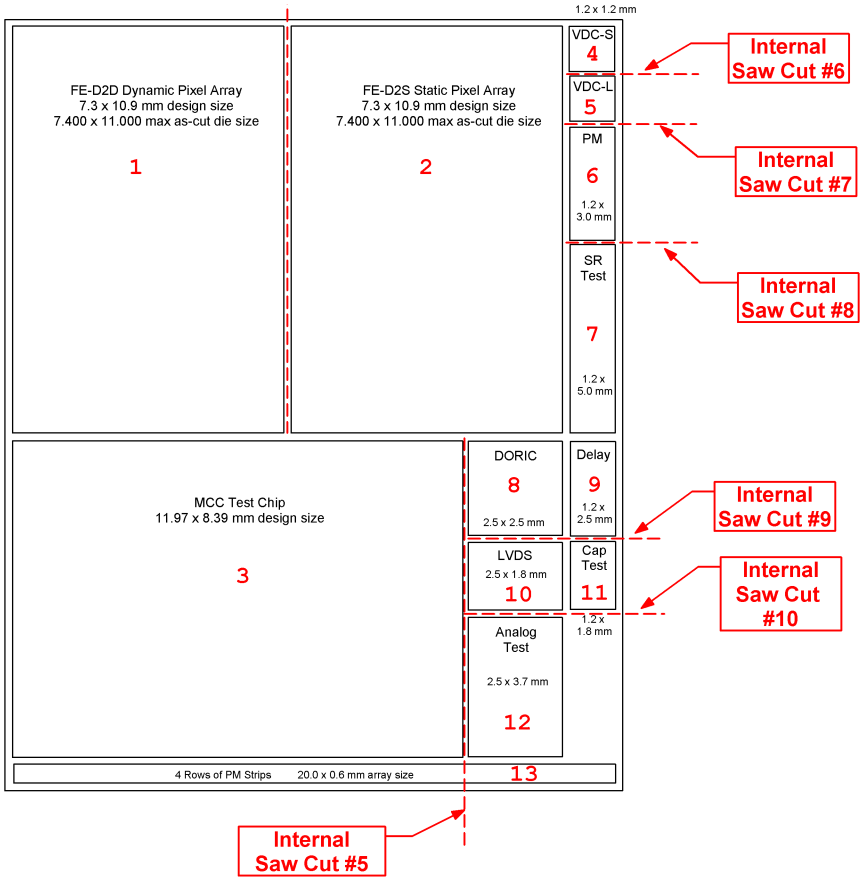




- Measurements of the state of the dynamic node (green trace) were made directly using FET probe (20fF load capacitance).
- Good pixels show stable logic high value over relevant timescale.
- Exponential slope for bad pixel corresponds to dynamic phase when logic value is “leaking” away.
- Depending on clock frequency for column readout, it is possible to produce a “digital oscillation”

Summary of FE-D2 Run

- Submitted second run to ATMEL for fabrication July 26 00. ATMEL agreed to fabricate a standard prototype run (8 wafers delivered), plus a special collection of 9 corner runs where three separate parameters were varied (Leff, poly etch, and contact etch). The goal was to look at yield correlations to understand the technology problems observed in the FE-D1 run.



- Run included two versions of the FE chip. One with same design but all known errors fixed (FE-D2D), and one with the two low-yield dynamic blocks (Hit Logic and Pixel Register) replaced with static versions but with threshold trim circuitry removed (FE-D2S).
- Included MCC-D2 as a complete design addressing the final pixel system needs. Also included second generation opto-chips, and several test chips.

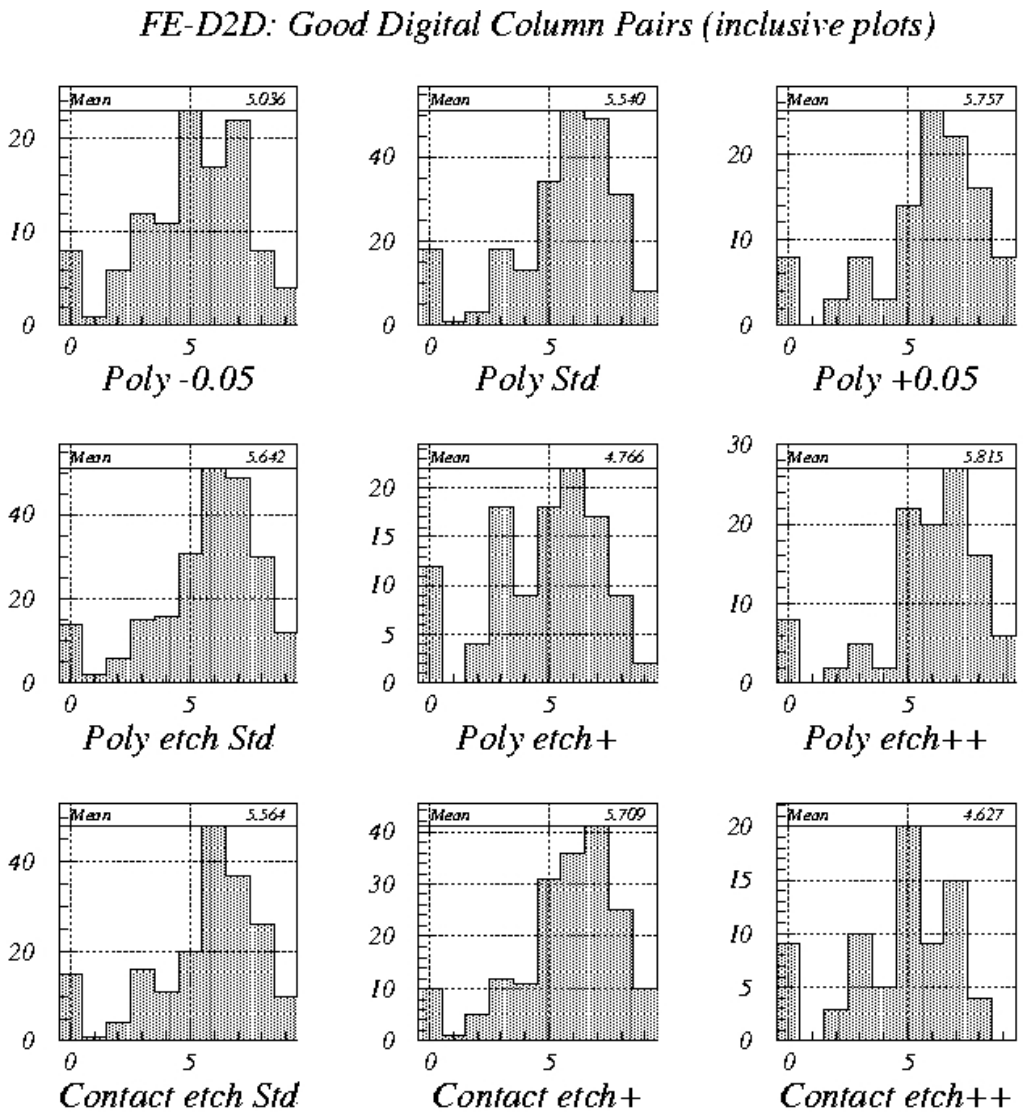
Results from FE-D2 Run

- Yield for original design (FE-D2D) was similar to the FE-D1 run, and still unacceptable:

FE-D2D (DYNAMIC IMPLEMENTATION) STANDARD WAFERS							
	GLOBAL REGISTER	PIXEL REGISTER		GOOD COLUMN PAIRS		PERFECT COLUMN PAIRS	
WAFER	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*
03	39/39 100%	334/351 95%	30/39 77%	155/334 45%	0/30 0%	47/334 14%	0/30 0%
04	38/39 97%	337/342 99%	33/38 87%	204/337 61%	0/33 0%	47/337 14%	0/33 0%
05	41/42 98%	348/369 94%	22/41 54%	154/348 44%	0/22 0%	66/348 19%	0/22 0%
06	41/42 98%	310/369 84%	27/41 66%	169/310 55%	0/27 0%	71/310 23%	0/27 0%
07	41/42 98%	329/369 89%	26/41 63%	161/329 49%	1/26 4%	57/329 17%	0/26 0%
08	41/42 98%	324/369 88%	25/41 61%	183/324 57%	0/25 0%	69/324 21%	0/25 0%
09	42/42 100%	348/378 92%	30/42 71%	200/348 57%	0/30 0%	75/348 22%	0/30 0%
10	33/42 79%	241/297 81%	16/33 48%	118/241 49%	0/16 0%	32/241 13%	0/16 0%

- Minimal digital test criteria are working Global and Pixel Register and nine Good Columnpairs. Only one chip in 8 wafers satisified these requirements !

- Comparison of yield distribution for each corner run parameter value does not show any correlation with the processing variations tried by ATMEL:



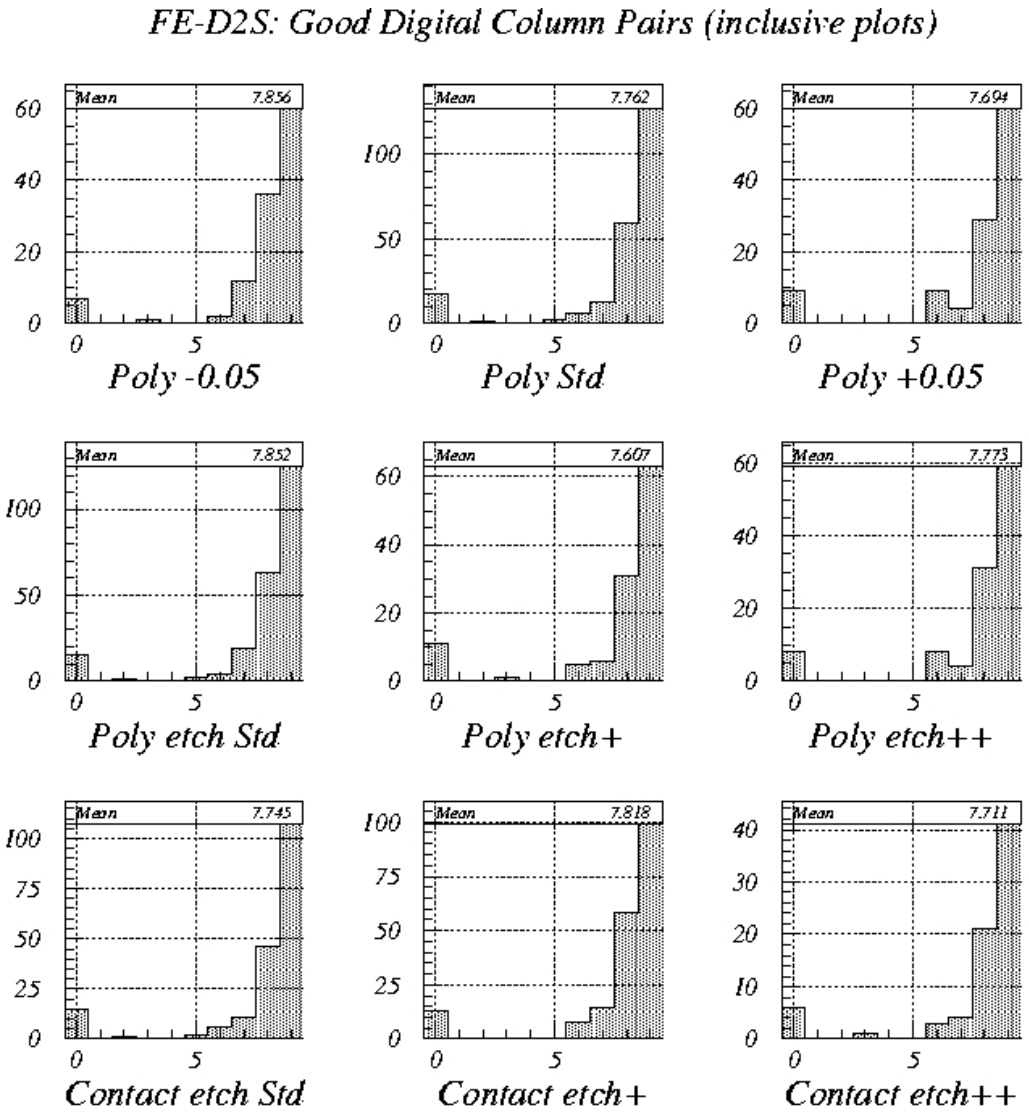
- Corner runs included 8 corners with 2 wafers each plus standard set with 6 wafers. We received a subset of 16 of these 22 wafers for evaluation.
- Bin data according to particular value for each of the three parameters (actual runs varied more than one parameter in some cases).
- No combination observed with improved yield.

- Yield for FE-D2S design looked much more promising:

FE-D2S (STATIC IMPLEMENTATION) STANDARD WAFERS								
	GLOBAL REGISTER	PIXEL REGISTER		GOOD COLUMN PAIRS		PERFECT COLUMN PAIRS		MEAN BAD PIXELS
WAFER	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER CP*	*PER CHIP*	*PER GOOD CHIP*
03	40/40 100%	349/360 97%	34/40 85%	299/349 86%	18/34 53%	244/349 70%	3/34 9%	101/18 = 5.6
04	40/40 100%	356/360 99%	37/40 93%	319/356 90%	23/37 62%	282/356 79%	12/37 32%	33/23 = 1.4
05	40/40 100%	355/360 99%	36/40 90%	324/355 91%	29/36 80%	279/355 79%	6/36 17%	88/29 = 3.0
06	43/43 100%	327/387 85%	29/43 67%	274/327 84%	16/29 55%	190/327 58%	2/29 7%	135/16 = 8.4
07	41/43 95%	336/369 91%	32/41 78%	284/336 85%	22/32 69%	238/336 71%	8/32 25%	49/22 = 2.2
08	41/43 95%	325/369 88%	30/41 73%	298/325 92%	21/30 70%	247/325 76%	6/30 20%	56/21 = 2.7
09	42/43 98%	371/378 98%	38/42 92%	297/371 80%	15/38 39%	235/371 63%	2/38 5%	94/15 = 6.3
10	40/43 93%	298/360 83%	26/40 65%	224/298 75%	11/26 42%	181/298 61%	1/26 4%	54/11 = 4.9

- Observe decent yield for simple digital tests (about 50%), but almost all chips had some bad pixels.

- Small correlations with corner runs were observed for Pixel Register yield and single bad pixel fraction. No other global yield correlations seen:



- FE-D2S chips looked sufficiently promising that decided to pursue a complete evaluation program for them.
- Large threshold dispersion with no TDACs makes operation and characterization of the chips more challenging.

Status of Rad-Hard Developments in 0.8μ

Continuing to evaluate chips from FE-D2 run:

- FE-D2S wafers being bump-bonded into single-chip and 16-chip module assemblies using 6 wafers at two vendors (AMS and IZM) for further study.
- FE-D2S single die have been irradiated recently at LBL 88" Cyclotron. First results show some circuit elements survive to 50MRad, and others do not:

FE-D2S being tested at 88" Cyclotron using N_2 coldbox to irradiate at about -5 C.

- Irradiations taking place using opto-chips (VDC-D2 and DORIC-D2) in the April PS run. Further irradiations of FE-D2S could be performed at the PS in May, and irradiations of MCC-D2 could be performed in July.
- Further testing of MCC-D2 continuing. However, low yield (less than 10%) makes the testing difficult. Problems in event building still being studied.
- ATMEL presently running new experimental lots using different epi deposition vendor for wafer preparation. Should get wafers for evaluation in late May.

Factors driving us to suspend design work on FE-D/MCC-D:

- Design short-cuts required to fit into available space. Process density lower than expected, dynamic logic used in several blocks poses SEU and yield problems.
- Experience with yield and technology quality. Even for FE-D2S, observe significant number of isolated defects (bad channels, both digital and analog).
- Problems with radiation hardness for our application. Device parameter shifts very large, and often seem to observe “mysterious” circuit failures in large chips.
- Relatively high cost (given low and erratic yields) and lack of future for process.
- Honeywell SOI work suspended as of July 2000 due to large cost increases.

Present direction:

- All design effort is being directed to the use of commercial 0.25μ processes with radiation tolerant layout rules.

Deep Sub-micron Approach:

- One of dominant effects of irradiation of CMOS devices is creation of trapped charge in the critical gate oxide layers. Below about 10nm oxide thickness, the charge trapping largely vanishes due to quantum tunneling effects. Modern 0.25μ processes are the first to operate fully in this regime (they have 5-6nm oxides).
- The RD-49 collaboration has studied details, confirming that if one controls leakage paths using layout, then a commercial 0.25μ process can be very rad-hard (circuits tested to 30MRad). Many technical concerns addressed, but basically little experience with full-scale devices, so some concerns still remain.
- All experience so far with analog and digital designs suggests that the silicon behaves almost exactly like the SPICE BSIM3 simulations. Nevertheless, given our lack of experience with these processes, we are making several prototypes.
- CERN has negotiated a frame contract for LHC with IBM for their CMOS6 0.25μ process which extends through 2004. This fixes prices and terms for engineering and production runs, and would provide the basis for our production procurement. We can also access the TSMC 0.25μ process in production quantities via the MOSIS consortium as a back-up should problems arise.
- This path places us into commercial mainstream, where we can be assured of low prices and availability in the future. Depending on R&D in 0.18μ and smaller feature sizes, it provides a technology path for upgrades to the B-layer. By 2005, roadmaps suggest “baseline” process would be 0.10μ 9-metal, operating at 1.0V.

Test System for FE Chips and Modules

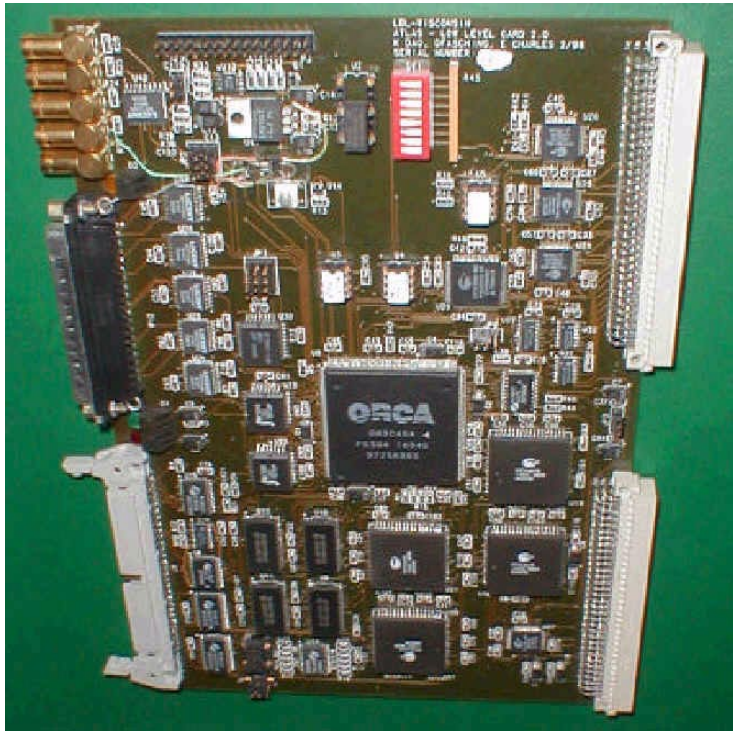
History:

- LBL/Wisconsin developed original test system in 97/98 for use with initial rad-soft pixel “demonstrator” prototypes.
- This system has been successfully used for wafer probing, and characterizing single chips and modules in the lab and in the testbeam.
- A total of 16 such systems are presently in use throughout the pixel collaboration. They are the standard with which all chips and modules are evaluated.
- The use of a common, high-performance test system for this full range of activities has allowed greater efficiency and easier comparison of results.

Overview:

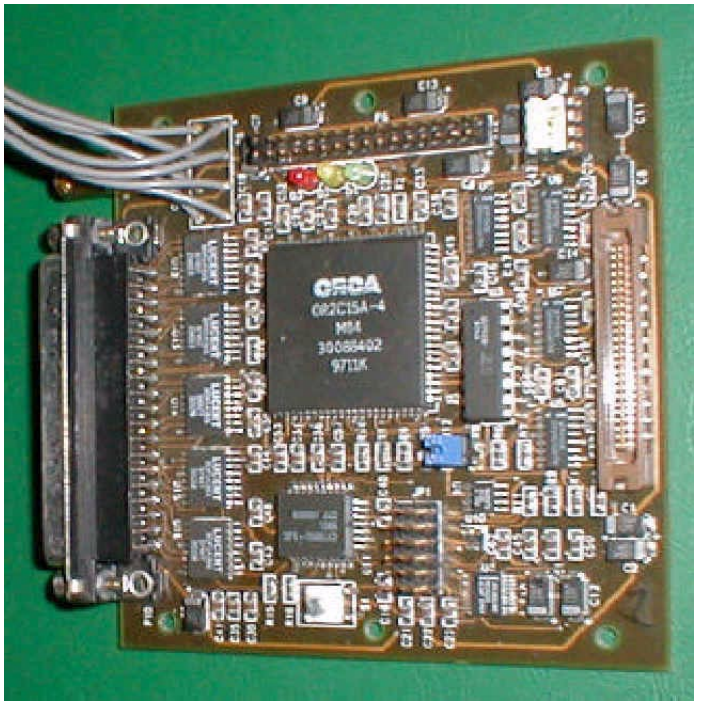
- The system consists of a PC host running National Instruments software environment and one or more VME boards (so-called PLL).
- Each VME board drives a local control card (PCC) over a long cable (20m), which in turn drives the individual test cards (support cards) over a short cable (1m).
- There are now several generations of test cards supporting the different applications from wafer probing to single chip testing to bare module testing and the first two generations of Flex modules.

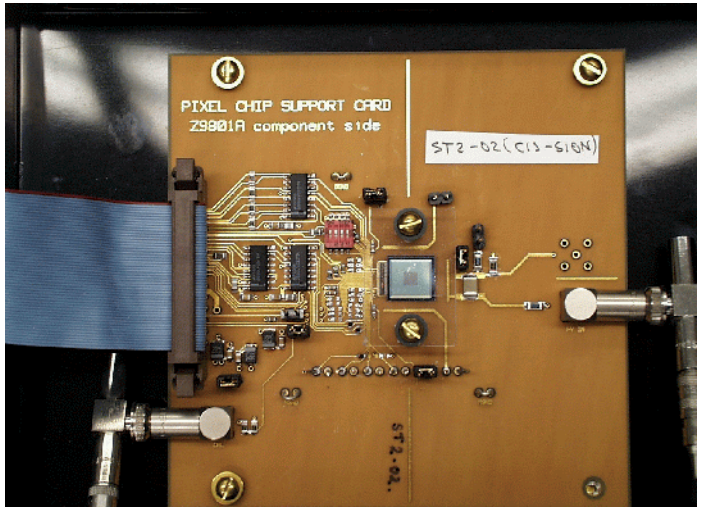
Components of Current Test System:

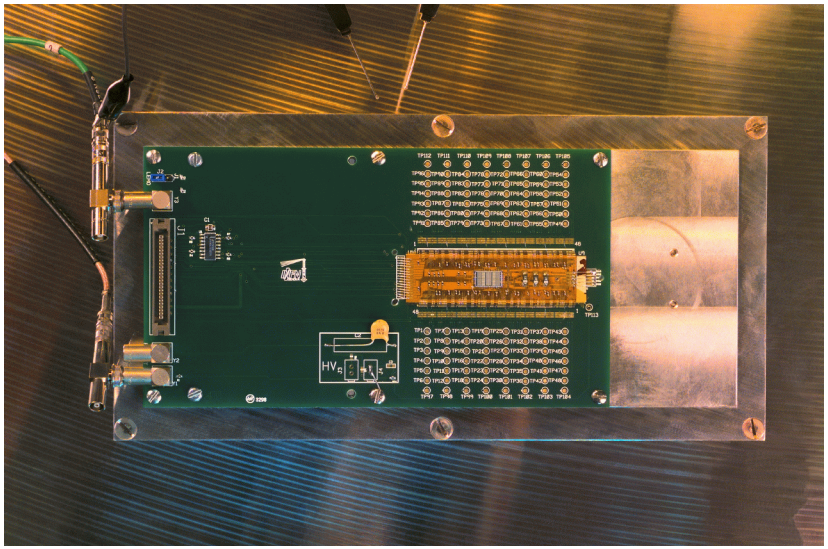


PLL

PCC





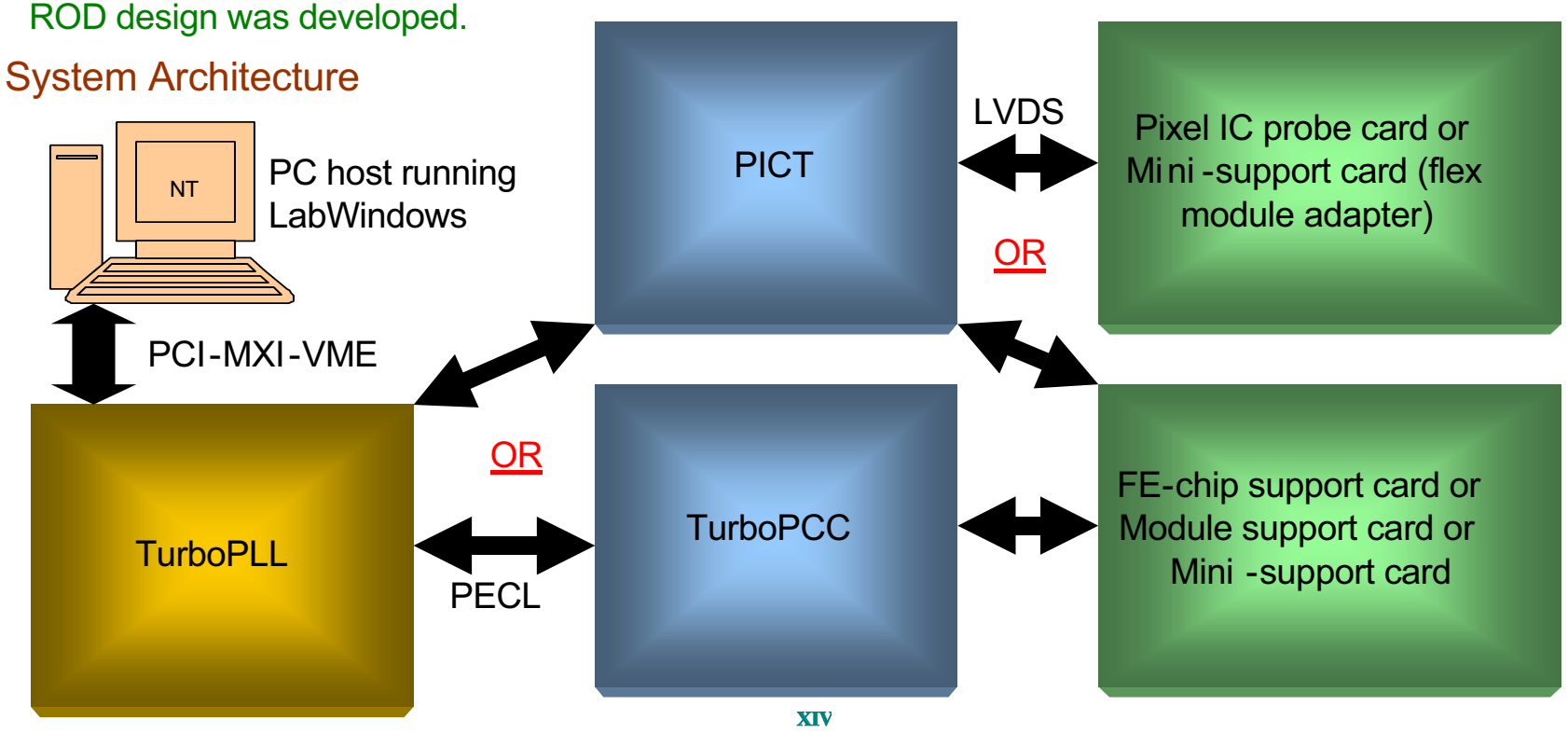


Upgraded Test System

- New generation under design. Incorporate experience with present system, and optimize to cover complete range of production needs with one modular set of hardware and software, keeping same basic interfaces to provide flexibility.
- Includes upgrades for greater range of test capability (vary amplitudes and timing), plus optimized buffering and variable frequency testing:

Architecture is directly based upon the original PLL approach, which had proven so ideally tailored to our needs and which represents the model upon which the ATLAS ROD design was developed.

System Architecture



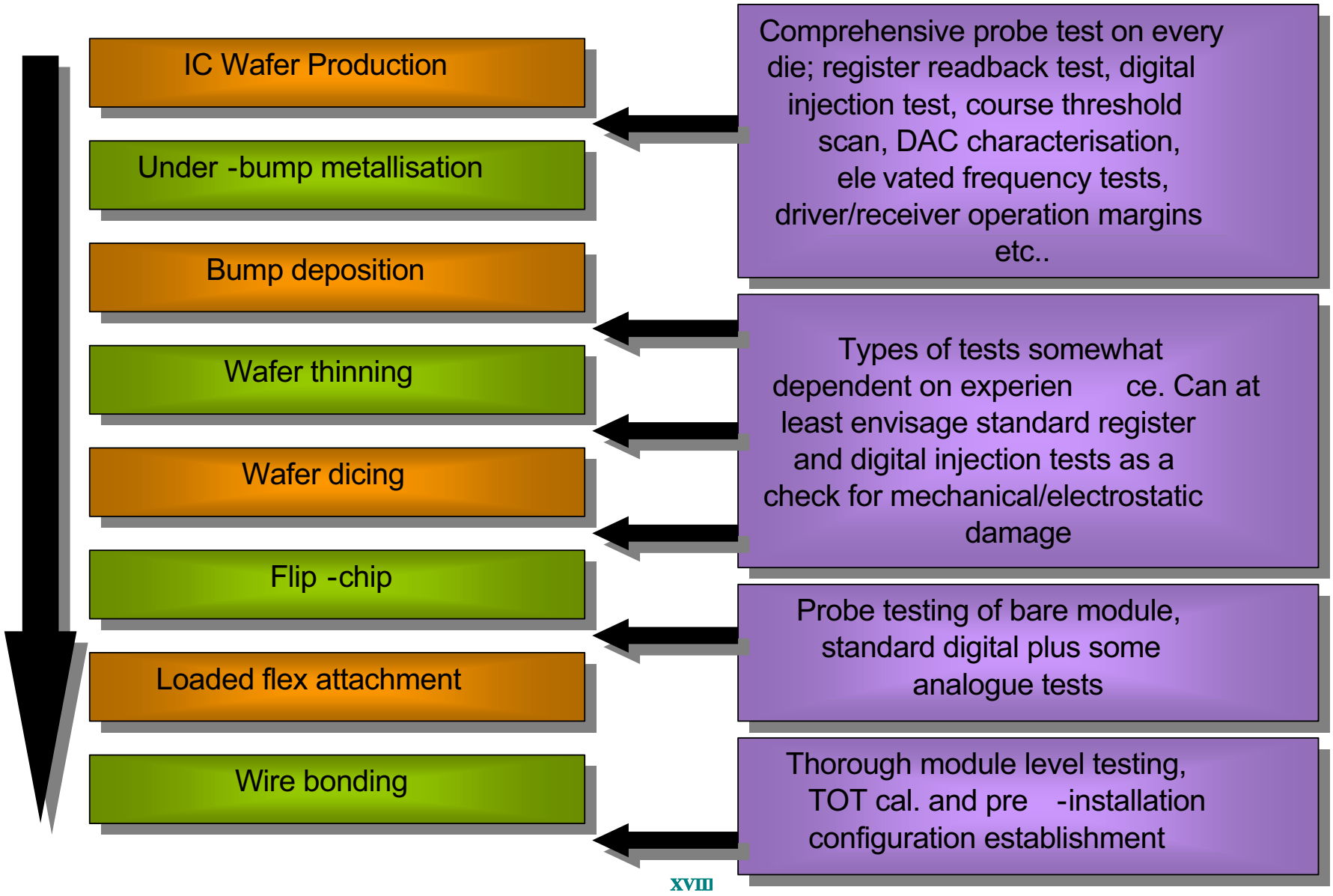
Design Goals:

- New system allows complete evaluation of operating margin available in each chip. Optimized cuts can then be used to select die and modules that should continue to work properly after full lifetime radiation doses.
- Cover wider range of needs, including parametric testing at all stages from initial wafer probing, to module testing, and module burn-in.
- System designed to allow operation over wide range of supply voltages, from a minimum of 1.6V up to 4V, to cover testing of 0.8µ and 0.25µ (and below) chips.
- New system will be operating in time for complete characterization of 0.25µ FE-I chips described in next talk.

Schedule:

- TurboPLL design is complete. Transfer of VHDL from previous system is complete, almost all upgrades now defined and written. Board layout is complete, but optimizing routing of critical high-speed paths. Should go out for fabrication within next month. Components purchased for first 10 cards.
- PICT/TurboPCC schematics are complete, board layout starting in April. Most components in hand for initial construction of 5 PICT cards.
- Higher performance probe card designed and simulated.
- On schedule to deliver total of 15 PLL/PCC systems and 5 PLL/PICT systems to the pixel collaboration this calendar year.

Production Testing Plans



- New system addresses range of needs from wafer probing to module burn-in.

Deliverables:

US Responsibilities include:

- FE chip design, testing and production (LBL): Contribute roughly 20% towards the common procurement of the series production. Test roughly 50% of FE ICs.
- Opto-link chip design, testing and production (OSU): Contribute approximately 50% towards the common procurement of the series production.
- Design and provide hardware/software for lab/testbeam single chip and module testing, production FE wafer probing, production module testing/burn-in (LBL).

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.3	Electronics	0	0	0	0	0	615	621	354	26	0	1616
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	446	161	0	0	989
1.1.1.3.1.1	IC design	0	0	0	0	0	189	269	11	0	0	469
1.1.1.3.1.2	Test design	0	0	0	0	0	140	75	0	0	0	216
1.1.1.3.1.3	Systems Engineering	0	0	0	0	0	52	101	151	0	0	304
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	234	133	0	0	0	367
1.1.1.3.2.1	Atmel/DMILL prototypes	0	0	0	0	0	130	0	0	0	0	130
1.1.1.3.2.2	Honeywell	0	0	0	0	0	10	0	0	0	0	10
1.1.1.3.2.3	0.25 Micron	0	0	0	0	0	0	54	0	0	0	54
1.1.1.3.2.4	Test	0	0	0	0	0	94	79	0	0	0	173
1.1.1.3.3	Production	0	0	0	0	0	0	42	193	26	0	261
1.1.1.3.3.1	Front-end ICs	0	0	0	0	0	0	19	140	26	0	185
1.1.1.3.3.2	Optoelectronics	0	0	0	0	0	0	23	53	0	0	76

Summary and Conclusions

Sensors:

- Extensive design and prototype program now complete. Prototype performance, including operation after lifetime radiation doses, is acceptable.
- Oxygenated material provides significant increase in operating margins (lifetime dose and access scenarios) and will be used for production sensors.
- Pre-production with two final vendors completed and under evaluation.
- Would be ready to proceed with production order later this year.

Opto-links:

- Second generation of opto-chips in DMILL are working relatively well. System-level evaluations will continue using complete opto-card with 6 opto-links.
- Improved design submitted in 0.25μ. Both DMILL and 0.25μ processes remain candidates for opto-chip production.
- Expect to select package in June 01, and proceed to finalize opto-card design.

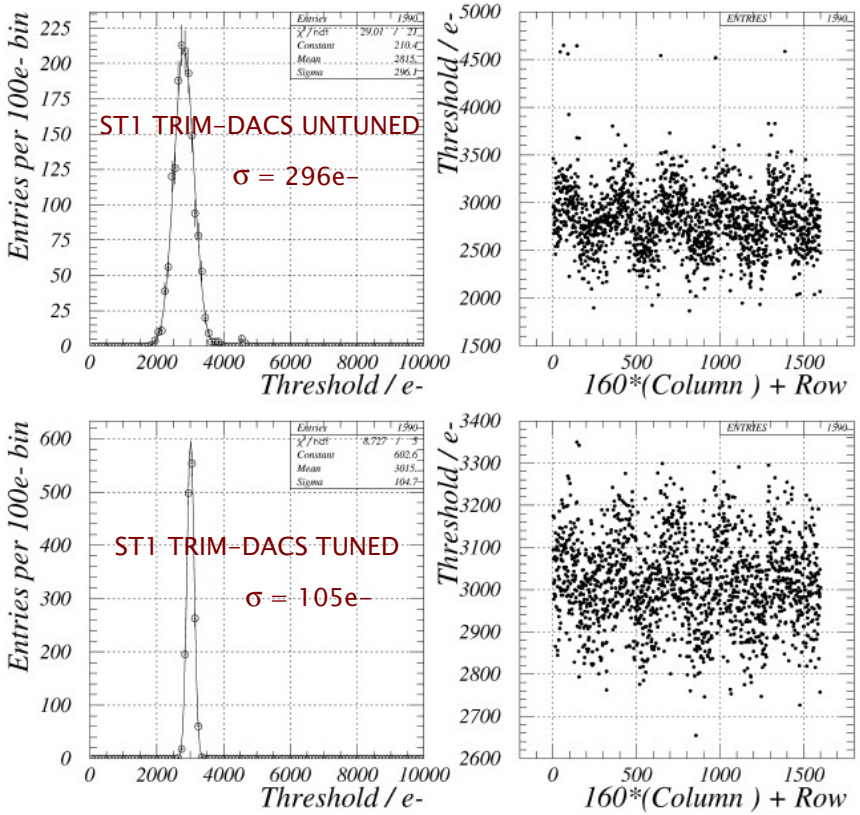
On-Detector Electronics:

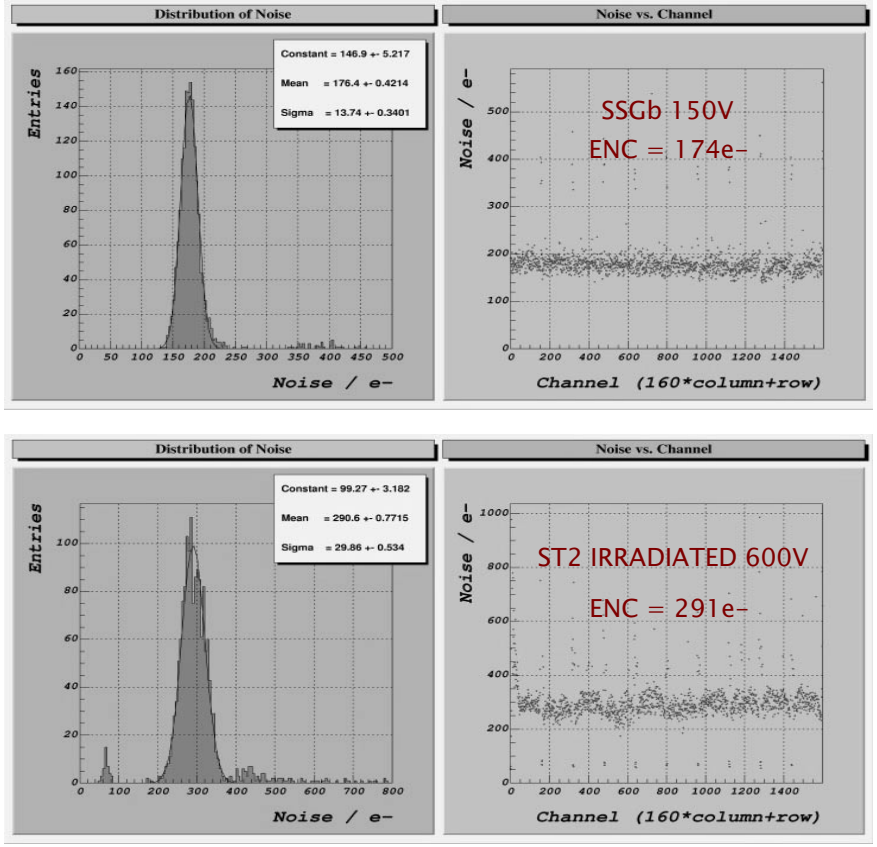
- Prototypes built using rad-soft electronics have been extensively tested in lab and testbeam, Present designs basically meet all ATLAS requirements.

- Honeywell SOI design for FE chips has been abandoned due to catastrophic cost increases from vendor.
- Transfer of FE chip design to DMILL has basically failed for technology reasons. Will continue to evaluate FE-D2S design over next months to look for generic problems and to develop and refine test methods. Have suspended all design work towards a production DMILL FE.
- Opto-chip designs in DMILL appear to be working, and are undergoing further evaluation. First prototype opto-packages and opto-cards appear to work, and intensive characterization is now beginning.
- Design of production version of test system is almost complete, and is on schedule for delivery to the collaboration by the end of this year.
- All on-detector design activity and cost/schedule definitions have now been focussed on 0.25µ versions of electronics (see next talk).

Lab Measurements using Rad-soft Prototypes

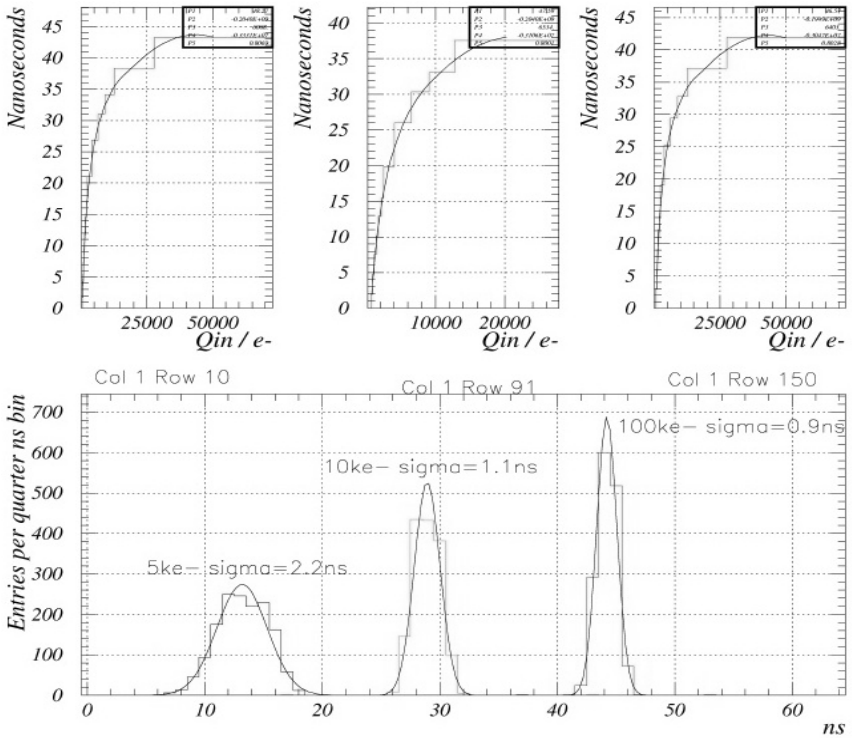
Examples of threshold and noise behavior in single chips:



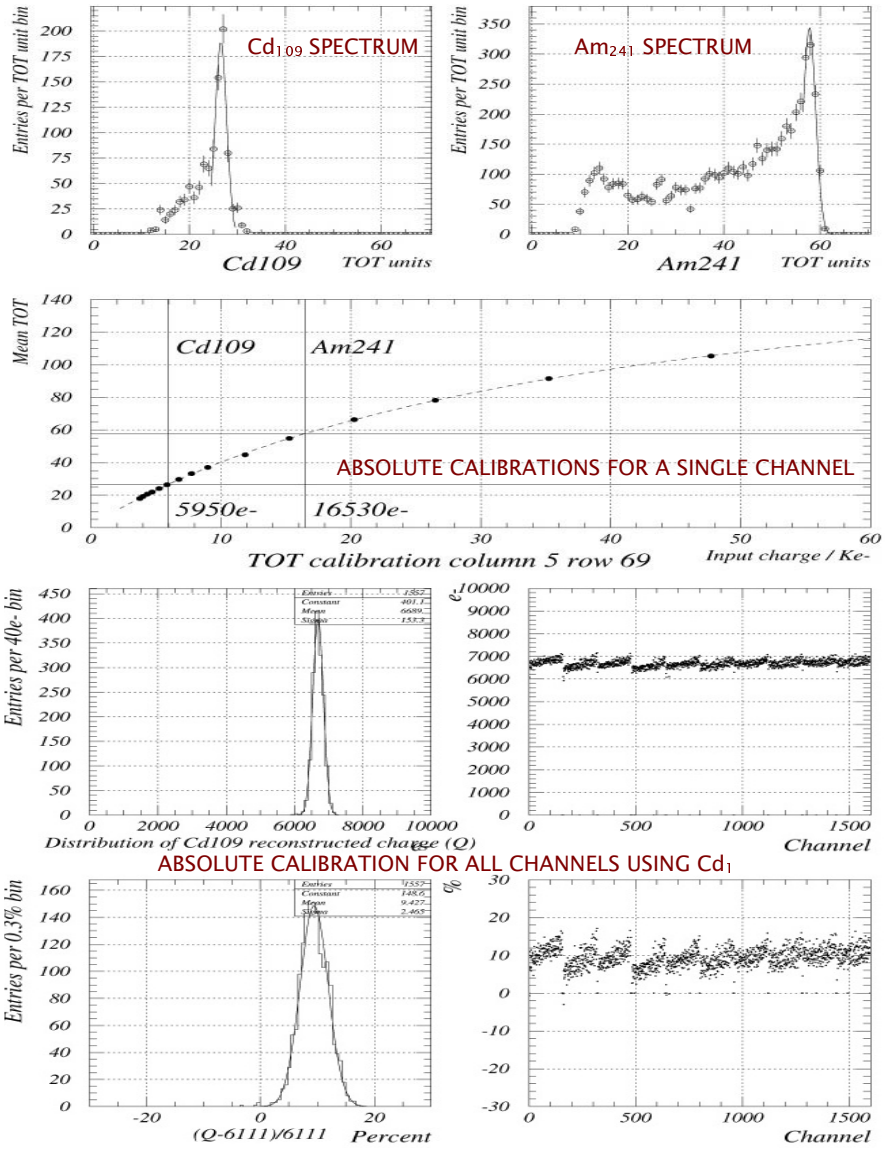


- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

Examples of timing and charge measurements:

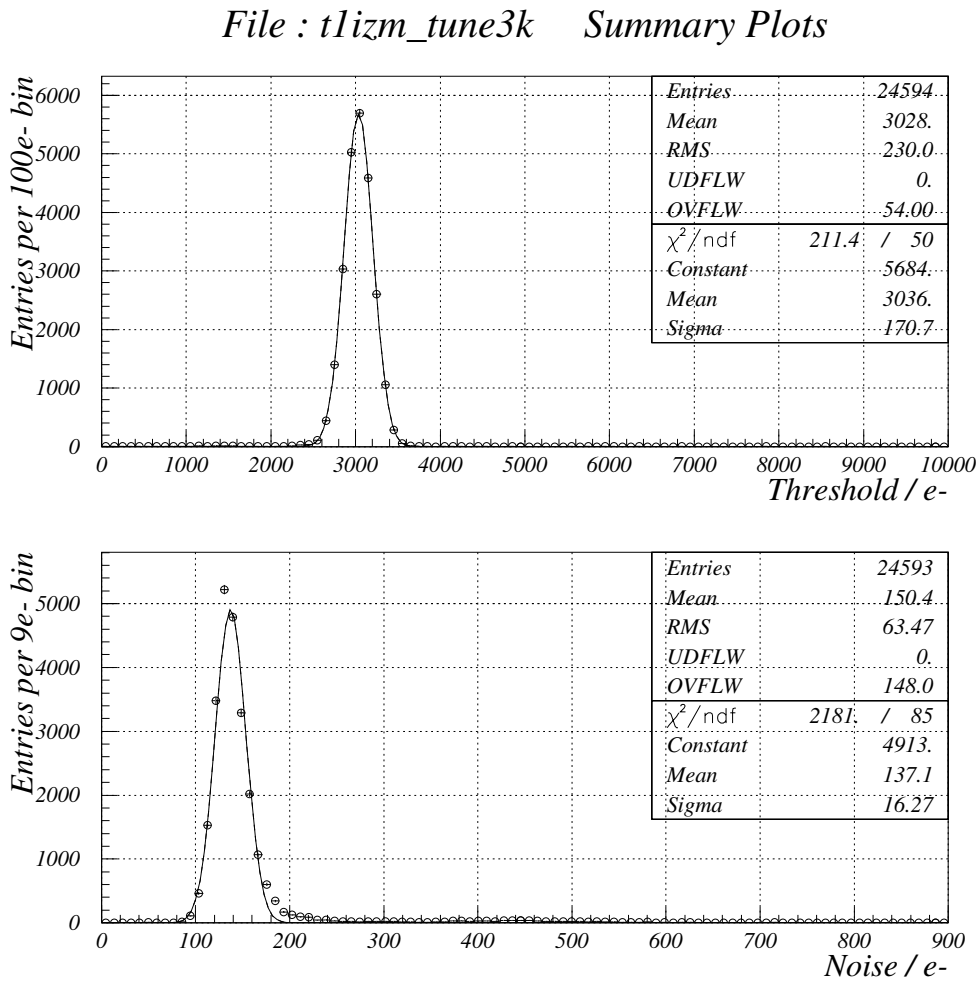


- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.



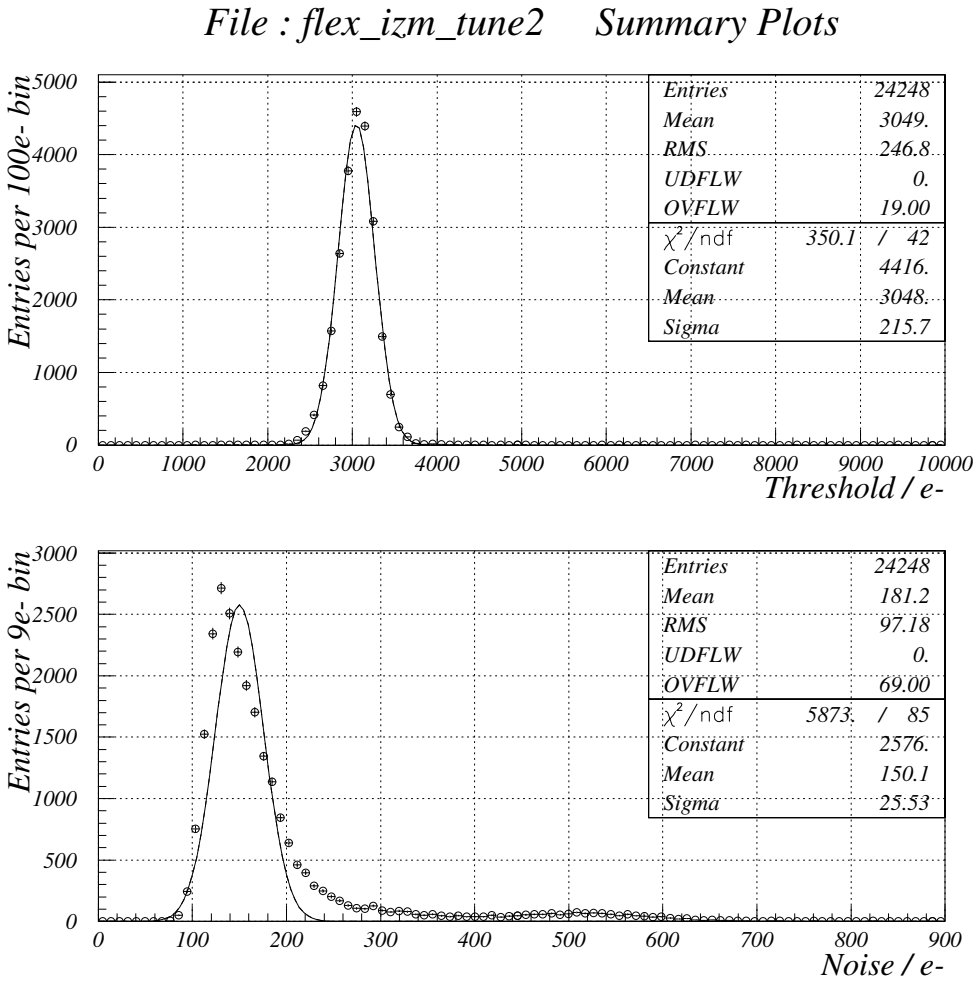
Examples of Module Results:

Bare Module (FE chips wire-bonded to PC board):



- Module has excellent threshold and noise behavior. For FE-B module should be only 16x1600 = 25600 good channels. Dead channels here are apparently all from bump-bonding problems (shorts).
- Threshold dispersion (230e) and noise (150e) for whole module are about same as for single chips.
- Module was operated in self-trigger mode at 70 KHz with excellent performance.

Performance of best Flex module is not as good:



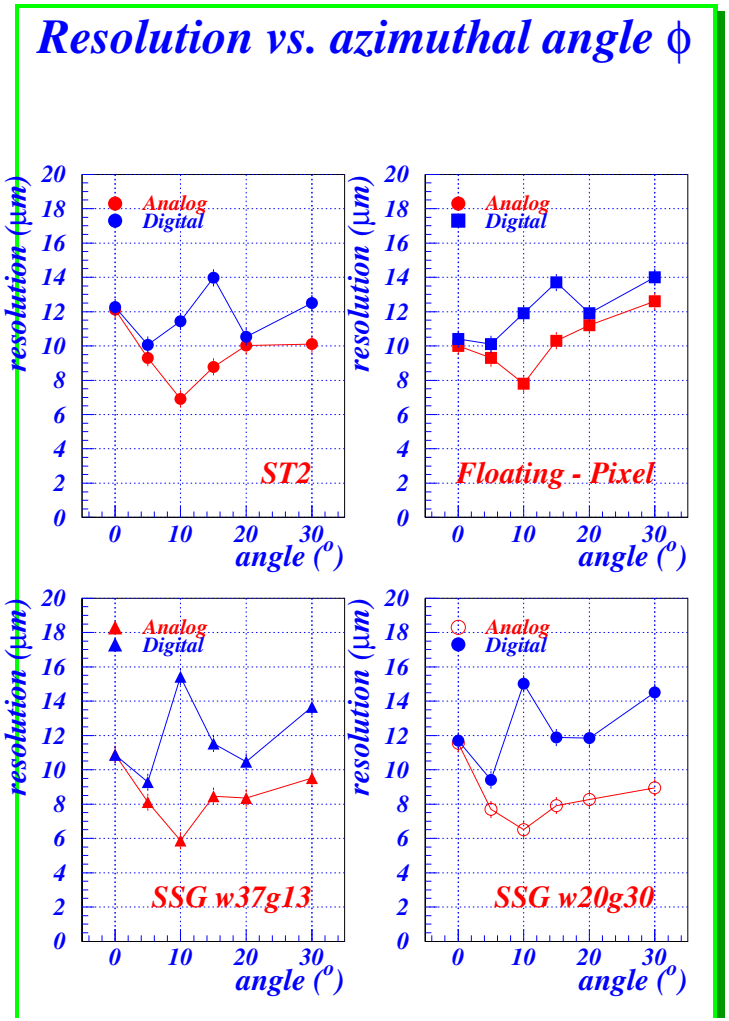
- Threshold dispersion is the same as for bare module.
- Noise distribution has a long tail. The origin of these noisy channels in this module is not clear.
- These results are from Spring 99, and have not been improved due to subsequent bumping problems with IZM which are still under study.

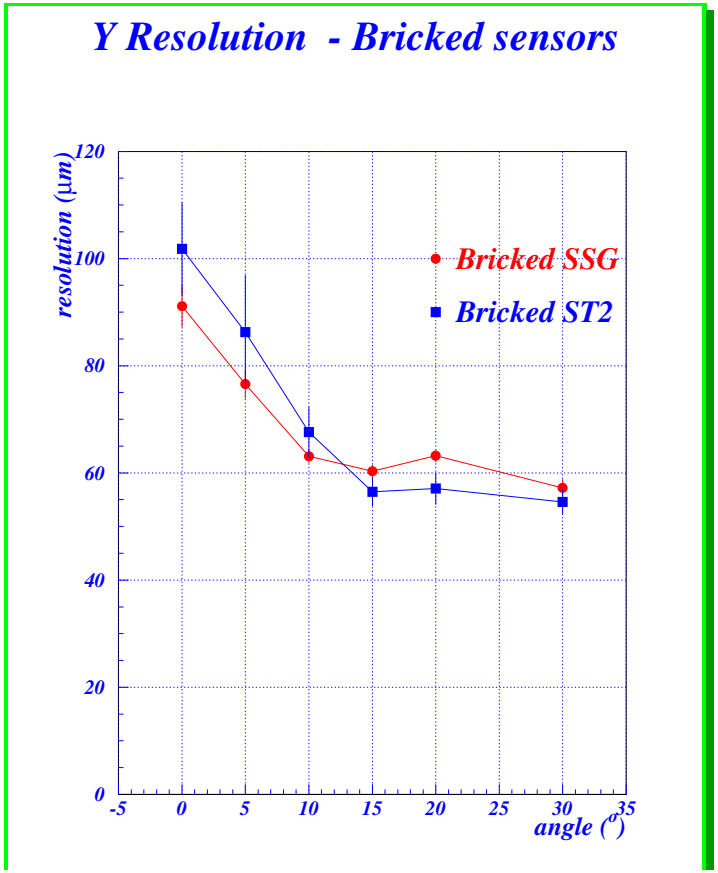
- Many impressive results from first prototype modules, but much larger statistics needed to check whether high quality modules can be built in a reproducible manner. Lab and testbeam characterization ability is now well-developed.

Sensor+Rad-soft Electronics Prototype Testbeam Results

Measure resolution versus incident track angle:

- Compare digital (binary) and analog algorithms for different sensor types, and also compare effect of "bricking" (half-pixel stagger) in long direction of pixel:



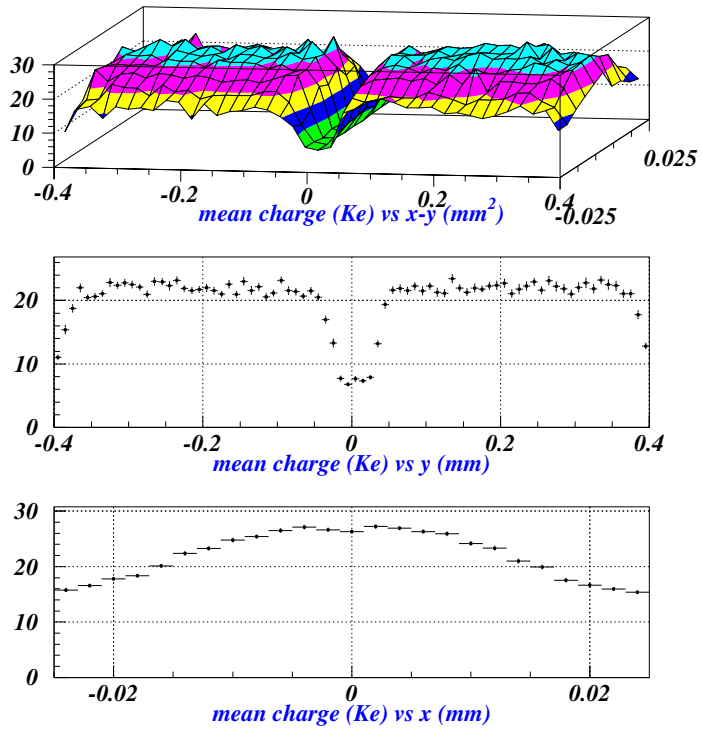


Could achieve perhaps 8-10μ in narrow and 60-80μ in wide direction for best case in barrel

Measure charge collection versus track location in pixel:

- Original n-ring design has serious charge loss problems, while new small-gap design is much better, with only small loss at bias dot location:

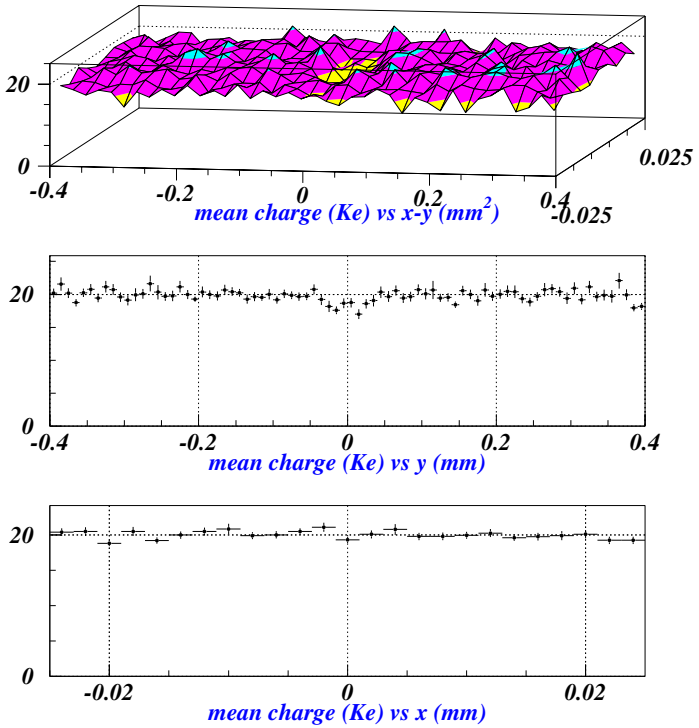
Tile 2 Design Threshold 2 Ke



large loss (0.7) near the grid
loss located ± 30 μm around the grid
losses at the pixel edges

Design 1.b:

- *p-spray insulation*
- *no floating atoll*
- *modified bias grid*



Measure efficiency as a function of track arrival time:

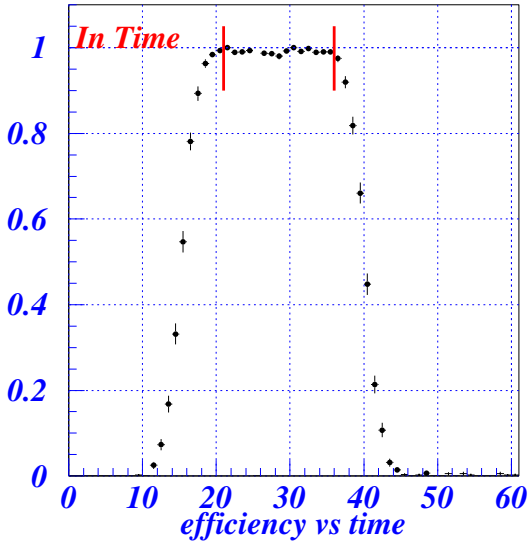
- Behavior of new design (pre-rad) is excellent, and behavior of old design (post-rad) is very good, provided that poor charge collection regions are removed:

Efficiency 'In Time'

Detector Tile 2 new design (with bias grid)

not Irradiated - Thr. 3 Ke

efficiency	*99.1*	*Losses*	*0.9*
1 hit	*81.8*	*0 hits*	*0.4*
2 hits	*15.6*	*not matched*	*0.1*
>2 hits	*1.7*	*not in time*	*0.4*

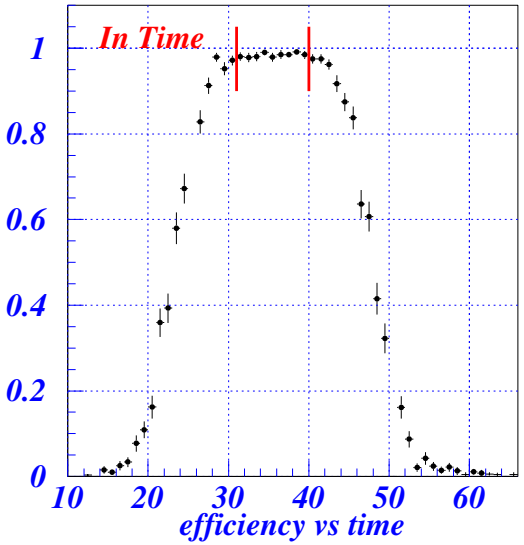


Efficiency 'In Time'

Detector Tile 2 - Irradiated V_{bias} = 600 V

Fluence 10^{15} n/cm^2 - Thr. 3 Ke

efficiency	*98.4*	*Losses*	*1.6*
1 hit	*94.2*	*0 hits*	*0.4*
2 hits	*3.1*	*not matched*	*0.0*
>2 hits	*1.1*	*not in time*	*1.2*



|xloc| < 0.01

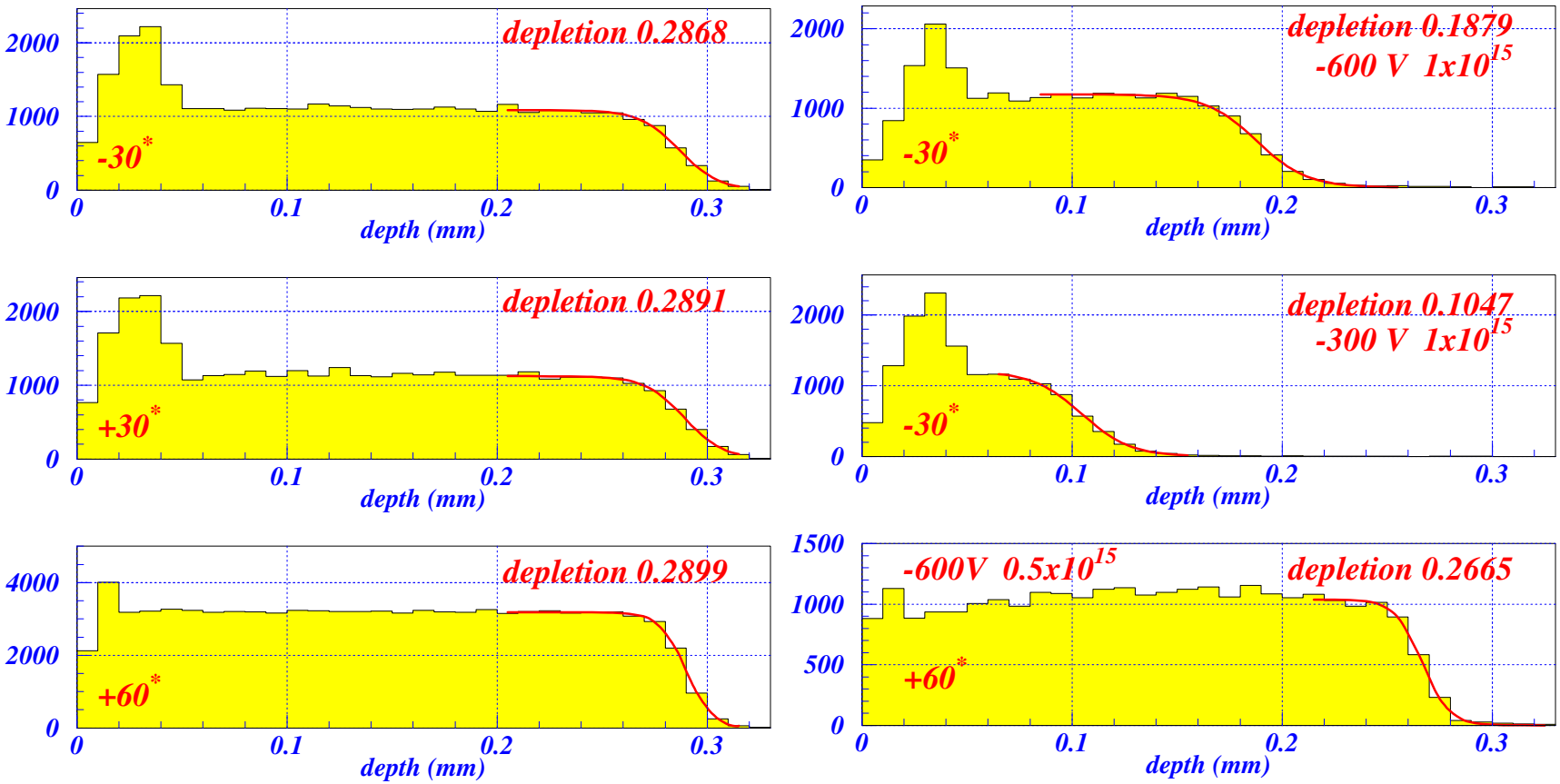
|yloc| < 0.15

Measure depletion depth in sensors:

- Look at cluster width for highly inclined tracks and use this to measure uniformity and depth of charge collection inside of sensor:

Not irradiated - depletion depth

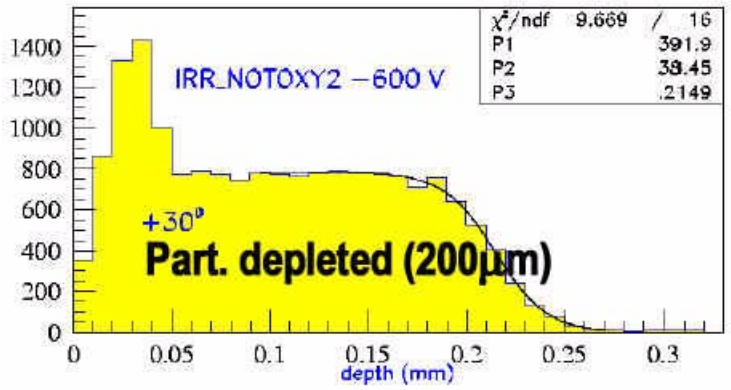
Irradiated - depletion depth



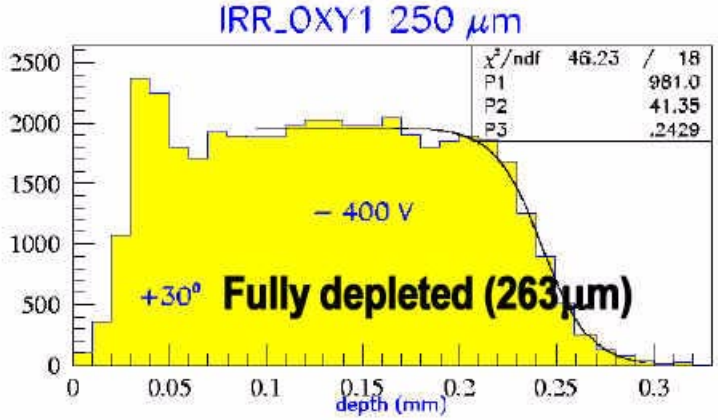
- Pre-rad result agrees with 280μ thickness. At 600V bias, lose full depletion at about half the lifetime dose, and still collect from about 180μ after lifetime dose.

Test Beam Results for Oxygenated Silicon

- First tests with irradiated single chip sensors in CERN testbeam in June 00.
- Additional tests, including single chips with full lifetime dose, completed in July 00.



Not-Oxy



Oxy

Comparison of oxygenated and non-oxygenated after 5.6 10^{14} n/equiv.

- Measure depletion depth by using tracks at large incidence angle to extract cluster length.
- Compare two sensor types after irradiation to about 6x10^{14} n-equiv. (lifetime dose for outer layers).
- As expected, get significantly better performance with oxygenated sensors, with full depletion at 400V bias, compared to partial depletion at 600V bias for standard sensor.
- More detailed analysis shows no efficiency losses or other negative effects of oxygenation.

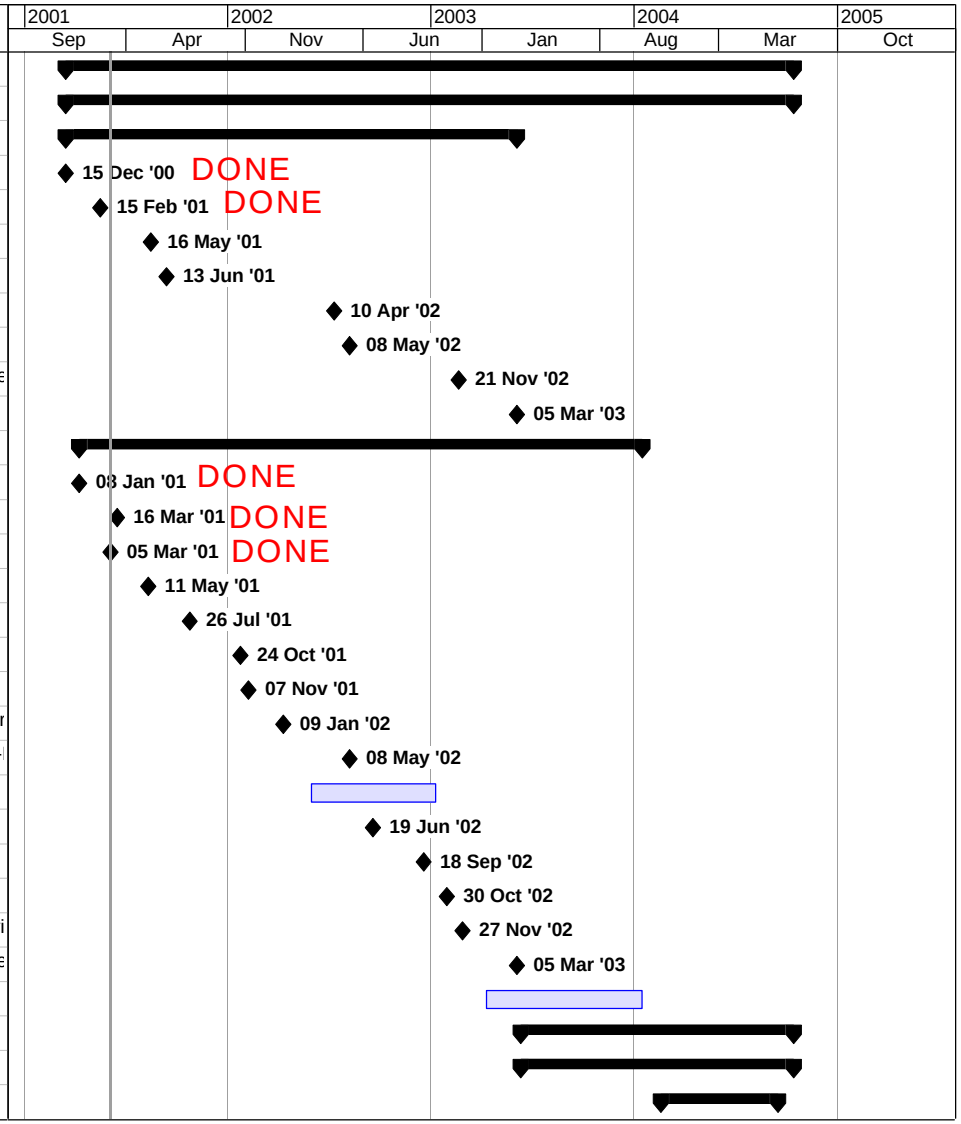
Pixel Frontend Electronics
in 0.25m CMOS

- Pixel → Radiation-tolerant CMOS design
  - CERN RD-49, FPIX for BTeV, ...
  - Smaller feature size has allowed design to become more conservative (*DMILL* design was space-constrained)

- Pixel FE-I Roadmap
  - Technology/Design developments required
  - Test chips
  - Planning and status

Plan as Presented in Pixel Baseline Review (11 '00)

ID	WBS	Task Name
1	1.1.1	**US ATLAS Pixel Project**
2	1.1.1.1	**Electronics**
3	1.1.1.3.	**Design**
4		DMILL Review
5		DMILL decision(FE-D3 or not)
6		FE-I1 spec complete
7		FE-I1 FDR
8		FE-I2 spec complete
9		FE-I2 FDR
10		Compl. Spec forIBM production order re
11		IBM FE PRR
12	1.1.1.3.	**Development/Prototypes**
13		Submit TSMC digital test chip
14		Digital test chip delivered
15		Submit TSMC analog test chip
16		Analog test chip delivered
17		1st IBM prototype submitted(FE-I1)
18		1st IBM prototype delivered
19		Complete initial wafer probe FE-I1
20		First bump bonded FE-I1 assemblies arr
21		Complete initial lab/ irradiation tests FE-
22		Beam/system tests of FE-I1 assemblies
23		2nd IBM prototype submitted(FE-I2)
24		2nd IBM prototype wafers delivered
25		Complete initial wafer probe FE-I2
26		First bump bonded FE-I2assemblies arri
27		Complete initial lab/system/ irradiation te
28		Beam/system tests of FE-I2 assemblies
29	1.1.1.3.	**Production**
30		**Outer FE Production**
35		**B-Layer FE Production**



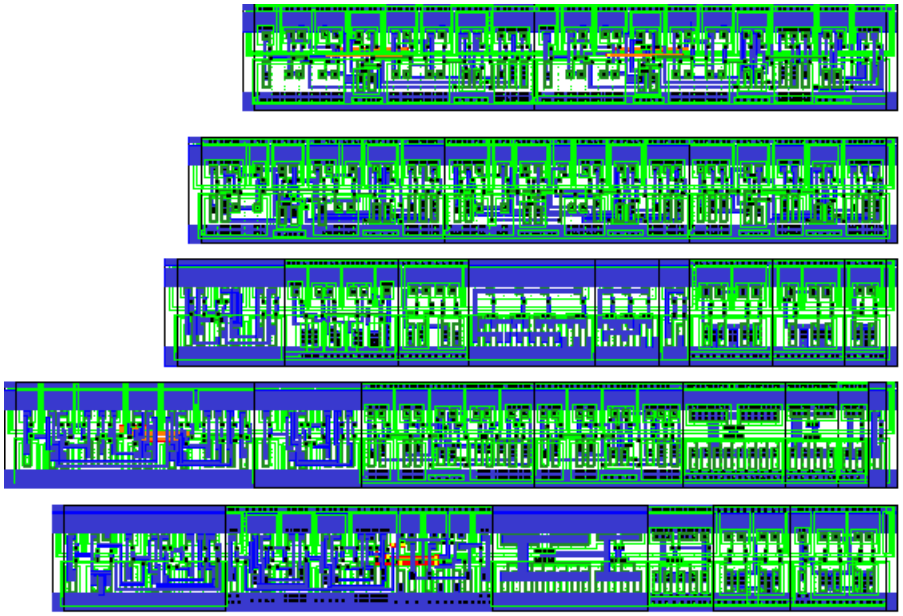
Roadmap

- Develop in two technologies
  Baseline: order via CERN frame contract, Backup: TSMC
- Insert test chip runs to cross-check (before full wafer run)
- Minimize layout time (Small feature size ⇒ extra space. Use synthesis + automated place-and-route wherever possible)
- Maximize verification time (2 000 000 transistor, mixed-mode chip)
- Submit 1st full-wafer run by end July '01

FE-I Design team

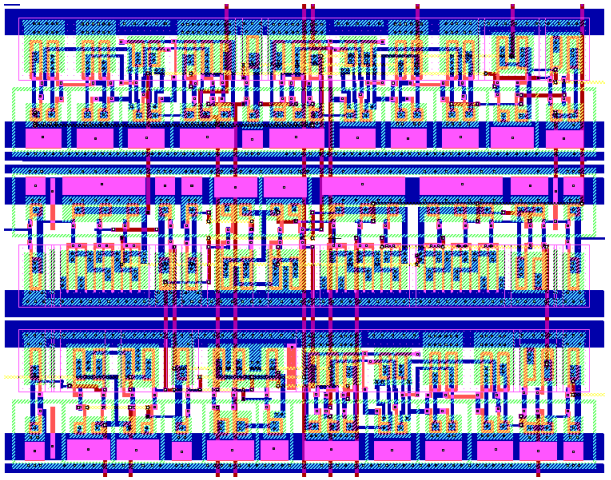
Mario Ackers - Bonn
Laurent Blanquart - Marseille
now LBL (from 28 Feb. 01)
Giacomo Comes - Bonn
Peter Denes - LBL
Kevin Einsweiler - LBL
Peter Fischer - Bonn
Ivan Peric - Bonn
Emanuele Mandelli - LBL
Roberto Marchesini - LBL (until 16 Jan 01)
Gerrit Meddeler - LBL

Technology / Design Developments



Mixed-mode standard cell library (Modification of CERN / RAL library - Bonn)

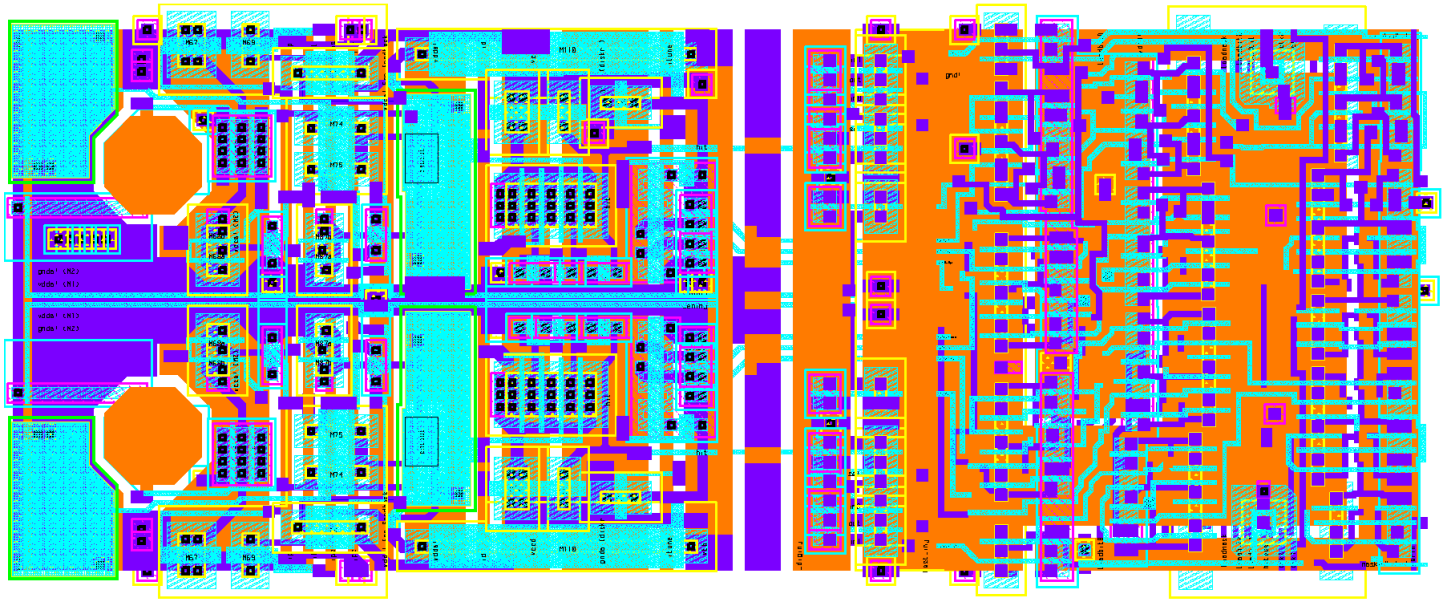
Implement Silicon Ensemble (to be able to autoroute standard cells - LBL)



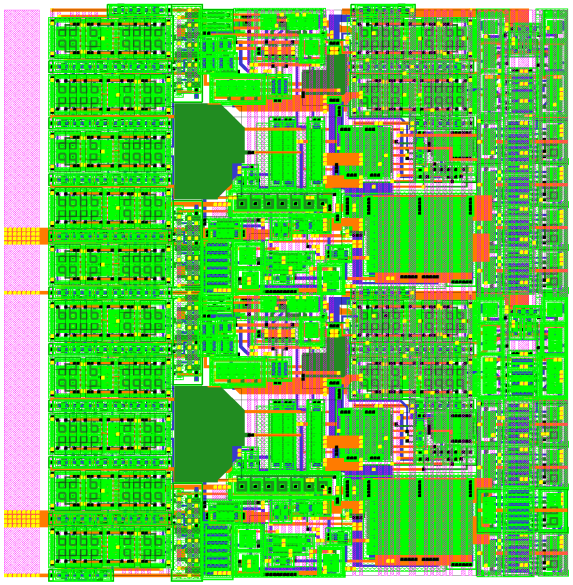
example - Pixel Logic

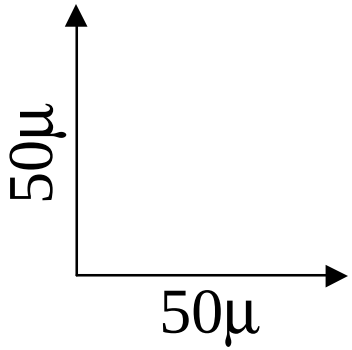
Comparative Size

Two pixels (analog) in *DMILL*

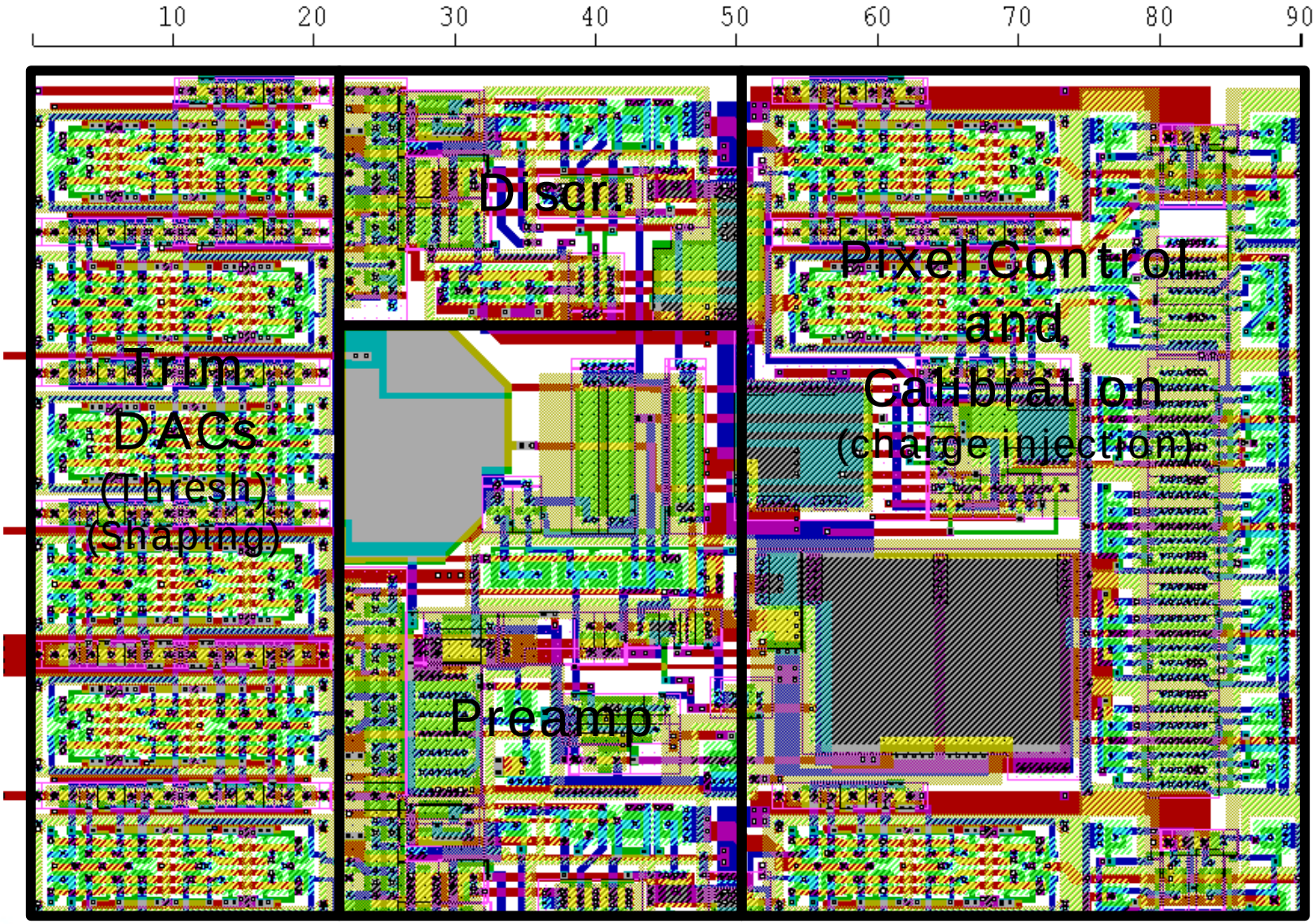


Two pixels in 0.25µ





In a Pixel

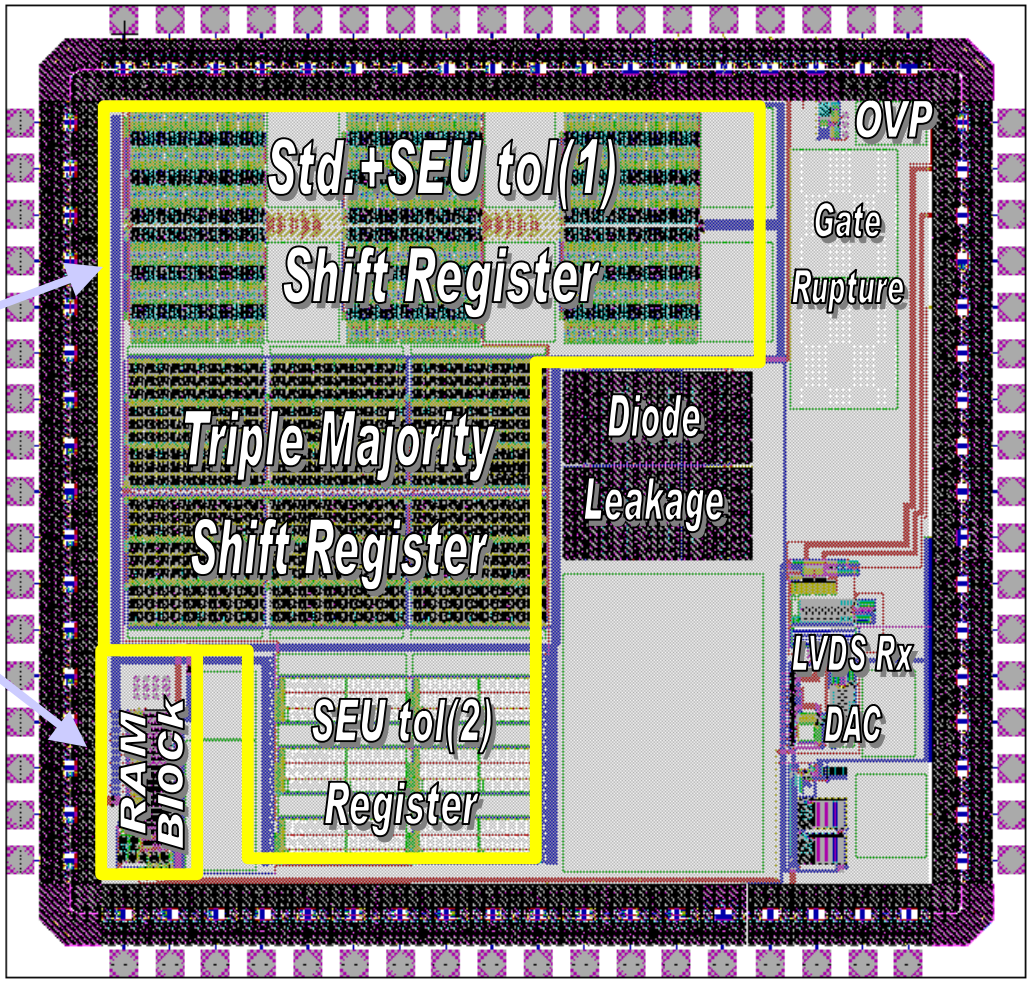

10
20
30
40
50
60
70
80
90
Trim
DACs
(Thresh)
(Shaping)
Discr.
Preamp
Pixel Control
and
Calibration
(charge injection)

Digital Test Chip

TSMC 0.25µ
Submitted 08 Jan ‘01

Structures to test SEU sensitivity of storage registers
Pixel RAM block

Irradiate Apr ‘01

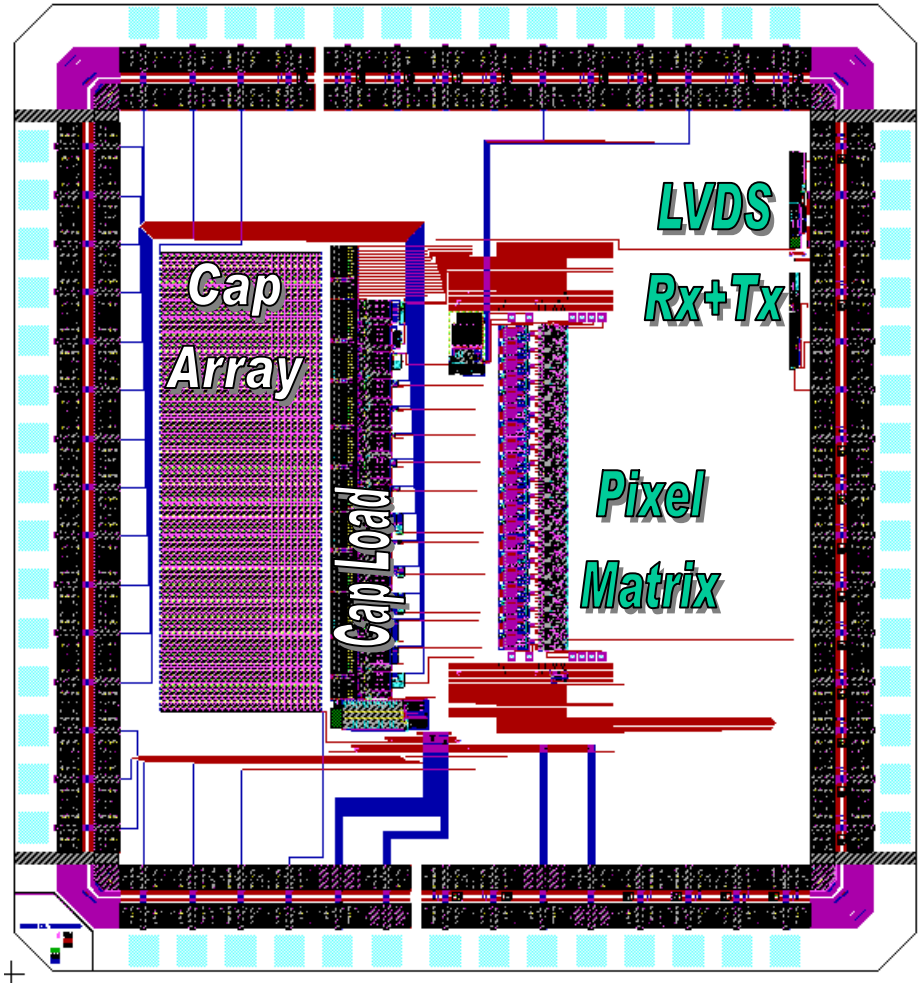


Analog Test Chip

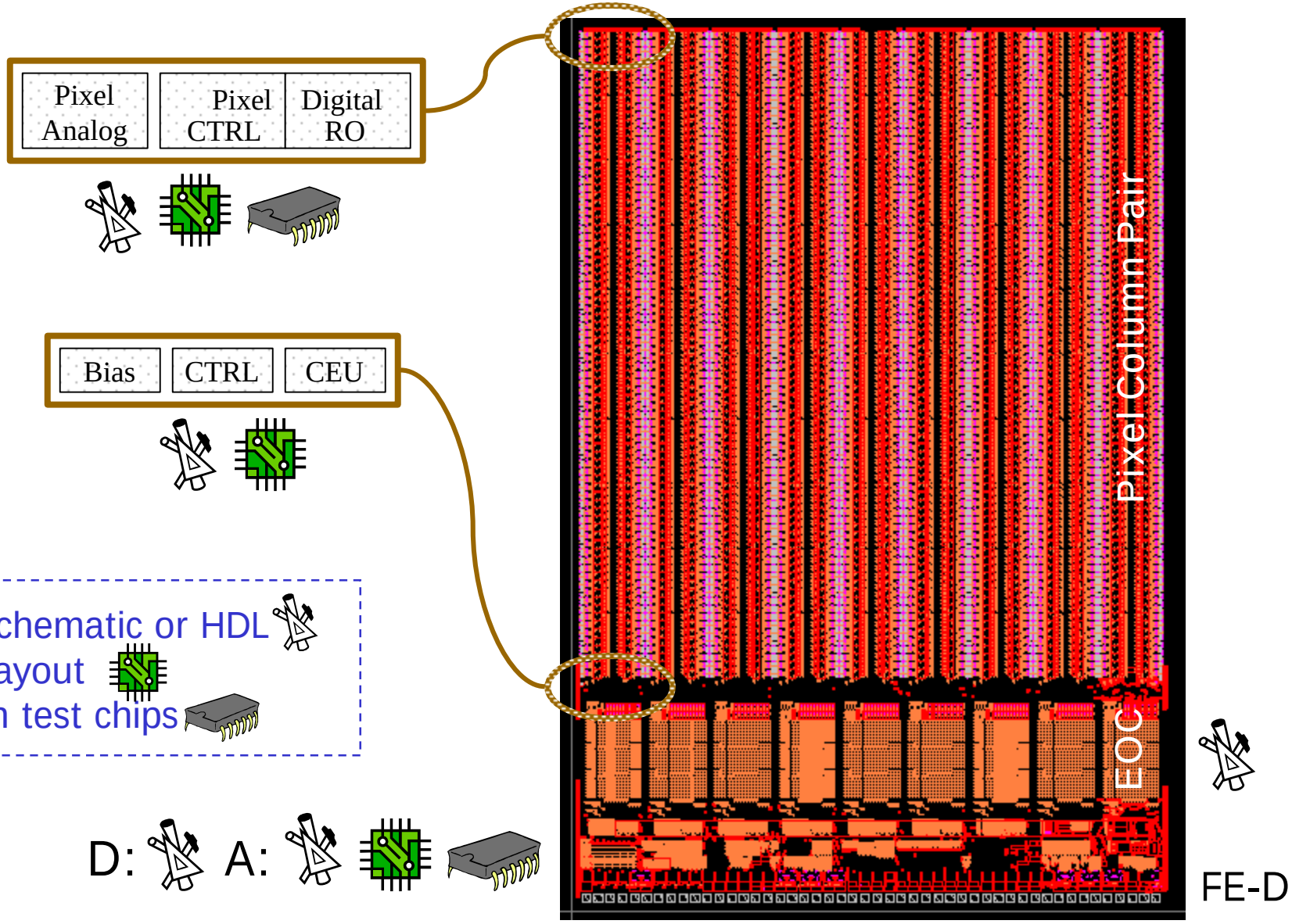
Submitted (CERN) 28 Feb 01
Submitted (TSMC) 6 Mar 01

Array of pixels along with other analog functions

- Preamp and discriminator
- Trim DACs
- Main DACs
- 50Ω output buffer
- Input capacitance test structure

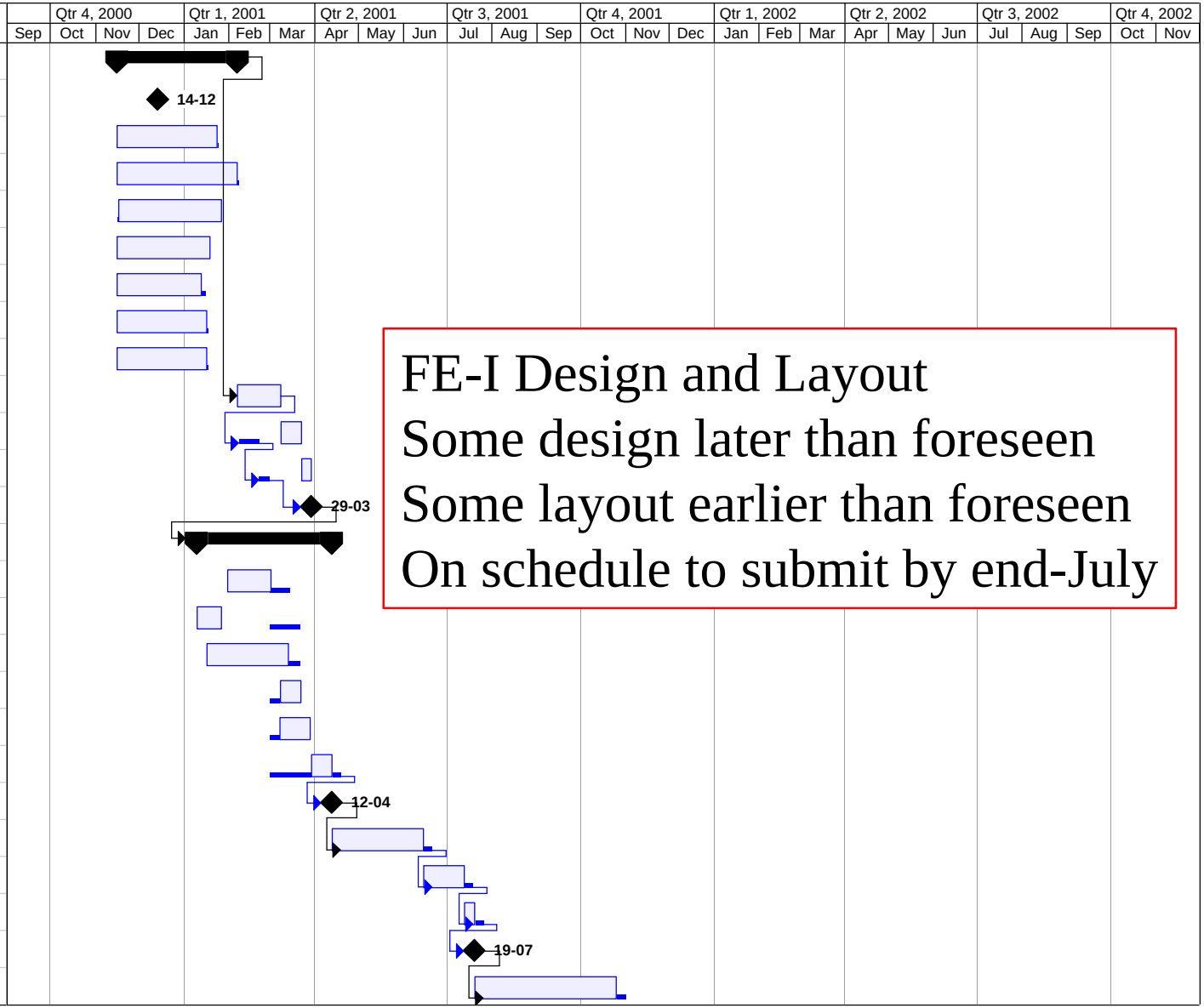


Status - Ready to Assemble Final Chip



Planning (1) - Design/Fabricate

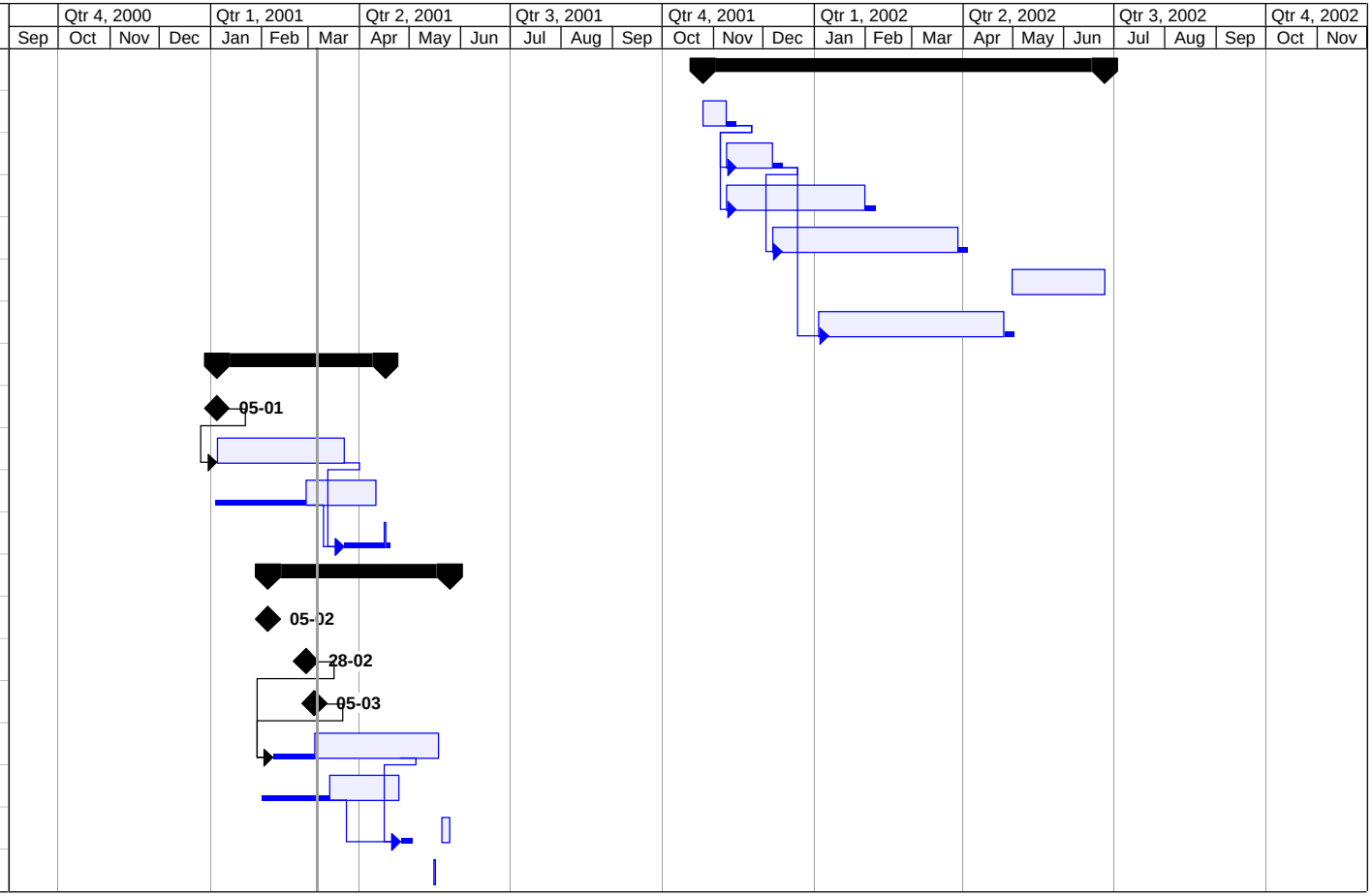
ID	Task Name
1	**Design**
2	Kickoff Meeting
3	Specification
4	Pixel analog
5	Pixel digital
6	EOC logic
7	Chip digital
8	Chip analog
9	Chip pad+ESD
10	Final Schematics
11	Top level sim (sch)
12	(Modifications)
13	PDR
14	**Layout**
15	Pixel analog
16	Pixel digital
17	EOC logic
18	Chip digital
19	Chip analog
20	Chip integration
21	Extract
22	Post-layout sim
23	(Modifications)
24	CDR
25	Submit
26	Fab



FE-I Design and Layout
Some design later than foreseen
Some layout earlier than foreseen
On schedule to submit by end-July

Planning (2) - Characterization

ID	Task Name
27	**Characterization**
28	Wafer Probe
29	Bump, thin, flip
30	Irradiate (chips)
31	Lab test of assemblies
32	Test Beam (modules)
33	Irradiate (modules)
34	**Digital Test Chip**
35	Submit
36	Fab
37	Test card
38	Irradiate
39	**Analog Test Chip**
40	Planned Submit
41	Submit Process 1
42	Submit Process 2
43	Fab
44	Test card
45	Test
46	Irradiate



US ATLAS E.T.C.

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.3	Electronics	0	0	0	0	0	615	621	354	26	0	1616
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	446	161	0	0	989
1.1.1.3.1.1	IC design	0	0	0	0	0	189	269	11	0	0	469
1.1.1.3.1.2	Test design	0	0	0	0	0	140	75	0	0	0	216
1.1.1.3.1.3	Systems Engineering	0	0	0	0	0	52	101	151	0	0	304
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	234	133	0	0	0	367
1.1.1.3.2.1	Atmel/DMILL prototypes	0	0	0	0	0	130	0	0	0	0	130
1.1.1.3.2.2	Honeywell	0	0	0	0	0	10	0	0	0	0	10
1.1.1.3.2.3	0.25 Micron	0	0	0	0	0	0	54	0	0	0	54
1.1.1.3.2.4	Test	0	0	0	0	0	94	79	0	0	0	173
1.1.1.3.3	Production	0	0	0	0	0	0	42	193	26	0	261
1.1.1.3.3.1	Front-end ICs	0	0	0	0	0	0	19	140	26	0	185
1.1.1.3.3.2	Optoelectronics	0	0	0	0	0	0	23	53	0	0	76

SCT Hybrids and Modules - Carl Haber(LBNL)

- 1.1.2.2 SCT Hybrids
- 1.1.2.2.1 Design
- 1.1.2.2.2 Prototypes
- 1.1.2.2.3 Production
- 1.1.2.3 SCT Modules
- 1.1.2.3.1 Design
- 1.1.2.3.2 Prototypes
- 1.1.2.3.3 Production

US SCT Group

Hybrids and Modules Responsibilities

Lawrence Berkeley National Laboratory

>Prototyping activities

>Assembly and test of hybrids

>Assembly and test of modules

>Development of module assembly setup

University of California, Santa Cruz, SCIPP

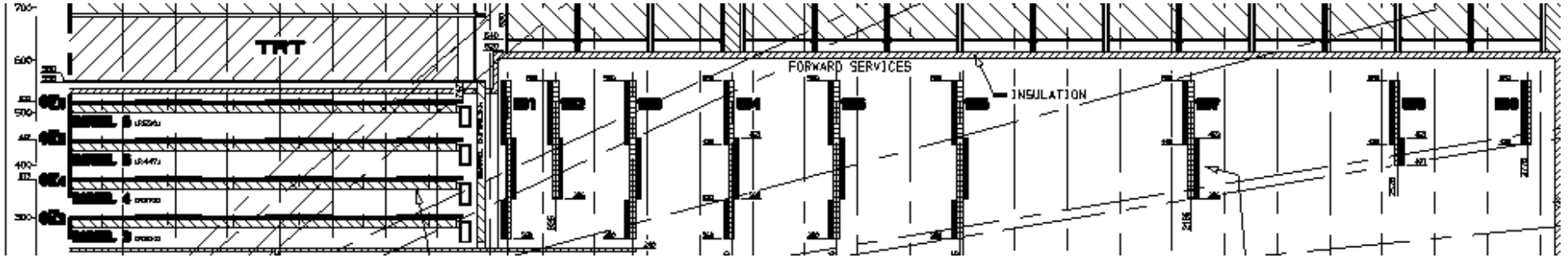
>Prototyping activities

>Assembly and test of hybrids

>Hybrid and module rework and repair

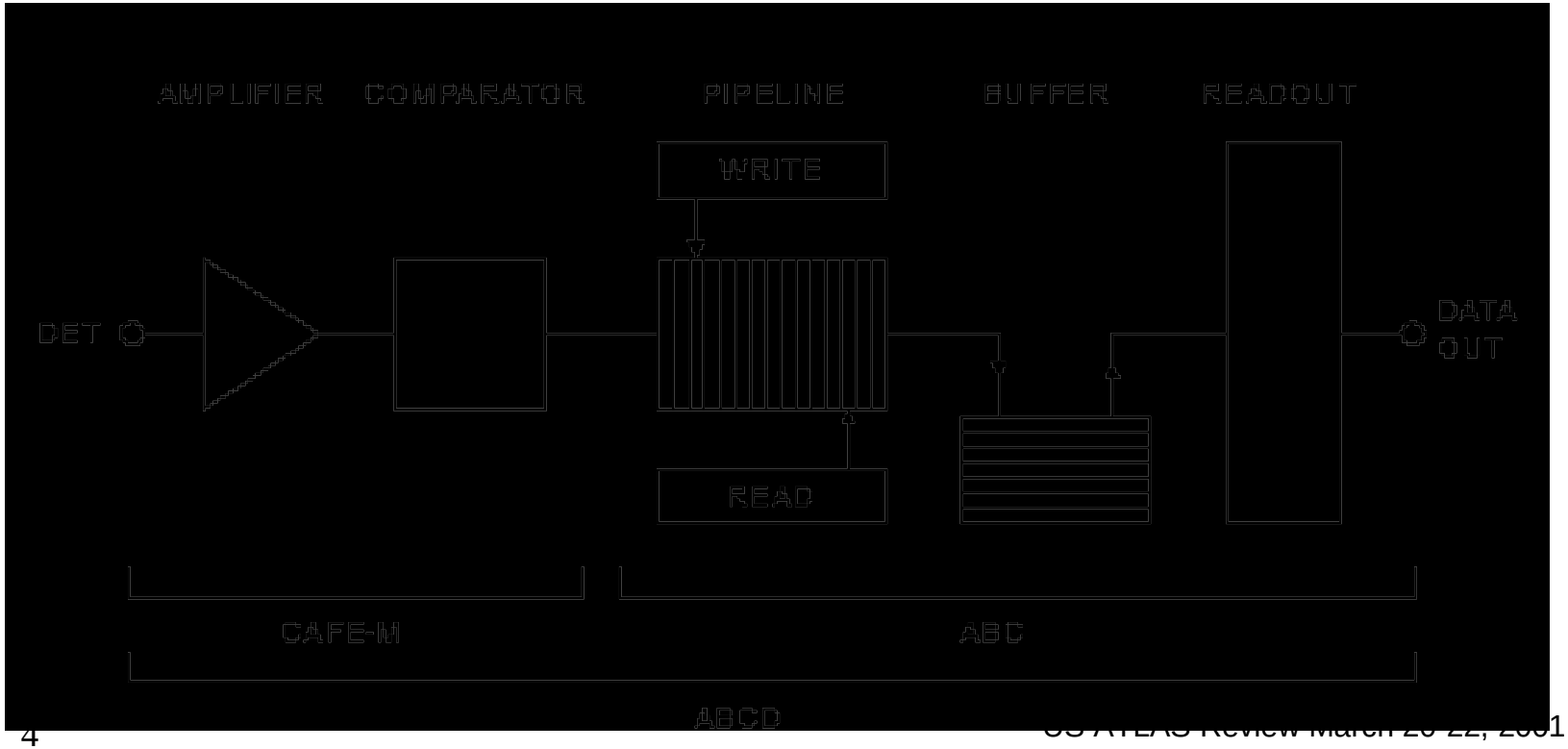
Semiconductor Tracker(SCT)

- Lots of silicon
  - ~60 m^2
  - ~6 million channels
  - Single-sided, p-on-n detectors bonded back-to-back to provide small angle stereo => modules
- Radiation environment is about 10M Rad worst case over lifetime.
- US has concentrated on electronics and module construction.



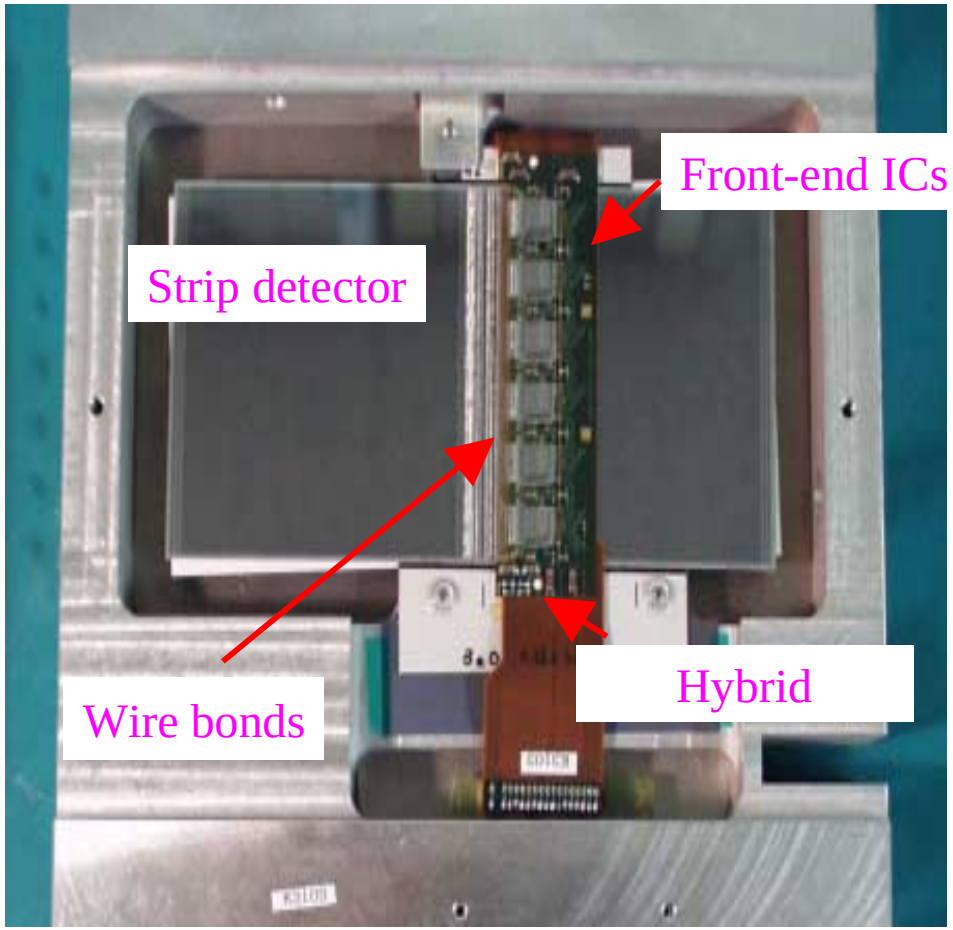
Silicon Strip IC Electronics

- The ATLAS signal processing scheme for silicon strips is based upon a binary hit/no-hit readout
- This approach was pioneered in the US originally for SDC and Zeus..
- Eventually two rad-hard solutions came under development
  - CAFÉ-M(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips..
  - ABCD(BiCMOS from Temic) - 1 chip.
- ABCD design chosen and under final development

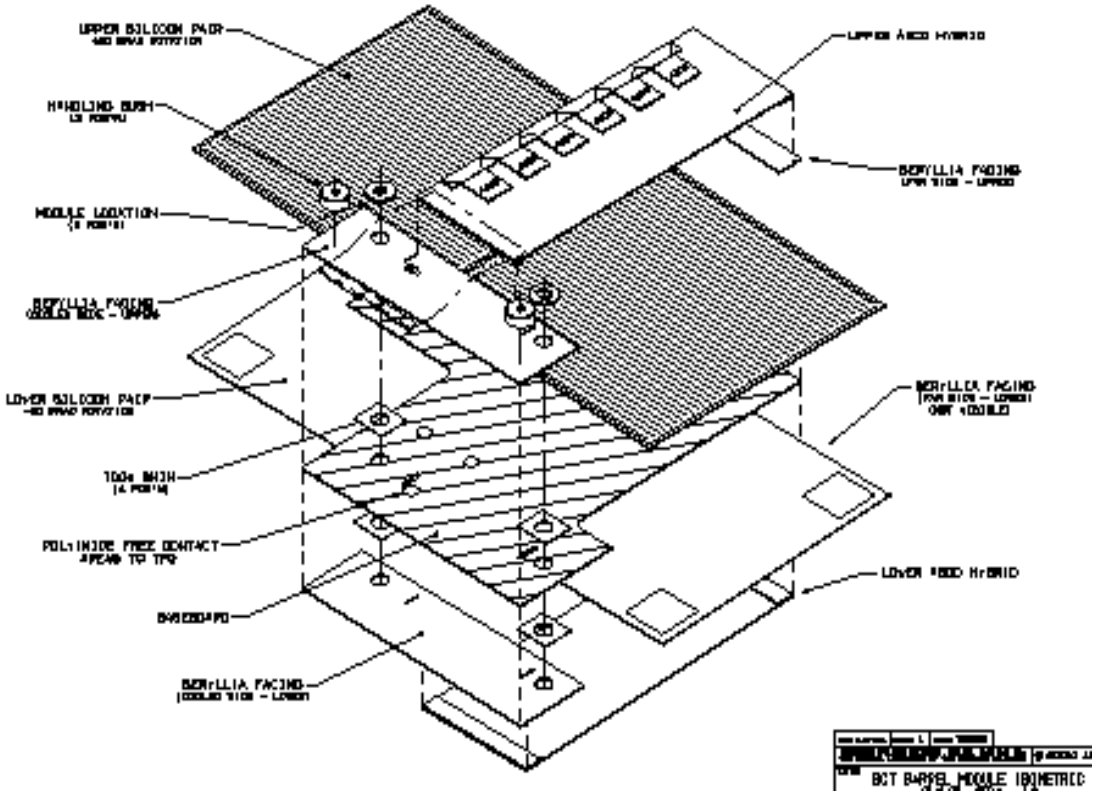


SCT Module

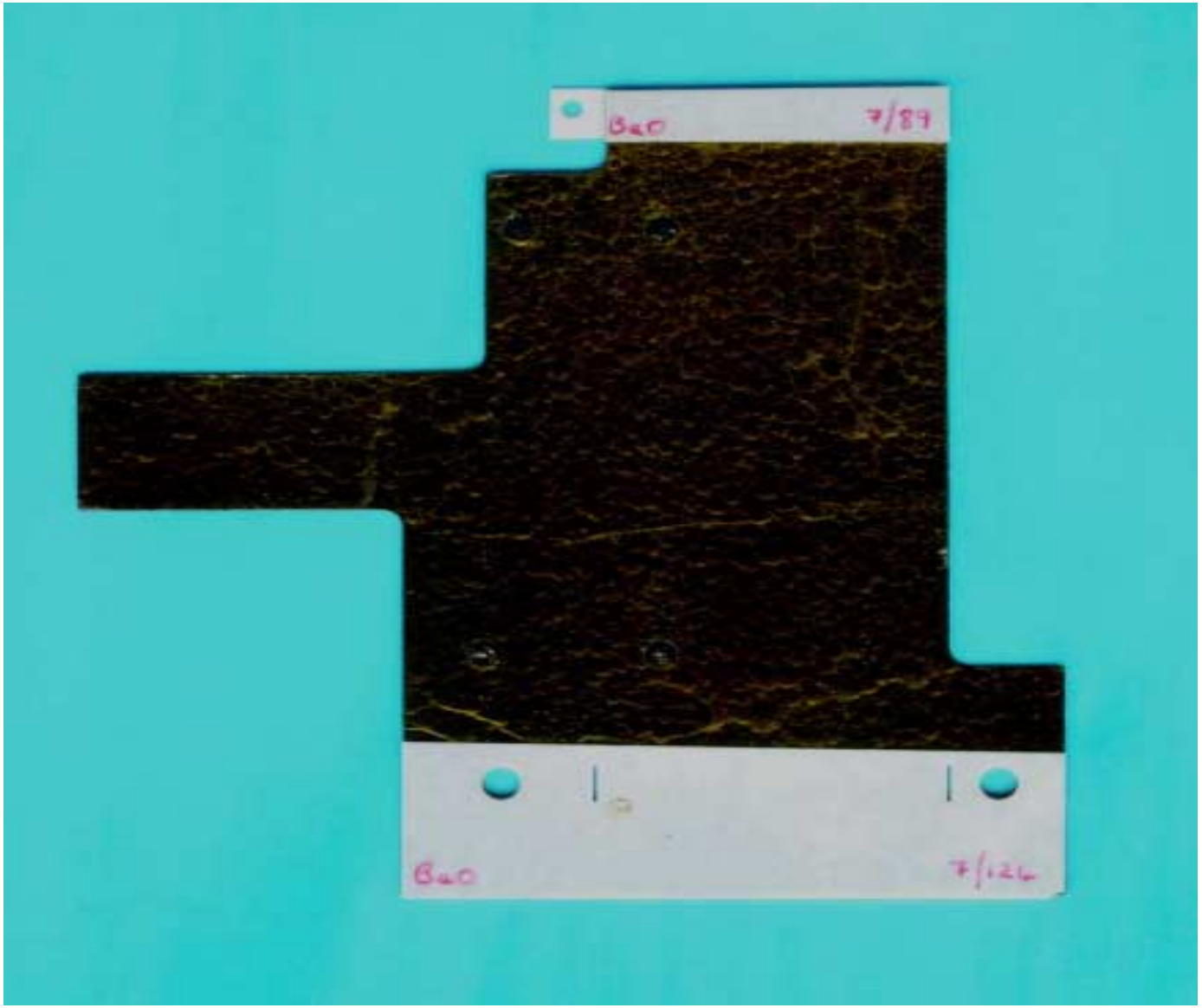
- **Modules are the building blocks of the SCT system**
- **Each module consists of:**
  - 4 single sided detectors, p implant in n type material, 500 V operation, 768 strips per side, 128 mm
  - Thermal baseboard of pyrolytic graphite with BeO side facings
  - Hybrid holding 12 ABCD chips
  - 4608 high density bonds
- **US to deliver 670 modules**



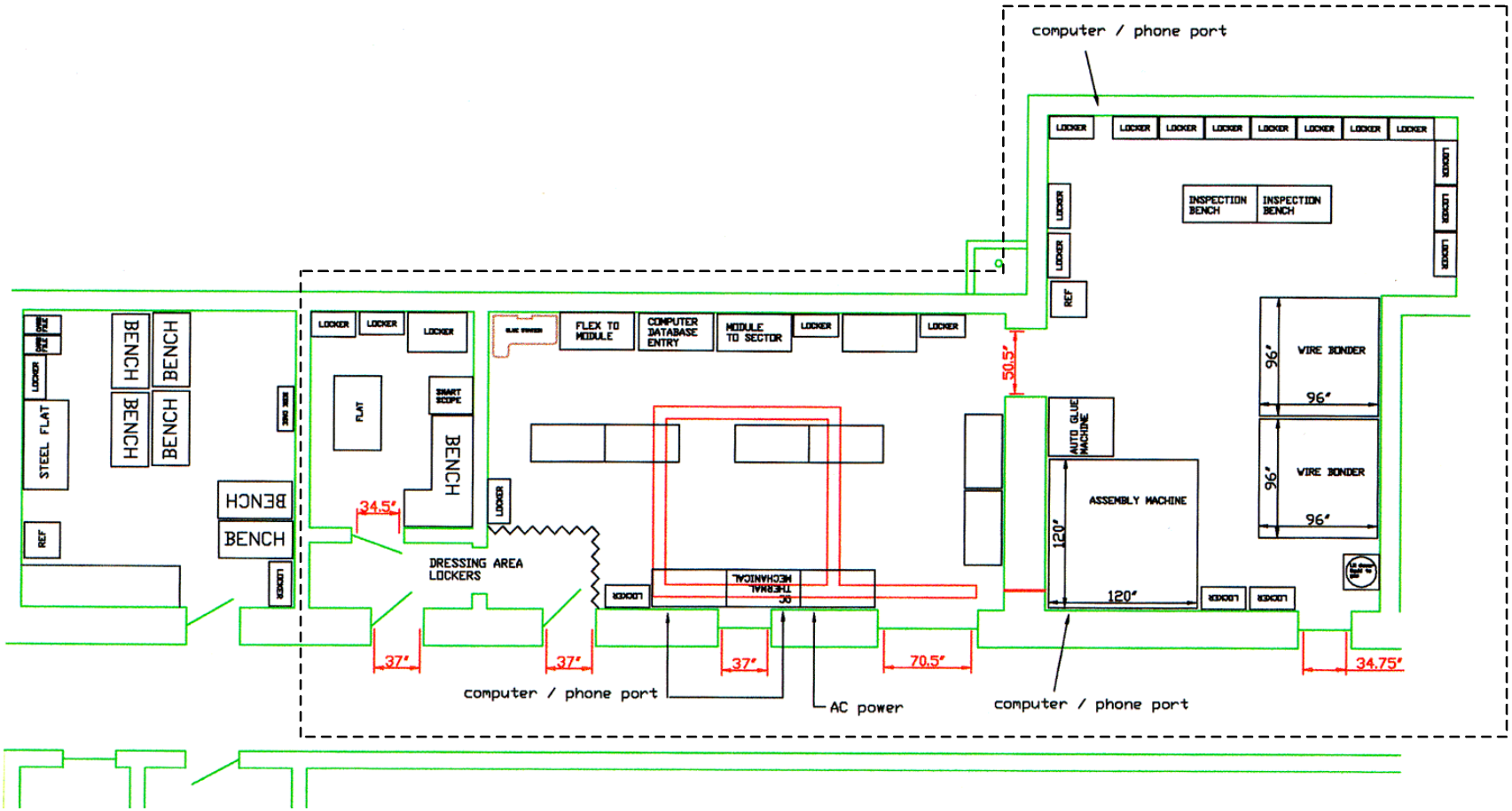
Expanded view of module



Thermal baseboard



Module Assembly Space at LBNL



Completed assembly areas

Pixel assembly area with gluing machine visable

Strips assembly area showing vision assisted alignment station

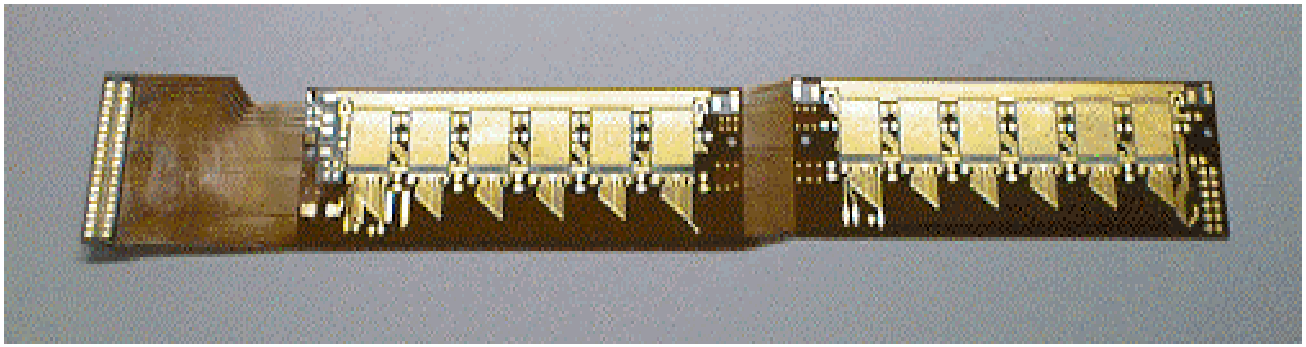
1.1.2.2.1 Hybrid Design

- The US group contributed to the hybrid design since 1995, developing the basic layout, interconnectivity, and schematic
- The US group executed a series of designs based upon high thermal conductivity ceramic (AIN and BeO) substrates (following on work for CDF)
- In 2000 Atlas chose a hybrid techology based upon copper/kapton flexible circuits developed by the KEK group. Cost was the primary driver.
- The US group no longer has design responsibility but continues to contribute to technical reviews and specifications for these parts.

1.1.2.2.2 Hybrid Prototypes

- The US Group fabricated a series of prototypes in the ceramic technology 1995 -1999
- These were used extensively in bench and beam tests, irradiations, and to validate the readout chips
- The chosen Kapton design is fabricated in Japan.
- Prototype samples have been distributed around the collaboration for tests and validation.
- Initial concerns were for etch and surface quality and seem to have been solved in most recent batch.
- We are in the process of studying these units.
- Noise, stability, and interference are issues still to be fully demostrated when FE chips are integrated into the hybrid/modules but present results look good.
- Deadtimeless operation tests recently begun

Kapton hybrid



1.1.2.2.3 Hybrid Production

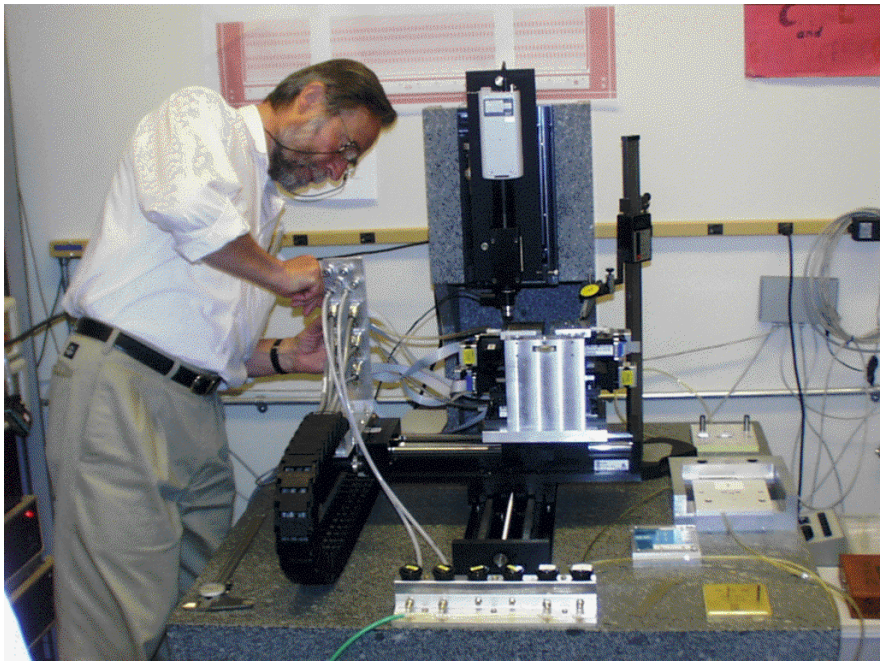
- Hybrids with discrete components mounted will be supplied by Japan
- US is to attach tested ABCD chips and wirebond
- Plan to to bond 2 hybrids in an 8 hour shift
- Bonding capacity and expertise in place at LBL and UCSC. Use of local industry also an option
- LBL bonder recently modified to clear components on Kapton hybrid, tested sucessfully in auto mode.
- First production level test system installed and commissioned at LBL, additional systems ordered.
- Comprehensive test protocols are under discussion and review within.
- Burn-in process still to be fully specified

Wirebonder installed in clean assembly space

Barrel Silicon Strip Modules

Double-sided dummy module

- **Tooling for large-scale production(we have to assemble 670 modules)**



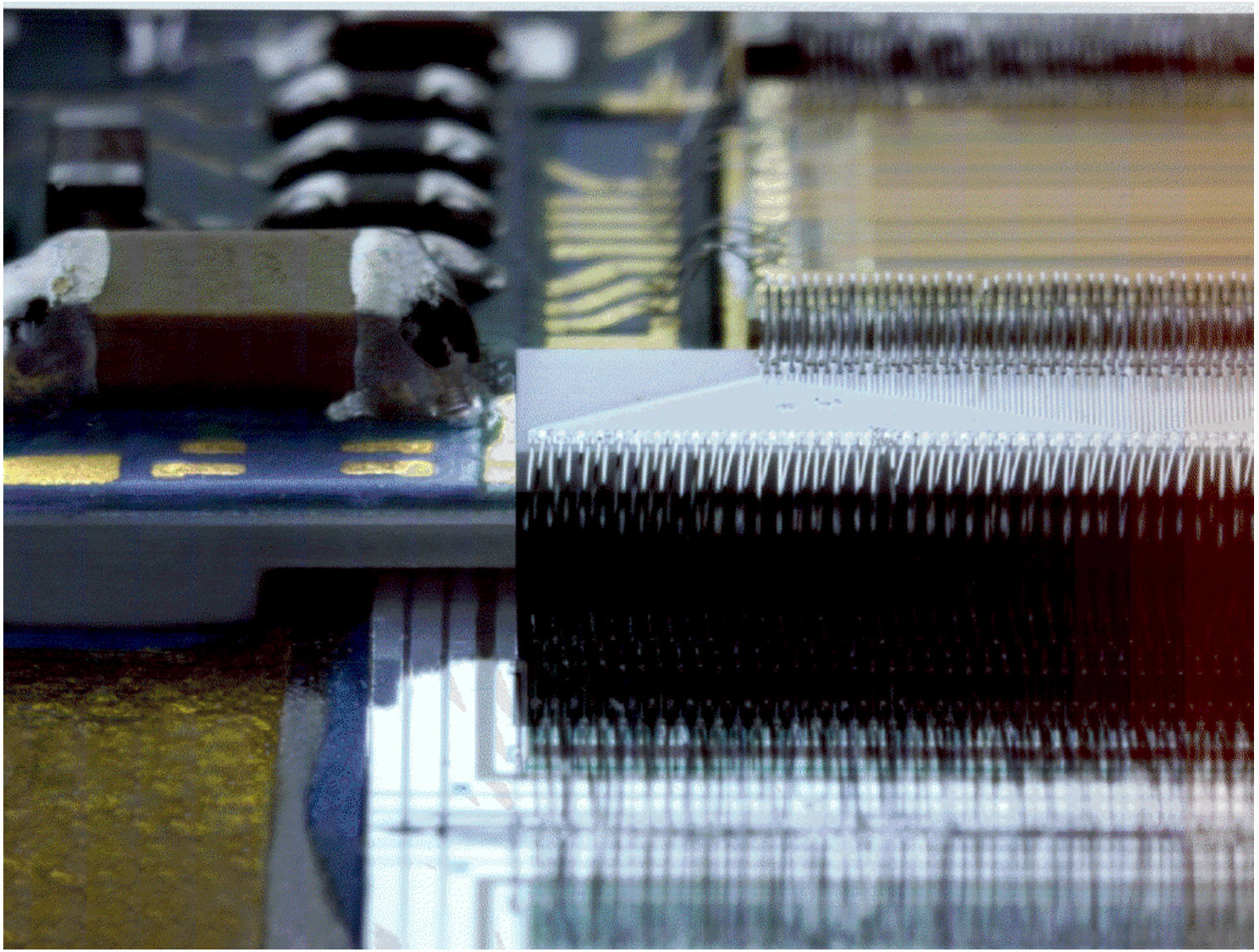
Module build process

- Modules will be built using a semi-automatic process to avoid operator error and control uniformity
- The same process will be used by a sub-set of the SCT module assembly sites
- The process is based upon precision stages driven by stepper motors, optical monitoring with pattern recognition of fiducials on detectors, and precision fixtures
- The plan is to build 2 modules/8 hour shift
- Module build rate is also effected by delivery of components from non-US sites (baseboards, hybrids, wafer fabrication, detectors)

1.1.2.3.1 Module Design

- The US groups have been involved in the design of the module since 1995.
- Significant involvement in hybrid/electrical interaction issues. Validated bridged construction concept.
- Collaboration with RAL on module assembly process
- Design of various assembly and bonding fixtures for use in the construction of prototype and production build (example: hybrid folding fixture)
- Development of build specification
- Organization of working group on module assembly process.

Bridged module concept



1.1.2.3.2 Module Prototypes

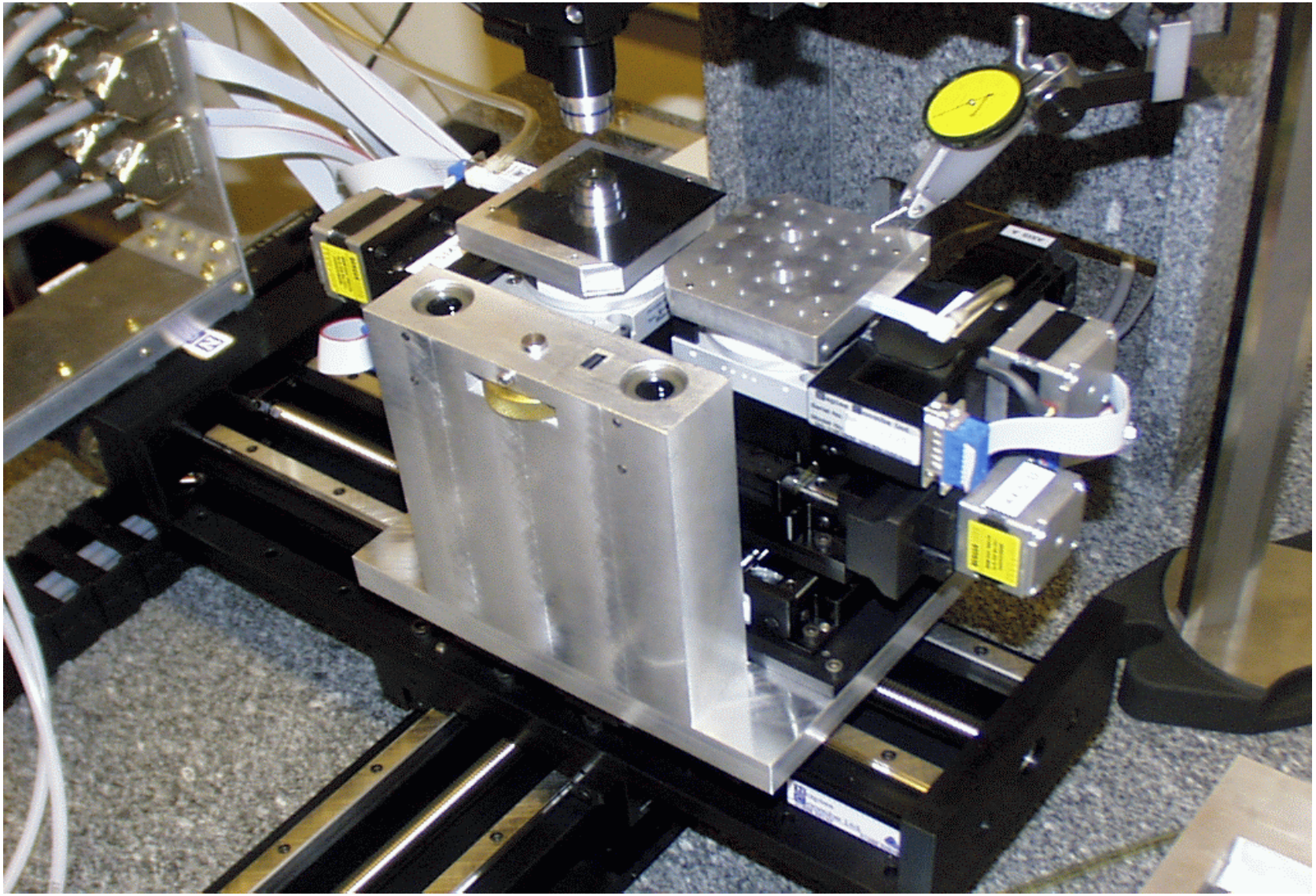
- Prototyping activities since 1995. Developed an early assembly process used for test beam module builds.
- Began to install production design system for assembly in 1998 following work of RAL group.
- V1 of that system tested in 1998
- In process of commissioning V2 consisting of new fixtures and new software
- Metrology based upon SmartScope tool. New fixture in hand and being tested.
- Module TDR in late May 2001. Plan is to show results on modules built with V2 system at TDR

Module assembly process

- **Components are 4 detectors, baseboard with glue applied, tested hybrid.**
- **Build system follows programmed sequence, twice per day**
  - **Load a pair of detectors on stages**
  - **Drive to approximate position of detector fiducials**
  - **Optics performs pattern recognition on fiducials and moves detectors into proper alignment**
  - **Detector pair lifted with vacuum plate.**
  - **Process repeated on second pair**
  - **Baseboard glue pattern applied with gluing robot**
  - **Baseboard mounted in "window frame" fixture**
  - **Vacuum plates engaged into frame with precision pins and linear bearings**
  - **Glue cures at room temperature**
  - **Metrology checked**
  - **Hybrid folded and glued around detector sandwich**
  - **Wirebonding performed**
  - **Test, rework, burn-in**

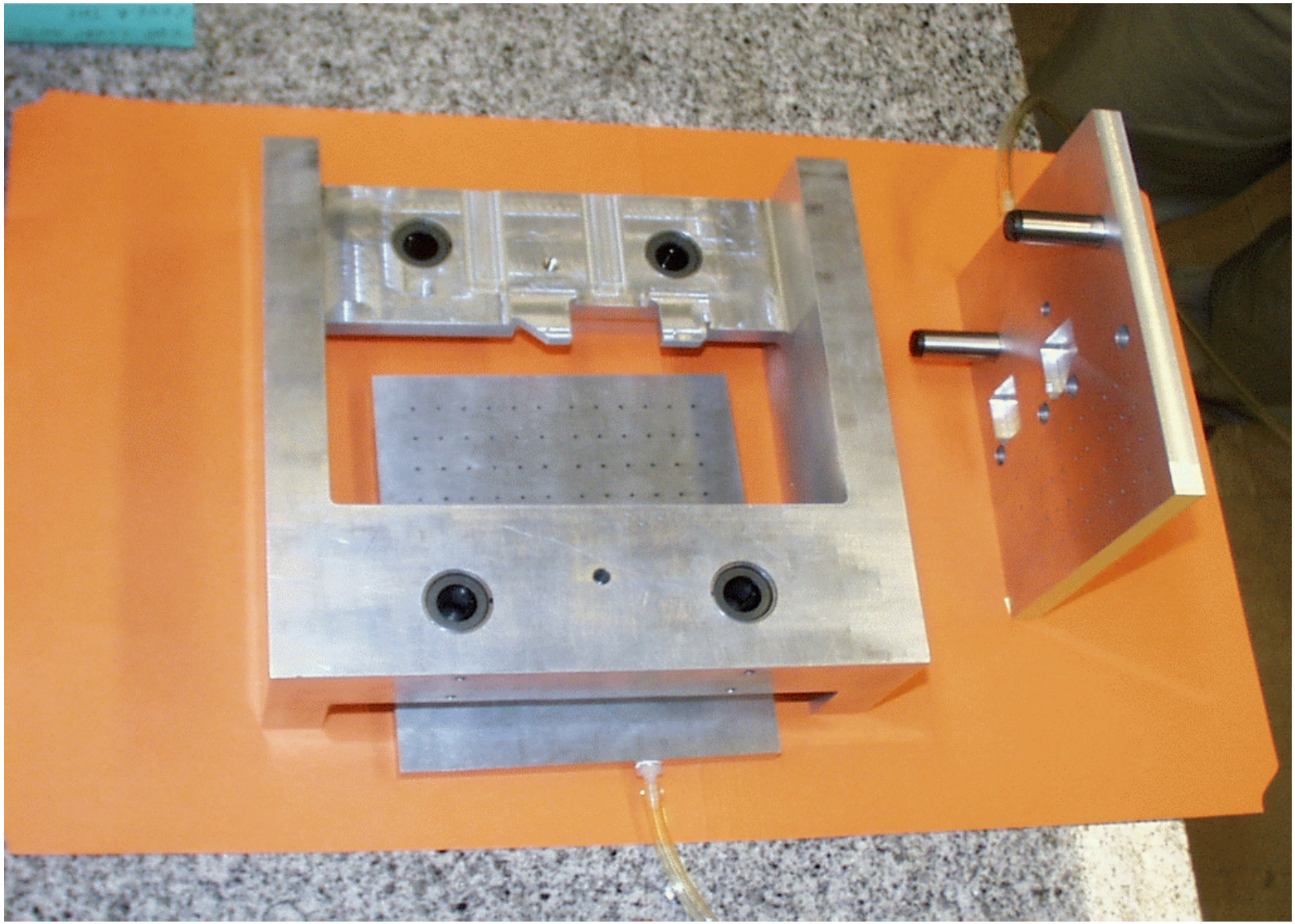
Assembly system

Stages

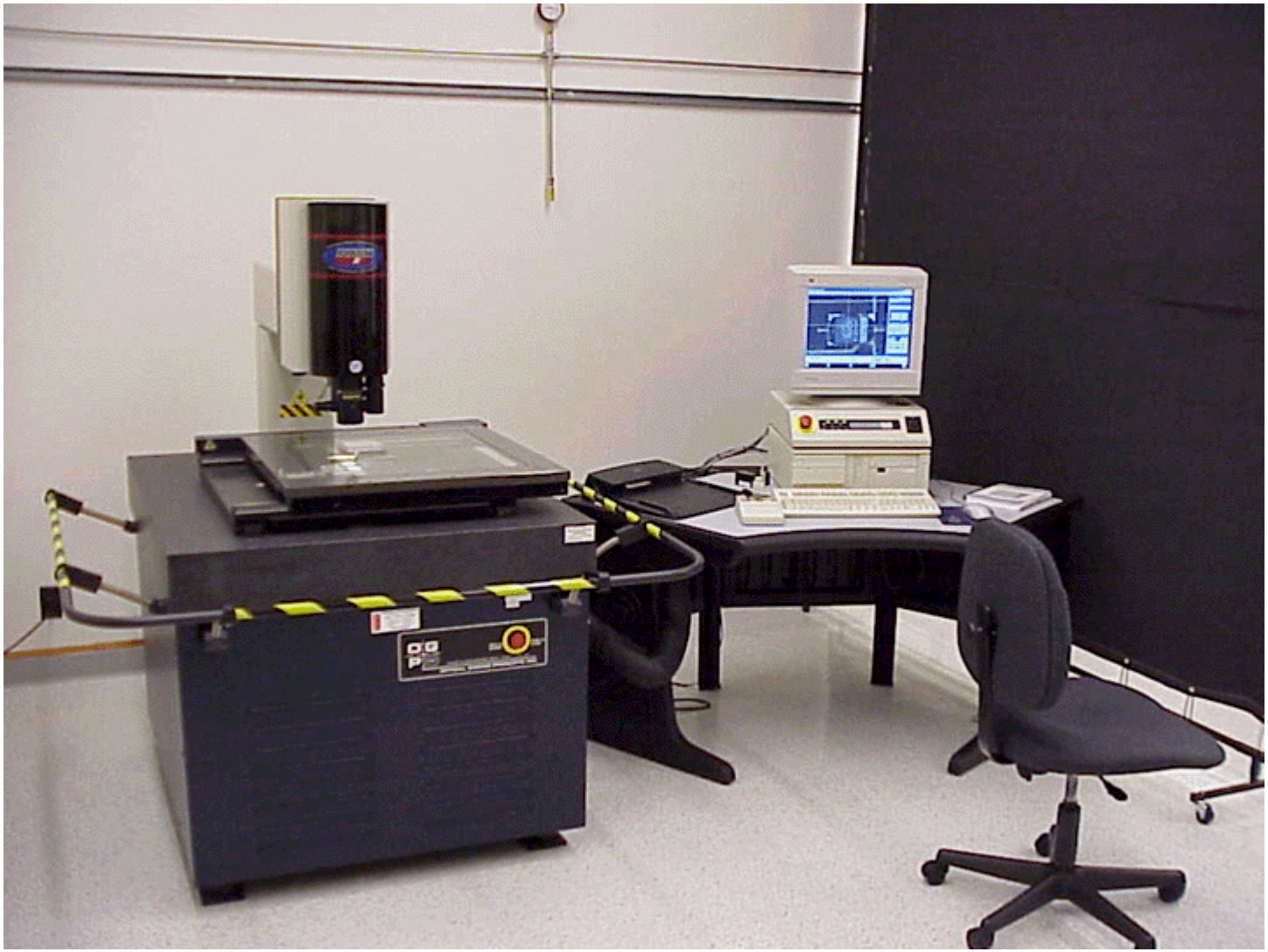


Fiducial Mark

Assembly fixtures



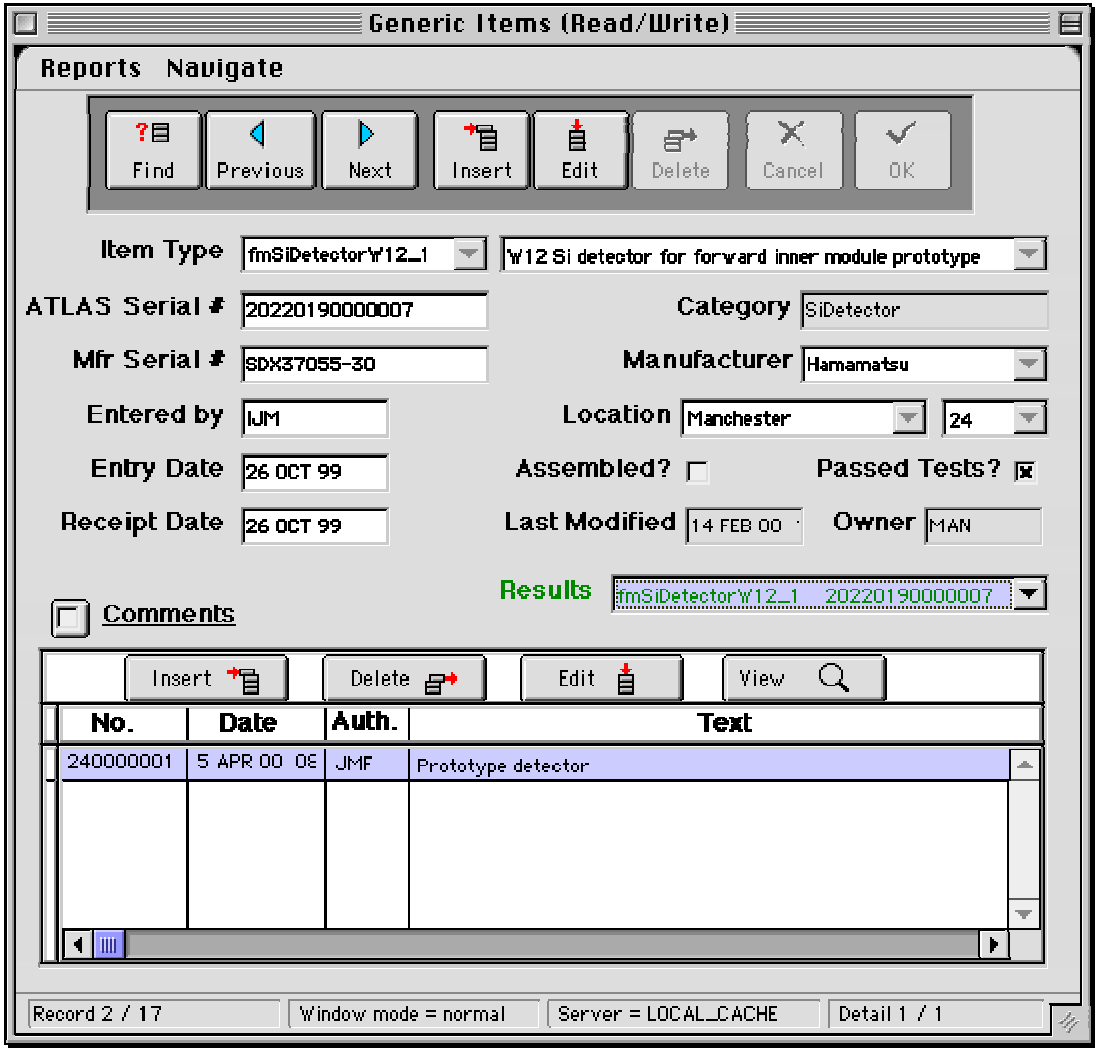
SmartScope



1.1.2.3.3 Module Production

- Build system will be used in production
- Assuming FDR is passed, plan is to use present fixtures, mechanics, and software in production build
- Clean space adequate and ready
- Database software in hand, needs to be loaded and understood.
- Expect to be ready for delivery of first production components in Fall 2001.

Production database



Manpower and Time

- **Plan is to build 2 hybrids per day**
  - **Wirebonding rate from tests and from CDF experience predicts that this is comfortable. One technician required**
  - **Sufficient electronics for test and burn-in on order.**
  - **Testing by physicists and students.**
- **Plan is to build 2 modules per day**
  - **Module build process has been timed in the UK and evaluated here. Slowest step is glue cure and multiple fixtures will be available. One senior and one junior technician planned for**
  - **Wirebonding rates as for hybrids. Plan for second shift, one technician required.**
  - **Sufficient electronics for test and burn-in on order.**
  - **Testing by physicists and students.**
- **Two technicians experienced in bonding in place, one senior technician in place, one junior required.**

Conclusions

- Most of tooling and process for hybrid and module assembly in place at US sites
- Production system being commissioned
- Good experience base exists
- Time for processes has been calibrated on practice runs and from previous projects
- Plan to be ready for components in Fall of 2001

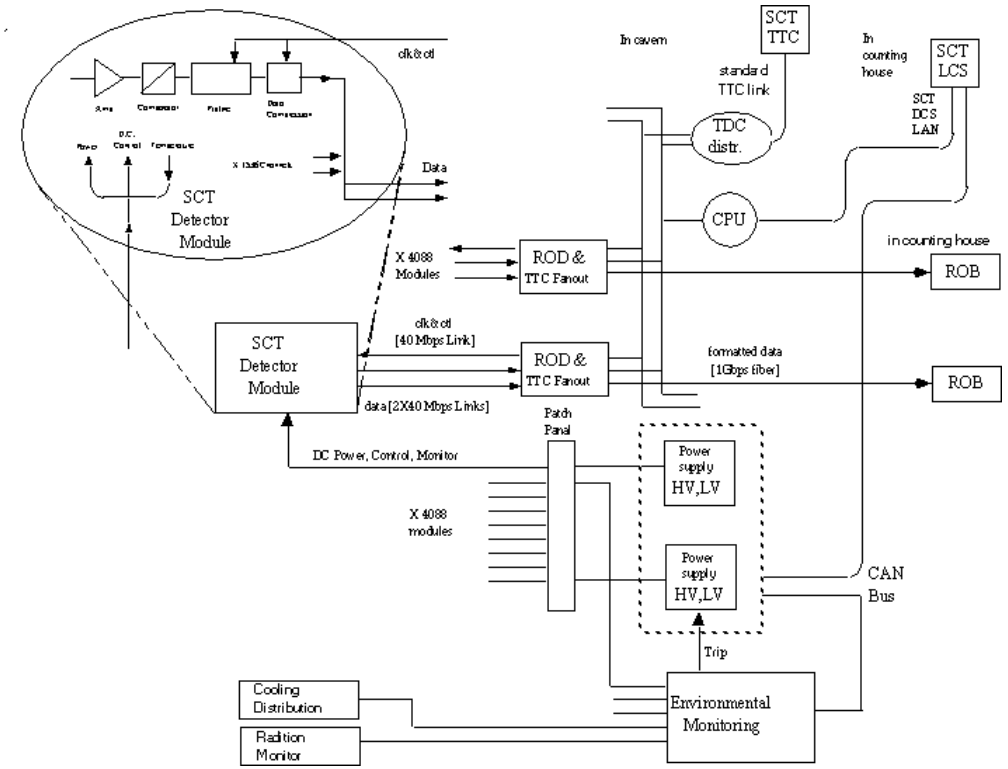
WBS 1.1.2.1
ATLAS SCT Electronics

US ATLAS DoE/NSF Review
20/23-Mar-2001

Alex Grillo

A Bit of History

The ATLAS-SCT electronics system has the following architecture:



The US deliverables include partial amounts of:

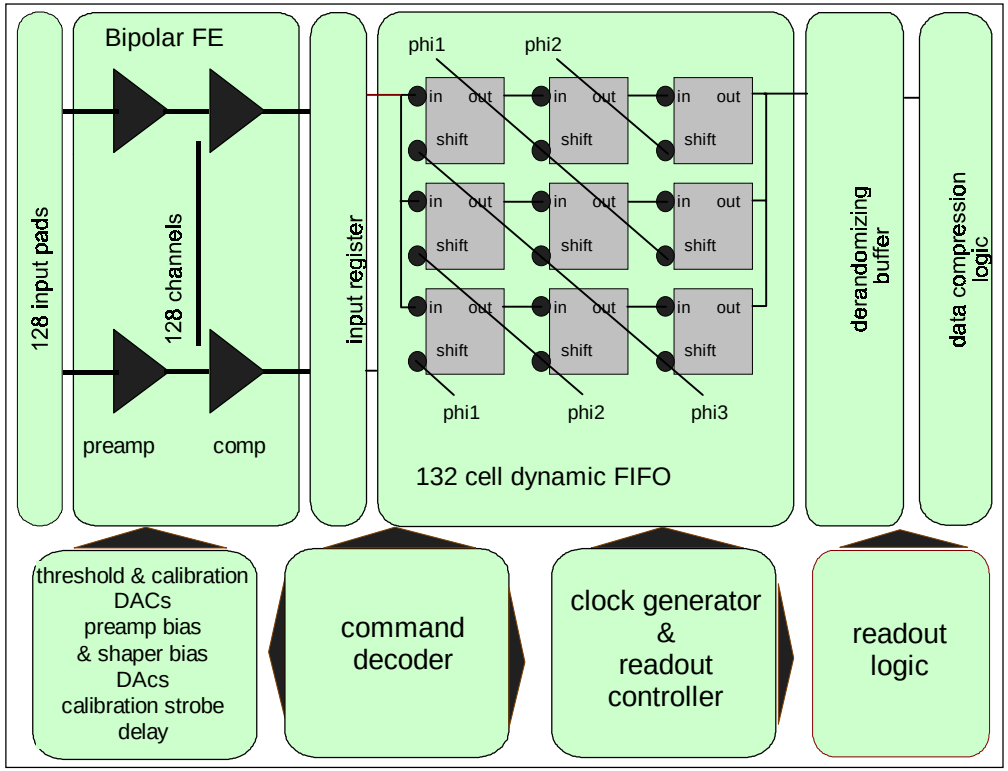
Front-end ASICs	**1.1.2.1 (This presentation)**
Detector Hybrids & Modules	**1.1.2.2 & 1.1.2.3 (Carl Haber's presentation)**
RODs	**1.1.3 (Dick Jared's Presentation)**

The US is also contributing to the electronics system engineering

The Front-End ASIC (Named ABCD)

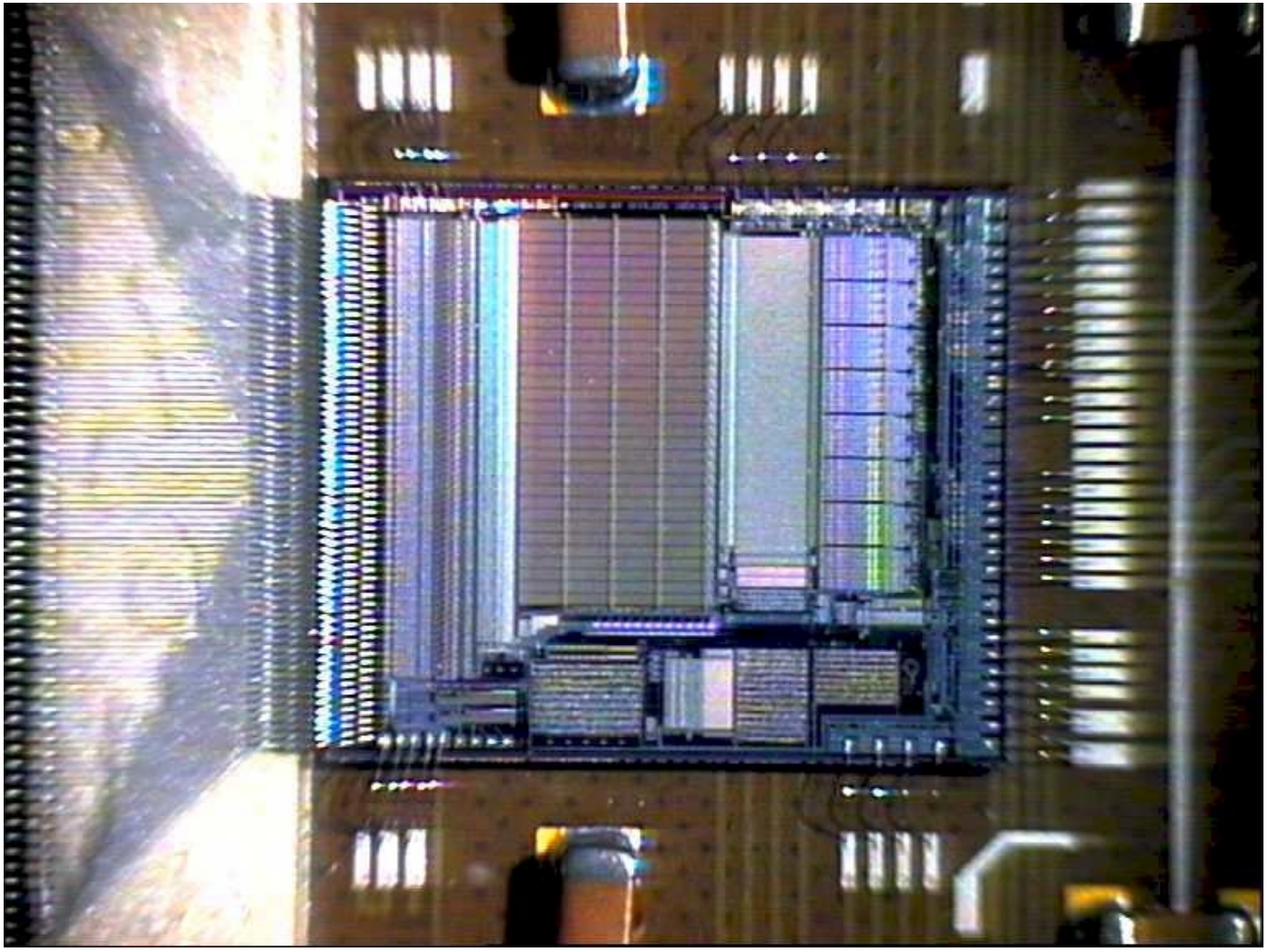
Several years ago the SCT Collaboration selected "Binary Readout" as its baseline.

After parallel developments of two technologies, the ABCD chip fabricated with the DMILL technology was selected last year as the best choice for final production.



This is a biCMOS IC that incorporates bipolar front-end amplifier and shaper circuits, a comparator with programmable threshold (each channel trimable), a pipeline, de-randomizing output buffer, data compression and output serializing circuits.

The ABCD in Silicon



A.A. Grillo
SCIPP - UCSC

Pre-Production Phase

Following the ABCD Final Design Review in March-2000, an order was placed for 40 wafers to be fabricated in 5 mini-lots of 8 wafers each.

The objective was to sample the DMILL fabrication line at 5 points in time and also to give the vendor (Atmel) the financial incentive to operate their DMILL line in a more continuous manner.

- **Atmel runs the DMILL process on the same line with several commercial CMOS processes.**
- **While a few hundred wafers have been processed as part of their qualification of the process after transferring the license and recipe from the French CEA lab, there are currently no designs in production with the technology. The ABCD may be the first.**
- **Yield has been lower than expected on prototype lots and remains a concern.**

A Frame Contract has been negotiated and is in place between CERN and Atmel which fixes the price per wafer (in Euros) and a minimum yield based upon die size (26% for the ABCD). This contract is the basis of our cost estimate and our assurance against disastrous yield.

Due to various delays in the fab line, some caused by an Atmel subcontractor, the delivery of wafers was more sporadic than expected. The last 3 mini-lots were delivered together at the very end of the planned period and were really processed all together. The last lot had an oxide thickness out of spec and has not been officially accepted by SCT pending test results.

Pre-Production Yield (so far)

The yield results for the wafers tested so far are:

	Date Received	# of wafers tested	Yield (perfect)	Yield (incl. 1 bad channel)	Comments
1st	Jul-00	8	10.6%	21.4%	
2nd	Nov-00	8	16.5%	31.0%	Process "Corner" Run
3rd	Feb-01	4	24.7%	42.4%	New inspection instituted
4th	Feb-01	3	8.1%	18.4%	High sheet resistance flagged
5th	Feb-01	2	12.1%	26.7%	Thin oxide flagged

As you can see, the yields for perfect chips do not meet the minimum guarantee.

The process "corner" run showed very little correlation of yield to process variations.
This shows that the design is robust against process variation.

The results of the "corner" run and the significantly higher yield when including one bad channel indicate that the primary yield limiter is defects.

Also, wafers demonstrate a non-random pattern of areas with 0% yield, again indicating a cause of defects.

Of the 25 wafers tested, 6 wafers had yields $\geq$ 26%.

Searching for the Key to High Yield

Analysis by Atmel of areas of 0% yield on a few wafers from the first lot found a correlation with defects in the oxide before first metal deposition. A new inspection was instituted prior to fabrication of the third lot. This may explain its improved yield.

The cause of the low yield on the last two lots is still being examined. All the wafers from the last three lots have not yet been tested.

Atmel now believes that their subcontractor used to deposit the epitaxial layer is introducing a large number of defects, especially defects that affect the bipolar devices.

This is supported by the fact that an alternate vendor was used for a test lot in 1999 and those wafers yield much better (38.2% with the worst wafer at 27.3%).

Atmel is now in the process of qualifying this vendor for production and fabricating a split lot (old and new vendor) of ABCD wafers to determine if this yield improvement is real. These wafers are expected out in April.

Another possible downside is that we are still developing our test specification, reviewing IC performance on modules and after irradiations, in an attempt to improve overall quality. Adjustments to the test specification to improve module performance could result in lower yields. We believe, however, based upon the test results of the "corner" run that such a yield decrease should not be more than a few percent.

If the high yield key is not found before production starts, Atmel will have to reduce the price of the wafers in proportion to gain our acceptance of the wafers.

We have, as a back up, a plan to increase test capacity to cope with this possibility.

Irradiation Tests

Six full modules (12 chips on each) were assembled from the wafers received in July and irradiated in the CERN PS in October.

The modules were irradiated to a total fluence of $3x10^{14}$ protons/cm^2, which corresponds to the full 10-year lifetime at the inner most SCT radius with agreed safety factors.

All performance characteristics (e.g. noise, gain, time-walk) were found to meet requirements after the full irradiation.

Two problems did show up.

Problem 1: Trim-DAC Range Adjustment:

> **A new feature was added to the design prior to the pre-production submission to provide a global range adjustment to the 128 trim-DACs.**
>
> **After full irradiation, it was found that the 2-bit range adjustment could no longer be re-written. However, the trim-DACs continued to operate correctly at the range set prior to irradiation.**
>
> **The problem was quickly diagnosed and a fix found. The fix required a change the VIA mask. This was implemented and the new mask supplied to Atmel fab in time to be included in the last 3 lots which were still in fabrication.**
>
> **Pre-rad tests of the fix indicate that no new problem was introduced. Parts from the new design will be irradiated in April. The expectation, based upon careful simulation, is that the problem will not re-appear.**

The Remaining Nagging Problem

The Vdd Protocol Violation:

The second problem appeared at slightly past 50% of the full fluence.

The symptom is that data, which is serially passed from one chip to the next during readout on the way to the serial optical driver, is corrupted with a few 0s changed to 1s.

Since the chips are operated continuously during the irradiation we have indication when the problem started to occur.

The problem can be mitigated by raising Vdd (power to the digital portion of the chips).

Analysis at the present time:

Of the 72 chips irradiated, only ~20% show the problem.

All failing chips come from the same wafer, however, it was an unfortunate coincidence that most of the 72 irradiated chips came from that same wafer.

The failing chips will work correctly if Vdd is raised to approximately 4.8 V (4.0 V is nominal)

External signals between chips are good. Probing of internal signals indicates the problem is in the digital logic after the data receiver circuit on failing chips.

Curiously, lowering the temperature requires a higher Vdd. There is significant correlation between CMOS speed (as measured by on-chip delay generator) and minimum Vdd for acceptable performance.

Continuing Studies

Work is continuing to understand this problem:

Further analysis of wafer test data, looking for a correlation with failing chips

Studies of the post-receiver data processing circuit including simulations looking for a cause for the extra delays measured by probing the failing chips

More radiation studies of chips from different wafers and with different speeds as measured at wafer test

Several possible remedies are being considered:

A design fix once the cause has been identified

A new screen at wafer test to bin the parts into those most likely and most unlikely to show this problem. If continued irradiation studies show that the problem only appears late in the expected lifetime fluence, the weak parts could be used for modules at the outer radius.

Increase the operating voltage for modules at the inner radius, possibly up to 5.0 V.
This will increase the power consumption so it has implications for cooling and for issues related to over-voltage protection.

Plans

Planning optimistically to keep on the production schedule, we scheduled the ABCD "Production Readiness Review" (PRR) for 4-Jul of this year.

The target is to have a remedy (likely one of those mentioned above) for this last problem with the added expectation that the further radiation tests in April do not turn up any new problems.

With regard to the yield, we expect that the combination of the new epitaxy sub-contractor and much more careful attention to detail by the Atmel fabrication personnel will move the yield above the minimum guarantee point.

If the remedy to the Vdd Protocol Violation problem requires more time to implement (e.g. a mask change with follow-up fabrication) we could start production of approximately 50% of the ICs to be used on modules only at the outer radii. This could buy us approximately 6 months to execute a final solution but critically depends upon confirmation in the April radiation tests that the problem does not appear until the chips have been exposed to at least 50% of the total expected fluence.

We will make the final decision on whether to proceed with the PRR on 4-Jul or to delay it when the data is reviewed for the Module Final Design Review in late May.

If the PRR is delayed because we must first fully execute a fix to this last problem, the production schedule could be delayed by 6 months.

Systems Engineering

Alex Grillo has been the Electronics Coordinator for the SCT since 1995.

After several failed attempts to recruit an electronics system engineer for SCT at CERN or at one of the other European institutes, Ned Spencer, also from UCSC, has taken on that job.

A comprehensive plan for grounding and shielding has been developed.

This plan is being tested in the SCT System Test Lab at CERN. As of this time, only a small number of modules have been operated simultaneously due to the lack of assembled modules. This number is expected to grow this summer to 18 barrel modules and 18 forward modules.

There is a severe limitation on material inside the tracker volume. This means that each element of shielding must be justified and proven to work.

There is considerable concern about common mode noise injected by the power supplies (custom designed by another SCT collaborator) or picked up on the long cable runs. Work is now starting to analyze these effects and develop proper filtering.

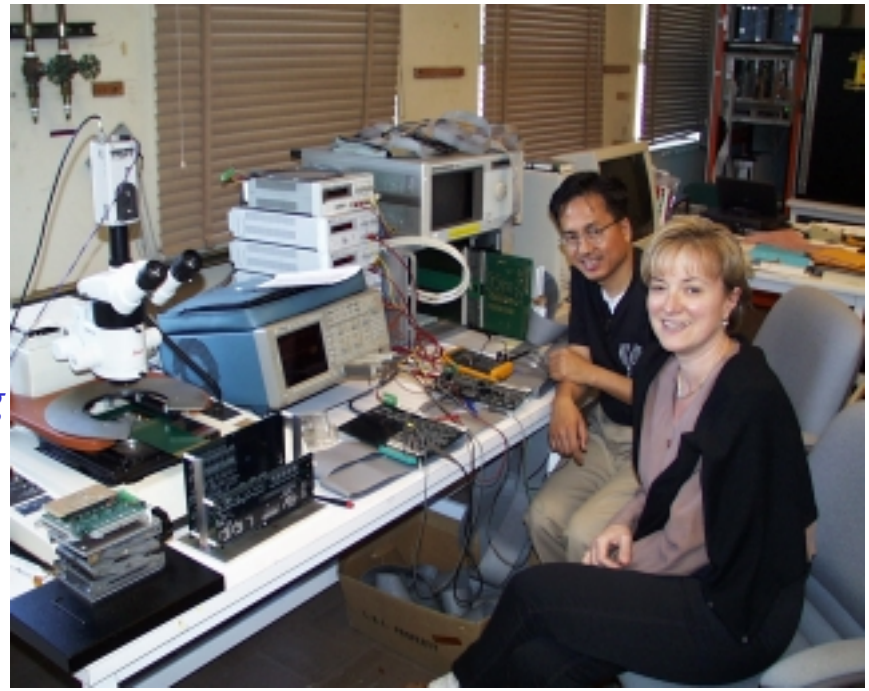
Adding to this challenge is the severely limited space for services exiting the tracker through the calorimeter and muon system.

A detailed power supply specification review was conducted last summer and a grounding safety review for all of ATLAS was held in December. Much work is left to be done but we are finally focused on a coherent plan.

SCT ASIC Tester Development

Original LBNL design (Hubert Niggli)

LBNL - design, hardware production, software
Alessandra Ciocio, Vitaliy Fadeyev,
Chinh Vu, Thorsten Stezelberger,
Gil Gilchriese, Carl Haber,
Francesco Zetti
George Zizka, Helen Chen, Co Tran
Rhonda Witharm



UC SantaCruz – implementation, debugging
Alex Grillo, Abe Seiden,
Max Wilder, Ned Spencer

CERN – Wafer production
and Software for control and analysis
Francis Anghinolfi, Jan Kaplon,
Wladek Dabrowski,
Wojciech Bialas, Carlos Lacasta (Valencia)

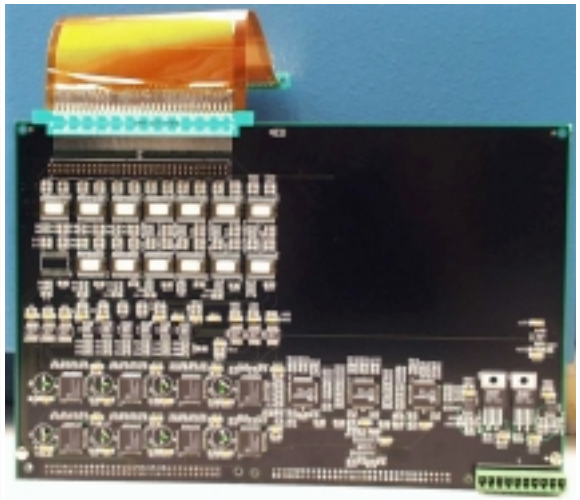
SCT ASIC Tester

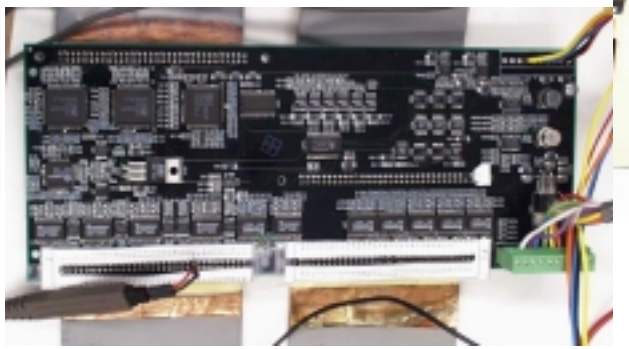
- **SCT DAQ electronics not sufficient to drive chips while under wafer probe**
- **LBL system was developed to allow high speed wafer testing and to scan signal and timing margins.**
- **The full production lot cannot be scanned without this system -> too much time**
- **First version of fully working systems delivered to CERN, RAL, and UCSC (January)**

SCT ASIC Tester

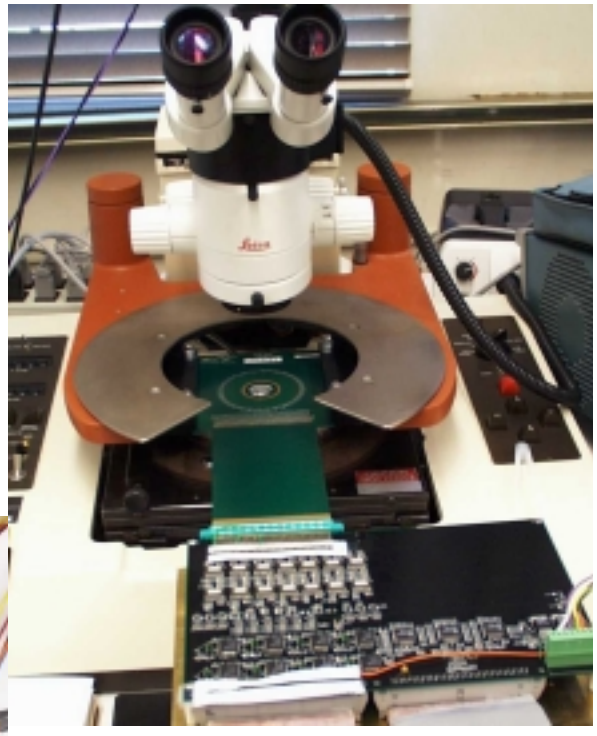
VME Board

Pindriver board(s)



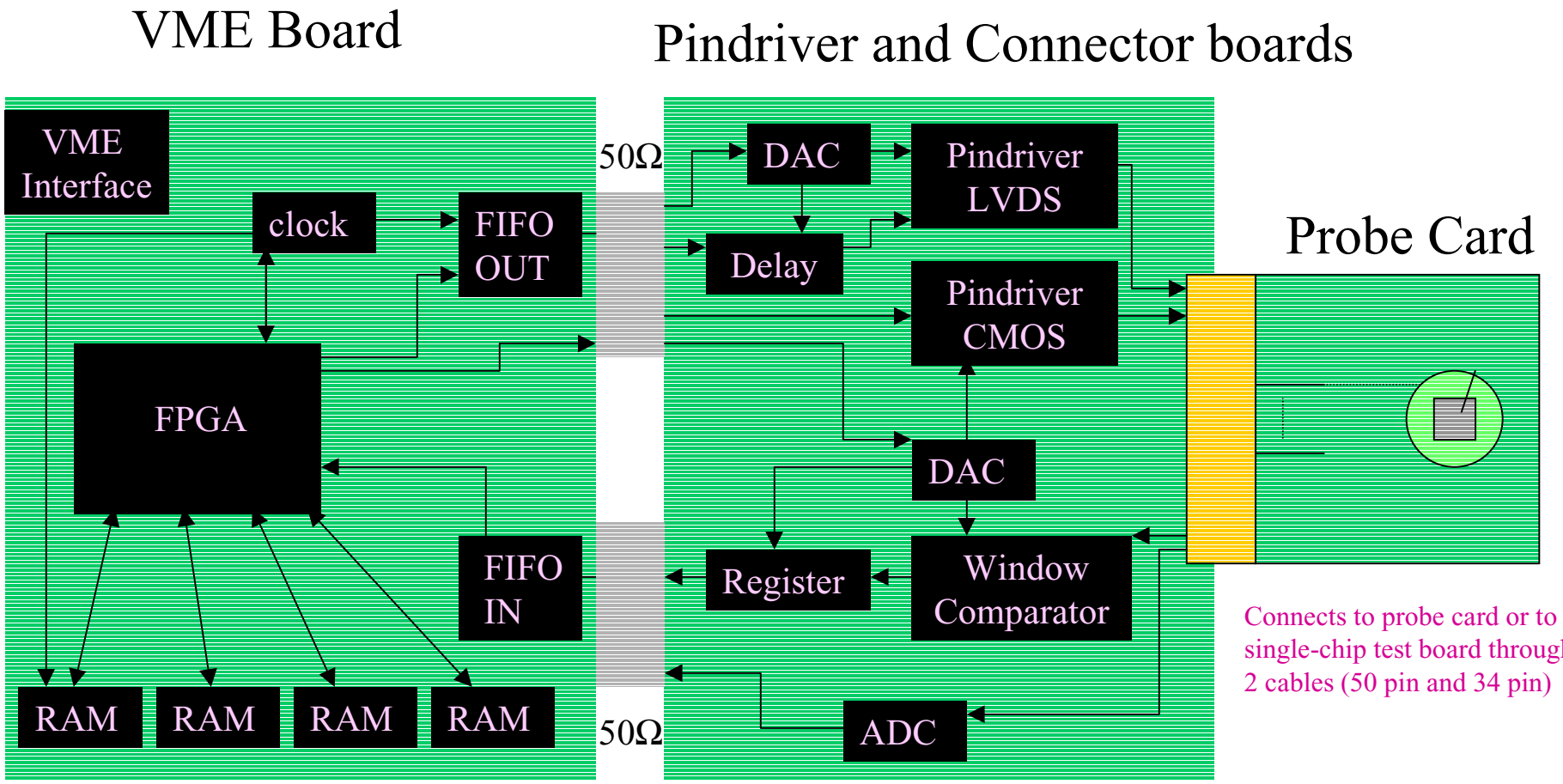


Probe Card



http://www-atlas.lbl.gov/strips/tester/

Overview



Connects to probe card or to a single-chip test board through 2 cables (50 pin and 34 pin)

All operations are programmed in the FPGA using VHDL
On-board comparison of chip response to testvectors with Verilog simulation. The simulation vector is stored in the sim vector memory. The result of the comparison is one bit in the FPGA status register. Frequency from 40-80 MHz

Allow to adjust amplitude and delay of the signals within a range to test functionality of ABCD by feeding signals through pindriver and delay chips. DACs allow varying parameters.
Signals from ABCD go through window comparators.

Status of the Hardware

Major steps for the past few months

- **During the summer 2000 we went through submission of new layout for all boards:**
  VME Board, Pindriver and Connector Boards
  - **We kept the original design but we fixed major bugs**
  - A50 pin and a 34 pin 3M connectors replaced the 128 pins edge connector on Connector Board
  - **We assembled Pindriver and Connector Board in a box with a built-in fan for cooling**

  Probe Card
  - **We designed a custom card to accommodate for different probe stations geometry**
    - Differential pair signals are layout in parallel and on the same trace layer
    - Low frequency filter is applied to the differential threshold lines (VT1, VT2) and Shaper+Preamp Current lines
    - 6 layers (50 ohm matched impedance ,full body gold) in the following order:
      Top traces, VDD, Digital and Analog layer spit plane, Analog ground, VCC, Bottom traces layer

  Single-chip test Board (see slide)
- **We sent one of two prototype systems to Carlos Lacasta (Valencia) to start developing software (July)**
- **Vitaliy Fadeyev (postdoc) joined the LBNL group in July**
- **New system was available at LBNL in September**
- **We sent a first prototype system to CERN (October)**

NEW fully operational systems installed at CERN, RAL, and UCSC in January

Status of the Software

- Stand-alone diagnostic software to perform Threshold Scan and Testvectors at LBNL running on PC/WNT, controlling VME using NI-MXI/PCI interface

- The new system functionality has been merged into CERN Online Control software (Visual C++ application, running on PC/W95 developed by Carlos) and Analogue + Digital tests have been implemented (Verilog simulation is provided by F. Anghinolfi/CERN)

- Beta release of Online Control Software (February 2001)
- Release of offline software for analysis of wafer screening data

- We need to define the additional tests that the new system makes possible, like signal phase and amplitude margins, and higher frequency clocking for a better screen of the IC's.
  The final test specification must be approved by Atmel in accordance with contract for yield guarantee.

- Documentation in progress
- UCSC and CERN have fully working system, RAL still developing integration of local probe station control software into Beta release.

In Progress

- New boards (pindriver and VME) under revision to clean up patches and jumpers. Completion by mid-summer.
- New design of single-chip test card for diagnostics (summer).

- A full comparison of the CERN old system and the LBNL systems will be performed first by testing wafers from current batch to verify same yield results.
- Comparison of new tester systems at CERN and UCSC with same wafers.

- Implementation of new tests (higher frequency, amplitudes and phases) in the control software (work to be done in collaboration with C. Lacasta/Valencia)

- Final version of offline software completed but under installation at different sites

- Getting ready for PRR in July

Concluding Summary
WBS1.1.2 SCT Subsystem

A. Seiden

BNL March 2001

Conclusions From Last Year

1. Rest of this Fiscal Year: very important to establish that the technical design of the SCT detector is sound through building and simultaneous operation of a of a number of modules.

2. The first 9 months of Fiscal Year 01 will focus on pre-production to establish and quantify our ability to do testing and construction.

3. Starting summer 2001 go into full production.

How are we doing on these goals?

- Verification of Technical Design:
  Have irradiated and tested six modules, also have run six modules in system test.

  Will culminate in system test with:

  18 barrel modules

  6 new modules for PS irradiation

  These are the target goals prior to hybrid/module FDR in May, followed by integrated circuit PRR in July.

- # Readiness for Testing and Construction

  Readiness for chip testing: Need to complete wafer tester. This is nearly done. Crucial to reduce test time from 22 hrs/wafer (original CERN tester) to about 5 hours/wafer, our target. Expect to meet target. Will have common wafers tested at all three test locations and with CERN tester to verify that test results are robust.

  Readiness for module construction: Status, now completing mechanics. Plan is to then construct 20 dummy modules. This will be in 2 groups of 10, using successively more realistic parts. Active modules will also be constructed in parallel.

Short Term Schedule (2001)

WBS	Description	Previous	Forecast
1.1.2.1.1 Electronics Design	Production Readiness Review	June 15	July 4
1.1.2.1.3 Electronics Production	Complete Pre-production Fab.	Feb 28	March 30
1.1.2.2.1 Hybrid Design	Hybrid/Module Final Design Review	April 16	May 25
1.1.2.2.3 Hybrid Production	Pre-production Hybrids Available	June 4	Sept 1
1.1.2.3.1 Module Design	Final Design Review	April 16	May 25
1.1.2.3.2 Module Development	Complete Assembly Proto Modules	March 5	May 1
1.1.2.3.3 Module Production	Complete Pre-production Module Assembly	July 30	Oct 30

Some Key Dates:

5/23/01	Complete IC Pre-production Design Verification
	Needed for hybrid/module FDR May 24-25
7/6/01	Start Full Electronics Production
	Follows PRR for Front-end Chips
11/23/01	First IC Lots Delivered
12/16/02	Production Testing of Chips Complete
1/7/02	Start Module Production
	Will Ship 670 Modules
10/13/03	Complete Shipment of Production Modules

Details Shown in Line of Balance Plan

WBS 1.1.2 SCT Wafers and ICs

Line Of Balance Data

All numbers are CUM complete numbers as of 1st of month

Shipments to LBNL shown; remainder of ICs to other assembly sites

	WafersReceived	At UCSC						
	by CERN	Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd	Dice to:	LBNL
Dec-01	120							
Jan-02	120	60	10					
Feb-02	320	60	40	12	776	388		120
Mar-02	320	160	70	40	2,592	1,684		519
Apr-02	520	160	113	70	4,537	3,564		1,099
May-02	520	260	156	113	7,316	5,926		1,827
Jun-02	720	260	199	156	10,095	8,705		2,683
Jul-02	720	360	242	199	12,874	11,484		3,540
Aug-02	920	360	285	242	15,653	14,263		4,396
Sep-02	920	460	328	285	18,432	17,042		5,253
Oct-02	949	460	371	328	21,211	19,821		6,109
Nov-02		475	414	371	23,990	22,600		6,966
Dec-02			457	414	26,769	25,379		7,822
Jan-03			475	457	29,548	28,158		8,679
Feb-03				475	30,666	30,107		9,279
Mar-03						30,666		9,452
Apr-03								
May-03								
Jun-03								
Jul-03								
Aug-03								
Sep-03								
Oct-03								
Nov-03								
Dec-03								
Jan-04								

Status

	WafersReceived	At UCSC						
	by CERN	Wfrs@UCSC	WfrsTested	WfrsCut	GoodDice	DiceShpd	Dice to:	LBNL
Plan								
Acita;								
Delta								

WBS 1.1.2 SCT Modules

Line Of Balance Data

All numbers are CUM complete numbers as of 1st of month

Components as proposed by collaboration March 2001

	FE ICs	Silicon Detectors	Thermal Baseboards	Kapton Hybrids	Assembled Hybrids	Tested Hybrids	Assembled Modules	Tested Modules	Shipped Modules
Oct-01			20						
Nov-01			40						
Dec-01		104	60	30					
Jan-02		208	90	60					
Feb-02	120	312	120	120					
Mar-02	519	416	170	180	10				
Apr-02	1099	520	220	240	35	9			
May-02	1827	728	270	359	70	34	9		
Jun-02	2683	936	330	478	110	68	32	9	
Jul-02	3540	1144	390	597	150	107	65	32	9
Aug-02	4396	1352	450	716	200	146	101	63	31
Sep-02	5253	1560	510	750	250	194	138	99	63
Oct-02	6109	1768	570		300	243	184	135	98
Nov-02	6966	1976	630		350	291	230	181	134
Dec-02	7822	2184	690		400	340	276	226	179
Jan-03	8679	2392	750		450	388	323	271	223
Feb-03	9279	2600			500	437	369	316	268
Mar-03	9452	2808			550	485	415	361	313
Apr-03		3016			600	534	461	406	357
May-03		3063			650	582	507	452	402
Jun-03					700	631	553	497	447
Jul-03					750	679	599	542	491
Aug-03						728	645	587	536
Sep-03							691	632	581
Oct-03								677	625
Nov-03									670

Status

	FE ICs	Silicon Detectors	Thermal Baseboards	Kapton Hybrids	Assembled Hybrids	Tested Hybrids	Assembled Modules	Tested Modules	Shipped Modules
Plan									
Actual									
Delta									

ETC01vs ETC00 Comparison

1.1.2.1 Electronics

Increase in cost of engineering and materials for IC test system+system test support.

Decrease in cost of ICs, more favorable $/Euro rate.

Decrease in systems engineering costs.

Correction of accounting errors and revised inflation estimate based on new schedule.

1.1.2.2 Hybrids

Correction of accounting errors and revised inflation estimate based on new schedule.

1.1.2.3 Modules

Correction of accounting errors and revised inflation estimate based on new schedule.

		ETC 00			ETC 01		
	ETC		TPC	ETC 01		TPC 01	
	Access	Actuals	Access	New Access	Actuals	New Access	
WBS	(in FY00 $s)	Thru FY99	Plus Actuals	(in FY00 $s)	Thru FY00	Plus Actuals	Delta
1.1.2	4,996.4	911.0	5,907.4	4,611.9	1,414.3	6,026.2	(118.8)
1.1.2.1	3,628.2	771.0	4,399.2	3,208.9	1,184.5	4,393.4	5.8
1.1.2.2	463.9	67.0	530.9	488.6	107.9	596.5	(65.6)
1.1.2.3	904.3	73.0	977.3	914.4	121.9	1,036.3	(59.0)

Contingency

Management Contingency in original SCT Plan was $988k, all in IC production costs.

Cash Contingency left for IC Electronics is about $1M.

Cash contingency left for Hybrids and Modules is about $400k.

Total Cash contingency appears more than adequate to cover risks for baseline scope.

Risk Analysis

Items: Parts supplied by other groups (Kapton Hybrids and Baseboards), chips, rate of chip testing and hybrid and module construction.

1. Hybrid (without front-end chips) and baseboard schedules are projected to be well ahead of other construction items.

2. Some possible risk scenarios involving chips and modules:

a) FE IC yield is roughly 1/2 that expected and Atmel delivers extra wafers to meet the contractual guarantee of minimum yield or we have a 6 month delay in starting production. Doubling the number of wafers to test or late start should be handled by a modest increase in manpower costs (doubling the manpower would add about $0.1M), there is already an additional probe station (if needed) in the budget and having multiple test systems (ie, various electronics boards) at each site is already in the budget.

b) There are additional losses of ICs during handling and assembly and about 15% more wafers have to be procured and tested. Procuring an additional 15% wafers would be about $0.3M.

c) We have to roughly double the steady-state rate of module assembly/test, resulting from unexpected delays in delivery of components. Our conclusion is that the current cash contingency for hybrid and module assembly/test (about $0.4M) is probably too low by about $0.1M for this scenario.

Baseline Deliverables:

45% of front-end chips,

670 modules.

Goal with management contingency allocated is to provide 65% of front-end chips.

Rest of SCT has significant cost over-runs in items such as cables and power supplies, which we can't help with. Therefore important to try to supply the full 65% of the chips. We believe there is a good chance that we can do this (and cover risks) within the current cash contingency for the Silicon Strips.

ATLAS Lehman Review, Silicon ROD

March 20 to March 22, 2001

Wisconsin

Khang Dao, Damon Fasching,

Richard Jared, John Joseph,

Mark Nagel, Lukas Tomasek,

Sriram Sivasubramaniyan and

Will Wang

ATLAS Lehman Review, Silicon ROD

Material Covered

- **Major Events**
- **ROD Overview**
- **Current Status**
- **ROD Schedule**
- **ROD Cost**

May 25, 2000 ROD Schematic Review

July 31, 2000 BOC, ROD, TIM Review

ATLAS Lehman Review, Silicon ROD

Major Events

1. May 25, 2000 ROD Schematic Review

"Extraordinary amount of good work was carried out since the Dec. 99 review. There is progress on all fronts, and well-organized team now functioning on both hardware and software."

2. July 31, 2000 BOC, ROD, TIM Review

"The two-day review of the entire Off Detector Electronics System was very informative and provided an excellent opportunity for interaction among the developers, a small subset of the users and the outside reviewers. The developers come from four institutions from the UK and the US and have demonstrated a very satisfactory working relationship in spite of their large geographical separation. The team has the technical expertise to complete the development work and deliver the needed equipment. The presentations and the documentation made available show a good understanding of the requirements and much effort in designing the necessary hardware and software. The review board was impressed by the quantity and quality of the work presented. The presenters are to be commended for their good work. The summary following will concentrate on the concerns and recommendation of the review board. It should not be detract from the good work done."

3. The ROD card infrastructure is tested and functional.

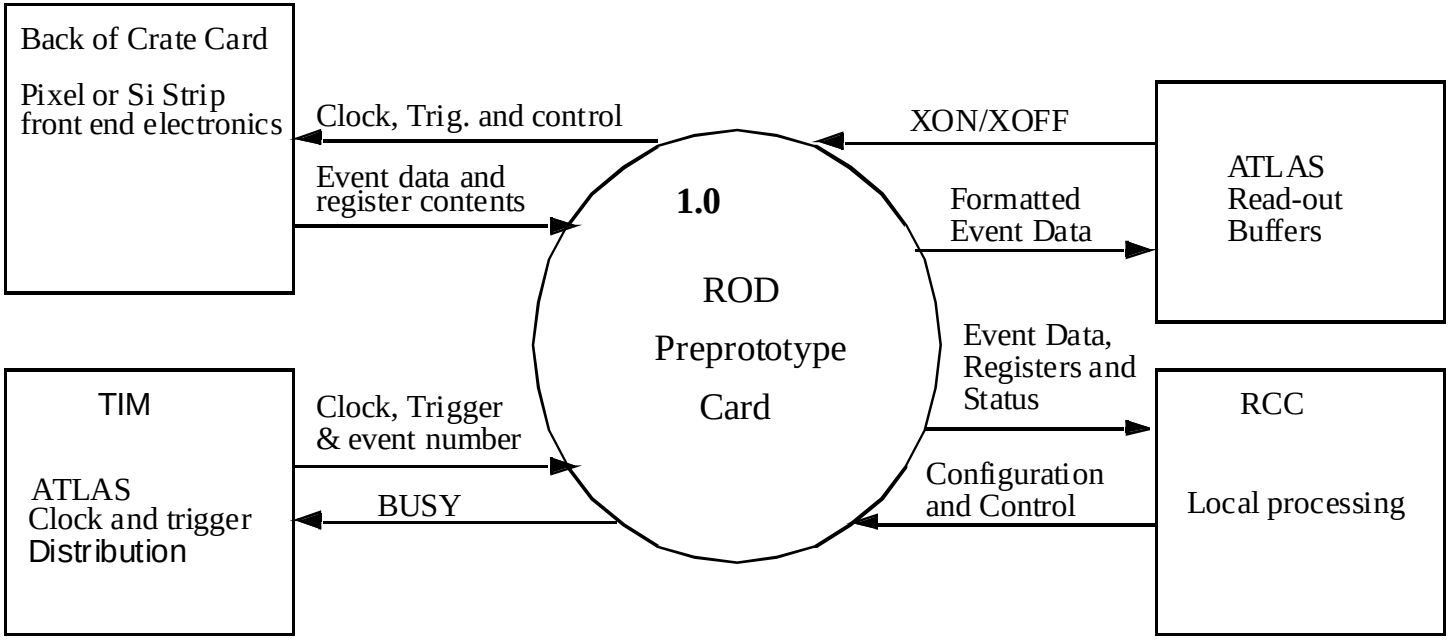
4. The initial test stand software is working.

5. SCT and pixel off detector electronic workshops (4)

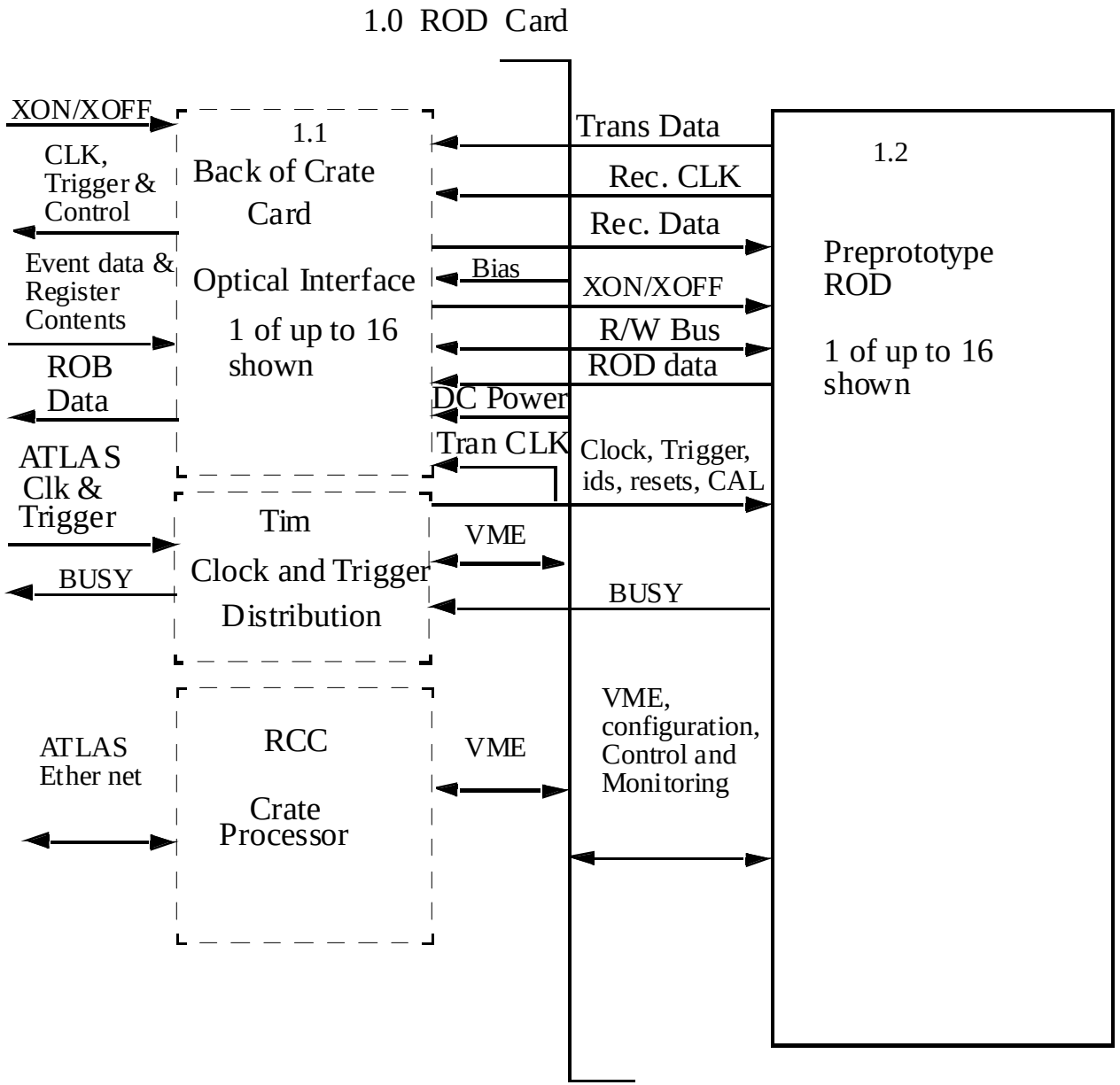
6. Test plan is fully developed, necessary Hardware is fabricated and necessary VHDL and software is near completion.

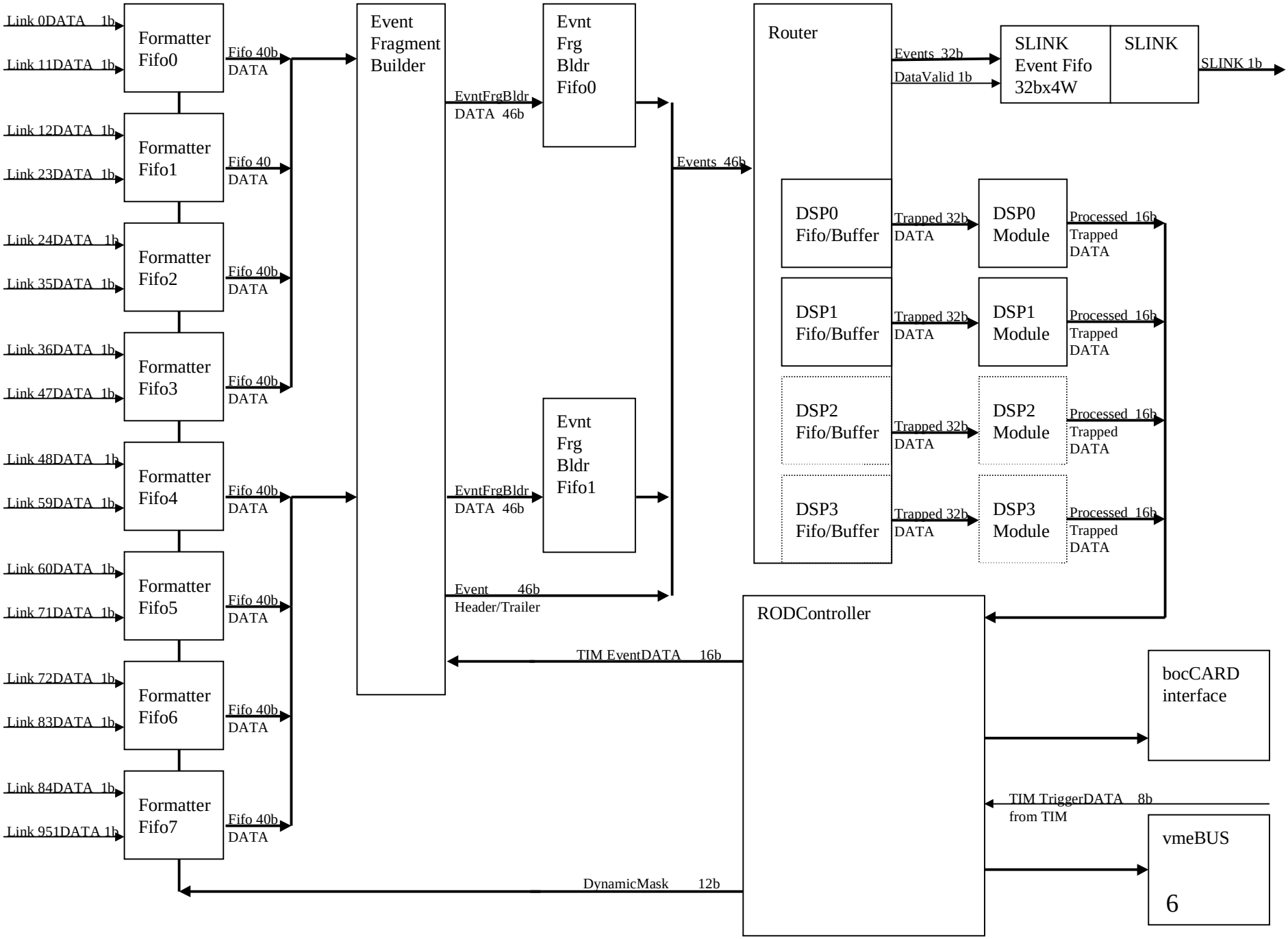
ATLAS Lehman Review, Silicon ROD

ROD Overview

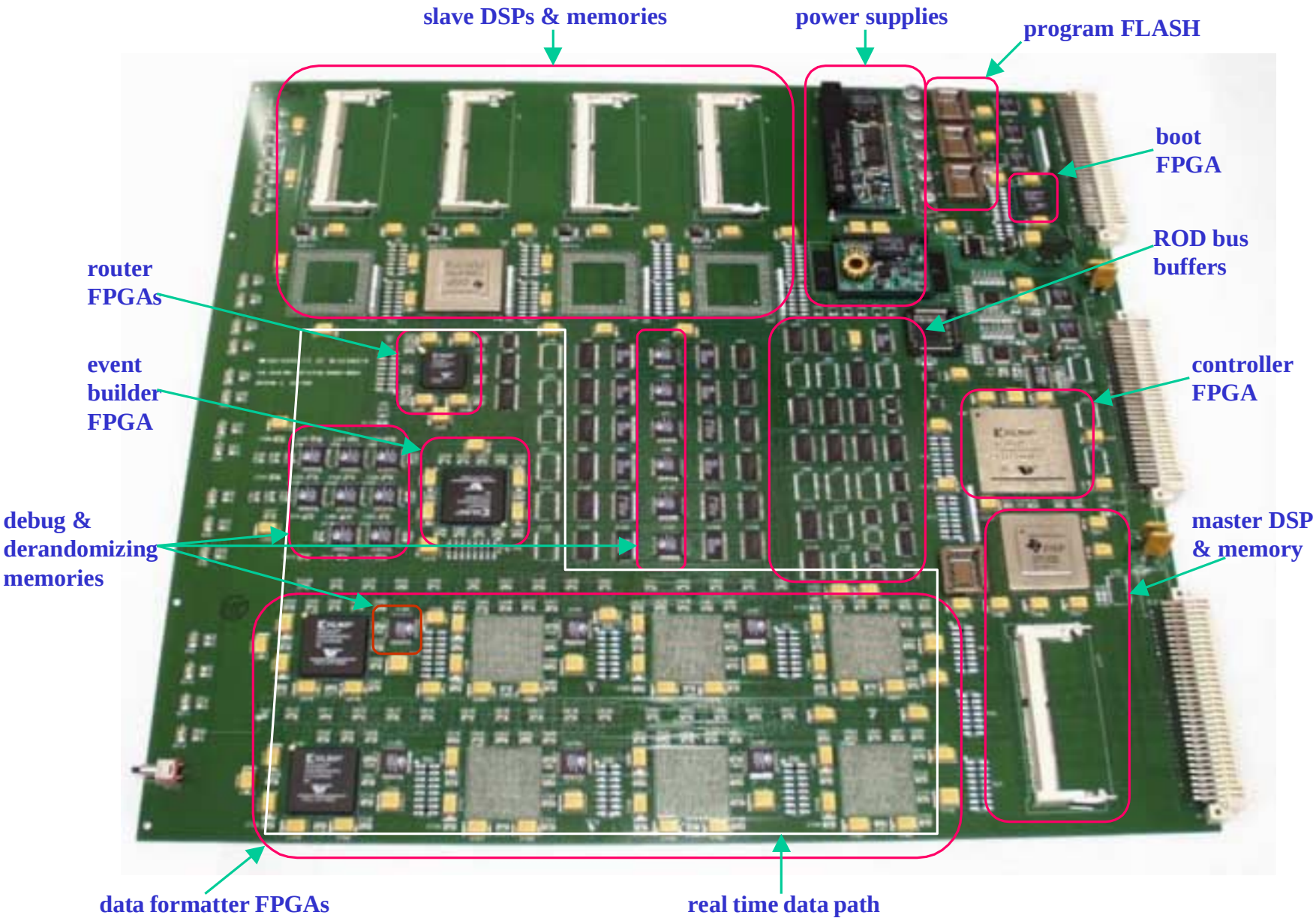


ATLAS Lehman Review, Silicon ROD




Link 0DATA 1b
Link 11DATA 1b
Formatter Fifo0
Fifo 40b DATA
Link 12DATA 1b
Link 23DATA 1b
Formatter Fifo1
Fifo 40 DATA
Link 24DATA 1b
Link 35DATA 1b
Formatter Fifo2
Fifo 40b DATA
Link 36DATA 1b
Link 47DATA 1b
Formatter Fifo3
Fifo 40b DATA
Link 48DATA 1b
Link 59DATA 1b
Formatter Fifo4
Fifo 40b DATA
Link 60DATA 1b
Link 71DATA 1b
Formatter Fifo5
Fifo 40b DATA
Link 72DATA 1b
Link 83DATA 1b
Formatter Fifo6
Fifo 40b DATA
Link 84DATA 1b
Link 951DATA 1b
Formatter Fifo7
Fifo 40b DATA
Event Fragment Builder
EvntFrgBldr DATA 46b
Evnt Frg Bldr Fifo0
EvntFrgBldr DATA 46b
Evnt Frg Bldr Fifo1
Event 46b Header/Trailer
Events 46b
Router
Events 32b
DataValid 1b
SLINK Event Fifo 32bx4W
SLINK
SLINK 1b
DSP0 Fifo/Buffer
Trapped 32b DATA
DSP0 Module
Processed 16b Trapped DATA
DSP1 Fifo/Buffer
Trapped 32b DATA
DSP1 Module
Processed 16b Trapped DATA
DSP2 Fifo/Buffer
Trapped 32b DATA
DSP2 Module
Processed 16b Trapped DATA
DSP3 Fifo/Buffer
Trapped 32b DATA
DSP3 Module
Processed 16b Trapped DATA
RODController
TIM EventDATA 16b
DynamicMask 12b
bocCARD interface
TIM TriggerDATA 8b from TIM
vmeBUS

ATLAS Lehman Review, Silicon ROD



ATLAS Lehman Review, Silicon ROD

Current Status (ROD hardware)

The design of the ROD has been completed.
Simulation of the ROD is complete with the exception of the controller FPGA that is only 90% complete.
Three ROD PC cards have been fabricated.
One ROD card have been partially loaded.
One ROD card have been fully loaded.
Three crates have been delivered.
The fabrication of the ROD test cards that loop outputs to inputs have been fabricated.
Booting of FPGAs and DSPs is working
VME r/w to the program manager works.
VME Read/write via the DSP host port interface to/from DSP program memory, data memory, flash memory, SDRAM memory and controller FPGA is working.
Controller FPGA read/write to ROD bus is working.
The ROD bus communicates to the BOC card, Formatter FPGAs, event fragment builder FPGA, router FPGA and slave DSPs.
The data path has been simulated is being debugged

ATLAS Lehman Review, Silicon ROD

Current Status (ROD software)

Master DSP infrastructure code has been written:

memory map (.h), initialization, process list from RCC state machine, master process list from slave state machine, primitive list handler, interface between master and slave, error diagnostic buffers, transfer text buffer to RCC state machine, readout of slave text buffer state machine, error handling.

The master DSP code for maintaining communication to the RCC when the slave is processing a primitive has being written.

The DSP infrastructure code is complete.

Primitives code has been written:

Echo (diagnostic), R/W field of register or single r/w, r/w block of data, configure slave DSP (on, off and type (error checking, etc.)).

Echo has been tested successfully with the ROD.

Only primitive code needs to be written.

ATLAS Lehman Review, Silicon ROD

Current Status (ROD test stand)

The ROD test stand software for initial testing has been written.

Windows have been tested that support the following:

VME r/w block (supports create and or store for later use) or single register, Master DSP r/w block (supports create and or store for later use), command and status register r/w, Flash memory r/w, Primitive generation (supports create and or store for later use) and r/w data to the ROD locations.

These windows communicate to the following tested modules:

Buffer handler communicates to ROD(regular r/w, list transfer to DSP, poles and transfers text buffers), Primitive list formatter (format list for transfer to ROD), Reply list processor (check sum, converts data and store/distribute data), Host control (initialization, etc), Text buffer processing (formats data, adds headers and place text in files).

The test stand software is functional. It will be refined and improved in the future.

ATLAS Lehman Review, Silicon ROD

Current Status (current work)

The testing of the ROD is ongoing. It is estimated that the ROD will be functional in 4 weeks.

Current work is debugging of the data path.

Concerns:

The ROD is complex. This complexity could result in schedule slippage during the debugging stage.

ATLAS Lehman Review, Silicon ROD

ROD Schedule

Comparison of Old and New Schedule

Task Name	Old Dates	New End Dates
Design ROD Cards	12/99- 8/00	3/01
ROD Prototypes	4/00- 6/01	8/01
ROD Fabrication	3/01- 5/02	6/03
ROD Installation	9/01- 2/05	2/05

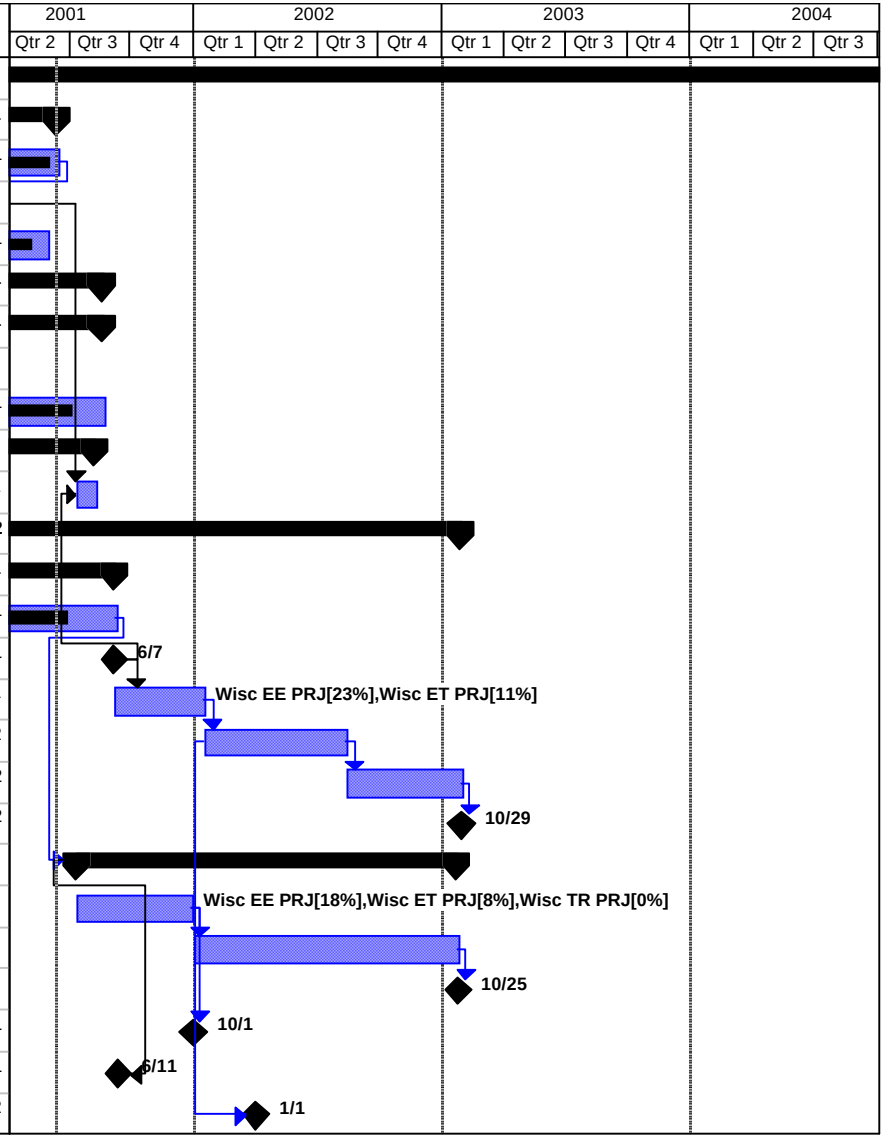
In general there has been about a 5 month slip of the early delivery items.

The project delivery of SCT ROD is about one month late.

ATLAS Lehman Review, Silicon ROD

ROD Schedule

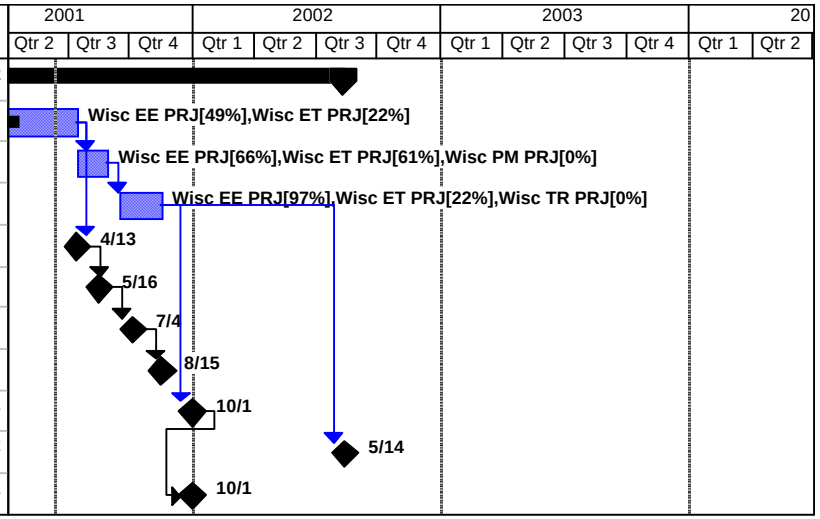
ID	WBS	Task Name	Start	Finish
1	**1.1.3**	**ROD Design & Fabrication**	**Sun 10/1/95**	**Wed 2/2/05**
10	**1.1.3.3**	**Design ROD Cards**	**Thu 12/3/98**	**Thu 3/15/01**
16	1.1.3.3.6	Board Level Simulation	Mon 4/3/00	Thu 3/15/01
17		ROD Prototype Design Review	Fri 5/26/00	Fri 5/26/00
18	1.1.3.3.7	Pixel specific Formater VHDL	Fri 5/26/00	Thu 3/1/01
21	**1.1.3.4**	**ROD Test Stand**	**Mon 12/20/99**	**Mon 5/21/01**
24	**1.1.3.4.3**	**SCT/Pixel Test Stand Software**	**Thu 6/1/00**	**Mon 5/21/01**
26		Production Diagnostic Test Sta	Fri 9/29/00	Fri 9/29/00
27		SCT Pix T.Std S/W FY01 Mat'l/	Mon 10/2/00	Mon 5/21/01
28	**1.1.3.5**	**ROD Prototypes**	**Thu 1/13/00**	**Wed 5/9/01**
32		ROD Prototype PC Loading(7 each)	Thu 4/12/01	Wed 5/9/01
33	**1.1.3.6**	**ROD Prototype Evaluation**	**Mon 7/17/00**	**Tue 10/29/02**
34	**1.1.3.6.1**	**SCT Prototype Testing**	**Mon 7/17/00**	**Thu 6/7/01**
36		SCT Proto Test FY01 Mat'l/Lab	Mon 10/2/00	Thu 6/7/01
37		SCT Complete ROD Proto Testing	Thu 6/7/01	Thu 6/7/01
38	1.1.3.6.2	Pixel Prototype Testing	Thu 6/7/01	Wed 10/17/01
39		Pixel User Evaluation	Thu 10/18/01	Tue 5/14/02
40		Pixel User Evaluation Phase II	Wed 5/15/02	Tue 10/29/02
41		Update Pixel DAQ from User Evalua	Tue 10/29/02	Tue 10/29/02
42	**1.1.3.6.3**	**User Evaluation of ROD in Europe**	**Fri 4/13/01**	**Fri 10/25/02**
43		User Eval of ROD FY01 Mat'l/L	Fri 4/13/01	Fri 9/28/01
44		User Evaluation of ROD Phase	Mon 10/1/01	Fri 10/25/02
45		Update SCT DAQ from User Ev	Fri 10/25/02	Fri 10/25/02
46		SCT ROD User Evaluation Complete	Mon 10/1/01	Mon 10/1/01
47		SCT ATLAS Final Design Review	Mon 6/11/01	Mon 6/11/01
48		Pixel ATLAS Final Design Review	Tue 1/1/02	Tue 1/1/02



ATLAS Lehman Review, Silicon ROD

ROD Schedule

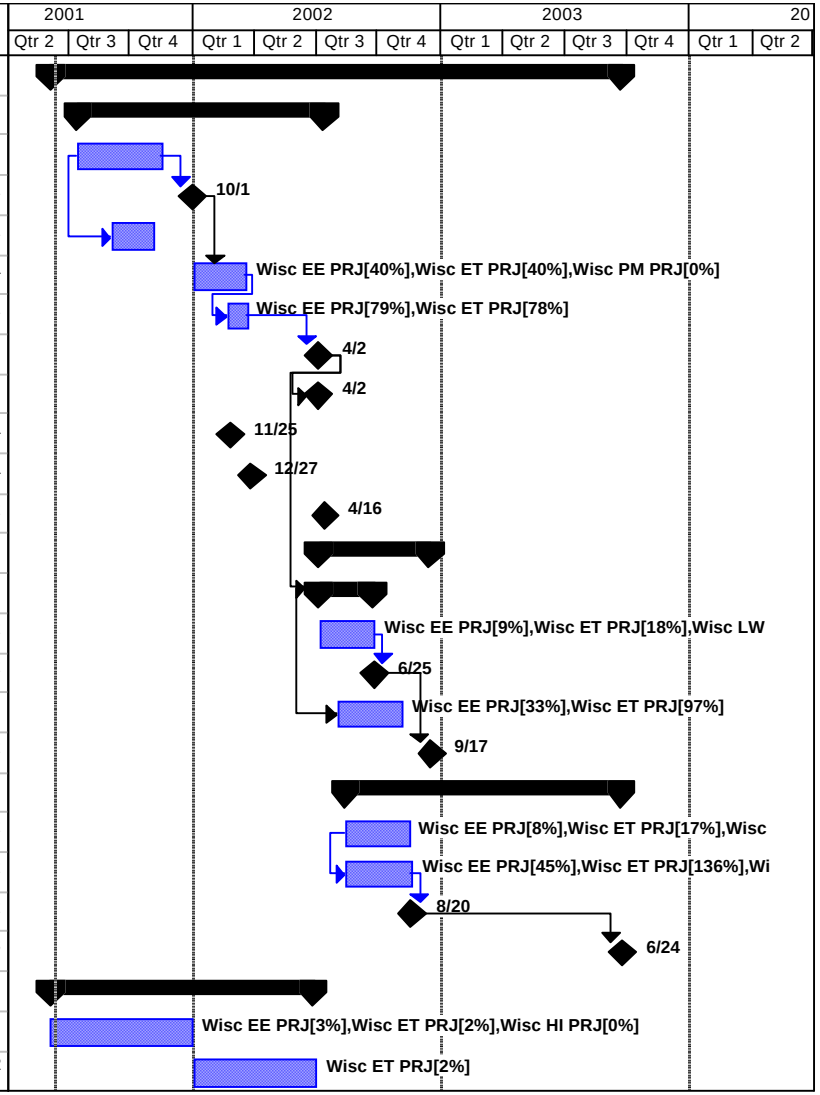
ID	WBS	Task Name	Start	Finish
49	**1.1.3.7**	**Rod Production Model**	**Thu 11/30/00**	**Tue 5/14/02**
50	1.1.3.7.1	Udating of ROD to Production Mode	Thu 11/30/00	Fri 4/13/01
51	1.1.3.7.2	Fabrication of Production Model	Mon 4/16/01	Wed 5/30/01
52	1.1.3.7.3	Evaluation of Production Model	Thu 6/14/01	Wed 8/15/01
53		Start Production Procurements	Fri 4/13/01	Fri 4/13/01
54		Release Production Dwg/Specs	Wed 5/16/01	Wed 5/16/01
55		Release Production Bids	Wed 7/4/01	Wed 7/4/01
56		Bid Evaluation Complete	Wed 8/15/01	Wed 8/15/01
57		SCT ATLAS ROD PRR	Mon 10/1/01	Mon 10/1/01
58		Pixel ATLAS ROD PRR	Tue 5/14/02	Tue 5/14/02
59	**Sil L2/3**	**SCT ROD Design complete**	Mon 10/1/01	Mon 10/1/01



ATLAS Lehman Review, Silicon ROD

ROD Schedule

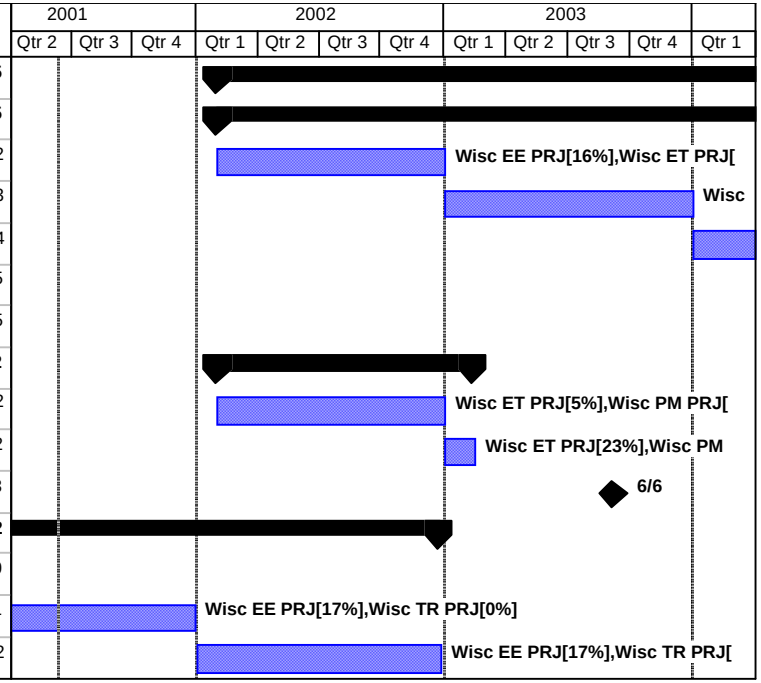
ID	WBS	Task Name	Start	Finish
61	**1.1.3.8**	**ROD Fabrication**	**Tue 3/6/01**	**Tue 6/24/03**
62	**1.1.3.8.1**	**ROD 5% Production**	**Mon 4/16/01**	**Tue 4/16/02**
63		ROD 5% Contract Negotiations	Mon 4/16/01	Wed 8/15/01
64		Project Managers Approval 5%	Mon 10/1/01	Mon 10/1/01
65		ROD SCT & 5% Production Pa	Mon 6/4/01	Thu 8/2/01
66	1.1.3.8.1.1	ROD 5% Production Fabricatio	Tue 10/2/01	Mon 12/17/01
67	1.1.3.8.1.2	ROD 5% Production Debuggin	Mon 11/19/01	Tue 12/18/01
68		ROD 5% Production complete	Tue 4/2/02	Tue 4/2/02
69		Release Management Continge	Tue 4/2/02	Tue 4/2/02
70		Begin First End Cap SCT Modu	Sun 11/25/01	Sun 11/25/01
71		Begin First Barrel SCT Module	Thu 12/27/01	Thu 12/27/01
72		First SCT Full Assembly Test S	Tue 4/16/02	Tue 4/16/02
73	**1.1.3.8.2**	**SCT ROD Production**	**Wed 4/3/02**	**Tue 9/17/02**
74	**1.1.3.8.2.1**	**SCT ROD Production Fabrica**	**Wed 4/3/02**	**Tue 6/25/02**
75		SCT ROD Prod Fabr FY0	Wed 4/3/02	Tue 6/25/02
76		SCT ROD Production Complete	Tue 6/25/02	Tue 6/25/02
77	1.1.3.8.2.2	SCT ROD Production Debuggin	Wed 5/1/02	Fri 8/2/02
78	**SIL L4/2**	Baseline Scope Complete	Tue 9/17/02	Tue 9/17/02
79	**1.1.3.8.3**	**Pixel ROD Production**	**Wed 5/15/02**	**Tue 6/24/03**
80	1.1.3.8.3.1	Pixel ROD Production Fabricati	Wed 5/15/02	Tue 8/13/02
81	1.1.3.8.3.2	Pixel ROD Production Debuggi	Wed 5/15/02	Tue 8/20/02
82		Pixel ROD Production Complet	Tue 8/20/02	Tue 8/20/02
83	**Sil L2/5**	**Pixel ROD Production/Testing**	Tue 6/24/03	Tue 6/24/03
84	**1.1.3.8.4**	**Purchase ROD Crates**	**Tue 3/6/01**	**Thu 3/28/02**
85		Purchase ROD Crates FY01 M	Tue 3/6/01	Fri 9/28/01
86		Purchase ROD Crates FY02 M	Mon 10/1/01	Thu 3/28/02



ATLAS Lehman Review, Silicon ROD

ROD Schedule

ID	WBS	Task Name	Start	Finish
87	**1.1.3.9**	**ROD Shipping, Installation and Repair**	**Fri 11/2/01**	**Wed 2/2/05**
88	**1.1.3.9.1**	**ROD Installation and Repair**	**Fri 11/2/01**	**Wed 2/2/05**
89		ROD Install & Repair FY02 Mat	Fri 11/2/01	Mon 9/30/02
90		ROD Install & Repair FY03 Mat	Tue 10/1/02	Tue 9/30/03
91		ROD Install & Repair FY04 Mat	Wed 10/1/03	Thu 9/30/04
92		ROD Install & Repair FY05 Mat	Fri 10/1/04	Wed 2/2/05
93		ROD Installation/Final commiss	Wed 2/2/05	Wed 2/2/05
94	**1.1.3.9.2**	**ROD Shipping**	**Fri 11/2/01**	**Wed 11/13/02**
95		ROD Shipping FY02 Mat'l/Labo	Fri 11/2/01	Mon 9/30/02
96		ROD Shipping FY03 Mat'l/Labo	Tue 10/1/02	Wed 11/13/02
97		Begin SCT all barrel test at CERN	Fri 6/6/03	Fri 6/6/03
98	**1.1.3.10**	**Project Management**	**Fri 10/1/99**	**Thu 9/26/02**
99		Proj Mgmt FY00 Mat'l/Labor $s	Fri 10/1/99	Fri 9/29/00
100		Proj Mgmt FY01 Mat'l/Labor $s	Mon 10/2/00	Fri 9/28/01
101		Proj Mgmt FY02 Mat'l/Labor $s	Mon 10/1/01	Thu 9/26/02



ATLAS Lehman Review, Silicon ROD

ROD Cost Comparison of Costs

No calls on contingency

No changes in estimate except inflation

ATLAS Lehman Review, Silicon ROD

May 25. 2000 Schematic Review Report

Summary of the May 25, 2000 ROD Schematic Review Report:

Review Board: Gil Gilchrese, Kevin Einweiler, Alex Grillo, Chris Bebek,
Bob Minor, and John fox

ROD Schematic Review
Date: May 25, 2000
Location: LBNL

The purpose of the review is to have permission to fabricate the PC board.

Extraordinary amount of good work was carried out since the Dec. 99 review. There is progress on all fronts, and well-organized team now functioning on both hardware and software.

Status Summary:

The design has now been completed. There is a complete schematic, with all parts and interconnects defined. For the major FPGA blocks, the initial pass through the VHDL is either complete, or estimated to be within a few percent of completion. An initial parts placement was made, and the board has been successfully routed at better than 99% level.

The near-term schedule has the following goals:

* Completing all parts orders for a total of 12 boards. This is essentially done now, but some parts have longer lead times than desired. All parts should be available by middle to late July.

* Loading of first three boards by August 1.

Completion of board level simulations by August 1. There are presently some technical problems in integrating tools from Mentor, Synopsis, and Xilinx, that prevent the board-level simulations from working. This makes it difficult to commit to a schedule.

6/5/00 Note: The current status is that the Mentor, Synopsis, and Xilinx tool are working but the FPGA utilization is 10% higher than the PC based tools. The new version of the Synopsis sysnithesizer will be loaded to see if the utilization will be compatible with the PC tools (new version of Synopsis).
7/17/00 Note: The tools are now working and the board level simulation in progressing on all VHDL code.

Comments on implementation:

A short summary of two areas which were not yet designed in the previous review, and whose implementation is now much clearer:

The board initialization (upon power up) is complex. It is initiated by power-on reset circuits holding off start-up of the Reset Manager FPGA until after all the relevant power supplies have stabilized. Then, the Reset Manager FPGA is configured using standard serial PROMs. This FPGA then configures the other FPGAs by converting the configuration data stored in FlashRAM into the appropriate serial data stream, and emulating the serial PROM protocol to load each FPGA. Similarly, the Master DSP has a FlashRAM available containing the relevant boot code to get itself started.

The VME interface is physically connected to three major objects. Two are FPGAs (the Reset Manager FPGA and the Resource Manager FPGA). The principle connection is to the Host Port of the Master DSP. The paths through the two FPGA are control/status paths. The path through the Reset Manager can be used to re-write the FlashRAM which stores the configurations for all FPGA on the board (except the Reset Manager), and initiate the reconfiguration of FPGAs and DSPs. The real data flow occurs over the Host Port path through the Master DSP. For the present generation of C60 used (C6201), this is a 16-bit port, connected to the DMA engine inside the DSP, which can operate at the same speed as the SDRAM that is being accessed (but only transferring 16 bits each cycle). This VME interface is somewhat complex, but should provide good bandwidth, while automatically resolving contention issues with the DSP CPU, and using the built-in SDRAM controller in the DSP to access the memory.

Concerns:

1) **Initialization of the ROD FPGAs**: A complex sequence of events required to initialize the board has been defined. This begins with a Reset manager FPGA that is initialized from a serial PROM. This FPGA then directs the loading of the configuration data into all of the other FPGA on the ROD. This procedure will take some hundreds of ms, and it is critical to verify that, during this extended time period, there are no major conflicts between bus driver chips, and that all chips are in suitable "default" states. Although the design team has clearly thought through these issues carefully, given the complexity of the ROD design, we recommend that these issues be carefully checked once more.

6/5/00 Note: The FPGA initialization has been reevaluated with no problems found. The tri-state buses have also been reevaluated. No problems with bus contention were found in the schematic. There may be some minor changes to the VHDL code to insure that the tri-state busses are break before make. All control lines will be pulled up with resistors to protect the tri-state drivers during initialization.

2) **Spare Connection Between Parts on the ROD**: The present technique used to map from VHDL to a physical part for placement on the PC board is such that all presently unused pins are left unconnected (in fact, no via is generated, so no access to the FPGA pin would be possible after board assembly). It was felt that, given the aggressive schedule in which board fabrication and board-level simulation will proceed in parallel, this was risky. It is strongly suggested that someone familiar with the detailed data and control flow between the different FPGAs should add an appropriate number of spare pins and wires to allow additional handshakes or data bits that could conceivably be required after completion of all detailed design and simulation. In addition, control pins on auxiliary chips, which might possibly need to be changed from a default ground or VDD setting, should be connected by pull-up or pull-down resistors, so that modifications could be possible. These techniques will significantly add to the range of improvements that could be made after board fabrication.

6/5/00 Note: This area has been reevaluated. The chosen solution is to bring out all unused pins to through hole vias. When connections are need. Wires will be added. This solution was chosen because it is very hard or next to impossible to determine where signals need to be connected. A few dedicated lines were also added.

3) **DSPs in the Real Time Path**: During discussions, it was stated that the present role for the Master DSP included processing real-time interrupts for each L1 trigger (100KHz maximum rate). Although some latency is tolerable here, this was still felt to be a somewhat riskier approach. In addition, it includes the DSP as a critical element in the ROD data path. This means that the board-level simulations which are needed to determine the ability of the ROD to meet the critical rate and bandwidth requirements will also have to include some fairly detailed model for the DSP (technically, it is not clear how to implement such a model). A lower risk approach would involve attributing this critical task to the ROD Resource FPGA, which the Master DSP could influence in a "non-realtime" manner by for example making a request to drop an event on some links to restore synchronization.

6/5/00 Note: The plan is to take the real-time path out of the DSP. The resource manger will contain the code in VHDL.

4) **Diagnostic Capabilities**: The present ROD design has extensive diagnostic capability, in many cases implemented using a large number of bidirectional buffers and latches to direct data flow between special memories. This allows injecting test data before each major circuit block, and then capturing it after each block. We would like to see a more detailed investigation of what fraction of faults on a board (PC fabrication faults, and/or component faults) can be detected by the types of algorithms that would be used in the test system. Typically, data paths are easy to test, but there are often many miscellaneous control lines that are equally critical, but harder to test. What fraction of the connectivity and functionality of the board can be easily checked?

6/5/00 Note: This will be studied.

5) **Library Parts Verification**: There was a concern (based on previous experience) about the number of parts in the parts database which were generated for this board at LBL Error-free entry of all pins is difficult, and finding minor errors, etc. can be difficult. We urge careful cross-checking of these parts before submission of the PC board for fabrication.

6/5/00 Note: A check of the parts has been made. No errors were found. A further check will be made in the next week with two people checking each others work.

6) **Selection on Pins on FPGAs**: The description of how the assignment of signals in the VHDL to FPGA pins was made raised some issues. One issue was whether the placement of complete busses of 30-40 pins within a particular I/O bank on the Xilinx parts exceeded recommendations on the number of simultaneous transitions. In addition, there was a concern about how much flexibility was left to the place and route tools for the future. The concern was that by freezing the pin assignment in a (possibly) somewhat unnatural configuration it would become increasingly difficult to successfully route the parts as VHDL changes occurred in the future. Careful attention should be given to the internal constraints on connecting CLB's and I/O pads to try to minimize the possibility of the chosen pin assignments causing such "getting trapped into a corner" routing problems as the ROD firmware evolves.

6/5/00 Note: The pins on the router have been released to be selected by the Synopsis tool. This was the only FPGA that had forced pins for busses. The I/O bank on the Xilinx part have been checked for over current. No problems were found.

7) **Verification of Printed Circuit Board Connections**: The proposed PC board is very complex, and manufacturer test is a concern. We urge the design team to explore whatever techniques the board vendors have at their disposal to try to assure a high-quality board. Beyond the usual flying-probe continuity test, it is not clear what options exist. This concern involves both the debug time of the initial small number of PC boards, and the production risks for larger numbers of cards (since the cards can only be tested once all components are loaded).

6/5/00 Note: Holmes is contacting venders to find alternatives that will check the ROD PC card.

8) **Protection of the ROD from Over Temperature**: We were presented with a first power analysis on the board, which did not look unreasonable (85W). Given the high power densities on the card, it could be useful to investigate some type of thermal monitoring to detect over-temperature conditions.

6/5/00 Note: A thermal switchs will be added to the ROD. These switchs on over temperature will place all FPGAs and DSPs in the initialization mode (standby power state). This will reduce the power on the card to a minimal value. The crate over temperature sensor (normal part of the crate) will be relied on to turn off crate power in extreme circumstances. The status of the ROD temperature sensor will be displayed on the front panel.

9) **Development of a Testing Plan**: The general issue of a test plan was. It is not clear whether it will be easily possible to debug a complete card, or whether it would be useful to begin with a partial loading of at least some cards. This raises issues of BGA loading and replacement capabilities needed during testing (for example, can additional BGA be easily added to a partially loaded board). Also, the DSP debug environment will be critical. Presently, the JTAG interface required to connect the development system is provided for each DSP on a separate connector. We strongly encourage the design team to be thinking through some of these issues during the period of board fabrication, so they can "hit the ground running" once the first boards are fabricated.

6/5/00 Note: A testing plane will be developed.

ATLAS Lehman Review, Silicon ROD

May 25. 2000 Schematic Review Report

10**) Design Rule Checking**: There is some concerned about the amount of design-rule checking that has been done as part of the Mentor schematic editor. I think the design group should confirm that the fanouts and electrical loading of the I/O ports on the EPLDs, and of the other parts on the board is OK. We worry a little bit about the timing of the various 3-stated multiplexed busses, because without any timing verification. Were concerned that skews or delay variations are going to have possible bus contention problems as slow drivers stay on a little bit while fast drivers turn on, leading to high-current transients in the bus structures.

6/5/00 Note: The design has been changed to have all I/O to/from the ROD going through buffers with the exception of the VME interface that is designed to be connected directly to the VME bus.

Concerns from previous review revisited:

1) **ESD Protection for the ROD**: Concern was expressed on the question of physical I/O protection. The board will contain many low-voltage complex parts which will be very sensitive to static. Particularly for FPGA's which power on with their I/O pins configured in a sensitive mode, there was concern that the basic interface to the BOC through the backplane would be very sensitive to grounding. Given that these boards will surely not be handled with full ESD precautions over their full lifetime, it would be worthwhile to study all I/O lines connected to the outside, and make sure that they have adequate protection against ESD, perhaps only in the form of pull-up or pull-down resistors to ensure that a low impedance is always defined.

6/5/00 Note: The design has been changed to have all I/O to the ROD go through buffers with the exception of the VME interface that is designed to be connected directly to the VME bus.

Conclusions:

We propose that the group should go ahead and fabricate PC boards based on schematics which would be very similar to the ones we were shown during the review. The risk of errors (due to the lack of completion of the board-level simulation effort), seems to be more than balanced by the need to get boards into the hands of users for evaluation as soon as possible. However, we feel strongly that the ROD prototype would benefit from the completion of the board-level simulation effort on the earliest possible time scale, preferably before loaded boards enter the initial test phase.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

BOC, ROD, TIM Review July 31 to August 1, 2000

Review Board:
Murdock Gilchriese, John Fox, Bob Minor , Abe Seiden, Larry Premisler, Alex Grillo, Kevin Einsweiler and Paul Keener

Participants:
John Lane. (TIM), Martin Postranecky (TIM), Dominic Hayes (TIM)
Eli Rosenberg (Pixel DAQ)
Maurice Goodrick (BOC)
John Hill (SCT DAQ)
Mark Nagel (ROD) , Damon Fasching (ROD), Lukas Tomasek (ROD),
Richard Jared (ROD) and John Joseph (ROD)

Summary Off-Detector Electronics Review 31-Jul/1-Aug-2000

The two-day review of the entire Off Detector Electronics System was very informative and provided an excellent opportunity for interaction among the developers, a small subset of the users and the outside reviewers. The developers come from four institutions from the UK and the US and have demonstrated a very satisfactory working relationship in spite of their large geographical separation. The team has the technical expertise to compete the development work and deliver the needed equipment. The presentations and the documentation made available show a good understanding of the requirements and much effort in designing the necessary hardware and software. The review board was impressed by the quantity and quality of the work presented. The presenters are to be commended for their good work. The summary following will concentrate on the concerns and recommendation of the review board. It should not be detract from the good work done.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Key global items that should be addressed:

1. The BOC-ROD-TIM team should plan on an integrated ATLAS FDR by February 2001. An integrated schedule should be part of this review, and thus should be available for internal review in the US and UK by early December at the latest.
Note9/15/00: The Off Detector Electronics (ODE) group will try and meet the review date. Jared will coordinate producing an integrated schedule by Oct 1, 2000.

2. Having test results from all of the BOC-ROD-TIM, particularly together, was deemed very aggressive to meet the February FDR schedule. An integrated test plan, with responsibilities assigned, should be developed immediately so that it can be reviewed by the appropriate SCT, Pixel, UK and US entities by the end of September.
Note9/15/00: A plan has been developed by Cambridge (J. Hill) for the testing of the ODE crate and cards.

3. The SCT need for BOC-ROD-TIMs is substantially in advance of the current Pixel schedule and there is some risk that freezing the design too early, necessary for the SCT, may cause problems for the Pixels. This needs to be addressed directly in the integrated schedule, by a combination of sufficient design flexibility and/or phased fabrication.

4. Finally, the goal to complete the fabrication and testing of the RODs and probably the BOC and TIM (need integrated schedules) by early 2003, practically guarantees that some parts for these items will be obsolete by the time of commissioning in 2005 or so. There should be a clear proposal how to handle this situation for the February FDR with a final proposal to be ready by the ATLAS PRR.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Global Issue:

L1 Latency:
There is a time budget for each component. The design of TIM, BOC and ROD indicate that they will meet their budget maximum. It will be important to confirm the time budgets in the system test at Cambridge in the November-December 2000 test.

SCT Module Reconfiguration:
Single Event Upsets (SEU) measurements are starting to be made on the FE ASICs. As expected the rate is non-zero. A plan needs to be developed between FEE group and Off-Detector Group to handle the to be measured rate of SEUs. This plan should include the possible use of the periodic reset.
Note9/15/00: When the rates are understood a plan will be developed.

Module Testing:
It became clear during the review that it will not be an easy task to test all of the components in the ROD crate in fully realistic conditions. One ROD crate services such a large number of detector modules that there will not be enough detector modules in existence to connect a full complement of modules to a ROD crate, not even a full complement for one ROD/BOC card, until much later than the planned FDR. The group is encouraged to look at alternatives which could test all the requirements of the ROD crate in a more piecewise fashion.
Note9/15/00: Three cards are being fabricated that will provide testing of I/O pins between the ROD and BOC. In addition partially loaded ROD in memories (play or record) will be used with a optical to electrical and electrical to optical being designed at Cambridge to test optical fiber inputs and outputs.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Spare Pins:
There should be an effort to try to increase the number of spare pins on each connector to allow for future changes. There were some connectors that have 0 spare pins.
Note9/15/00:This item will need to be evaluated in detail in November 00.

ROD Crate Testing:
A plan should be developed that outlines how each element of the combined TIM/BOC/ROD requirements can be demonstrated prior to the PRR. This could specify a different test for each element of the requirements even though no one test set up emulated the entire SCT or Pixel environment.
Note9/15/00: Each cards test plan will measure the requirements compliance prior to the Cambridge test. The Cambridge test plan will measure system performance.

Integrated Schedule:
An integrated schedule for all components of the Off Detector Electronics showing activities through the completion of production units is needed.
Note9/15/00: An integrated schedule draft will be produced by Oct 1, 00.

SLINK Interface:
It should be made clear to the ATLAS DAQ Group that we plan to use the mezzanine SLINK card and that the electrical interface, connector and form factor of that card must be frozen at the time of the Off Detector FDR (i.e. Feb-2001). There must be sign-off by someone in ATLAS-DAQ for that.

Pixel Module Interface:
A formal interface document describing the Pixel data stream is needed.
Note9/15/00: We will attempt to have the pixel module people write the interface specification.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Back Of Crate (BOC) (Optical Interface) Items:

Requirements:
BOC requirements need to be more quantitative. Such as detailed information of the command delay range.
Note9/15/00: The requirements are being updated.

BOC without ROD:
A check should be made if the BOC "idles" in the right state if its corresponding ROD is unplugged.
Note9/15/00: This will be investigated by Oct 30, 00. Future BOC designs will have a local clock that will maintain clocking to the modules when other components/cards fail.

BOC laser interlock:
There was much discussion of the interlock mechanism whereby fibers from the on-detector electronics are disabled if unplugged at the BOC. The interlock system must be understood and implemented.

BOC schedule:
The short term schedule is understood but the long term schedule needs to be developed.

BPM12 and VCSELS12 Parts:
The availability of BPM12 and VCSEL12 parts must be monitored. The time they are needed should be clearly marked on the integrated schedule so it can be tracked with the Links Group.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Read Out Drivers (ROD) Items:

Temperature of ROD PCB
Temperature sensors on the ROD PCB will trip at over temperature. Not clear what temperature the "hot" ICs will be at that point. Need to measure IC package temperatures at PCB trip point and make sure this is below spec limit for packaged ICs. ROD card over temperature monitor needs to be read out remotely- not
just as an led on the card.
Note9/15/00: The trip state of the temperature sensor readout is still open. The temperature of the ICs and board will be measured.

ROD Cost:
The parts cost are stable at the 10% level. The new pricing from Xylinx seems to indicate they are favoring their new products and discouraging older ones. We should determine if some of these older products which are designed into the ROD are going to obsoleted soon. If so, we need to plan accordingly with larger/earlier buys or designing in another part.
Note9/15/00: This will be evaluated in early 2001 after the system test is running.

ROD Simulation:
Simulation of the data path is 75% complete. Simulation of the logically more complex controller section has not begun. This is unfortunate since this section of the board is required to function early in the debugging process. The simulation must be completed to aid in debugging.
Note9/15/00: Simulation of the data path is complete. The controller simulation is starting.

Requirements:
The requirements document is stable.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

DSP Software:
This seems to be well advanced. The host-masterDSP and masterDSP-slaveDSP communication protocol is done and in fact is done very symmetrically. I like the attention paid to communicating error messages to the host. How to handle these error reports is still in development.

Test Stand:
Software is impressive. It is hard to anticipate if it will meet the demands of the board debuggers, ie, how flexible and easy is it execute new sequences of commands.

ROD Test Plan:
A sequence of steps for commissioning the first ROD board was presented. It seemed to progress logically from the VME interface to greater board depths such as booting FPGA's and testing memories and data paths. The plan is in the early stage of development. A detailed test plan needs to be developed that determines if the requirements have been meet.
Note9/15/00: A detailed test plan has been generated. This plan compares requirements to test.

Pixel anxiety

No pixel specific VHDL code exists to "prove" that ROD can deal with pixel issues. Einsweiler asked how can ROD get through a February FDR without this crucial input. In the end, the answer seems to be, "Too bad. If a different ROD is needed by the pixels it will be developed when the pixel system is stable."
Note9/15/00: Pixel ROD VHDL has been almost completed. Board level simulation needs to be performed after the SCT prototype ROD is functional. It is planned to use the test card that generate input patterns to fully test the known front end operations. This will help with understanding of the ROD performance for pixels.

ATLAS Lehman Review, Silicon ROD

July 31, 2000 BOC, ROD,TIM Review

Timing Interface Module (TIM) Items:

Requirements: TIM requirements need to be more quantitative.
Note9/15/00: The requirements have been updated and are in review.

TIM Simulation:
TIM is designed and in fabrication. The implementation is smallish CPLD's which can be individually simulated but their interaction cannot. The commissioning may take some time as the IC interaction are not simulated.

TIM Design Changes:
There is discussion about future incorporation of deadtime statistic accumulation per ROD. Fox pointed out that this might be doable with unused resources on each ROD. Another future change to the design is to mount the TTRx logic directly on the PCB instead of continuing with an "ATLAS standard" daughter board. There is concern that changes as the board is being fabricated may lead to schedule slippage.

VME Addressing:
It was stated that a switch is used to set the board base address. From the discussion that followed it, seems that the ROD used the nGA lines on the backplane to establish the board base address. It did not sound to be strictly VME64x compliant, but it will work fine. The TIM should do what the ROD does so that there is no confusion later on with TIM encroaching on ROD address space due to a mis-set switch.

TIM Schedule:
7 October - Two TIM boards are thought to be available.

ATLAS Lehman Review, Silicon ROD

May 25. 2000 Schematic Review Report

ROD Crate Controller (RCC)

RCC Software:

It is not clear what software is need in order for the Off Detector PRR to be completed. The RCC Software development should be included on the Integrated Schedule. It appears that there may be a manpower shortage in this area. Some estimates should be made of what is needed and then discussed with the SCT Steering Group if there is not sufficient manpower within the Off Detector Electronics Group.

Note9/15/00: The ROD test stand software will be initially used for testing. This software will be expanded to meet the system test needs. Cambridge and Wisconsin are in close communication on the design of the test stand software.