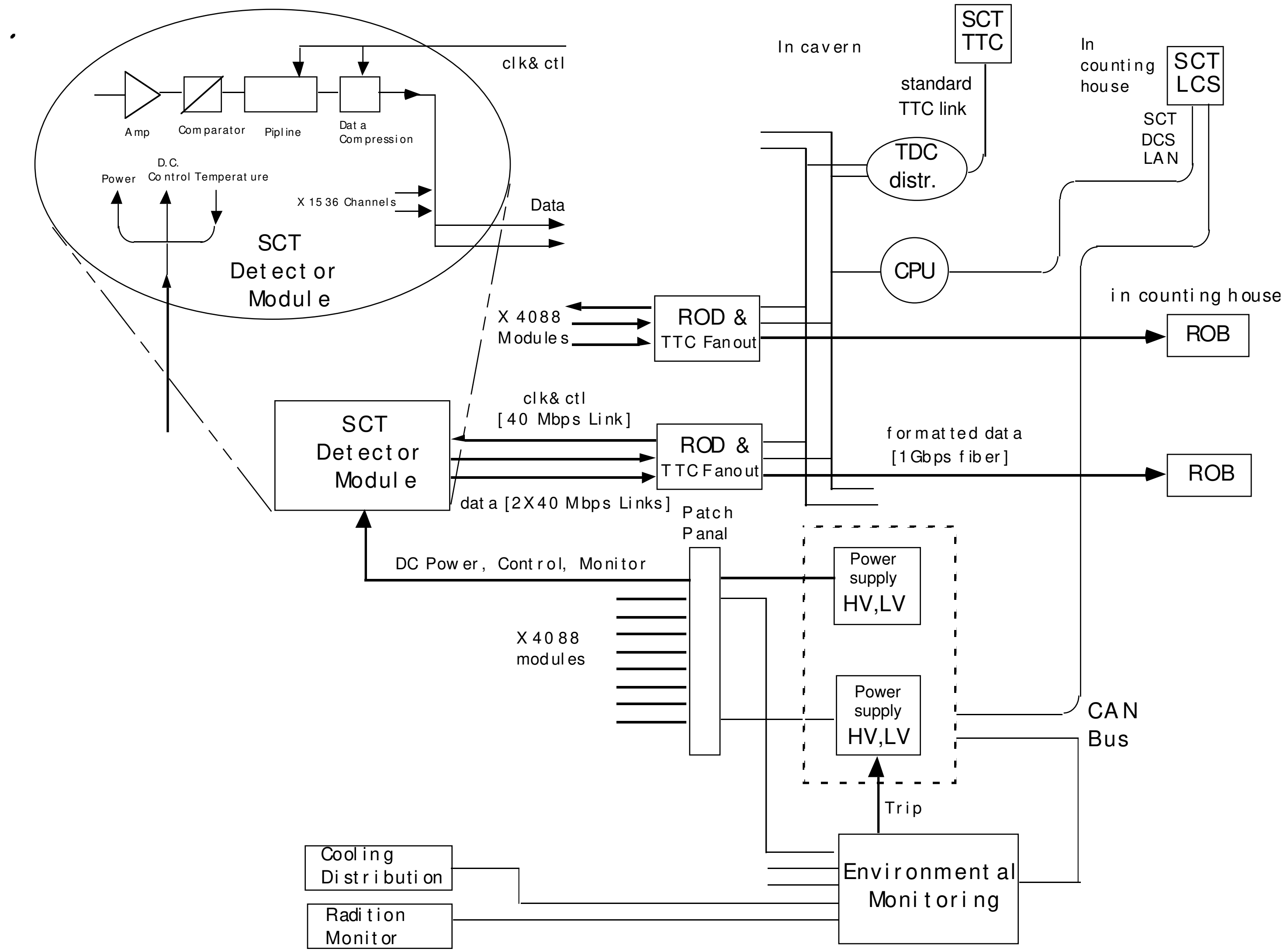
WBS 1.1.2.1
ATLAS SCT Electronics: Status

US ATLAS DoE/NSF Review
6/8-October-1998

Alex Grillo

SCT Readout Electronics Block Diagram



Specifications

Many specifications are now available to define the design of the full readout electronics.
They are available on the Web for easy reference with links from the ATLAS/SCT Web pages.
A procedure for Document Control is now under discussion and will be implemented soon.

Front-End ICs:	
CAFE-M Specification:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
ABC Specification:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
ABCD Specification:	**http://schp5.unige.ch/atlas/atlaspage/module/elect/home.html**
Data Links:	
DORIC Specification:	**http://www.cern.ch/Atlas/GROUPS/INNER_DETECTOR/sctnew/Electronics/links/**
BiPhase Mark Encoding Chip Spec:	**http://www.cern.ch/Atlas/GROUPS/INNER_DETECTOR/sctnew/Electronics/links/**
LDC Spec:	**http://www.cern.ch/Atlas/GROUPS/INNER_DETECTOR/sctnew/Electronics/links/**
Power Supplies and Cables:	
Power Supplies and Distribution Reqs Doc:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
Grounding Plans:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
Off Detector Electronics:	
Off-Detector Electronics Reqs Doc:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
ROD Essential Model:	**http://positron.ps.uci.edu/~rodatlas/rodwork.html**
ROD Input Data Format:	**http://positron.ps.uci.edu/~rodatlas/rodwork.html**
ROD VME Interface Req Doc:	**http://positron.ps.uci.edu/~rodatlas/rodwork.html**
ROD Slot Pinout:	**http://positron.ps.uci.edu/~rodatlas/rodwork.html**
Various ROD99 (prototype ROD) specs:	**http://positron.ps.uci.edu/~rodatlas/rodwork.html**
Monitoring and DCS:	
DCS Requirements Document:	**http://scipp.ucsc.edu/groups/atlas/sct-docs.html**
Draft Technical Proposal for DCS in SCT:	**http://www.tsl.uu.se/~brenner/atlas/dcs/dcs.html**

Front-end (On Detector) ICs

There are two options being pursued for the Front-end ICs:

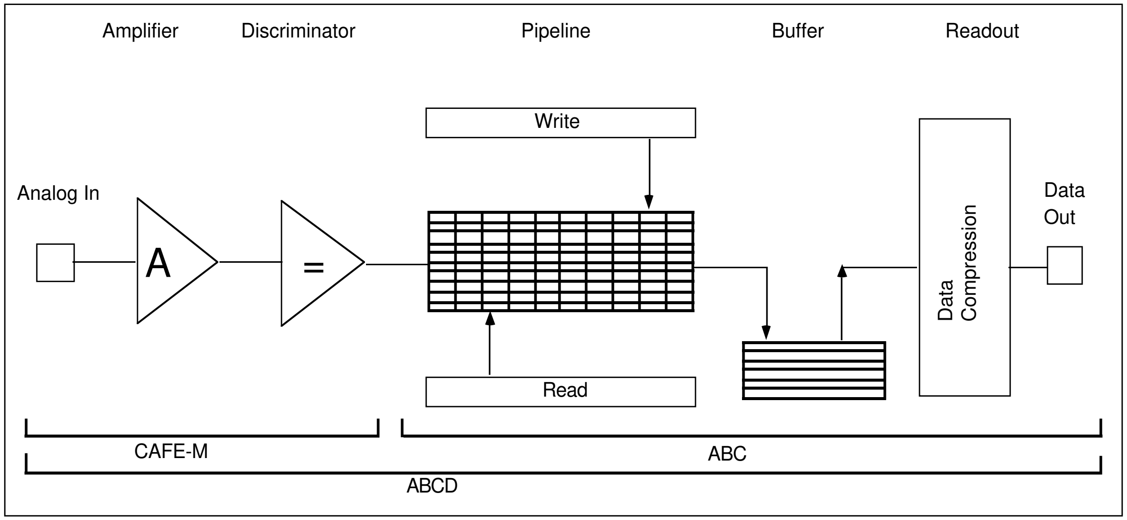
Two chip solution: **CAFE-M fabricated on Maxim bipolar process**
ABC fabricated on Honeywell rad-hard CMOS process

One chip solution: **ABCD fabricated on the rad-hard DMILL biCMOS of Temic**

The two different solutions are tailored to make use of the available rad-hard processes and maintain at least two suppliers until final production orders are placed.

Both solutions use identical architectures.

They are designed to meet identical specifications,
are functionally the same and
differ only in some circuit implementations dictated by the different processes.



CAFE-M Status

The CAFE-M was fabricated in 1997 as the first full function prototype.

It followed previous similar designs: ICs used in ZEUS, NA50 and prototypes for SSC and ATLAS.

Detailed design verification has been conducted on the CAFE-M.

All functions have been tested.

Some requirements are still to be checked using the accompanying ABC readout chip because they are a shared function, e.g. double pulse resolution.

The IC meets all other requirements before irradiation

After irradiation to full ATLAS dose, the channel-to-channel matching deteriorates to 24% (1 σ).
The matching before irradiation is 4%.
The cause of this problem is now understood and a fix is being designed.

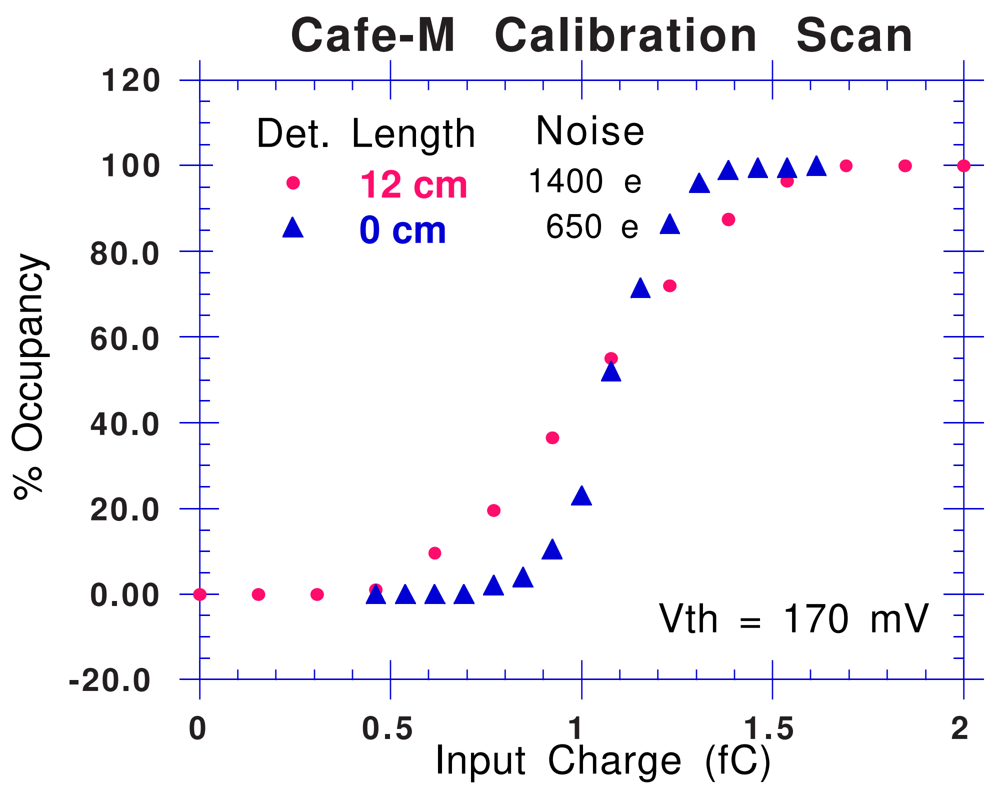
Two wafers were sorted using the automated wafer tester developed at LBL.

The tester performs a full AC test on each of the 128 channels of the IC with threshold scans.

Auxiliary functions (e.g. internal calibration control) are not yet tested but are being added.

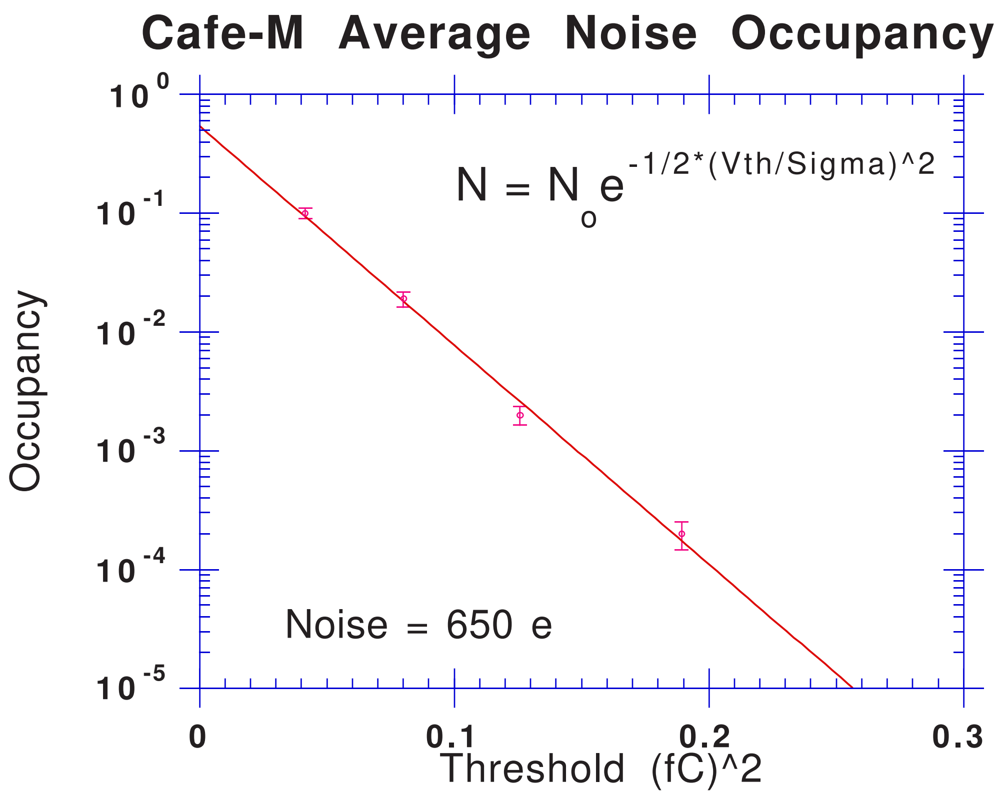
The cumulative yield was 61% which is about as expected.

Threshold Scans of CAFE-M

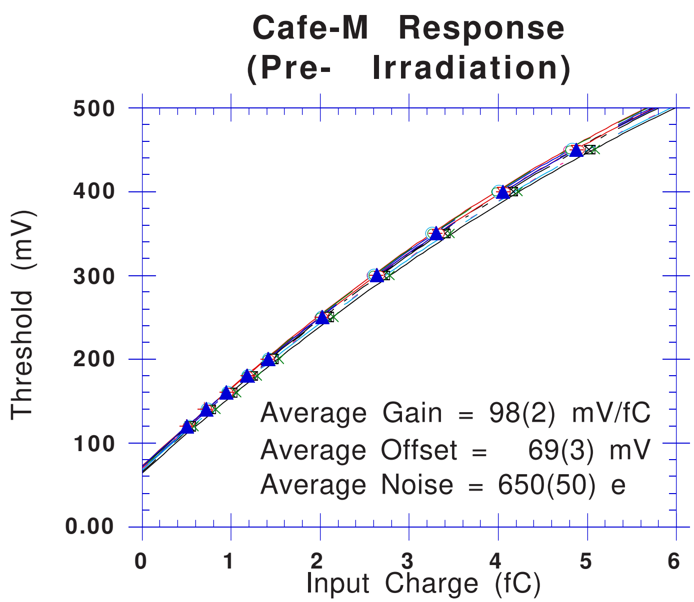


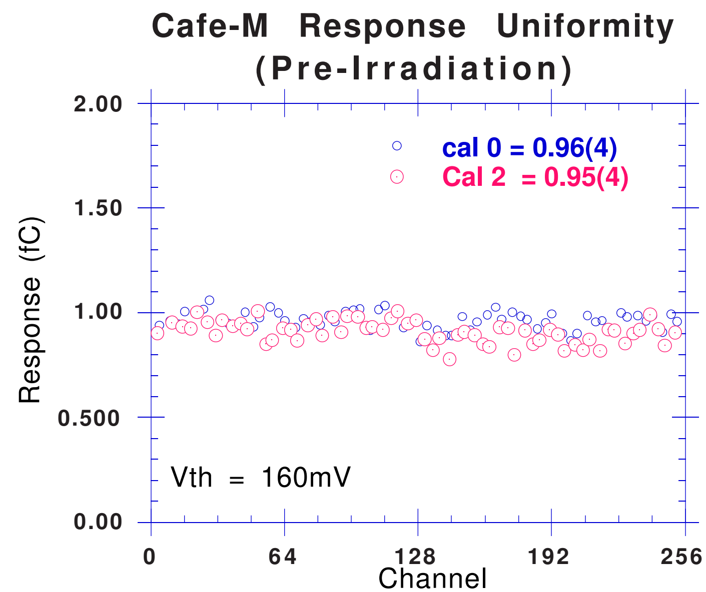
Noise Occupancy of CAFE-M

(with no detector connected)



Response before Irradiations



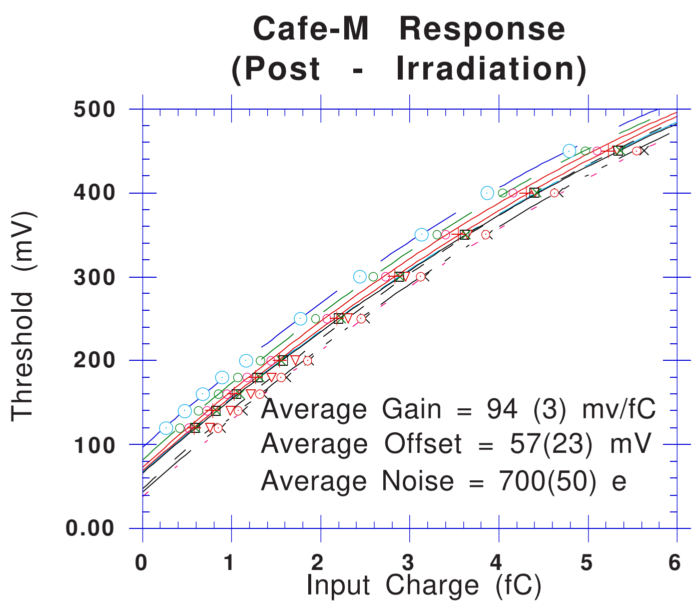


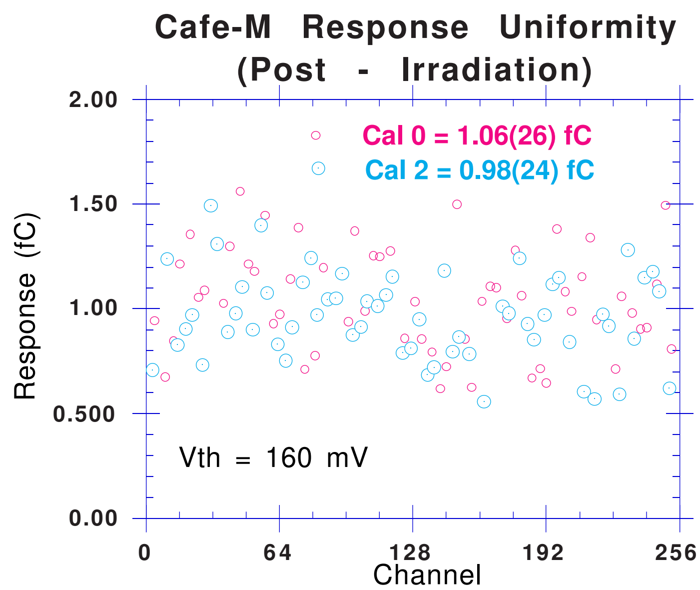
Response is defined here to be the threshold setting that produces 50% discriminator efficiency.

Channel-to-channel matching is 4%.

Response after Irradiations

(1x10^{14} 55 MeV protons; equivalent to 2x10^{14} n/cm^2 or 17 MRad)

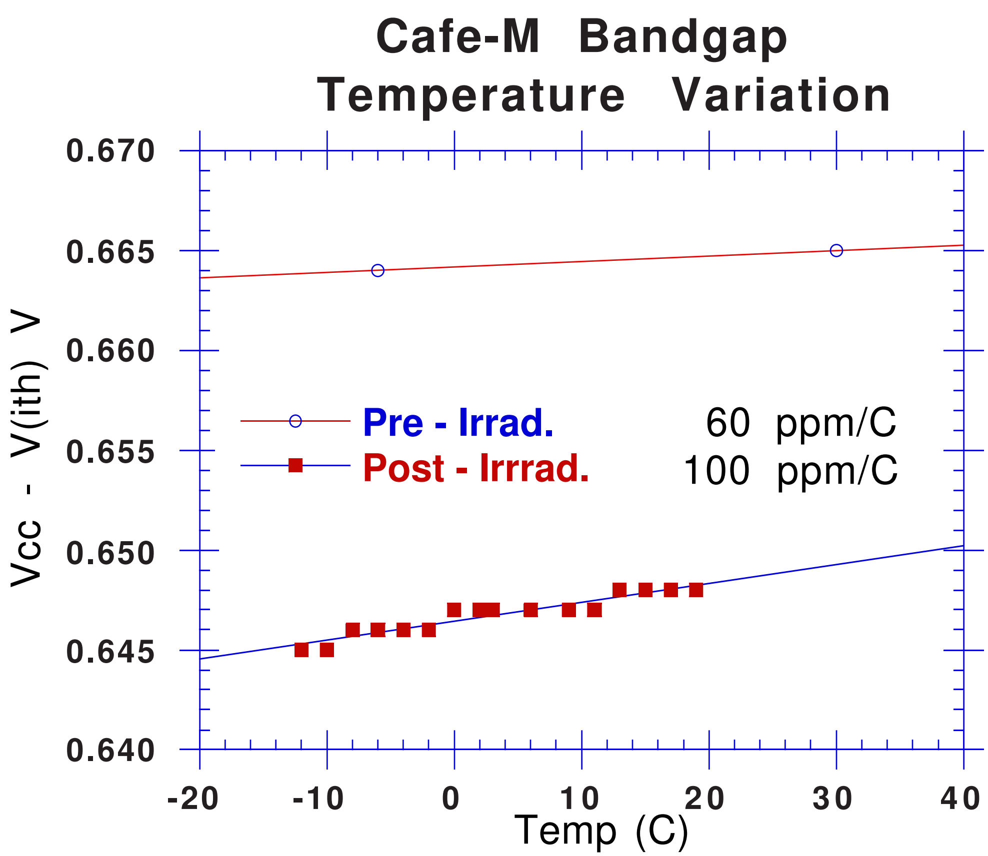




Note that the parallel response curves for different channels is indicative of a DC offset causing the channel-to-channel mismatch

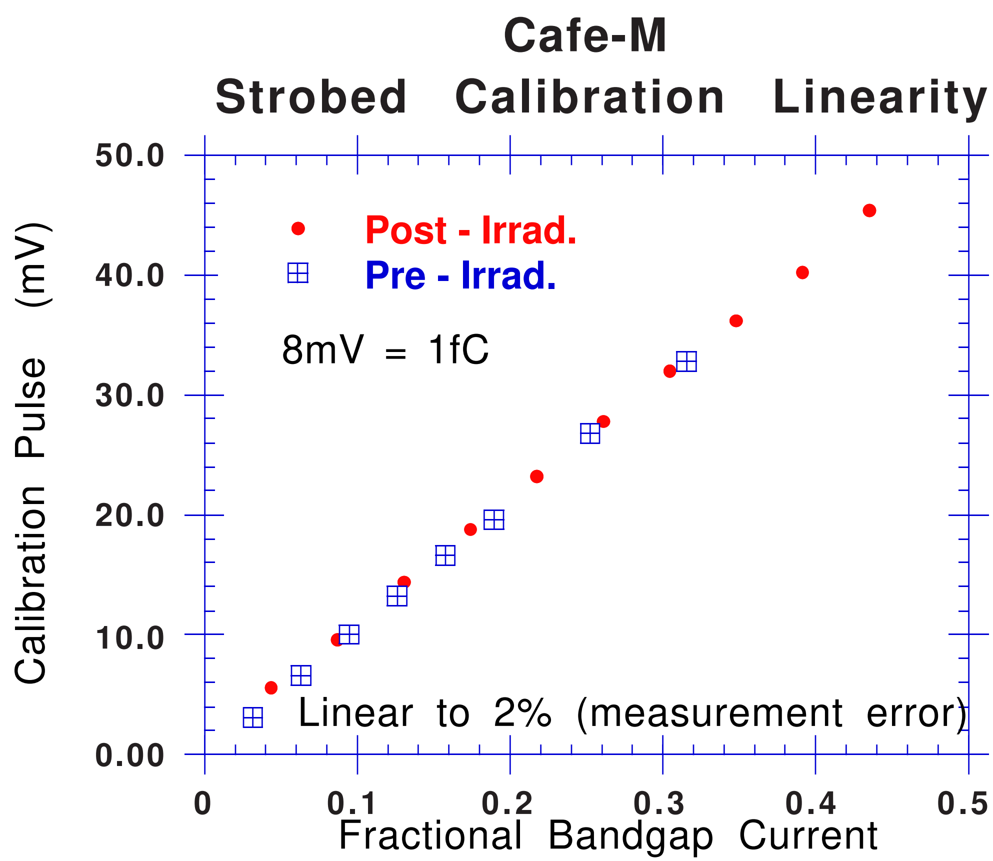
Band Gap Performance

(before and after irradiation with two different chips)



The linearity and temperature stability are maintained after irradiation. The approximately 3% difference in absolute value is partially due to chip-to-chip differences as well as radiation effects. Tests of a larger sample are needed.

Linear Response of Calibration Signal
(before and after irradiation)



Details of the CAFE-M Matching Problem and the Fix

The post irradiation channel-to-channel matching deteriorated to 24% (1σ) as a variation in offset at the discriminator.

This has been traced to the beta (DC current gain) matching of two transistors with 120 kΩ bias resistors.

> **The beta matching only deteriorated from 1% to 2% after irradiation but the 120 kΩ bias resistor has the effect of amplifying the resulting DC offset.**

The primary fix requires the reduction of the bias resistors to 40 kΩ and corresponding changes in capacitors to keep the time constants fixed. This reduces the mismatch by a factor of 3.

Other circuit improvements include:

> **Move a factor of 2 gain from third stage to second stage before AC coupling with a new global bias circuit to provide extra compensation for beta degradation with radiation damage**
>
> **Remove emitter followers in third stage (not needed with new lower gain) to improve matching**
>
> **Increase width of some resistors (with corresponding increase in length) to make them more insensitive to processing variations**
>
> **Reduce variation of output pulse amplitude (over process variations and pre- to post-irradiation)**

Simulations indicate a reduction in the DC bias mismatch by a factor of 18.

Chip size will remain approximately the same.

Plan for CAFE-P

The present CAFE-M design is being modified (named CAFE-P) at UCSC to change or fix the following:

> **Reverse the polarity of the accepted signal for p-strip detectors.**
>
> **Fix selection of voltage threshold control (diagnostic mode).**
>
> **Implement the performance improvements discussed in the previous list of details.**

It should be noted that if the matching problem were not improved, the CAFE-M could still be used in ATLAS-SCT (after reversing the signal polarity) with slightly degraded performance. Namely, after several years of operation, the threshold would have to be set at approximately 1.15 fC instead of the targeted 1.0 fC in order to maintain the target noise occupancy. This would result in a slightly lower tracking efficiency.

However, the problem is understood and the improved performance is achievable.

Schedule:

> **Schematic complete**
>
> **Layout of data channel complete; full chip layout nearly complete.**
>
> **Design Review Complete**
>
> **Submission by end of October.**

ABC Status

The ABC was fabricated in 1997 as the first full function prototype.

> **It follows previous prototype ICs: CDP64, CDP128 also fabricated by Honeywell.**

> **The new functions on ABC include edge sensing latch, 2 DACs for CAFE-M control, data compression, SCT protocol and LVDS I/O**

Unfortunately, the LVDS receiver circuit used for reception of clock and command signals is defective

> **At some point after the initial design was simulated, the schematic was corrupted resulting in a faulty design and layout.**

> **For reasons that cannot be reconciled at this time, this was not caught at the design review.**

The result is that the IC is completely non-functional as fabricated.

We have applied a repair technique using a focused ion beam (FIB) technology to jumper around the faulty circuits and allow us to operate the chips by applying external CMOS signals.

> **The first attempt resulted in 2 chips working only at 60 kHz**

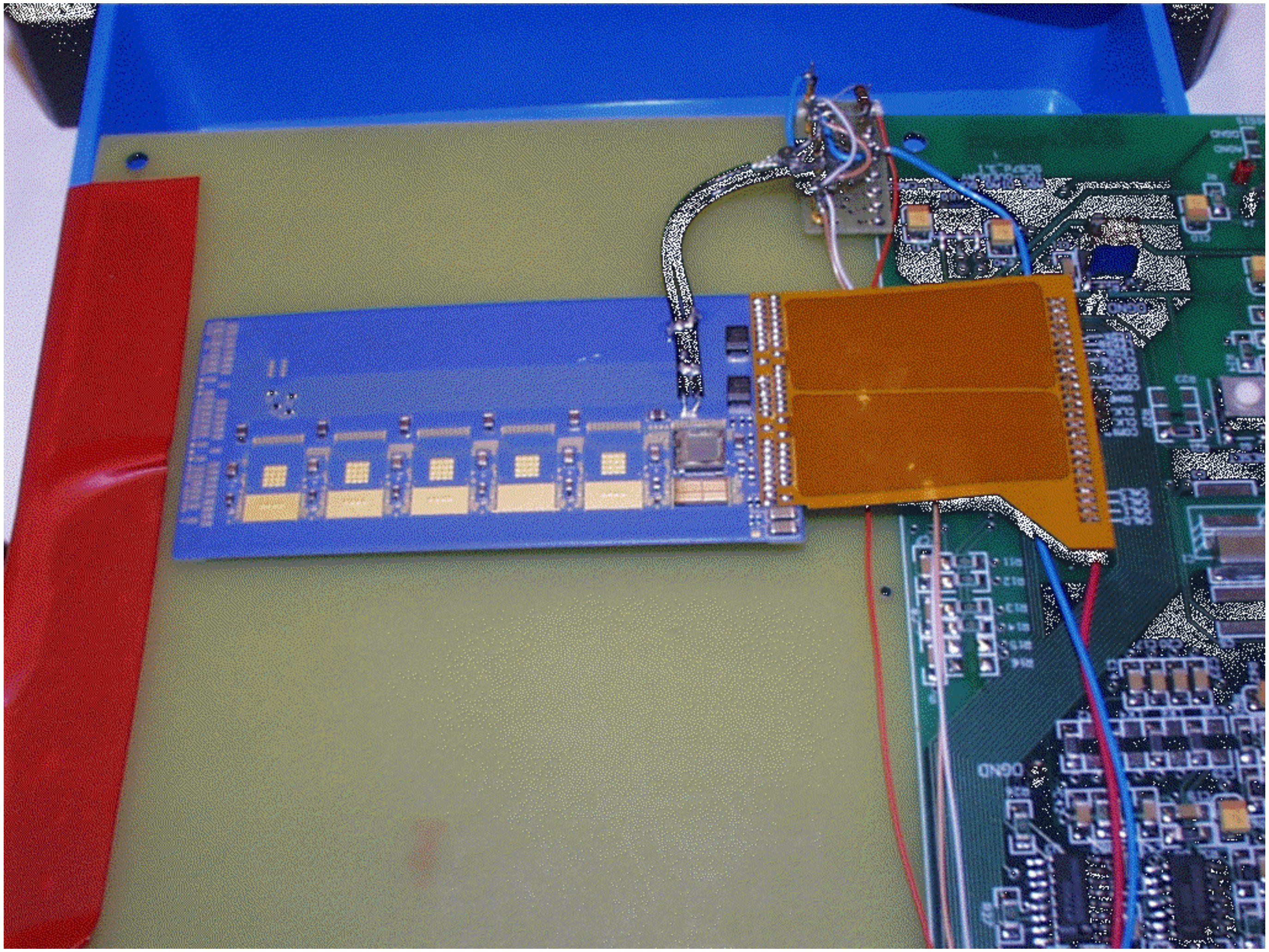
> **The second attempt was much more successful and we now have 8 chips operating at 40 MHz (full speed) and beyond.**

> **It appears now that we can fully test all functions of the chip after this repair is made.**

> **We now have two CAFE-M and ABC successfully operating on a hybrid even in the presence of the noisy 5 V CMOS clock and command signals.**

Tests are proceeding with single chips on test boards and also with chips mounted with CAFE-Ms on hybrids.

CAFE-M & ABC on Hybrid
(note the micro-coax cable feeding clock signal)



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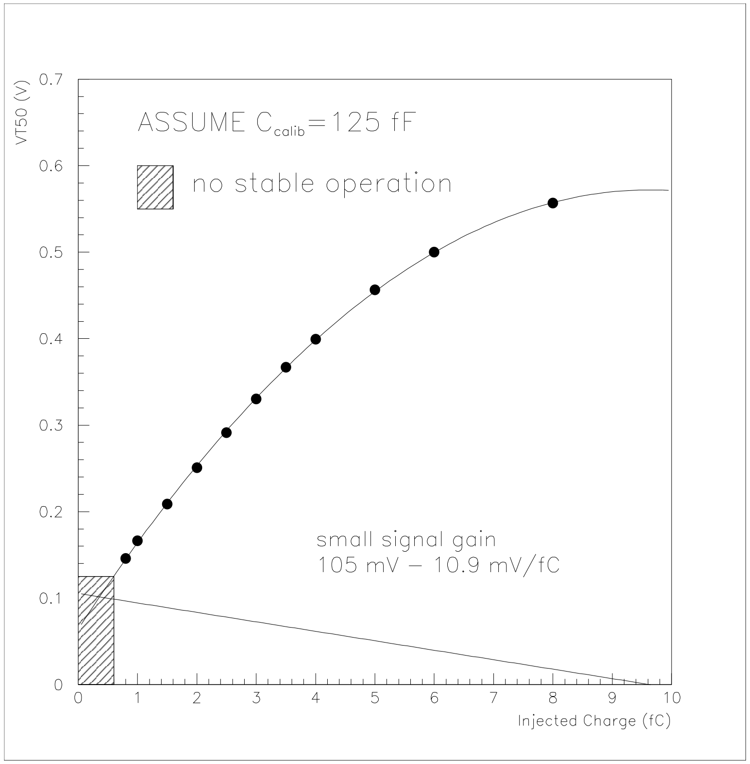
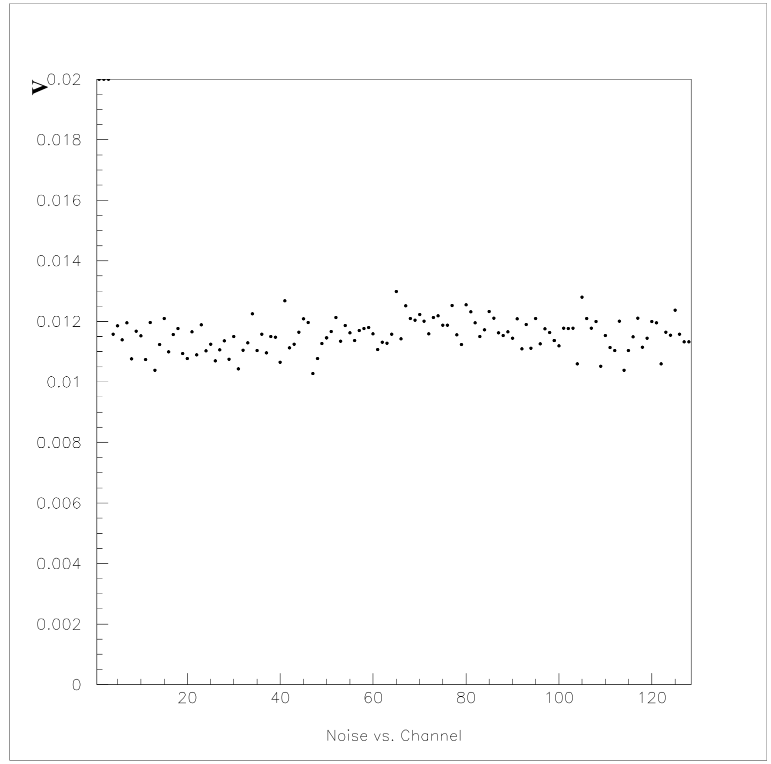
Response of CAFE-M with ABC on Hybrid

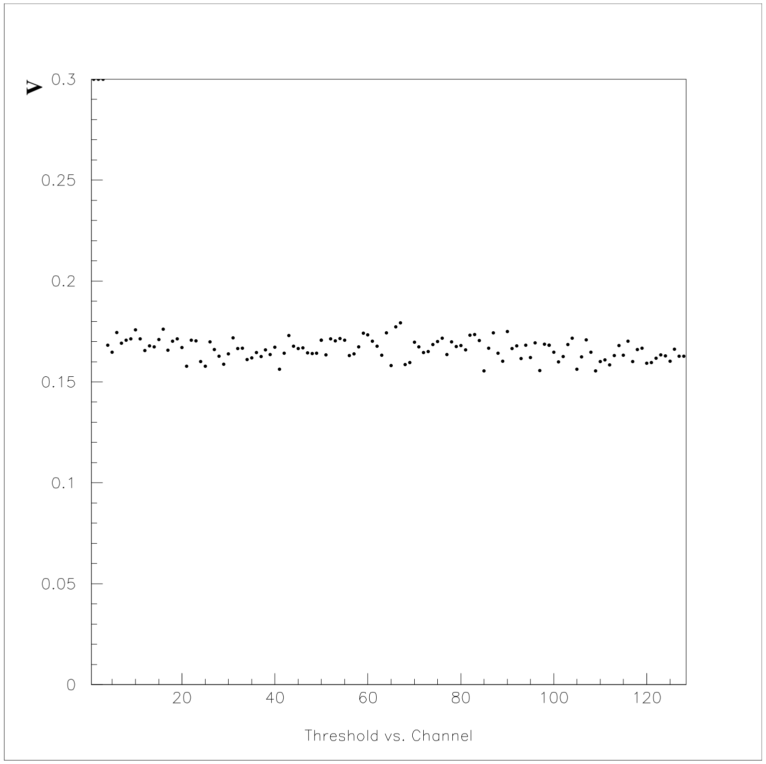


Threshold Setting for
50% Efficiency vs. Injected Charge

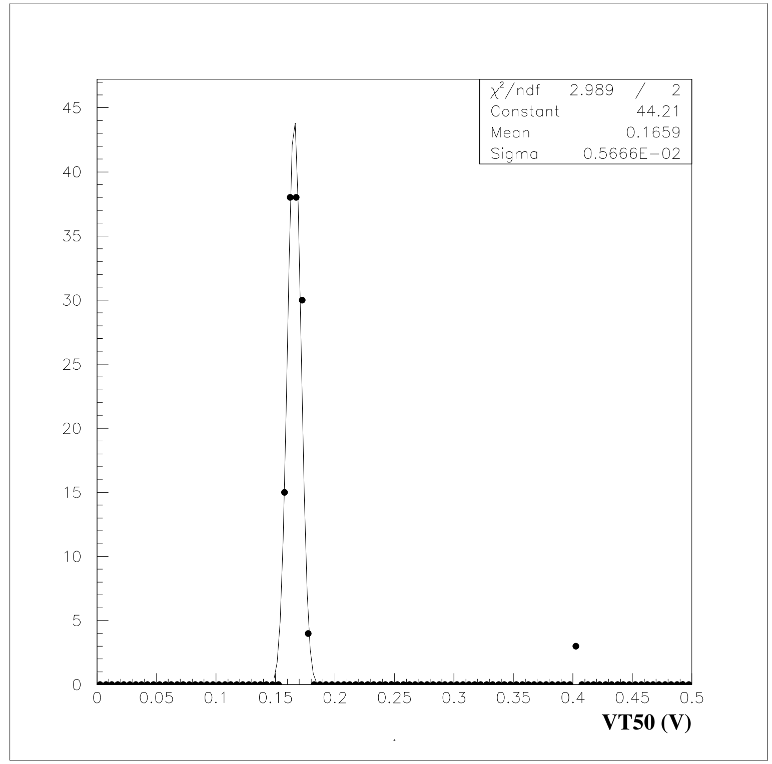


Noise by Channel
Average = 790 e⁻

Channel-to-Channel Variation of CAFE-M with ABC on Hybrid



Channel-to-Channel Variation of 50% Efficiency Threshold Point



Distribution of 50% Efficiency Threshold Points

Detailed ABC Bug List

So far our testing has located the following problems:

Problem	Who will fix
LVDS Receiver circuit non-functional.	RAL
Power-on Reset circuit switches at too high a threshold plus logic error in output.	RAL
DAC design is sensitive to radiation induced threshold shifts.	LBL
Some complementary I/O signals have pads reversed.	RAL
Data Compression logic does not handle overflow conditions correctly.	RAL/CERN
Readout Control logic fails to put trailer on data packet in some conditions.	RAL/CERN
Bunch Crossing Counter has one bit stuck at 0.	RAL
Data Compression logic does not work at full 40 MHz speed	RAL
Cal-Strobe delay register step size too large (diagnostic mode)	RAL
Power bussing, in Receiver/DAC area and in back pad area	LBL
LVDS Output has reduced signal swing	RAL
Receiver of CAFE-M data signals does not work at "worst case" CAFE-M level	LBL

Note that all bugs except the first two have been found with FIBed chips or inferred from ABCD results and cross-checked with the FIBed chips. It has been a major success to have been able to thoroughly check out all of the ABC circuit blocks.

Plan for ABC

Fixes for almost all known bugs are now complete at the schematic level, some at the layout level.

> **Some found recently from tests of FIBed chips are not yet "fixed".**

Testing is continuing in the UK and the US to learn as much as possible from the existing chips. Nearly all logic blocks have been tested but more testing is needed in the following areas:

> **Performance of I/O circuits (excluding faulty LVDS receiver) under full hybrid loads.**

> **A stuck bit in the Beam Crossing Counter which has not been located in the schematic.**

Radiation testing of the ABC has been done.

> **The radiation hardness of the Honeywell process was demonstrated with previous prototypes (CDP128). However, this design also needed to be verified.**

> **The speed limitation of the Data Compression Logic was degraded further after irradiation.**

> **No other problems were found.**

Once all the possible testing is complete, all design fixes are implemented and a complete set of simulations re-executed, the chip will be submitted again to Honeywell for fabrication.

> **Plan to have duplicate simulation and verification work on the completed chip done at RAL and LBL to minimize the chance of errors.**

> **Goal has been to make submission by end of October, sometime in November is more likely.**

ABCD Status

The ABCD was fabricated in 1997 as the first full function prototype of the single chip solution

It follows the previous prototype IC: SCT128B also fabricated on DMILL but by Leti

The new functions on ABCD include data compression, SCT protocol and LVDS I/O plus some changes to the front-end to improve channel-to-channel matching.

The digital functions of the ABCD are working nearly perfectly. A few minor bugs have been found.

The Data Compression Logic appears to have the same speed limitations as in the ABC.

The Readout Logic has a problem with the trailer as in the ABC

As with the ABC, the DAC design is sensitive to radiation induced threshold shifts.

This was learned with the prototype SCT128B but only after the ABCD had been submitted.

The front-end is also functioning but shows some important problems.

The shaper stage works over a bias range which is much more severely limited than expected.

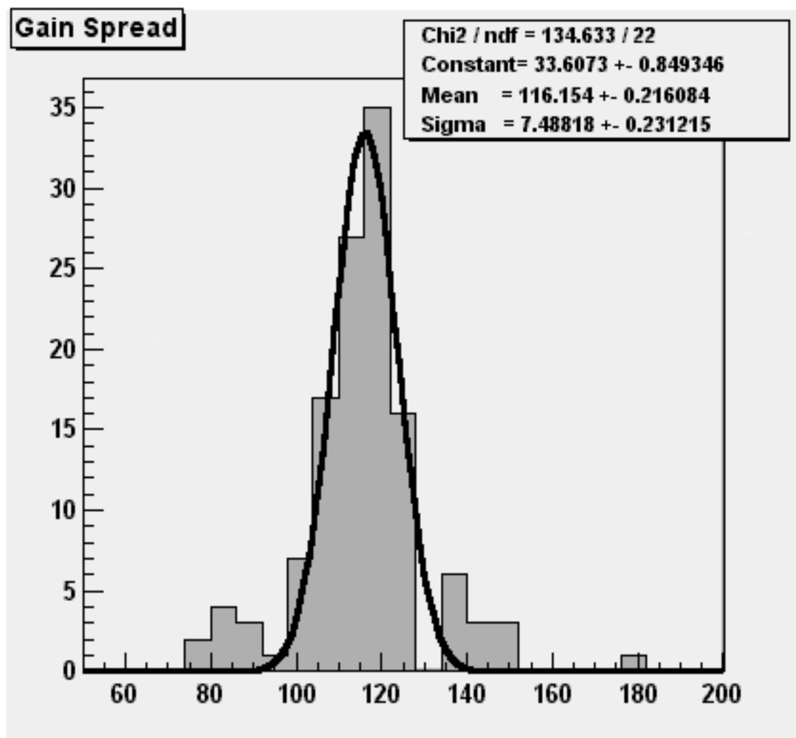
The channel-to-channel matching is also much worse than expected or acceptable (roughly 35%).

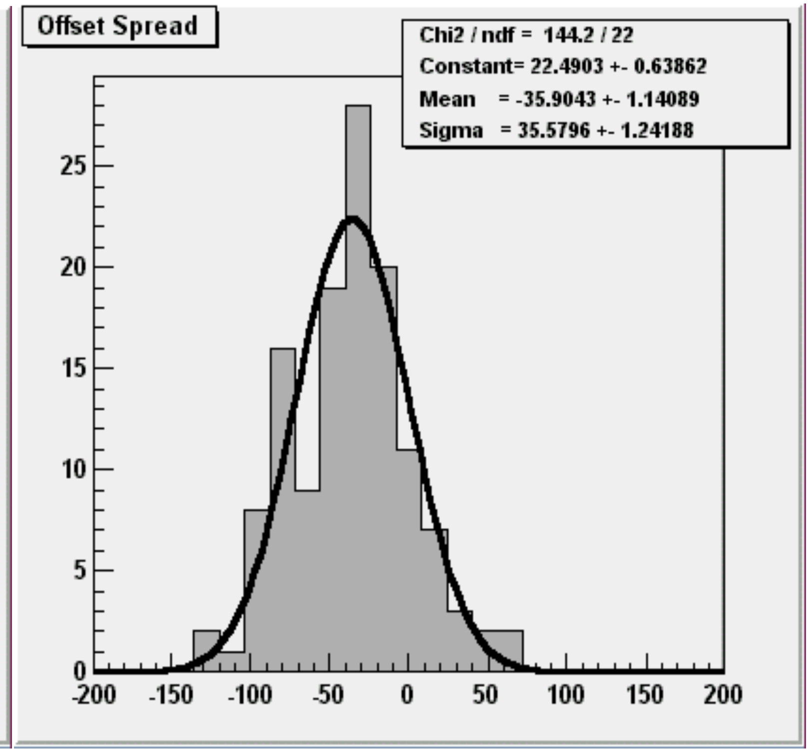
Process monitor data from Temic indicates that this lot was not processed near the center of the control limits. Rather some important parameters (e.g. DC gain) were near or beyond the spec limit.

This may explain some of the poor performance.
However, the design must be made to work over the full DMILL process range.

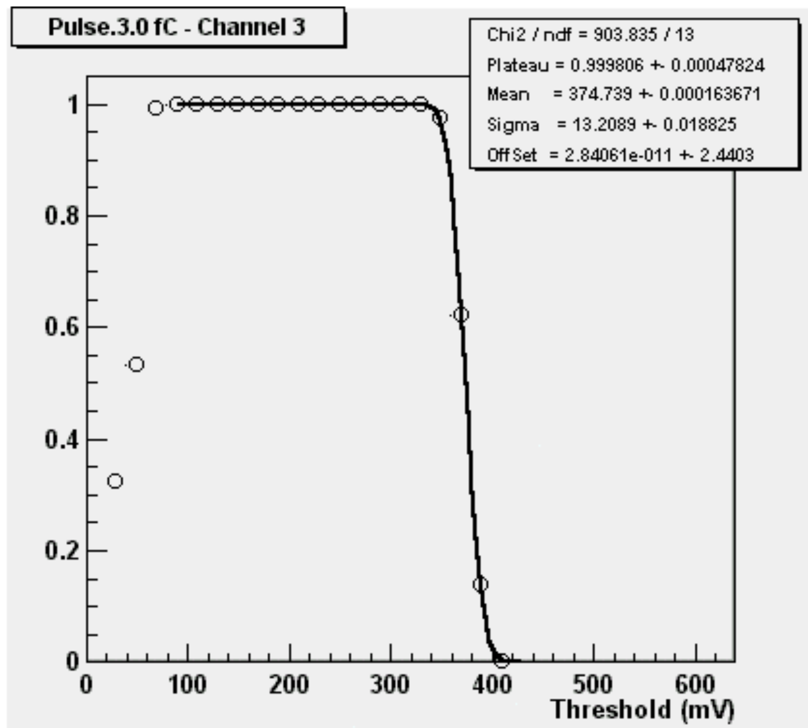
The wafer sort yield for 8 ABCD wafers was 24%.
This is below that projected by Temic based upon die size.

ABCD Gain and Offset Matching

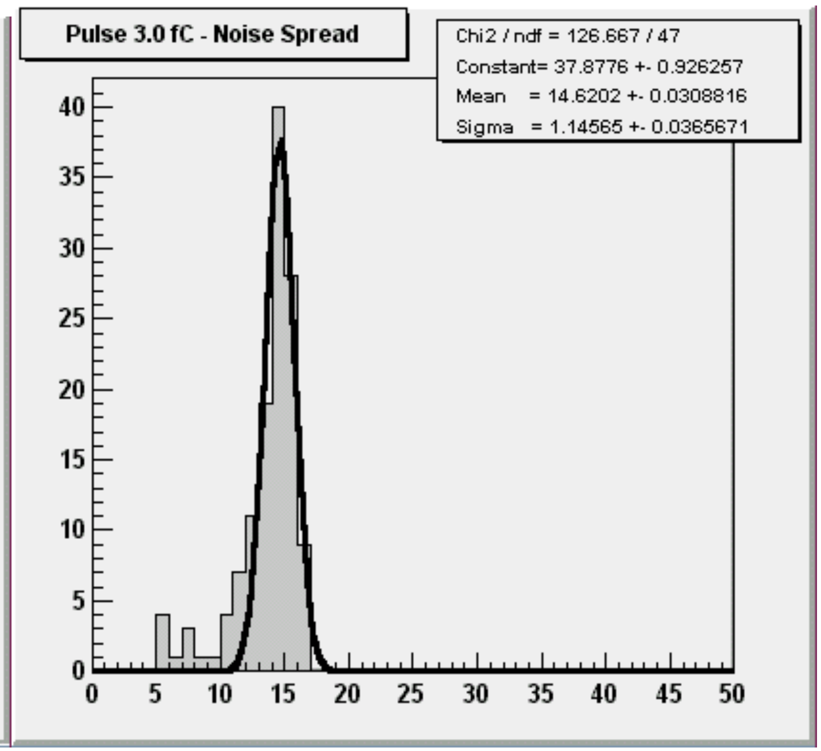




ABCD Single Channel Threshold Scan



ABCD Noise Matching



NOISE = 14.6 mV rms.
GAIN = 116 mV/fC
ENC = 780 e- rms.

Detailed Evaluation of the ABCD Digital Blocks

Test vectors were extracted directly from the Verilog models and applied to the ATS tester.
100 000 test vectors run to validate the logical functionality

Maximum working frequency for individual blocks and for the whole chip were evaluated.

Margins for timing and I/O signal levels were evaluated.

Maximum working frequency (in MHz):

Test #	Chip #2		Chip #4		Test Description
	A	B	A	B	
1	62.5	47.6	66.7	50.0	Send Id mode, address decoding
2	x	47.6	x	52.6	BC reset tests
3	58.8	45.4	62.5	50.0	DTM mode, no hit readout
4	50.0	47.6	58.8	50.0	DTM, single hit readout
5	58.8	47.6	58.8	47.6	DTM, multiple hit readout
6	58.8	47.6	52.6	50.0	Accumulator tests
7	34.5	34.5	45.4	45.4	Data Compression Logic test

x - test was not run
A - L1 and BC counters were excluded from data comparison
B - full data comparison

Other results

	chip #2	chip #4	
minimum v_{dd}	3.9V	3.4V	(at 40 MHz)
minimum width of clock sigma	8 ns	7 ns	(at 40 MHz)
command input delay range	16 ns	16 ns	(for 25 ns clk period)
LVDS driver output voltage range	1.1-1.4 V		

For the two chips tested, some differences in maximum operating frequency are observed.
Testing of more chips in progress.

Status of Second Fabrication of ABCD

A second lot of ABCD wafers has been fabricated without any design changes. This was to determine if the unexpectedly poor performance of the first lot is improved with the process better centered.

> **Note that this lot was originally promised mid-June, then delayed to mid-July and delivered in late-August. Temic delayed the completion while they "stabilized" the process.**

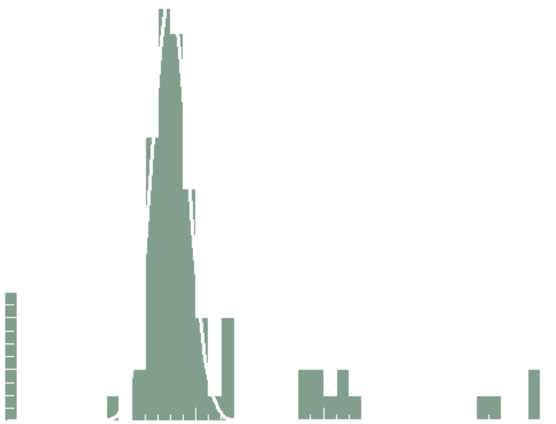
Initial indications from wafer sort data indicate that this chips from this lot are performing much better than the first.

> **The shaper stage works over a much wider bias range as it should.**
>
> **The channel-to-channel matching seems to be much better but still does not meet requirements.**
>
> **The wafer sort yield on the first four wafers tested is about a factor of two better (~ 50 %).**

Chips from this fab will be thoroughly tested before the next submission in an attempt to understand the issues and separate design from process problems.

Early Result from Second ABCD Fabrication

(Wafer sort results from one out of four wafers tested so far)



Wafer sort yield on four wafers is about 50%

A.A. Grillo
SCIPP - UCSC

Status of DMILL Process

While several prototype ICs have been fabricated on the DMILL process, this first ABCD fabrication was our first experience with one done by Temic. Previous fabrications were done by Leti.

Several issues remain with regard to the DMILL process:

> Present resistors change by 30% to 50% after irradiation.
>
> No specifications exist for matching of resistors or transistors.
>
> The DC gain (beta) has typically run at the low end (sometimes outside) of the specification since Temic took over the process.
>
> There are no process monitors in place to track some key parameters such as matching.

We have had very productive meetings with Temic concerning these issues and they have agreed to implement changes to address all of these issues. However, we continue to be concerned about the stabilization of the DMILL process in time to meet our schedule.

Plans for ABCD

Complete the evaluation of the second lot of ABCD wafers and continue to try to understand the strange performance of the first lot.

The front-end design will be modified to include the new DMILL resistor structures which Temic is introducing to improve radiation tolerance.

The front-end design will be re-tuned to accommodate the new worst case models which Temic will provide and which will also include limits on resistor and transistor matching.

A four-bit trim DAC will be added to the threshold control of each channel to allow corrections to the channel-to-channel matching.

The DACs will be re-designed make them much less radiation sensitive.

The few logic bugs in the back-end will be fixed.

Radiation tests will be conducted to determine any limitations introduced by the new design. If something is found (e.g. a speed limitation), it will be fixed before re-submission.

The goal is to submit the new design by the end of this year.

Summary of Front-End IC Status and Plans

All three ICs are undergoing revisions with submissions for fabrication planned before the end of this year.

> There is limited manpower for this effort with some engineers working both on design and on evaluation of the existing chips.
>
> The biggest risk to the near term schedule is that we cannot complete full evaluation of all issues before the scheduled submission date. But we are making the most of the available chips to understand all design issues.
>
> For the ABCD submission, there is the added uncertainty of Temic's stabilization progress.

The combination of no working ABC to match with the CAFE-M and the poorly working front-end of the ABCD matched with its working back-end, have made it virtually impossible to conduct serious system tests this summer as originally planned. The FIB process is too expense to repair sufficient chips for a real system test.

If the re-fabricated lot of ABCDs shows better front-end performance, several modules will be assembled to start system testing.

> Prototype power supplies and low mass cables will be ready fall of this year.
>
> Prototype Opto Links will also be available for approximately 16 modules with more available next year.

Serious system tests will await the new chips to arrive next Spring with system tests conducted next Summer.

IC vendor selection (i.e. choice of IC options) will be made after evaluation of chips and modules from the next round of prototype fabrications next year.

Costs for Next Prototype Fabrications

Maxim base order:	**140.75**	
Honeywell:	**120.00**	
Temic (200 kCHF):	**137.93**	**(using 1.45 CHF/US$)**
Total:	**398.68**	
US half:	**199.34**	

Vendor Issues

The biggest vendor issue is certainly the DMILL process from Temic as stated earlier.

Honeywell's bulk CMOS process (not the SOI version) has been stable for several years.

Only minor changes to the design rules since the CDP128 was fabricated in 1993.

Their conversion to 6" wafers is underway and on schedule with qualification wafers in process. They will be ready with 6" starts for our next ABC submission.

Discussions are now underway with both Temic and Honeywell to establish a Frame Contract for all LHC orders.

A few technical details need to be resolved.

The main technical issue is negotiating some sort of quality guarantee based upon yield.
This is difficult for typical "foundry" service which is usually not based upon yield of custom designs but rather on DC process monitor testing.
If we are successful in these negotiations, our cost risk will be greatly reduced.

The main time factor now is the business process at CERN (e.g. time to get approval of the Finance Committee) but this contract should be in place by next Spring.

Further negotiations have been held with Maxim concerning possible price reductions.

They seem agreeable (at least at this time) to such a price reduction.

We are discussing with them possible test scenarios which would allow us to purchase fully or nearly fully tested chips rather than untested ones. Again, if this can be done in a cost effective way, it will greatly reduce our cost risk.