

ATLAS

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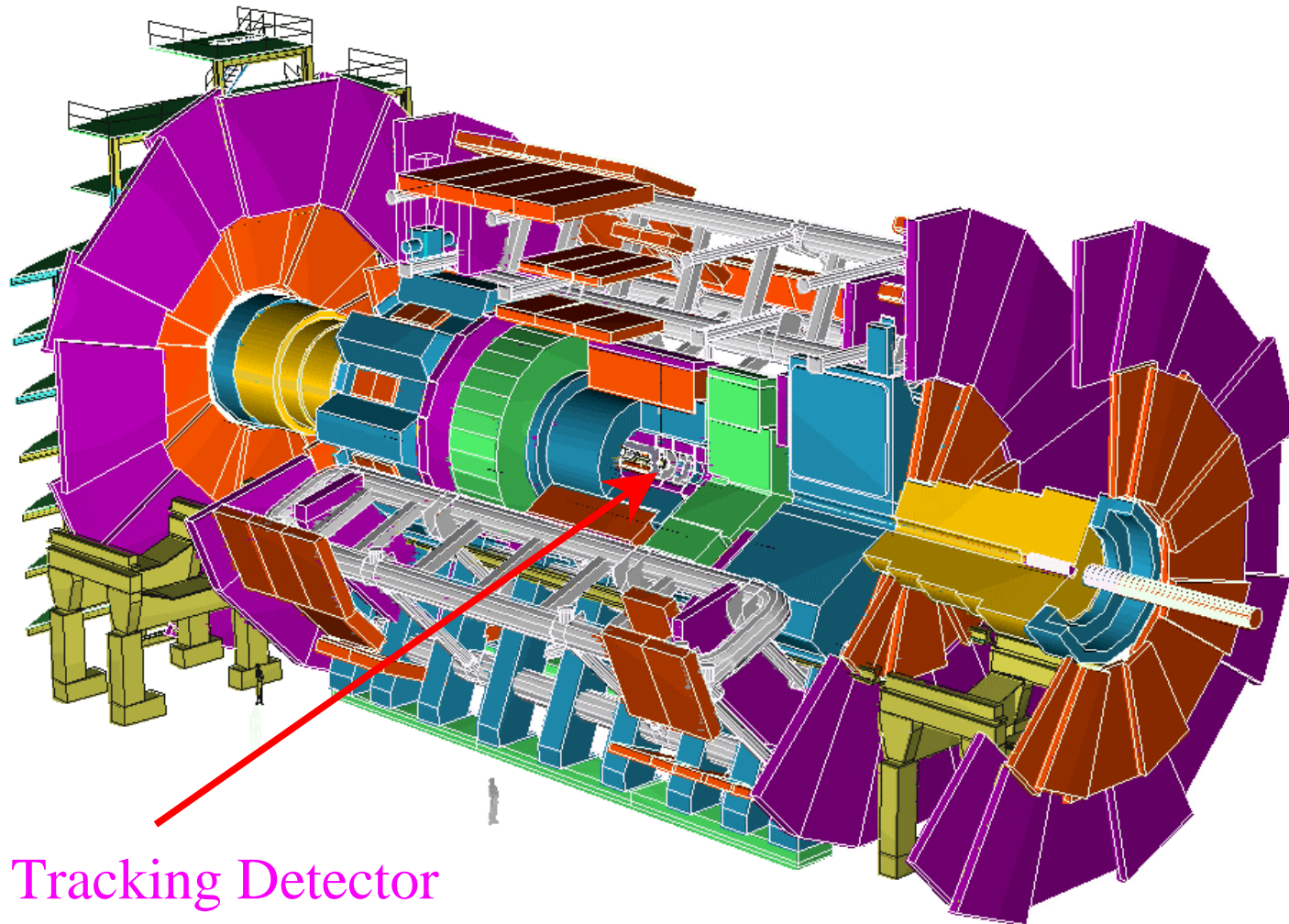
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ATLAS Silicon Tracking

M. G. D. Gilchriese

May 10, 2000

The ATLAS Detector

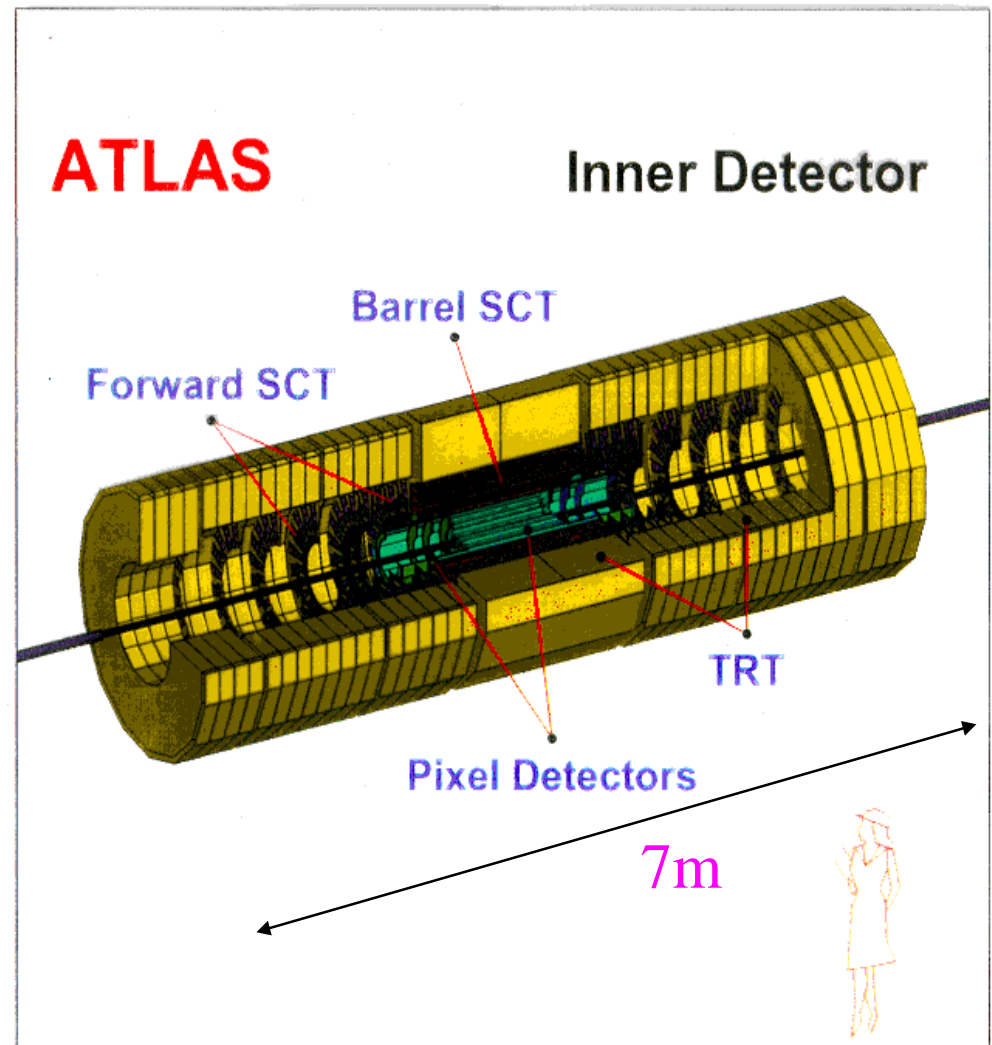


Inner Tracking Detector

Inner Detector and LBNL



- LBNL is currently involved in both the Pixel Detector System and the Semiconductor Tracker(SCT)(silicon strip detectors) for the ATLAS Inner Detector.

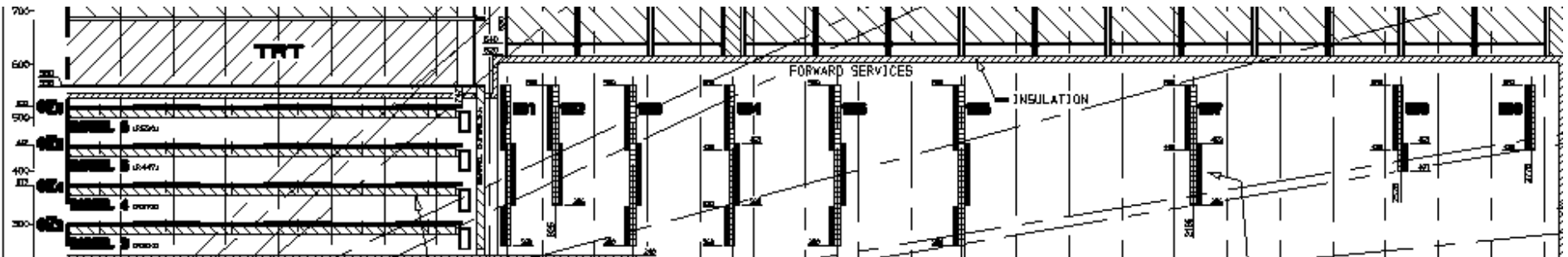


- **Pixel detector system**
 - ◆ Development of this new technology in all areas except silicon sensors.
 - ◆ Later production of about one-third of system
- **Silicon strip detector system**
 - ◆ Completing development of integrated circuit electronics and related testing to meet demanding LHC requirements
 - ◆ Later production with emphasis on modules, the building blocks of the system.
- **Management of US contributions to these systems**

Semiconductor Tracker(SCT)



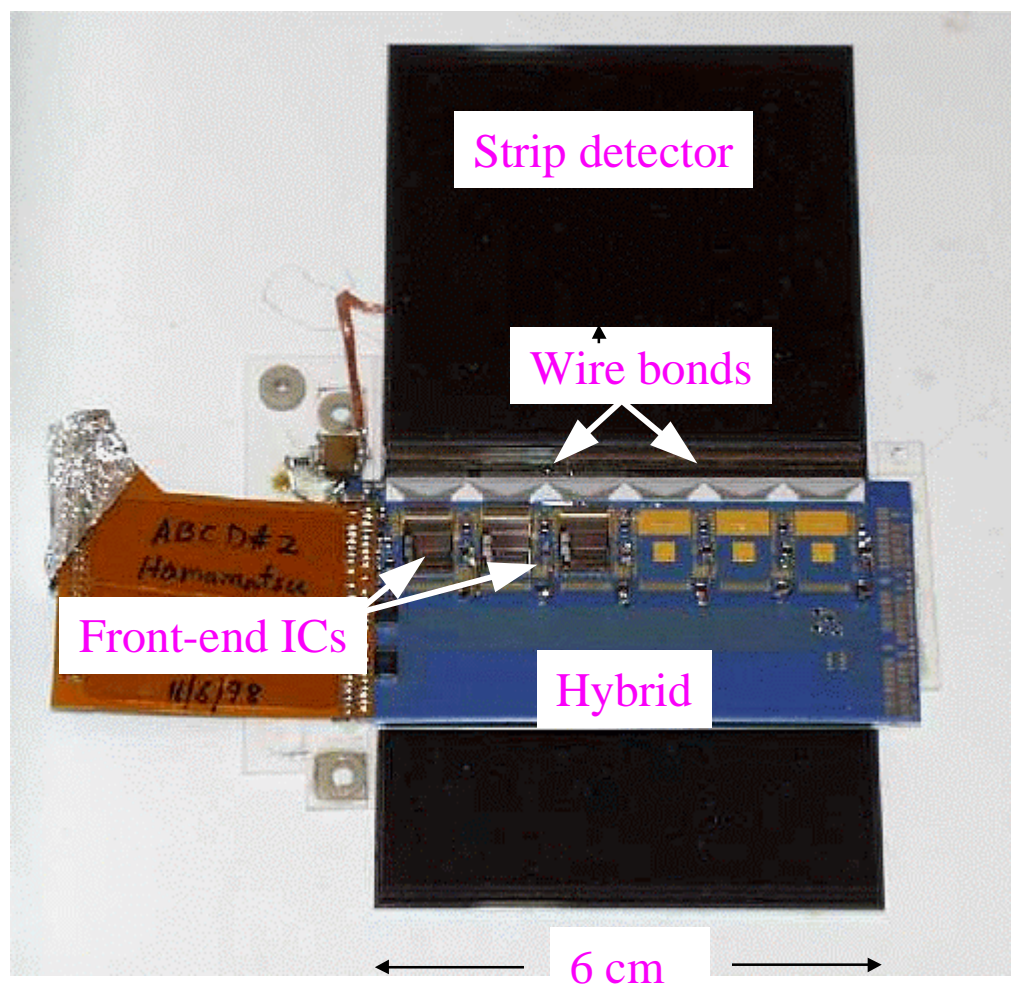
- Lots of silicon
 - ◆ About 60 m²
 - ◆ About 6 million channels
 - ◆ Single-sided, p-on-n detectors bonded back-to-back to provide small angle stereo => modules (about 4000 of them)
- Radiation environment is about 10MRad worse case over lifetime.
- US, and LBNL, have concentrated on integrated circuit electronics and module construction.



SCT Module



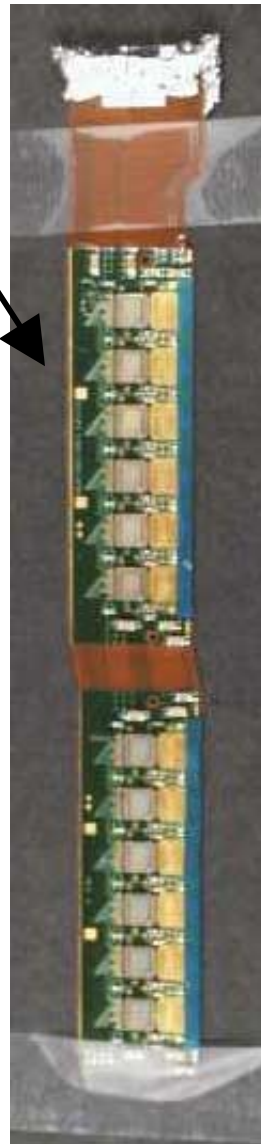
- Modules are the building blocks of the SCT system
- We have concentrated our efforts in the last year on
 - ◆ the design and testing of the integrated circuits (as die, on hybrids and with detectors attached)
 - ◆ prototype hybrids that hold the integrated circuits
 - ◆ completing the precision tooling needed for module assembly



Hybrid and Module Assembly



- Hybrid assembly in local firms and at LBNL.
- Testing to be shared between Santa Cruz and LBNL.
- All module mechanical assembly to be done at LBNL.
- Module testing again shared between Santa Cruz and LBNL.



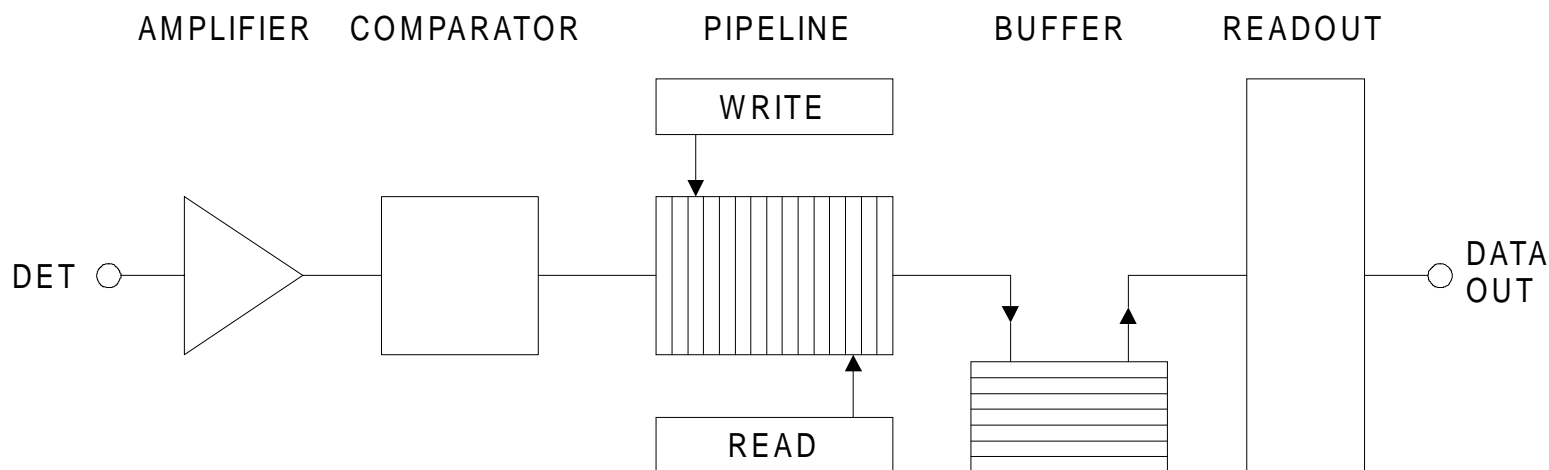
- Module tooling now in recently renovated clean area at LBNL in preparation for production assembly.
- Facility shared with pixels.



Silicon Strip IC Electronics



- A year ago, we were just starting to regroup after the failure of the first round of prototypes of two options for IC readout to meet specifications. Considerable progress has been made over the last year. A choice of design options and thus vendors has been made.
- Preproduction of integrated circuits(ICs) will begin this month with first deliveries by end of August.
- Irradiation tests performed at LBL 88" cyclotron. Long term irradiation tests at Cobalt source at LBNL are ongoing. And also irradiation tests at CERN and neutron sources in Europe.

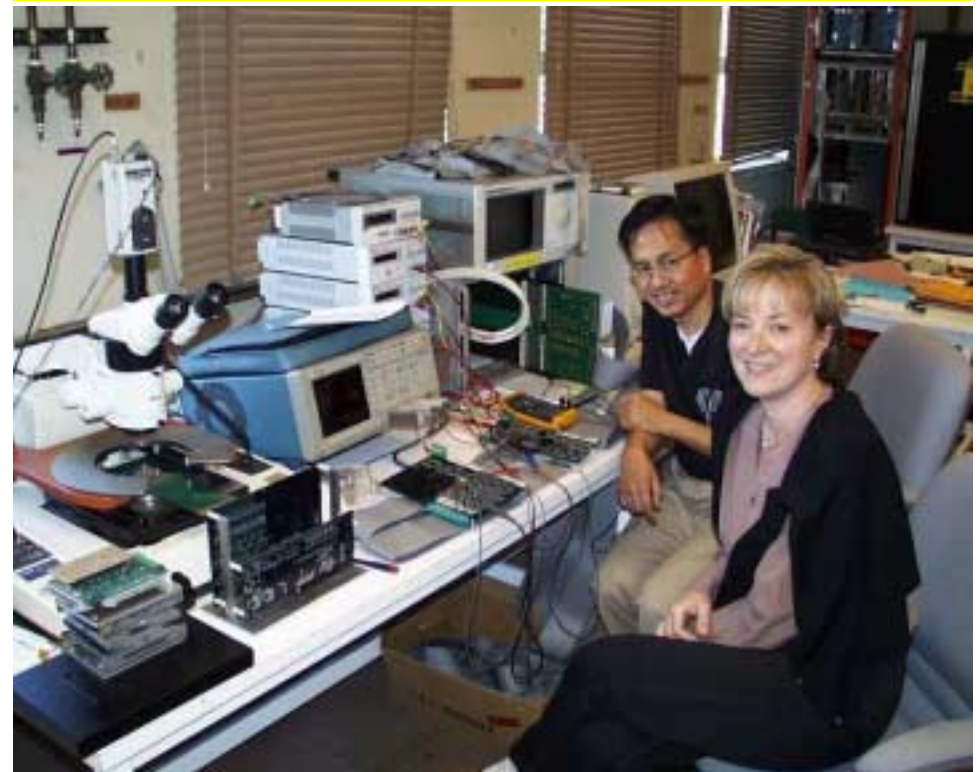
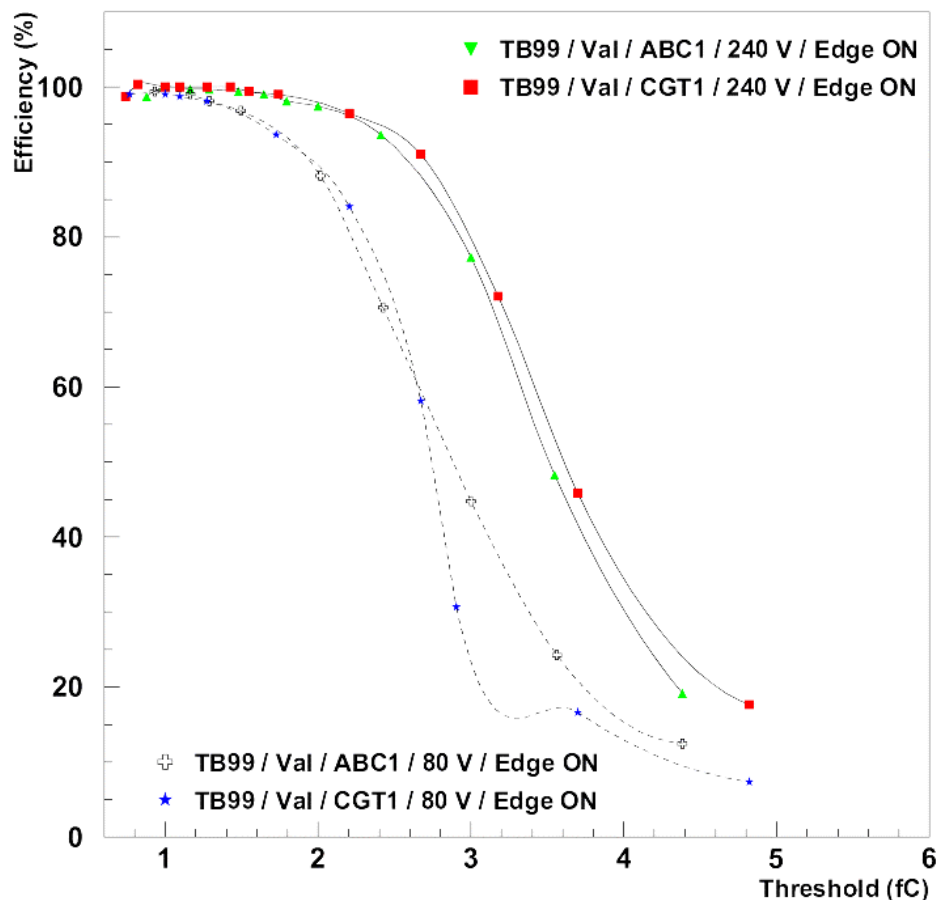


Binary(yes/no) readout of silicon strips. Store data at LHC speed of 40 MHz

IC Testing



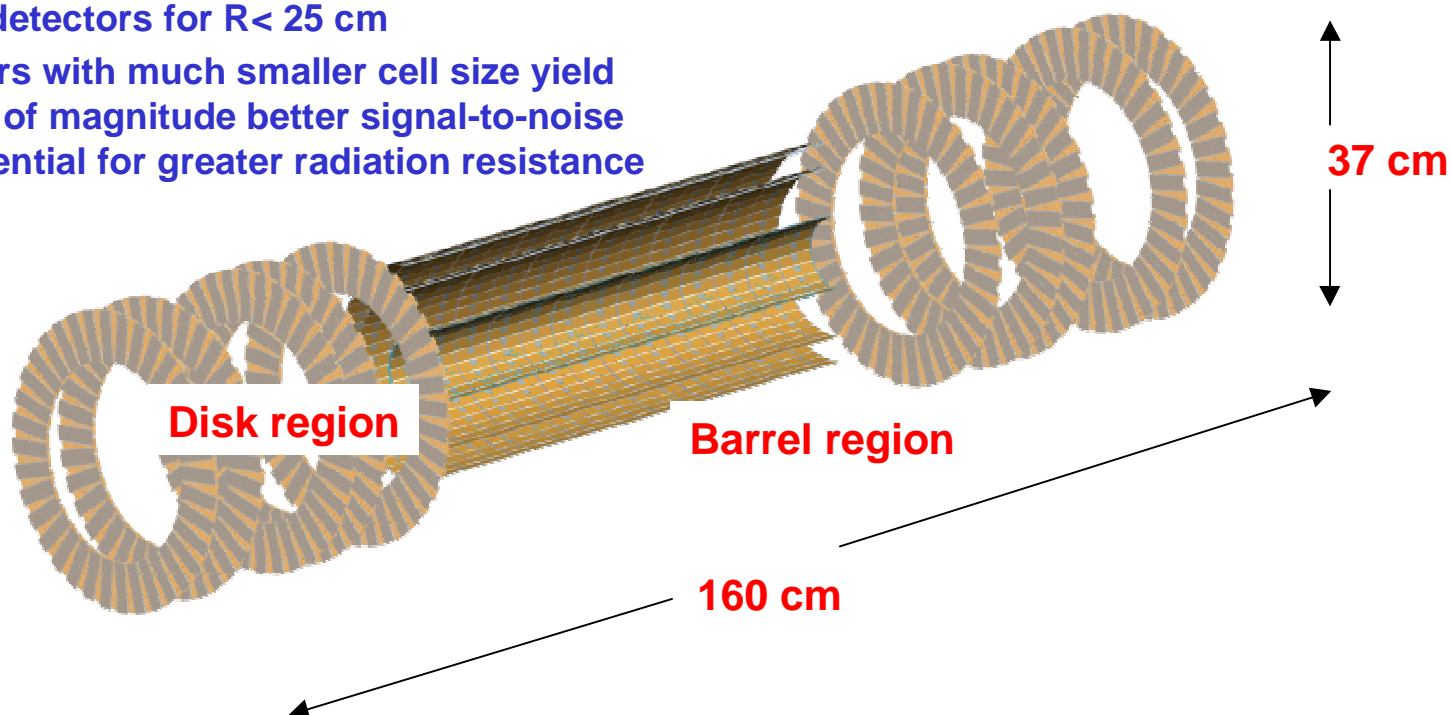
- Example of beam test last summer of silicon detectors at two bias voltages with prototype electronics.
- Up to about 1,000 wafers are to be tested in production.
- High speed test system under intense development at LBNL with expectation of use at Santa Cruz, RAL and CERN.



Pixel System



- LHC radiation levels prevent long-term operation of silicon strip detectors for $R < 25$ cm
- Pixel detectors with much smaller cell size yield almost order of magnitude better signal-to-noise and thus potential for greater radiation resistance

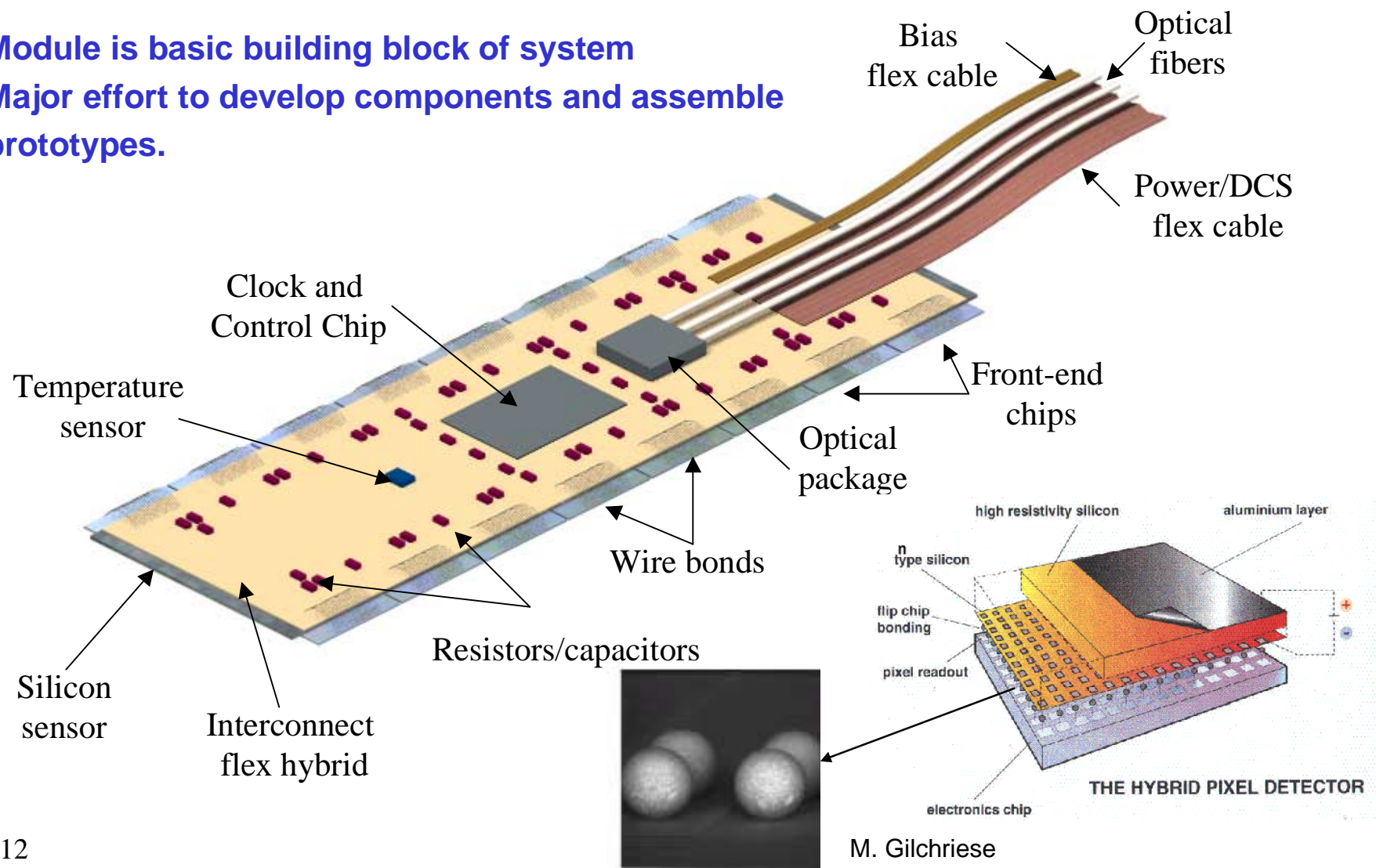


- Pixel size is 50×400 (300 innermost layer) μ .
- Three space points for all tracks $|\eta| < 2.5$
- Three barrel layers
 - ♦ Innermost is "B-layer" and is removable from outside the Inner Detector
- Five disks on each end
- Radiation levels 30-50 Mrads outer layers, larger B-layer

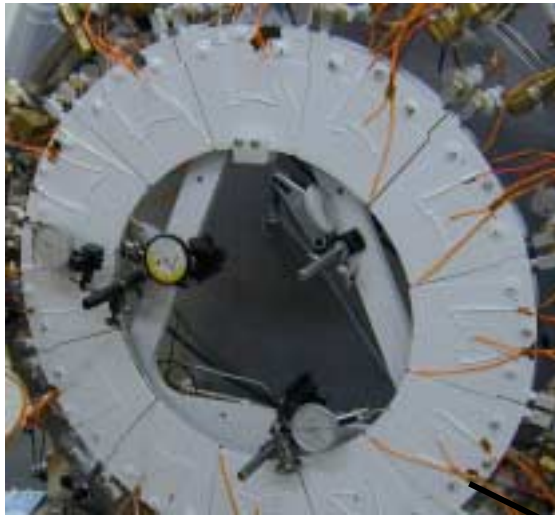
Pixel Module



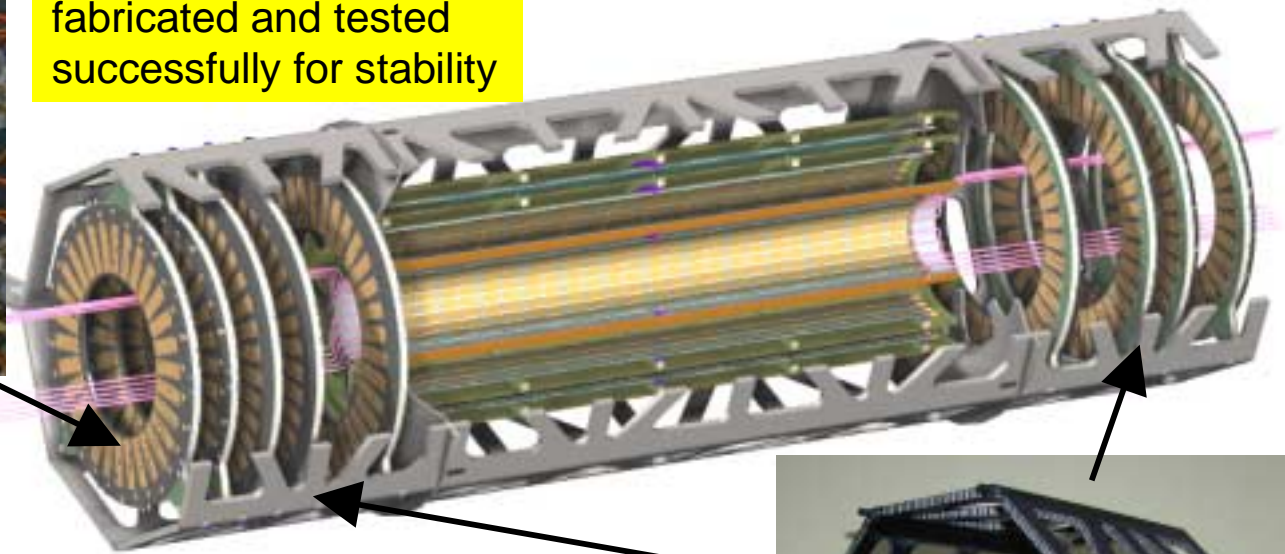
Module is basic building block of system
Major effort to develop components and assemble prototypes.



Pixel Mechanics



Thermal/mechanical
prototype disk
fabricated and tested
successfully for stability



- Ultra-stable, low mass structure.
- Provides integrated support and cooling for about 15 kW
- Major systems integration task to provide power/signal cabling
- And coolant connections at -25°C .

Prototype end frame
section fabricated
by December 1999.



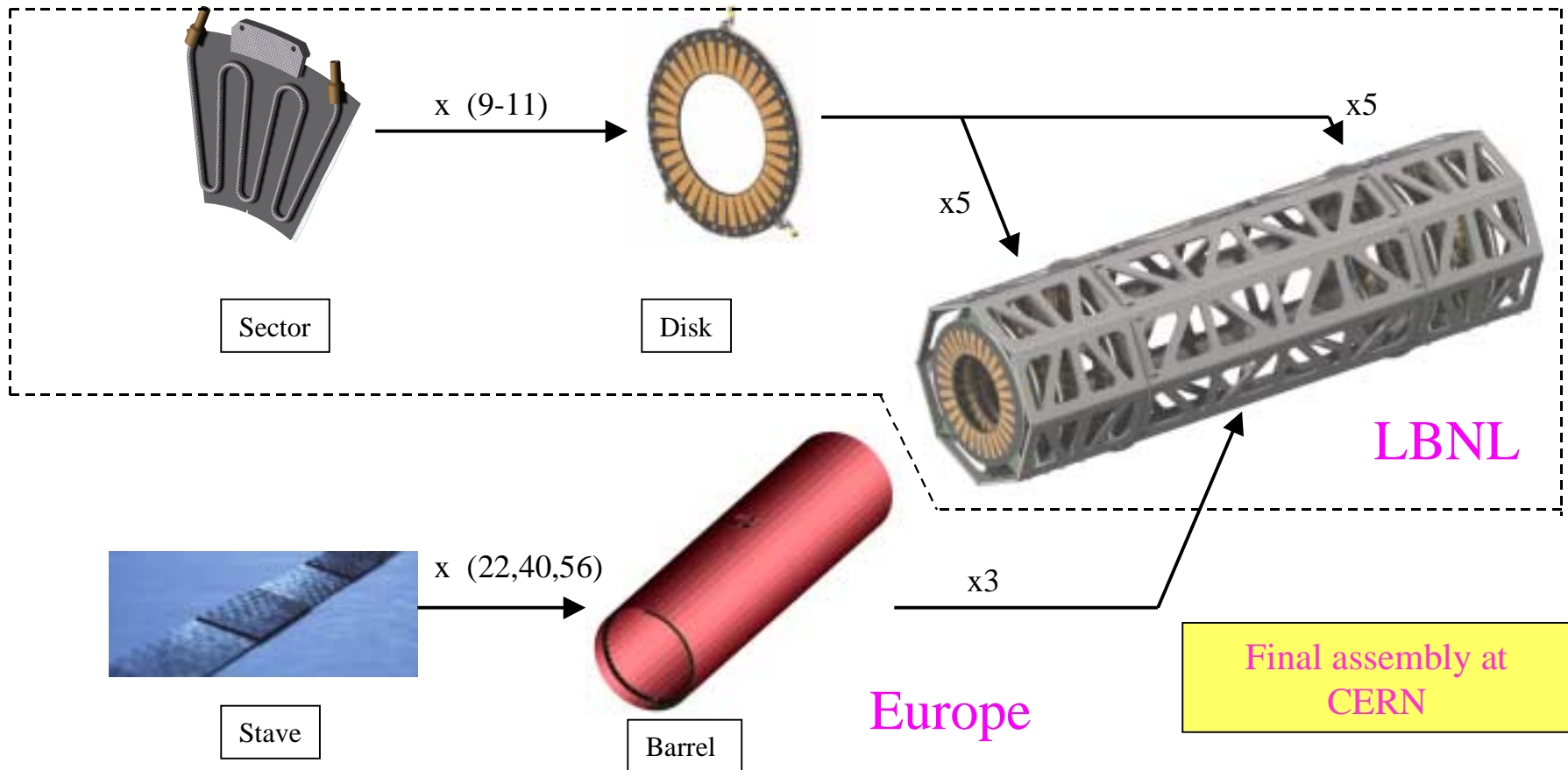
LBL Pixel Mechanics Role



Local support structure

Intermediate support structure

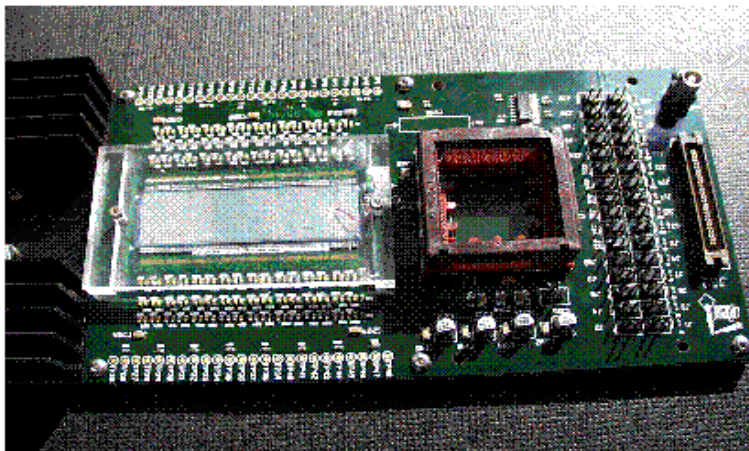
Global support structure



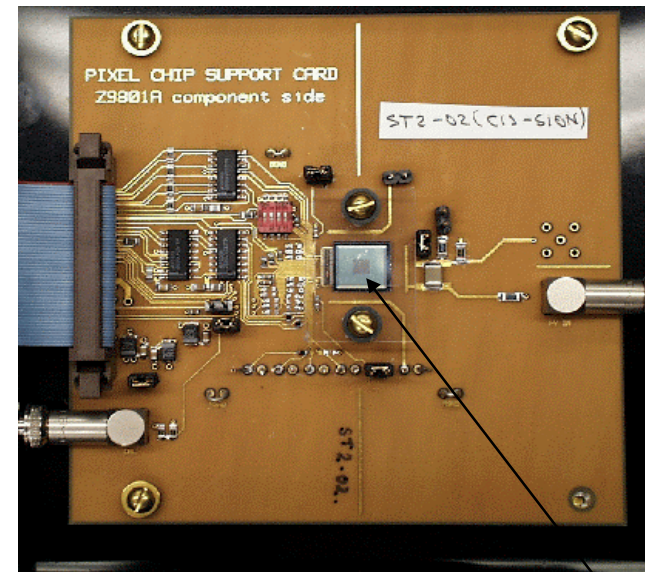
Pixel Electronics and Modules



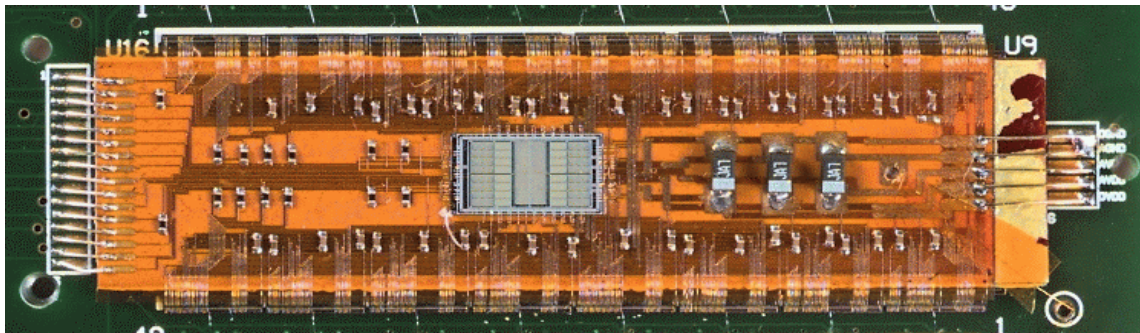
- Full-scale rad-soft electronics prototypes fabricated in rad-soft technologies in 1998 and tested extensively, including with irradiated detectors, since then.



Bare 16-chip modules



Dozens of single chip/sensor assemblies of different types

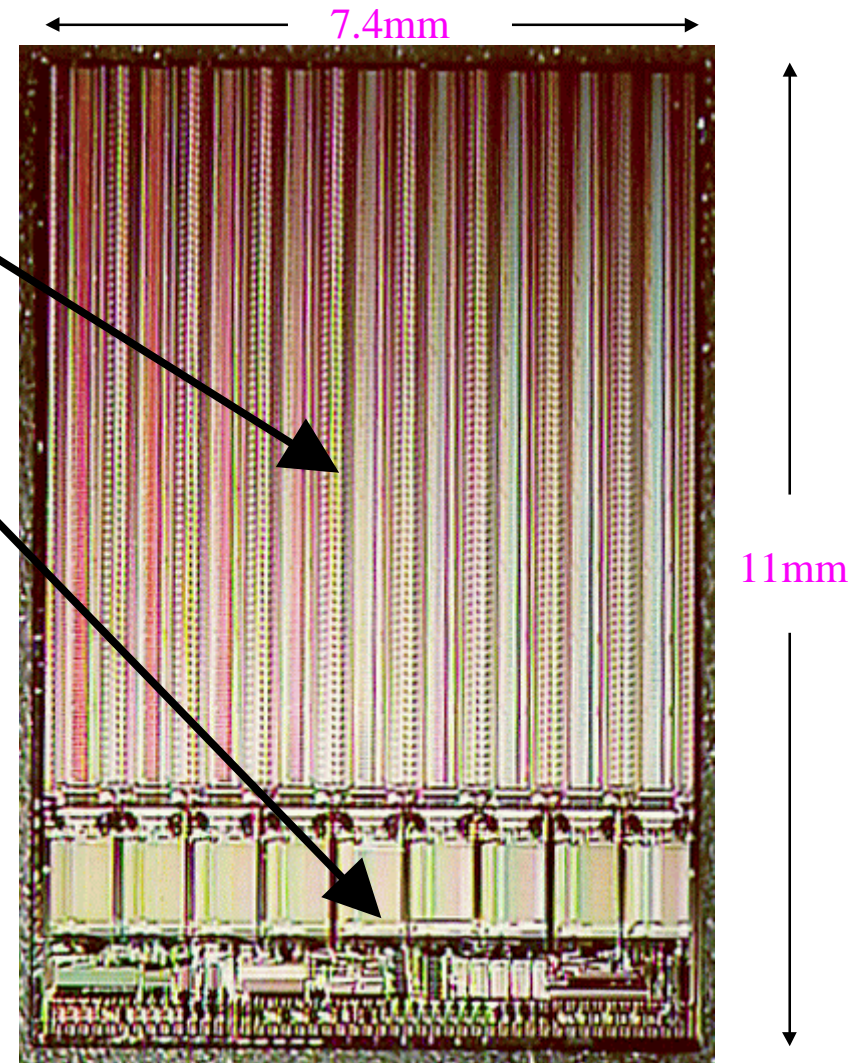


16-chip modules with flex hybrid

Pixel Electronics



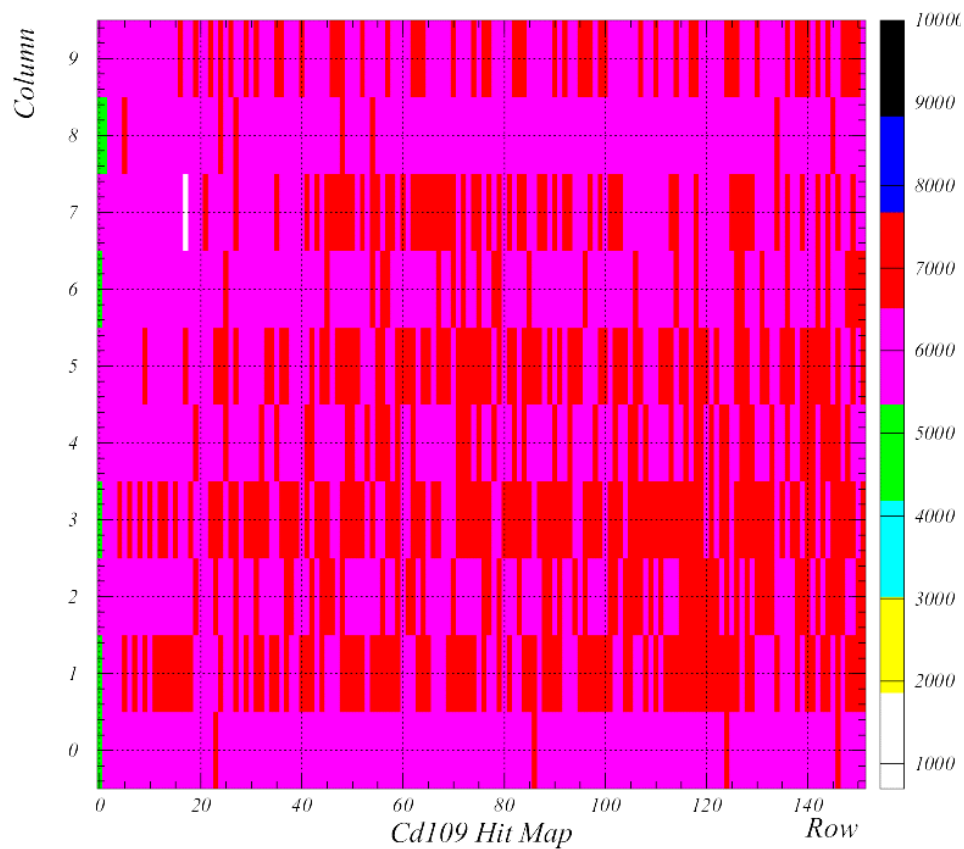
- **General features**
 - ♦ Active matrix 18x160 pixels
 - ♦ Inactive area for buffer and control
- **Critical requirements**
 - ♦ Time walk <20 ns
 - ♦ Timing uniformity across array(<few ns)
 - ♦ Low threshold(2-3K e⁻s)
 - ♦ Threshold uniformity (implemented by having DAC in each pixel)
 - ♦ Low noise(<few hundred e)
 - ♦ Low deadtime(<1% or so)
 - ♦ Robust(dead pixel OK, dead column not good, dead chip bad)
 - ♦ All of the above at 25 Mrad or more
- **Important requirements**
 - ♦ Time-Over-Threshold(TOT) measurement of charge
 - ♦ Maximize active area
 - ♦ Die size with acceptable yield
 - ♦ Thin(150 micron goal)



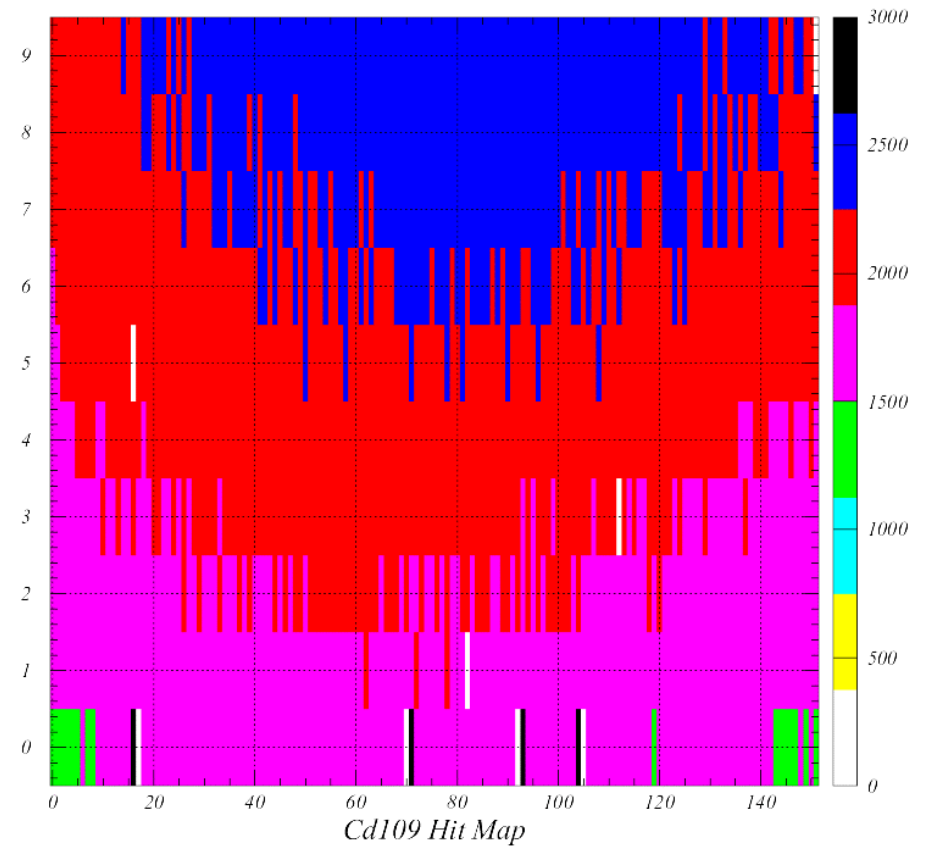
Photon Source Test



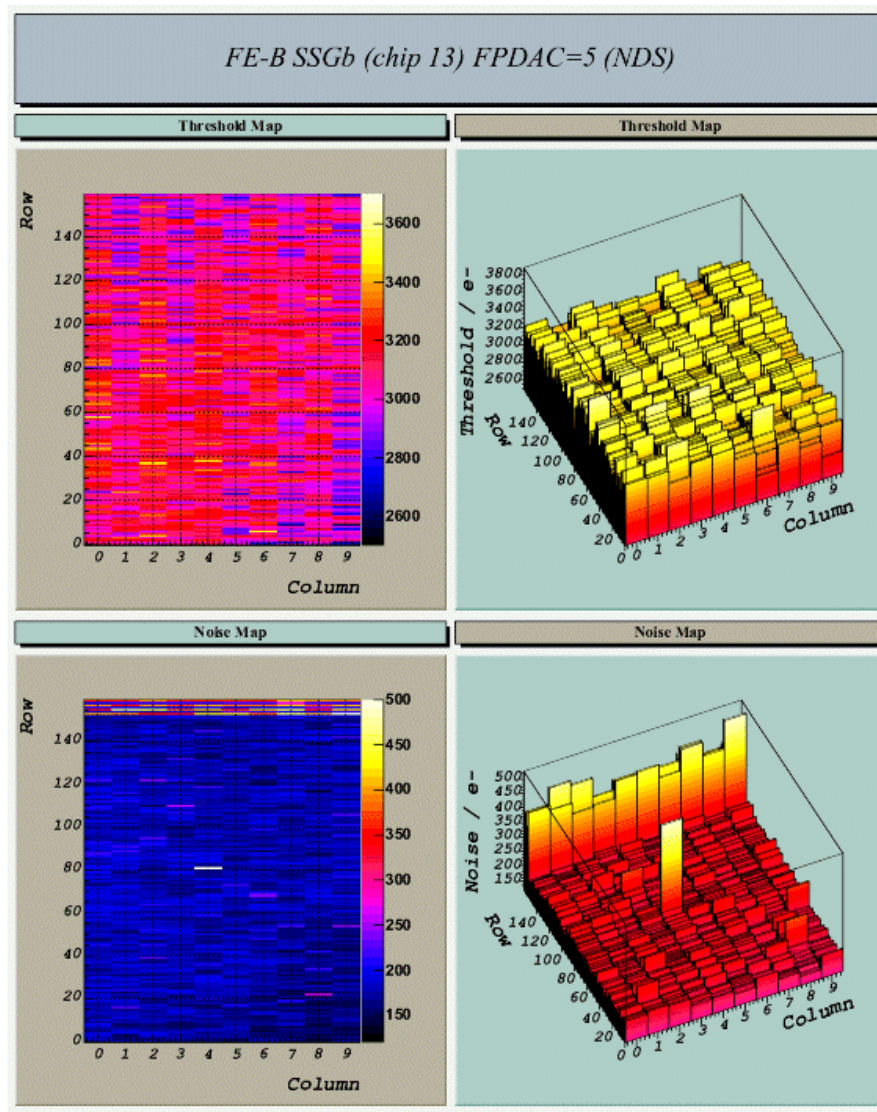
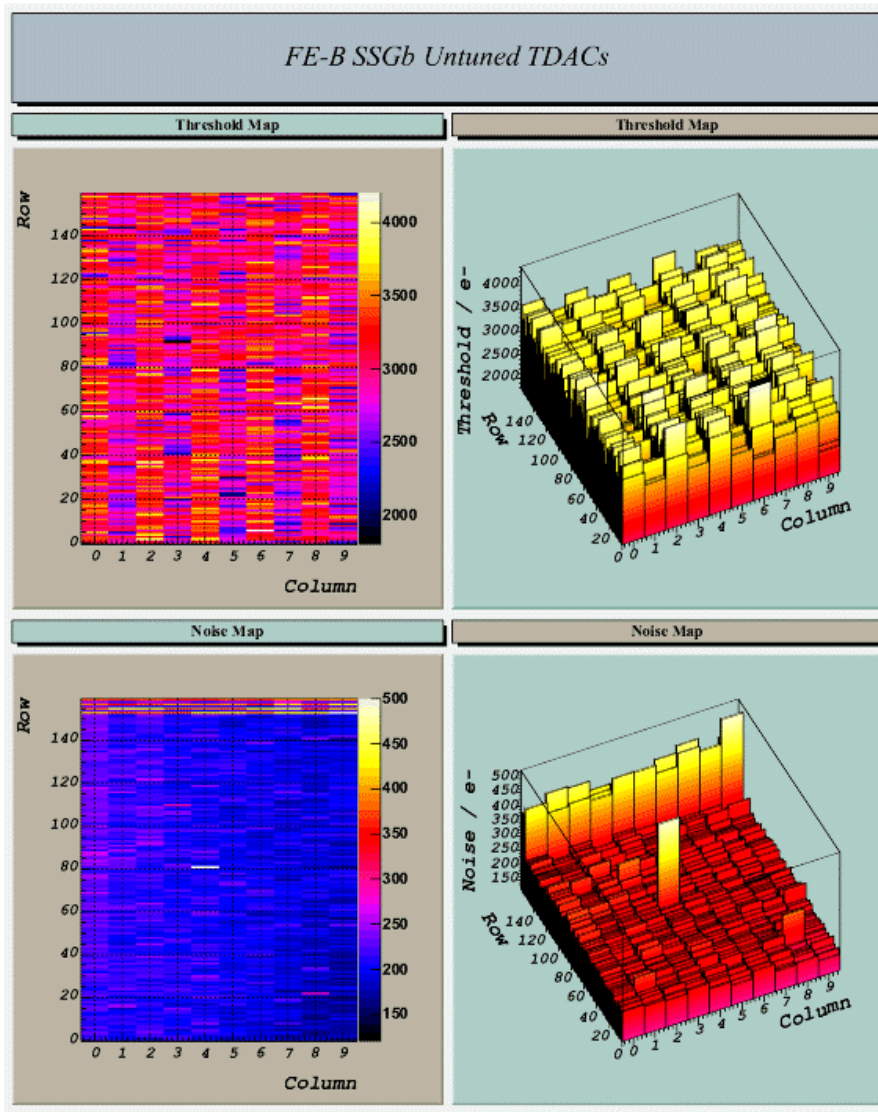
CIS_01 single-metal ST2_03 Cd109



CIS ST1 Cd109



Threshold Tuning and Noise

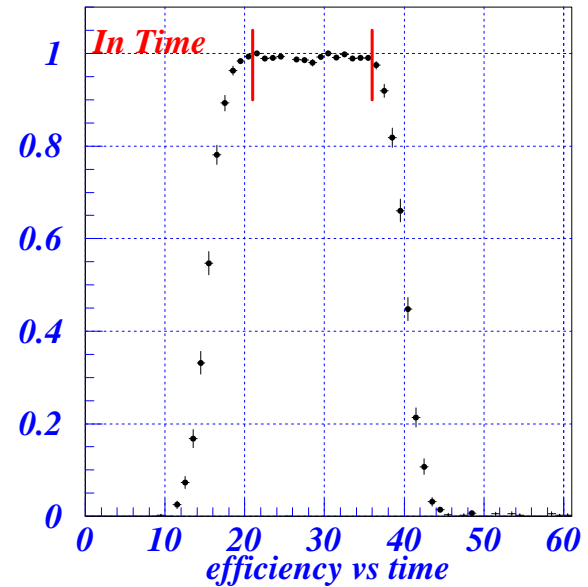


Efficiency Example



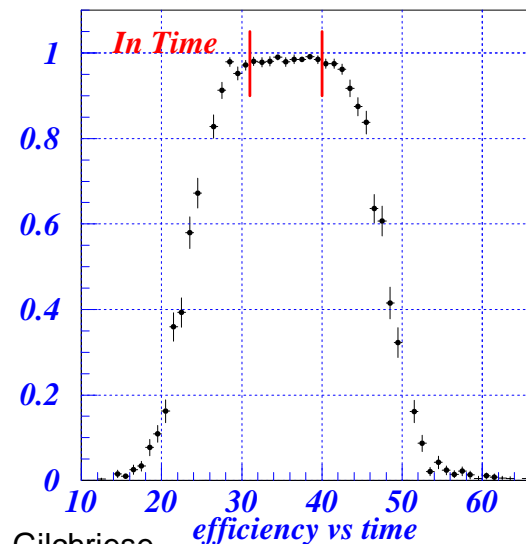
Not Irradiated - Thr. 3 Ke

Efficiency	99.1%	Losses	0.9%
1 hit	81.8	0 hits	0.4
2 hits	15.6	not matched	0.1
>2 hits	1.7	not in time	0.4



Irradiated $V_{\text{bias}} = 600 \text{ V}$ Fluence 10^{15} n/cm^2 - Thr. 3 Ke

Efficiency	98.4%	Losses	1.6%
1 hit	94.2	0 hits	0.4
2 hits	3.1	not matched	0.0
>2 hits	1.1	not in time	1.2



Lab and Test Beam Results Summary



- Extensive lab tests.
- Multiple test beam runs in 1998 and 1999
- Only rad-soft ICs so far(3 variants used - FE - A, - B, - C)
 - ♦ Dozens of single-chip/detectors have been operated successfully with multiple detector types and front-end ICs
 - ♦ 16 chip modules have been operated successfully
 - ♦ Detectors irradiated to lifetime fluence expected at LHC(10^{15}) have been read-out in a test beam with efficiency near 100%
 - ♦ Operation below full depletion voltage demonstrated
 - ♦ Preferred detector type identified in these studies and preproduction of detectors will begin by middle of this year.
 - ♦ Timing performance needed to identify bunch crossings has been demonstrated, albeit not at full system level.
 - ♦ Operation at thresholds 2,000-3,000 electrons demonstrated
 - ♦ Threshold uniformity demonstrated.
 - ♦ Spatial resolution as expected
- Conclusion
 - ♦ Proof-of-principle of pixel concept successful

Pixel Electronics/Modules

Current Status



- The transition from rad-soft to rad-hard has not been as smooth as we like(have you heard this before...)
- First rad-hard, full-prototypes were delivered end October 1999.
 - ♦ Some “dumb” mistakes, but not bad enough to prevent understanding behavior
 - ♦ But yield from vendor(Temic) was terrible.
 - ♦ Through very careful detective work, this is attributable to fabrication flaws in individual transistors at rate much, much higher than expected. Characterization of individual transistors in circuit via microsurgery done but source of fabrication problem not understood by vendor.
 - ♦ Backup run was launched by vendor and wafers received about 2 weeks ago. Preliminary yield from these wafers is very much higher but why is not yet understood. Need more data. Source of fabrication problem still not understood.
 - ♦ Detailed design verification proceeding as best as possible under these conditions and revised version ready to submit this month to vendor.
- Design work with second vendor(Honeywell) led by LBNL but slowed substantially as result of lack of IC engineering manpower and need to understand problems with Temic. Nevertheless design work is progressing well and will take into account lessons learned. This is likely a better, certainly denser, technology(albeit likely a more expensive one).
- Other aspects of module development are proceeding OK but held back by lack of IC electronics.

US Project Status



- US ATLAS recently finished an “Estimate-to-Complete” exercise that resulted in revised costs and schedules for all US responsibilities.
- Silicon strips
 - ◆ Revised schedule is within few weeks of original baseline established late 1998
 - ◆ Costs are about same(including contingencies)
- Pixel system
 - ◆ Continues to be approved for development-only
 - ◆ Mechanics, sensors about on original schedule
 - ◆ Electronics, and thus modules, delayed
 - ◆ Costs within original baseline envelope(including contingencies)
 - ◆ Production baseline review planned for November 2-3, 2000

LBNL Leadership Roles



M. Barnett	US member of ATLAS Education/Outreach Committee US ATLAS Education Coordinator
K. Einsweiler	Pixel Electronics coordinator Member Pixel Steering Group
M. Gilchriese	Outgoing chair of Inner Detector Institute Board Member Pixel Steering Group US ATLAS Silicon Project Manager
C. Haber	Convenor SCT barrel module assembly Member SCT Steering Group
I. Hinchliffe	ATLAS Deputy Physics Coordinator ATLAS Leader of Monte Carlo Group US ATLAS Physics Manager
D. Quarrie	ATLAS Chief Software Architect
J. Siegrist	Convenor of US ATLAS Institutional Board

Issues



- **Physicist Personnel and Demographics**
 - ◆ About 5 FTE senior physicists and two postdocs are now working on silicon tracking, computing and physics simulation.
 - ◆ This is at least one senior physicist and two postdocs short of need.
 - ◆ As noted last year, we have large age gap(decade+) between youngest senior physicists and few postdocs.