

Advances in Radiation Active Pixel Sensors (RAPS) Architectures

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In the recent years, active-pixel (APS) architectures, frequently exploited for the visible-light detection have been proposed for detection of minimum ionising particles (MIP), offering an alternative to more common architectures based on microstrip or passive pixel arrays. In APS schemes, each pixel includes control devices, for photodiode buffering, precharge and reset. This potentially improves SNR, making it unnecessary to adopt dedicated technologies. The adoption of standard fabrication processed brings a number of advantages, in term of both performance and costs [1]. This work aims at implementing a single-chip, complete radiation sensor system, including sensitive device as well as read-out and signal processing sections, by exploiting a fully-standard, commercial technology. The possibility of including versatile and performing circuitry, in turn, allows for the evaluation of innovative active pixel architectures, different read-out strategies, and complex data management algorithms. In [2], design and development of a prototype chip based on these principles were introduced, whereas its functionality was experimentally verified in [3].

In particular, for the fabrication of the RAPS01 chip, a 0.18 μm CMOS technology was used. The RAPS01 chip included several prototypal matrix structures, featuring different pixel layout options and different pixel number and pitch. Such a large amount of output data can be efficiently managed by means of a dedicated PCB test board, which has been designed and realized for the specific task at hand. It communicates with three National Instruments data acquisition boards. Two digital (PCI-DIO-96, PCI-6503) and an analog/digital (PCI-6014) boards are used, for a total of about 130 I/O and control signals. Several LabView routines, combined in a common graphic interface, allow for fast and inexpensive control and addressing signal setting and analog/digital output read-out.

After validating the detecting principle [3], the aim of test procedures is the evaluation of the sensitivity of the sensor response on the actual operating conditions. In particular, the bias scheme of the readout amplifiers is digitally programmable, allowing for the optimisation of the pixel responses in terms of voltage swing and propagation delay. Fig. 1 shows the actual output for the optimal configuration. Once amplifiers have been tuned-up, uniformity of the response over the whole matrix has been checked for. In particular, Fig. 2 shows the pixel response to a uniform flux of coherent white light for a 8 x 8 APS matrix. Remarkable voltage drops (above 1 Volt) are exhibited; the overall uniformity is pretty good, featuring deviations in the range of a few percent. with respect to the mean value. Correction of such noise effects can be achieved by means of correlated double sampling techniques. Extensive testing is now under way: cross-talk analyses and check of sensibility to different radiation sources are planned; to this purpose, the design of a sophisticated optical test bench has been completed, with high movement precision (position repeatability below 0.2 μm) and including an optical section with laser beam featuring few microns of spot size and MIP equivalent energy.

At the same time, next generation chip (RAPS02) is being designed. In particular, looking at particle-detection applications, an improved sparse-matrix read-out scheme is proposed. In the original WIPS scheme [3], the sensor array acts as a switch matrix, in which column- and row-lines are precharged at opposite values. As soon as a pixel is hit, its output turns on the switch and makes charge sharing between row and column possible, allowing for asynchronous detection of the event.

In this paper, this approach is extended, discussing the organization and design of a new architecture. We still focus on a flexible read-out scheme, capable of accessing the sensor array in different modes: by means of a programmable mode bit, the array can be read in a fast, sparse mode, or in a conventional line-scan mode. A potential weak point of the WIPS scheme consisted of the limited swing of the switch control-signal: due to this, the switch transistor is biased close to its threshold voltage, which may imply relatively large leakage (i.e., dark) currents. A further detail is the need of periodic reset cycle, which introduces some “blind” intervals in the operating routine. To cope with all these issues, we investigated the pixel scheme depicted in Fig. 3: the photodiode still drives a source-follower buffering stage, which, in turn, drives a high-gain, on-pixel CMOS amplifier: the pixel output swing is thus greatly enhanced, and the column-row switch can be more neatly controlled. Simulations have been carried out, accounting for an accurate model of the photodiode charge collection [2], for the competitive action of the n-well and for parasitic estimation: figures close to the 1V range have been estimated, as shown in Fig. 5. With respect to the WIPS scheme, the output signal is inverted, so that an nMOS switch can be used to control column-row charge sharing. Moreover, the output positive pulse can also be used to self-trigger the pixel reset: by means of the feedback path shown in figure, the pixel output pulse turns on the reset nMOS, thus recovering the precharge condition of the photodiode cathode. This is useful in a sparse read-mode, since it makes it unnecessary the adoption of an external reset signal: completely asynchronous operation is thus attained. In order to allow for conventional, frame-scan access mode, a “freeze” pass transistor is introduced, which may be used to inhibit the feedback path. Nevertheless, since a “zero-threshold” reset transistor is exploited, a smaller amount of reset current is available even during freeze conditions: time constants, however, are completely different; 100 ns are sufficient for self-reset if the feedback is active, whereas 80 μs are needed to recover the original status with inhibited feedback. This time interval allows for serial scan operations and do not impose too severe constraints on the frame cycle. The scheme has been named SHARPS (Self-resetting High-gain Active Radiation Pixel Sensor).

The overall SHARPS pixel layout is shown in Fig. 4: pixel size is 10.3 μm x 10.3 μm ; pMOS device size is small with respect to sensitive photodiode area, so that charge collection efficiency is not significantly affected by this. Simulation results, accounting for different relative positions of the impinging radiation, are shown in Fig. 5, and suggest that a fair charge resolution can be achieved. A 2-bit A/D conversion is performed at each row and column, so that a spatial resolution finer than the pixel pitch can be obtained by comparing neighbouring lines.

More generally, the adoption of CMOS technology makes it possible to implement versatile and powerful function in a straightforward manner: configurable row and column amplifiers have been designed, allowing for digitally programming bias point and gain. In order to reduce power consumption, power-switching techniques are used, placing unused amplifiers in stand-by. To

cope with SEU, fault-tolerant architectures have been devised, based on a TMR (Triple Modular Redundancy, [4]) approach, and the state sequences in the control-unit FSM's have been carefully encoded (Hamming codes). Simulation predicts an operating frequency in excess of 300 MHz for the readout system; a small area impact is expected, with respect to the controlled sensor array. It is worth emphasizing that even if the approach devised so far is capable of effectively detect sparse events, it is by no means limited to such a scope: by properly managing control signals (i.e., inhibiting the pixel feedback and activating in a given sequence line amplifiers) a conventional frame-scan readout can be carried out as well. Moreover, the pixel energy-resolution is exploited here to increase spatial resolution; nevertheless, thanks to flexible, configurable readout circuitry, the same chip will be evaluated for potential applications such as α -, β -, γ -microdosimetry, spectrography, and eventually (through coupling with a photomultiplying layer) X-micro-radiography.

References

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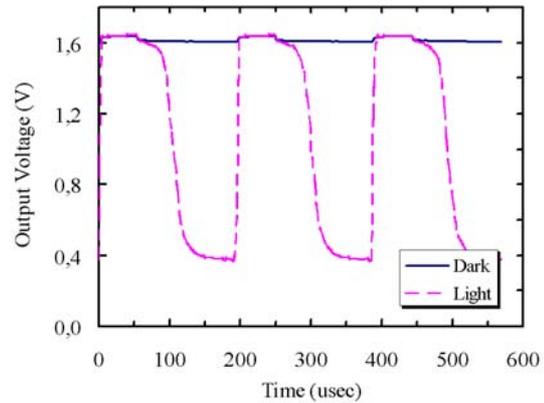


Fig. 1: APS responses, for optimized amplifier bias scheme.

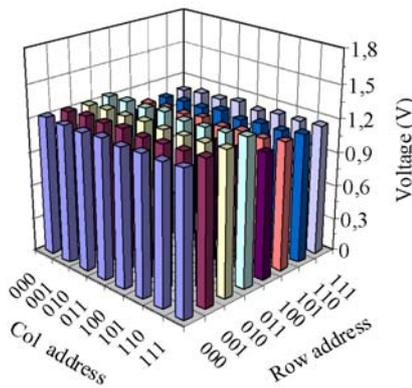


Fig. 2: Voltage drops at the end of the evaluation period (namely, immediately before the reset phase).

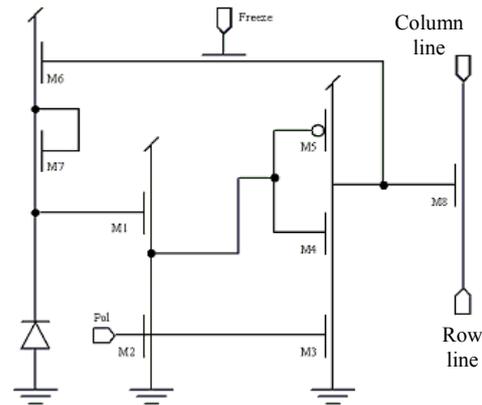


Fig. 3: SHARPS active pixel circuit.

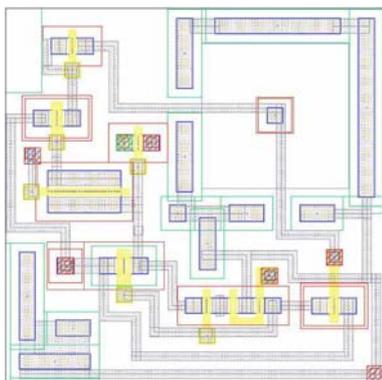


Fig. 4: SHARPS pixel layout.

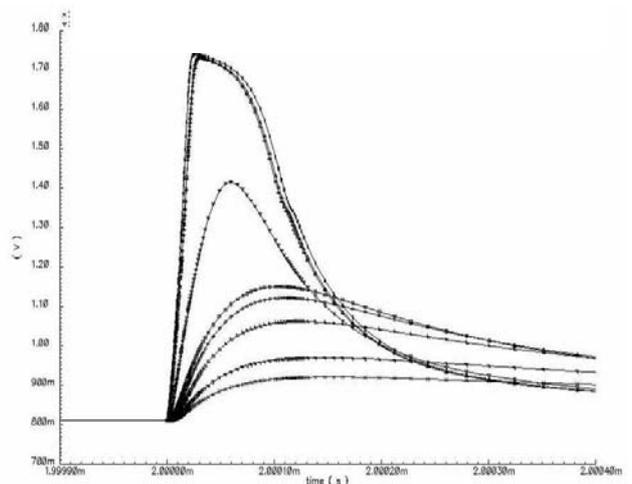


Fig. 5: SHARPS pixel simulated response, at different relative positions of the impinging radiation.