The Active DEPFET Pixel Sensor for Future e^+e^- Linear Collider Experiments

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***Abstract*--The e^+e^- linear collider physics program sets highly demanding requirements on the accurate determination of charged particle trajectories close to the interaction point. A new generation of DEPFET active pixel sensors with ~25 μm pixel size has been developed to meet the requirements in point measurement resolution and multiple track separation. The paper presents the design and technology of the new linear MOS-type DEPFET sensors and the gives a comparison between the previously simulated properties with the actually measured characteristics. The charge storage capability of the DEPFET pixels enables a read-out scheme where only one row is active at a time. The resulting low power consumption of the array together with the low noise operation of the devices allow the design of extremely thin sensors needed for efficient determination of secondary and tertiary vertices. A module concept and a technology for the production of ultra-thin fully depleted DEPFET sensors will be presented. The technology makes efficient production of thin wafer-scale pixel arrays and safe assembling of the sensor modules into a vertex detector possible.**

I. THE DEPFET PIXEL CELL AND THE MODULE CONCEPT

The vertex detector for a future linear e^+e^- collider (e.g. TESLA[1]) will be a set of cylindrical detectors arranged in ladders around the interaction point. Each ladder is an array of pixel cells read out at the end of the ladder outside the fiducial volume. In the case of a DEPFET as the pixel cell, the signal charge is measured in every pixel on a row-by-row basis and the DEPFETs are successively switched on by means of gating lines controlled by shift registers located at the long side of the ladder.

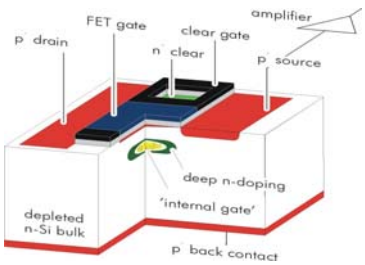

Fig. 1. DEPFET principle

The MOS-type DEPFET is integrated onto a fully depleted silicon substrate. All the charge generated by a traversing particle drifts due the electric field configuration inside the device toward the surface and is collected in a potential minimum for electrons underneath the external gate of the DEPFET. The charge cloud is stored and modulates the current in the channel of the FET which forms in this way the first amplification stage. After signal read out is finished, the charge is removed by applying a positive voltage to the "Clear" contact (see Fig.1). The combination of the detector material and first amplification stage in one single device has a number of advantages. The sensitivity of the entire bulk and the low capacitance of the read out node enable low noise operation over a large range of temperatures. This is of particular interest for application at linear collider experiments where the sensors have to be as thin as possible. A second important point is that the charge is measured at the place of generation, so trapping due to bulk damage by NIEL is not an issue. And finally, since the transistors can be turned off during charge collection and since only one row is electrically active during read out, the expected power consumption in the sensitive area is extremely low (≈1W for the entire TESLA vertex detector, taking advantage of the duty cycle at TESLA).

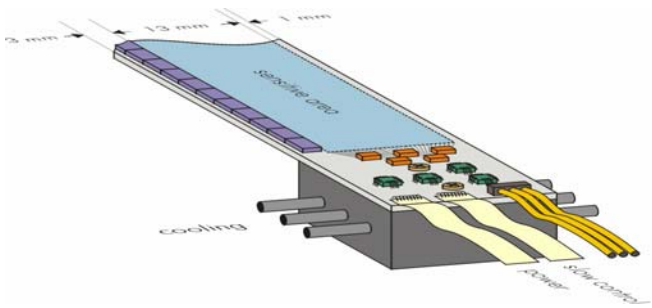

Fig. 2. Module concept for the first layer at TESLA.

In our concept the DEPFET pixel array is made on thin detector grade silicon supported by a directly bonded silicon frame of 300 μm thickness. Fig.1 shows the sketch of such a module for the innermost layer at TESLA. The material contribution the ladder is 0.11 % X_0, including the frame and the (also back thinned to 50 μm) steering chips at the edge. The details of the read out and steering chips[2] as well as the system aspects will be the topic of a separate presentation at

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this conference. We will concentrate here on the technology of the sensor production and the pixel cell itself.

II. Technology Description and first results

Fabrication of large wafer scale pixel matrices demands a fault-tolerant and reliable technology. In order to meet these requirements, a new technology with two polysilicon and two metal layers was introduced at the MPI Semiconductor Laboratory. In order to guarantee a high homogeneity concerning the operating parameters of the individual cells of the entire matrix, a MOS-type DEPFET was chosen as the pixel cell. Extensive simulations led to the design which can be seen in Fig.3. The figure of merit for such a device is the transconductance of the internal gate g_q=dI/dQ, a measure for the internal amplification of the device. The achieved value is with g_q=0.4 nA/e^- in very good agreement with dynamic 2D simulations.

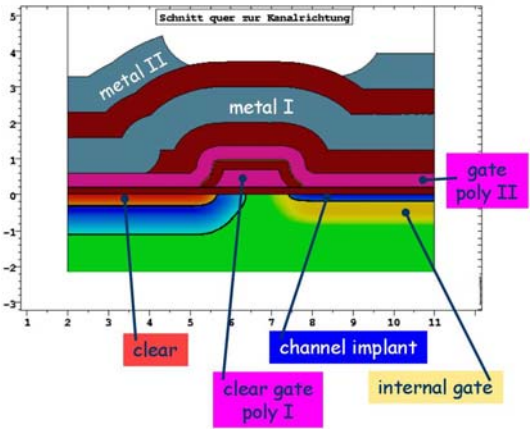

Fig. 3. Double polysilicon and double metal technology for MOS-type DEPFETs.

Another important issue is the ability of a complete removal of the charge in the internal gate after read out to avoid the associated reset noise. The complete clearing of the internal gate was proven by static measurements and results in the hitherto not achievable low noise of ENC=2.2e^-(rms) at room temperature (see Fig.4).

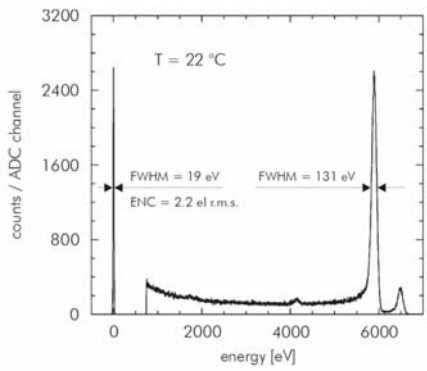

Fig. 4. ^{55}Fe Spectrum taken with a circular MOS-type DEPFET optimized for spectroscopic applications.

III. Thinning technology

Back thinning of ASICs is already widely used in semiconductor industry. However, these technologies are not applicable for fully depleted sensors with an electrically active backside. Fig.5 illustrates the thinning technology based on direct wafer bonding and deep anisotropic etching to build such thin devices with a minimum of processing steps after thinning.

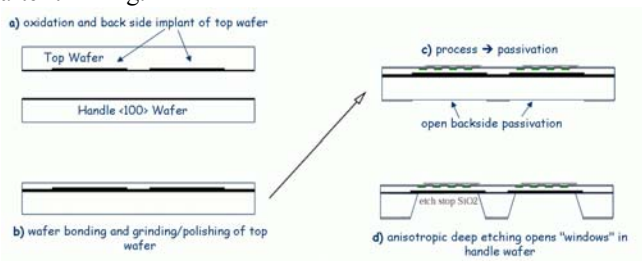

Fig. 5. The process sequence for production of thin silicon sensors with electrically active back side implant starts with the oxidation of the top and handle wafer and the back side implantation for the sensor devices(a). After direct wafer bonding, the top wafer is thinned and polished to the desired thickness(b). The processing of the devices on the top side of the wafer stack is done on conventional equipment; the openings in the back side passivation define the areas where the bulk of the handle wafer will be removed(c). The bulk of the handle wafer is removed by deep anisotropic wet etching. The etch process stops at the silicon oxide interface between the two wafers(d).

The feasibility of this approach has been shown with the production of 50 µm thin PiN diodes. The volume generated reverse current of the thin devices is with <1nA/cm^2 extremely encouraging. The mechanical stability of the diced chips is even for wafer scale devices sufficient for safe handling and mounting. There is no distortion visible on the 50 µm thin large area (6.5cm^2) silicon membrane with single sided aluminium metallization.

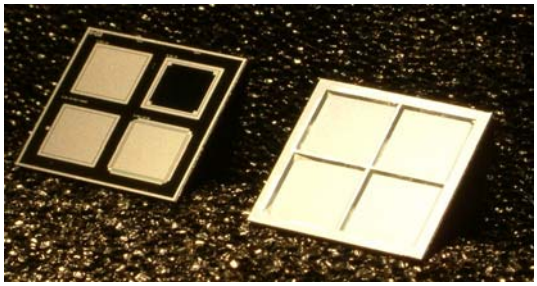

Fig. 6. Top (left) and handle wafer side (right) of two diced chips (1 cm^2) with four 10 mm^2 diodes on 50 µm thin silicon.

IV. References

[1] T. Behnke, S. Bertolucci, R. D. Heuer, and R. Settles, Eds., "TESLA Technical Design Report, Part IV: A Detector for TESLA", DESY, Hamburg, Germany, DESY 2001-011, March 2001

[2] M. Trimpl, L. Andricek, P. Fischer, G. Lutz, R.H. Richter, L. Strueder, et al., "A Fast Readout using Switched Current Techniques for a DEPFET Pixel based Vertex Detector for TESLA", *Nucl. Instrum. Methods*, vol. A511, pp. 257-264, 2003.