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WBS 1.1 Silicon Subsystem

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(LBNL)

PAP Review
April 1999

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WBS 1.1 Institutions

SUNY Albany

UC Berkeley/LBNL

UC Irvine

University of New Mexico

Ohio State University(new since last PAP review)

University of Oklahoma/Langston Univ.

UC Santa Cruz

University of Wisconsin

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Deliverables - Goals

1.1.1 Pixel System(Preliminary)

- 1.1.1.1 Mechanics - design, assemble and install disk system(100%)
- 1.1.1.2 Sensors - design(30%) + procure and test 250 wafers(20%)
- 1.1.1.3 Electronics - design(40%)+procure and test 8500 ICs(25%)
- 1.1.1.4 Hybrids - design, fabricate, test(25%)
- 1.1.1.5 Modules - design, fabricate and test disk modules(100%)

1.1.2 Silicon Strip System

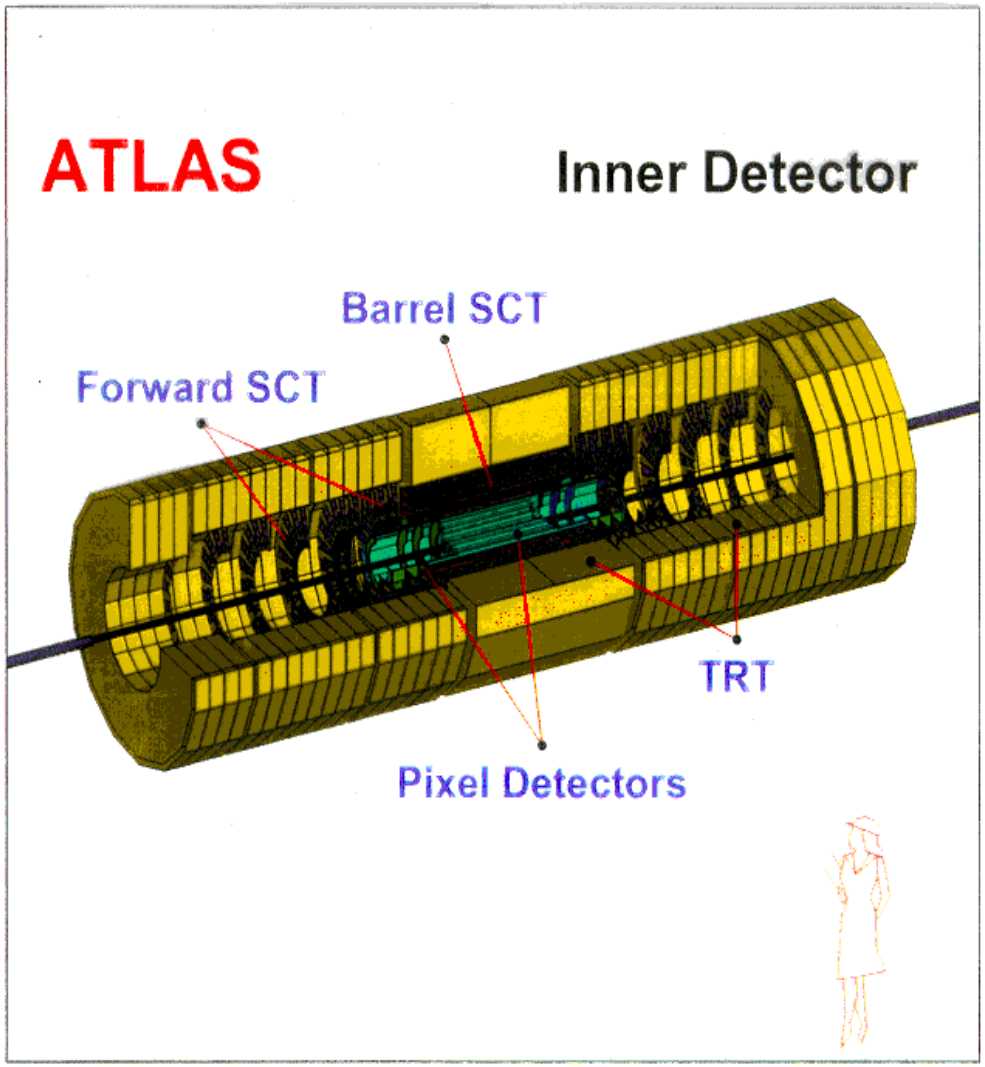
- 1.1.2.1 Electronics - design(25%)+procure and test ICs(50%)
- 1.1.2.2 Hybrids - barrel design (100%) + procure all needed for US modules
- 1.1.2.3 Modules - deliver 670 modules(15%)

1.1.3 Read-out Drivers

- Test beam support - pixel support boards(3 generations), DSP modules(50) + preprototype RODS(16)
- Design, fabricate, test and install pixel (100%) and SCT(75%) RODs.

Pixel deliverables preliminary

Other areas stable



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Summary Status

- **1.1.1 Pixel System(PIX)**
  - Pixel Technical Design Report completed(May 30, 1998) and approved by CERN
  - In U.S. approved for development through FY00 with construction baseline review to occur before start FY01.
  - Very substantial technical progress made in all areas
  - Underspending (other funding sources utilized)
  - In general, on schedule except for rad-hard IC development (currently six month delay projected relative to baseline)

1.1.2 Silicon Strip System(SCT)

- After long struggle, design of 2nd round of IC prototypes complete or nearly complete
- Spending on baseline target(include baseline change requests) but tight
- Delay in ICs by 3-5 months relative to baseline impacts other areas(hybrids)
- Items not tied to ICs on schedule

1.1.3 Read-Out Drivers(ROD)

- Test beam support provided on schedule and on budget
- Recent review on March 25-26 selected between competing designs for preprototype ROD
- Materials costs projected to be under budget. EDIA to be evaluated.
- New schedule under development but currently have five month delay in preprototype resulting from delayed decision on architecture for preprototype.
- No impact on SCT (since delays in ICs) or PIX(not planned until 2000)

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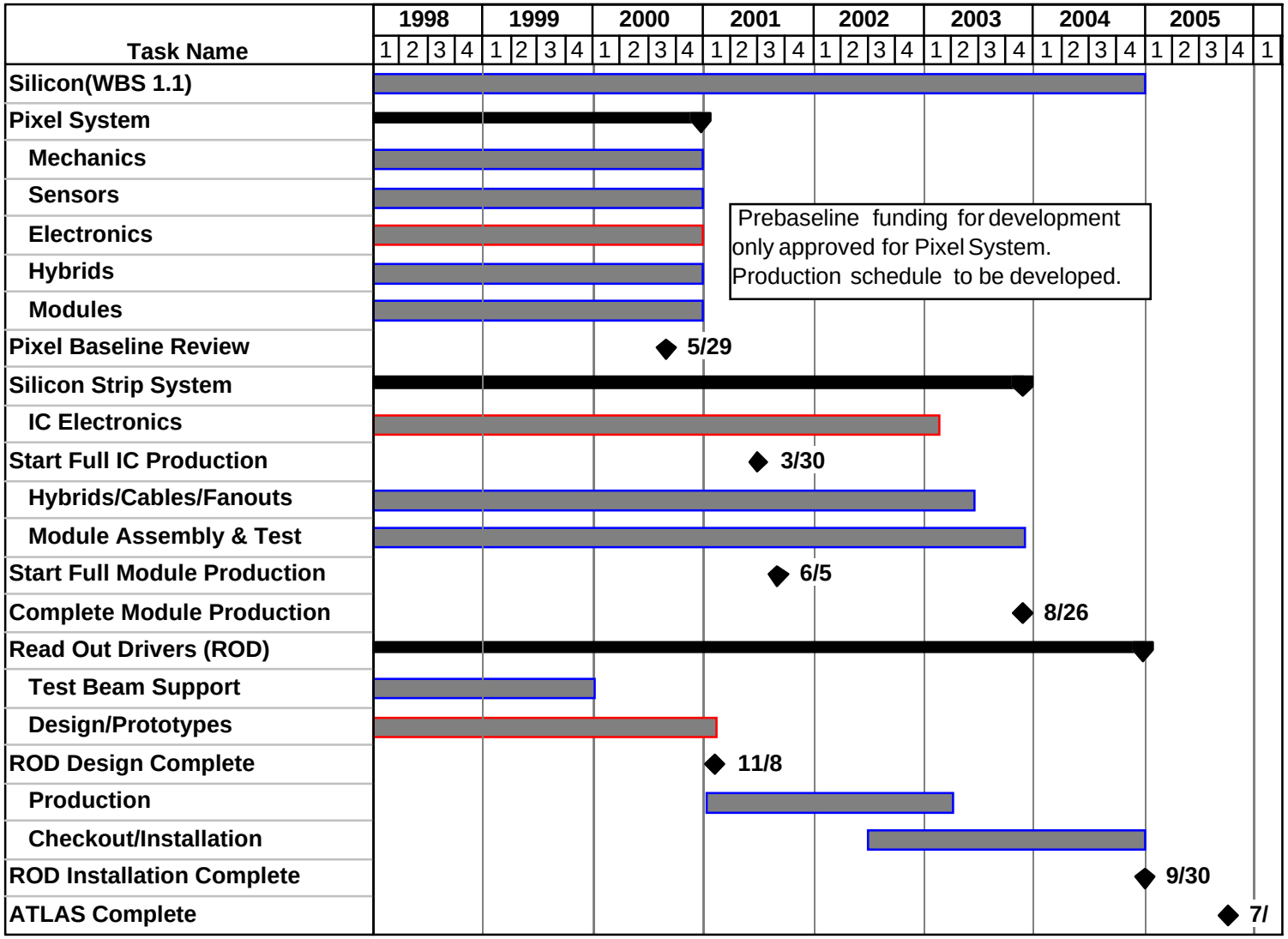
WBS 1.1 Baseline Schedule



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WBS 1.1.3 Read-Out Drivers

- **Test beam support**
  - **Digital Signal Processor(DSP) modules for both pixel and silicon strip laboratory and test beam measurement.**
    - **Ongoing for last three years.**
    - **Extensively made available to collaboration**
  - **Pixel support**
    - **First generation test chips supported by custom test boards - this work is complete**
    - **Custom VME boards for full-scale prototype pixel electronics essentially complete(upgrades only)**
    - **These boards are part of dedicated, PC-based test system developed. Under high demand as standard.**
  - **Overall - very successful**

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WBS 1.1.3 Read-Out Drivers

- **Preprototype ROD**
  - Requirements review completed.
  - Essential model reviewed
  - Preliminary interface documents complete
  - Two principal implementations pursued
    - FPGAs(in data path) + DSPs(for monitoring)
    - All DSPs
  - Design team unable to converge on single choice
  - Review held on March 25-26 and FPGA+DSP approach selected. Review committee report at http://www-physics.lbl.gov/~gilg/RODReport1.PDF
  - Organization of design team underway

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WBS 1.1.3 Read-Out Drivers

- **Cost and Schedule**
  - **Recent materials cost estimates appear to be significantly under the baseline cost estimate, primarily because many more optical links can be handled by a single board => fewer boards.**
  - **Schedule needs revision now that choice has been made**
    - **Preliminary 5 month delay to 1st preprototype**
    - **Preprototype more advanced => eliminate prototype step?**
    - **Although there is substantial float in production schedule, I propose holding PRR date until can review revised schedule**

	BASELINE	CURRENT
1st preprototype compl.	30-Mar-99	31-Aug-99
Prototype complete	8-Mar-00	TBD
Preproduction complete	11-Sep-00	TBD
Prod. Readiness Rev.(PRR)	8-Nov-00	8-Nov-00
5% production complete	18-Sep-01	18-Sep-01
Production complete	19-Feb-03	19-Feb-03

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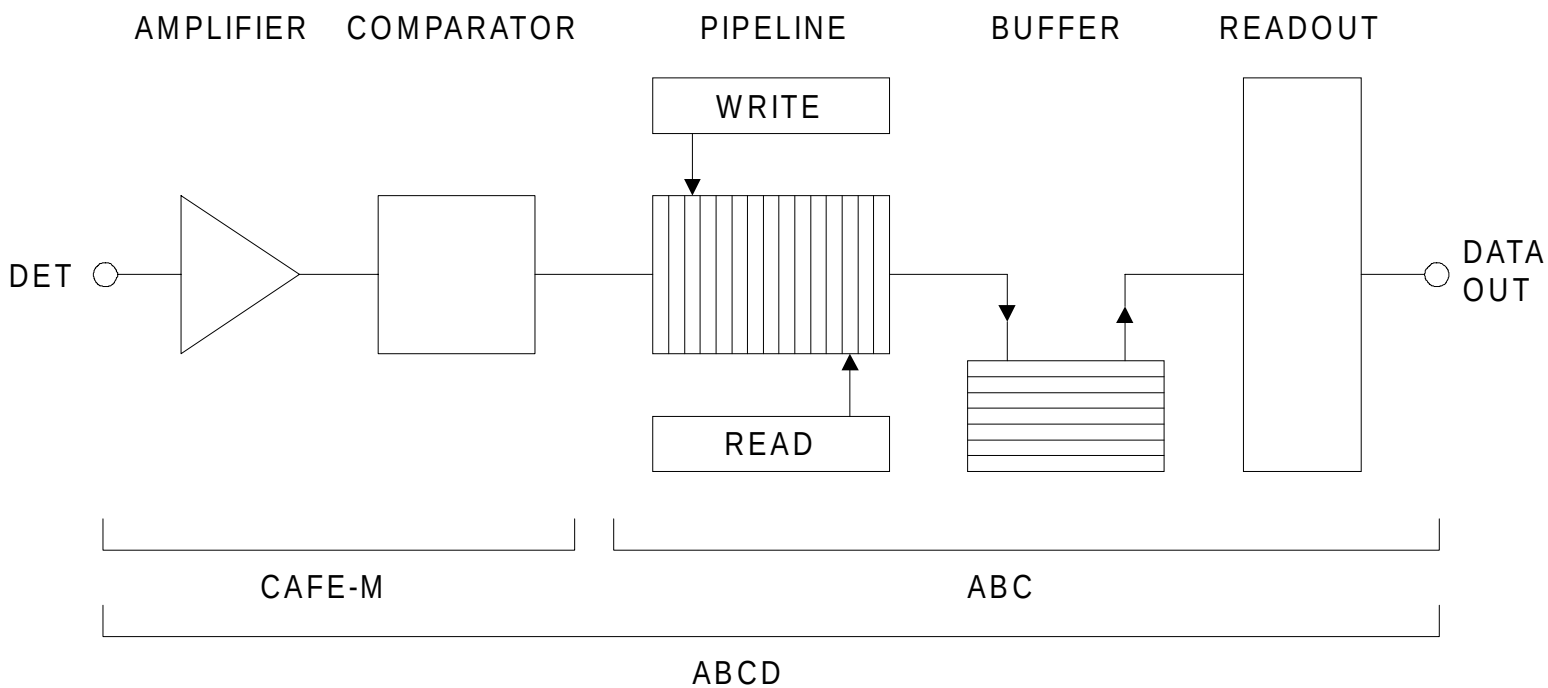
WBS 1.1.2.1 Silicon Strip IC Electronics

- **Two rad-hard solutions under development**
  - **CAFÉ(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips. This is the US cost baseline.**
  - **ABCD(BiCMOS from Temic) - 1 chip. Expected to be significantly cheaper than cost baseline.**



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WBS 1.1.2.1 Silicon Strip IC Electronics

- First prototypes for all three ICs were not satisfactory for different reasons
- CAFÉ(Maxim bipolar)
  - Resistance changes after irradiation not recognized, otherwise OK
  - Extensive radiation testing done
  - Took opportunity to look at other parts of circuit again
  - Able to test thoroughly
- ABC(Honeywell CMOS)
  - Many dumb mistakes
  - Inadequate simulation models (since improved) for specific problem
  - Honeywell made error in mask generation
  - Again took opportunity to look at circuitry
  - Able to test few die after focussed ion beam surgery.
- ABCD(Temic DMILL BiCMOS)
  - Digital part OK with minor errors
  - Analog part far from specs. Substantial revisions to circuit design made.
  - Process control on first run not adequate, Temic made second run
  - Instability in analog section, took long time to understand via measurements and simulation. Some uncertainties remain.
  - Able to test

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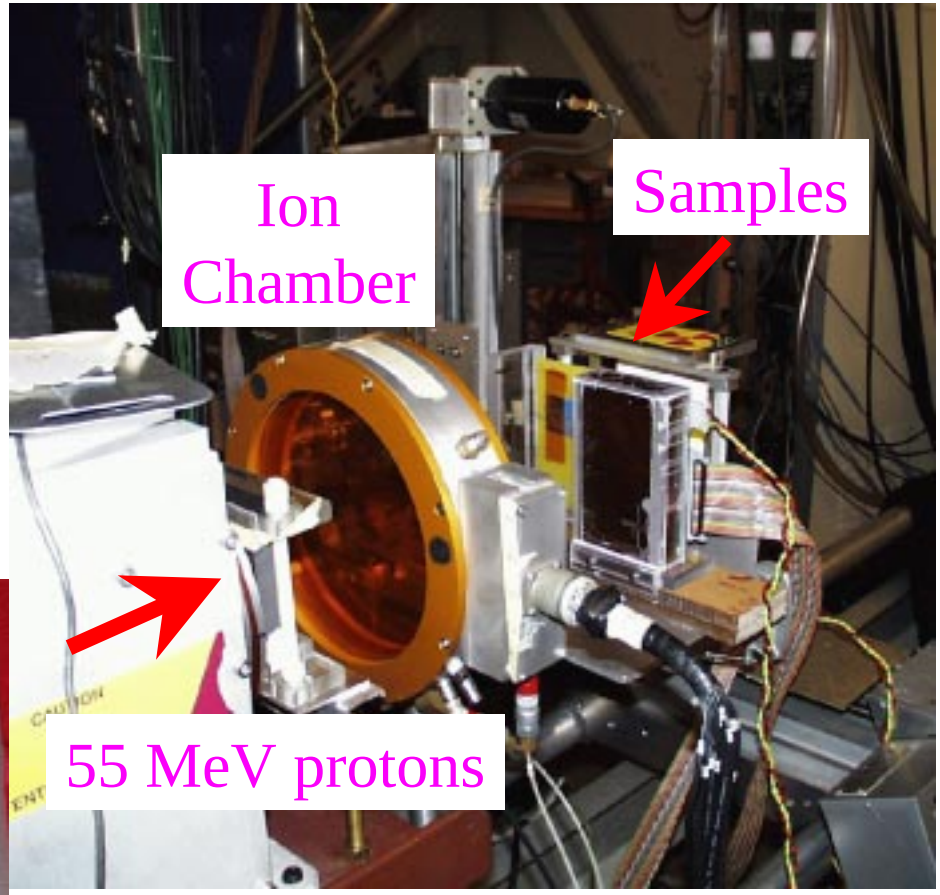
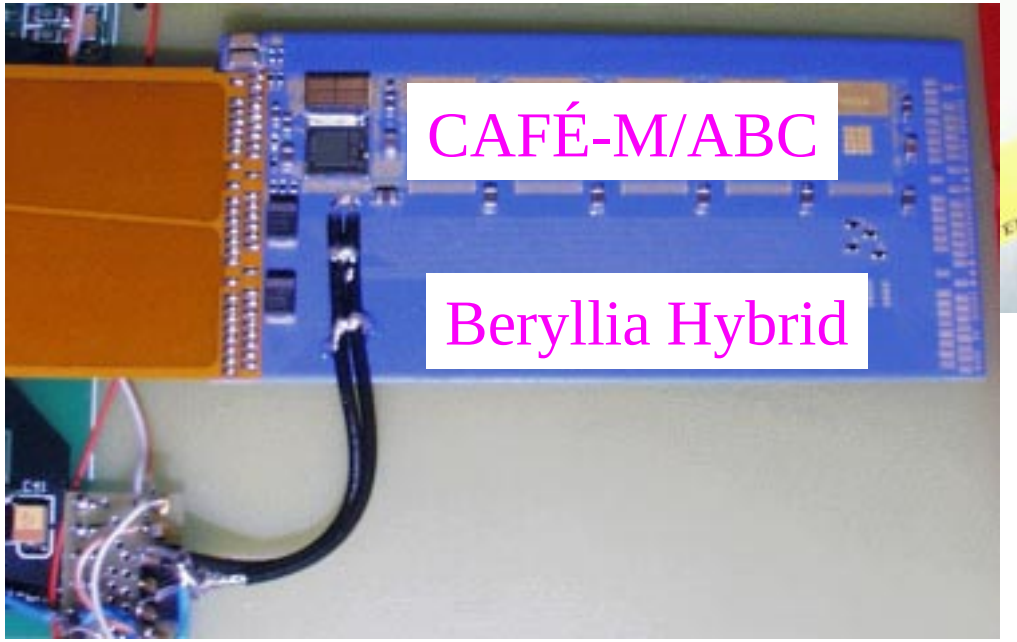
Irradiation Studies

- **The LBL 88” cyclotron has been used for irradiation studies of all three ICs.**
- **The CAFÉ-M/ABC(fixed) pair and the ABCD have been mounted on hybrids, irradiated and read out in place for full functionality tests.**





88” Cyclotron

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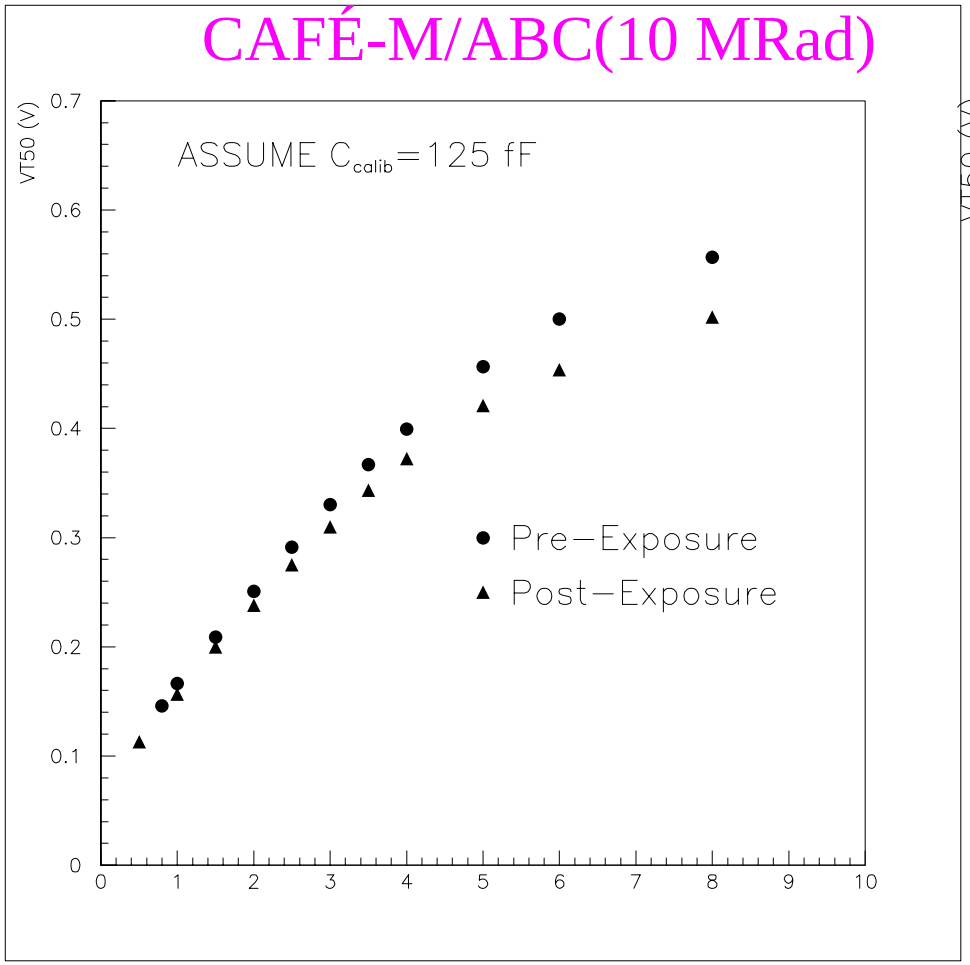
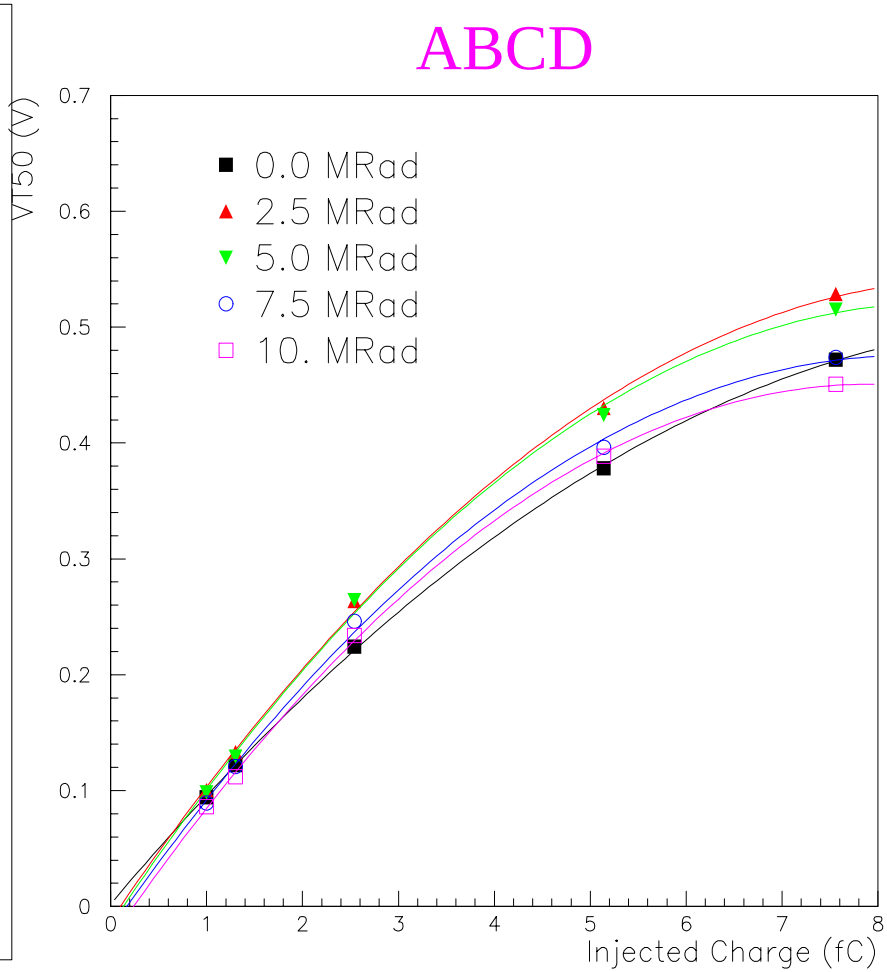
Pre-rad/post-rad Comparison





Injected Charge(fC)

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WBS 1.1.2.1 Silicon Strip IC Electronics

- Long and careful redesign of all three ICs. After first failure, have been very cautious(we hope). Multiple design reviews(with external experts)
- CAFÉ(Maxim bipolar)
  - Submitted for fabrication on january 26.
  - Maxim changed to 6” line after contract signed => will get 6” wafers for original price, thus about twice the number of die expected.
- ABC(Honeywell CMOS)
  - In final simulation and verification stage
  - Expect submission end of April
- ABCD(Temic DMILL BiCMOS)
  - In final verification stage
  - Submission is imminent
- Test system development for all three is advancing well and currently on schedule to be ready when fabrication is complete
  - CAFÉ-M at Santa Cruz
  - ABC at RAL and LBNL
  - ABCD at CERN and LBNL
  - Many other groups also involved in testing when mounted on hybrids
- Frame contract covering all orders to Honeywell, Harris and Temic in place at CERN. Revised cost information provided.

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WBS 1.1.2.1 Silicon Strip IC Electronics

Milestones*	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	30-Apr-99	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Done
*Submit 2nd ABCD	27-Jan-99	15-Apr-99	Delayed
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	Done
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	16-Jun-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	15-Sep-99	Delayed
*Test systems complete	26-Apr-99	31-Jul-99	Delayed
*1st ICs avail. For 2nd proto hybrid	18-May-99	30-Sep-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	31-Aug-99	Delayed

*As of March monthly report

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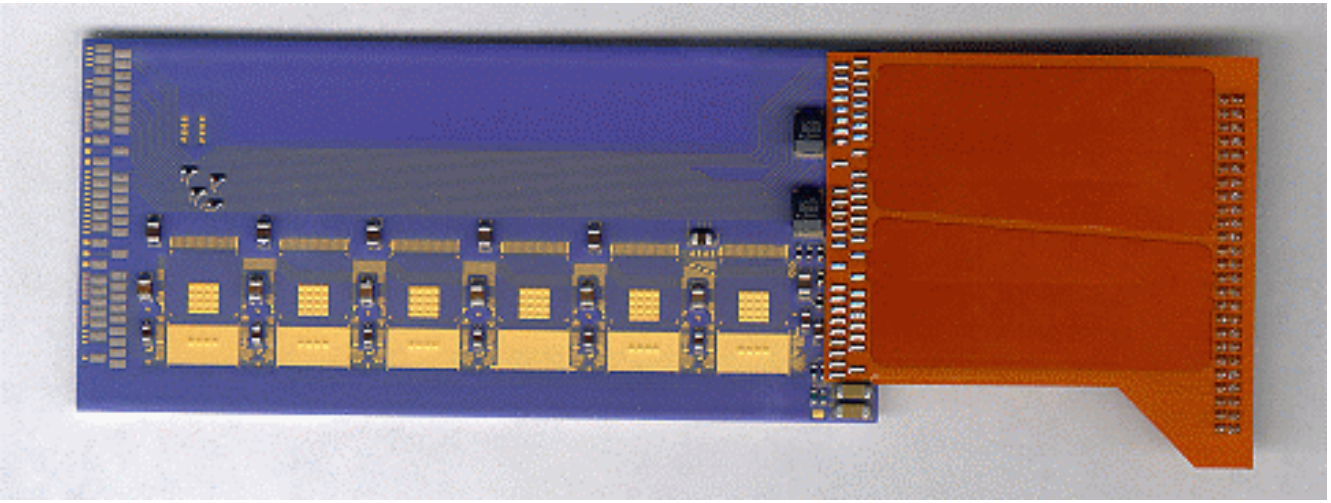
WBS 1.1.2.2 Silicon Strip Hybrids

- Prototype beryllia hybrids designed, fabricated and tested.
- Issues: yield from vendor was less than hoped and some bowing was observed.
- Cost of lower yield was absorbed by vendor allowing us to make another prototype run in future(for 2nd prototype ICs) with existing funds to resolve these issues.
- In meantime, additional vendors identified and at least one appears to be substantially lower in price. Will try this one also for 2nd prototypes.
- Schedule is tied to IC electronics schedule. Essential for IC testing.



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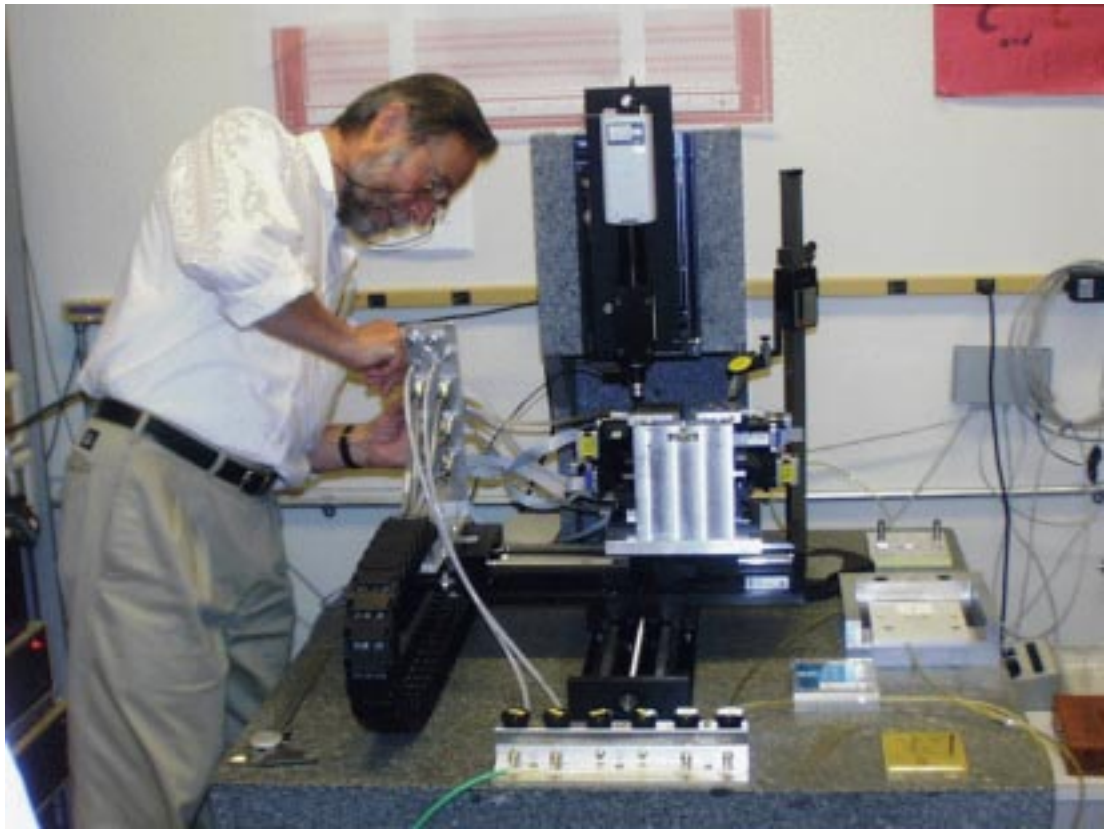
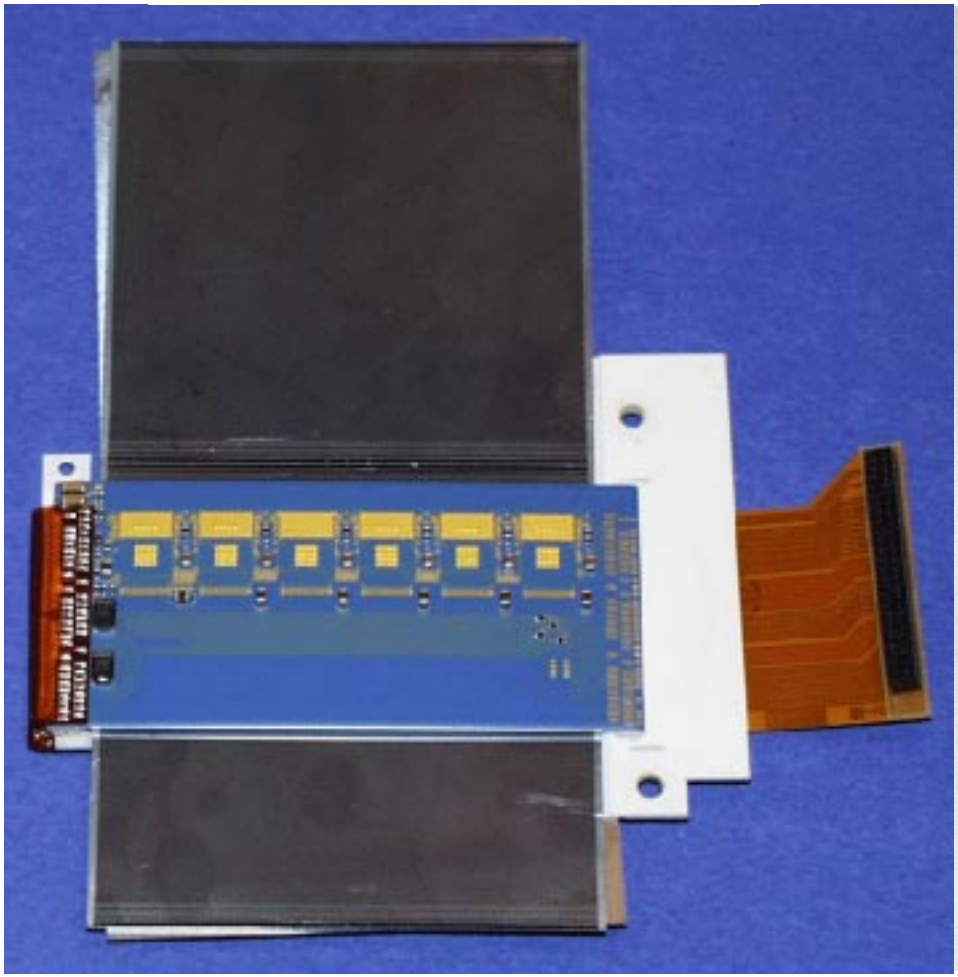
WBS 1.1.2.3 Silicon Strip Modules

- Tooling and equipment for module assembly is largely in place at LBNL, although some aspects(primarily related to measurements after assembly) will appear only later in FY99.
- Dummy parts ready and have started dummy module fabrication to debug system. First dummy modules fabricated.
- Work is slowly underway for “clean room” facilities at LBL.
- The module effort is under budget and there is considerable slack in the early part of the schedule, given delay in the IC electronics.
- But given delays in IC electronics and to try to hold to end date for installation, module production will have to be accelerated once it begins in late 2000

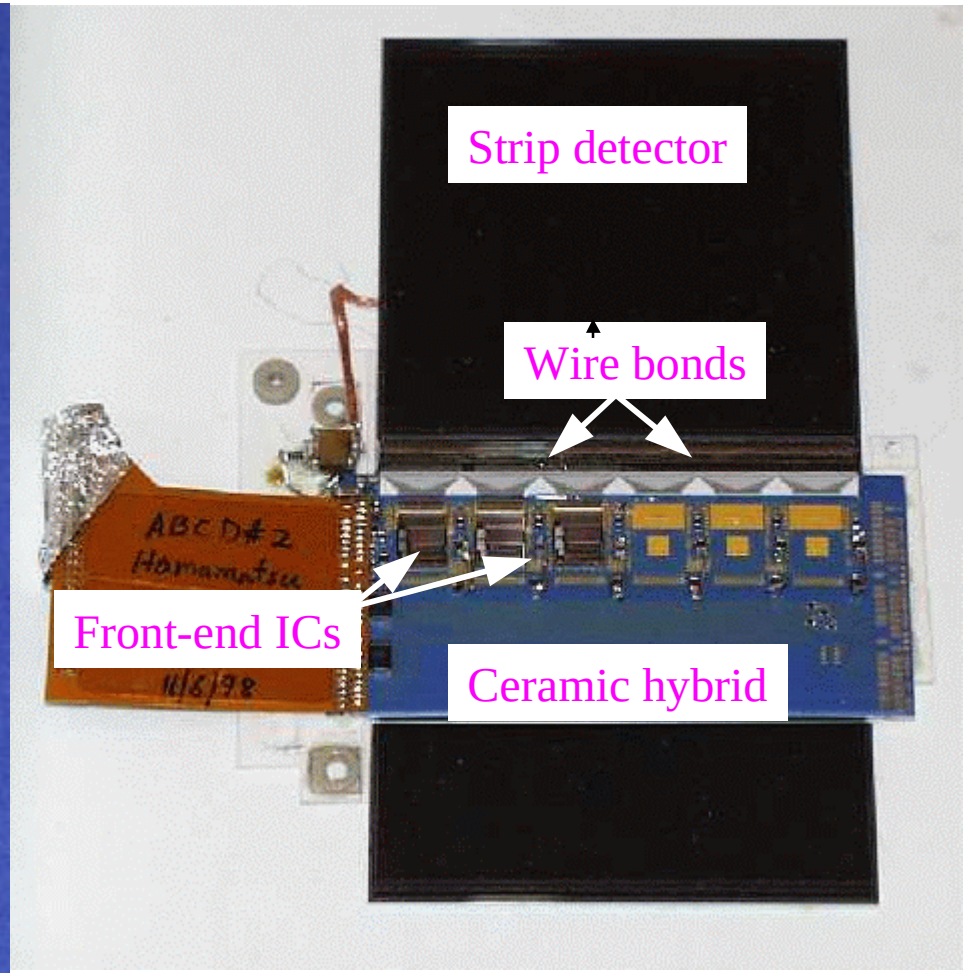


WBS 1.1.2.3 Silicon Strip Modules

Double-sided dummy module



Single-sided active module



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1.1.2 Silicon Strip Schedule Implications

- **Slippage in 2nd prototype round schedule puts at risk milestone for vendor selection**
- **At the moment, believe we can hold other milestones.**
- **Doesn't make sense to revise schedule until 2nd prototypes have been tested.**
- **In any case, I believe module production rate will have to be increased => take into account for cost-to-complete at end of this year.**

	BASELINE	CURRENT
1st ICs for 2nd proto hybrid	18-May-99	31-Aug-99
Select IC vendor	10-Dec-99	TBD
Start IC preproduction run	31-Mar-00	31-Mar-00
1st ICs for preprod. Hybrid	13-Oct-00	13-Oct-00
* Release full electronics production	30-Mar-01	30-Mar-01
* Start full module production	5-Jun-01	5-Jun-01
* Compl ship of prod modules	26-Aug-03	26-Aug-03

* Level 2 milestones

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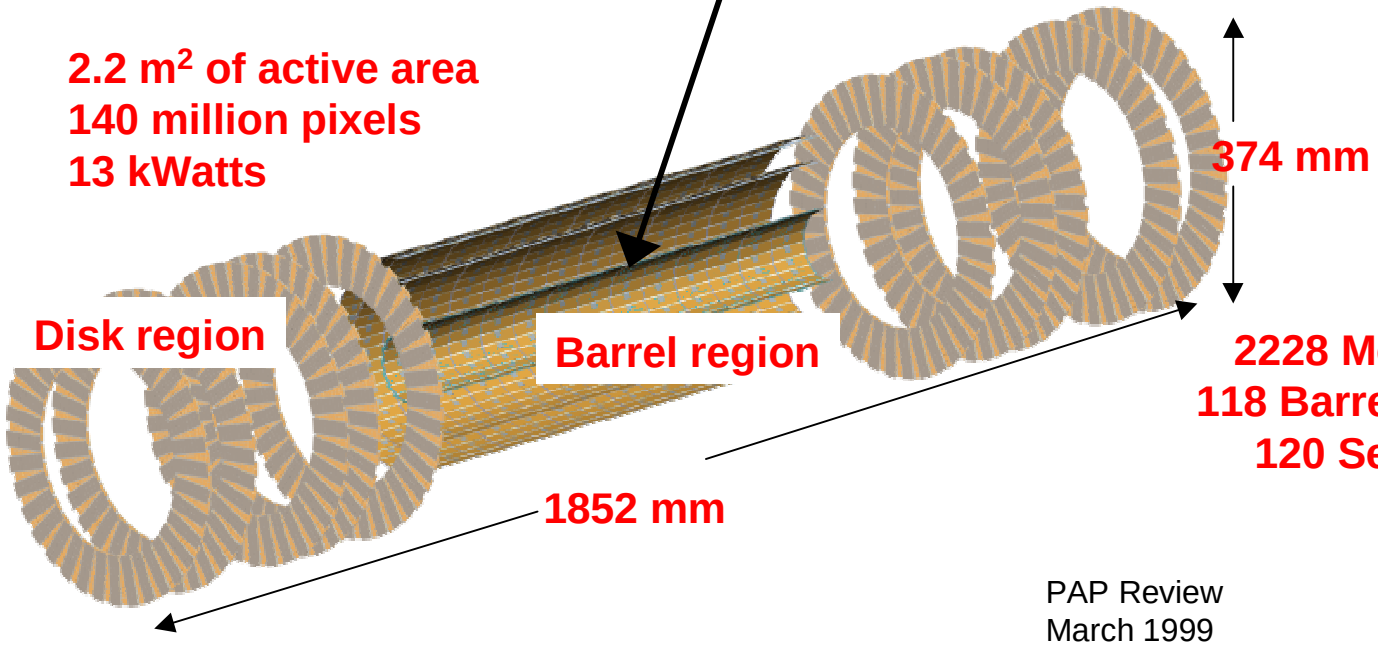
WBS 1.1.1 Pixel System

- **Layout**
  - 3 barrel layers, 2 x 5 disk layers
  - Three space points for $|\eta| < 2.5$
  - Modular construction(2228 modules)
- **Radiation hardness**
  - Lifetime dose - 25 MRad at 10 cm
  - Leakage current in 50μx300μ pixel is - 30 nA after 25 MRad.
  - Signal loss in silicon by factor 4-5 after 25 MRad(or - 10^{15} n/cm^2)
- **Pattern recognition**
  - Space points. Occupany of - 10^{-4}
- **Performance**
  - Critical for b tagging(big physics impact)
  - Need for 3 hits confirmed by simulation
- **Trigger**
  - Space points-> L2 trigger
- **B-Layer**
  - More demanding in almost all aspects
  - Evolving to essentially separate project

2.2 m^2 of active area
140 million pixels
13 kWatts



2228 Modules
118 Barrel Staves
120 Sectors

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WBS 1.1.1 Project Status

- Approved October 1998 for development through about FY2000 with fixed project support of $2582K(FY97) covering FY1996-2000(this includes funds already spent -$830K through FY98)
- Baseline review in summer 2000 leading to construction approval
- Two internal reviews before baseline review
  - March 1999 complete. Review report and response at http://wwwphysics.lbl.gov/~gilg/PixReviewMar99/Pixel_Internal_Review_Response.pdf and included in your books
  - and one again in about December 1999(needs to be folded into overall cost-to-complete exercise. Some strengthening of the technical review aspects also desirable)

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WBS 1.1.1 Technical Status Summary

- **1.1.1.1 Mechanics**
  - Prototype construction and evaluation underway for all aspects of U.S. deliverables to be complete by early 2000
  - Major technical issues and our response
    - Integration/interfaces: have accepted partial(currently lead) responsibility
    - Cooling: increased our calculation and prototype measurement effort but limit final commitment
- **1.1.1.2 Sensors**
  - First round prototypes successful. Intermediate round(1.5) tests just starting. Second round about to go to fab
  - Major technical issues and our response
    - None
- **1.1.1.3 Electronics**
  - Full-scale, rad-soft prototype tests very successful. First rad-hard prototype design nearing completion
  - Major technical issues and our response
    - Complete viability at 25 Mrad: fabricate, irradiate and test by end 1999
- **1.1.1.4 Hybrids**
  - First prototype successful. Next generation design nearing completion.
  - Major technical issues and our response
    - None
- **1.1.1.5 Modules**
  - Prototype modules fabricated, tests. Bump bonding for prototypes under control. Assembly steps understood and to be prototyped over next 18 months.
  - Major technical issues and our response
    - Compatibility of all assembly steps with specs: build >50 modules in next year

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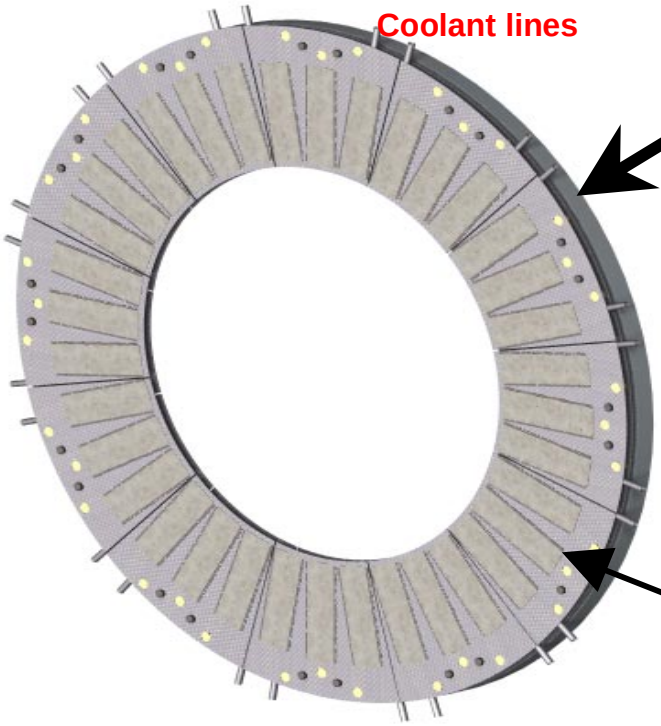
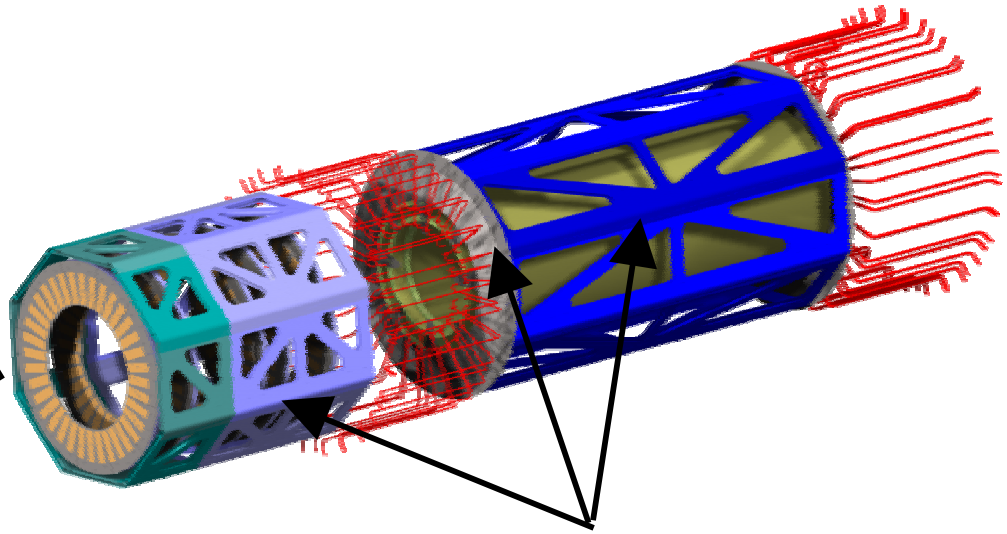
WBS 1.1.1.1 Pixel Mechanics

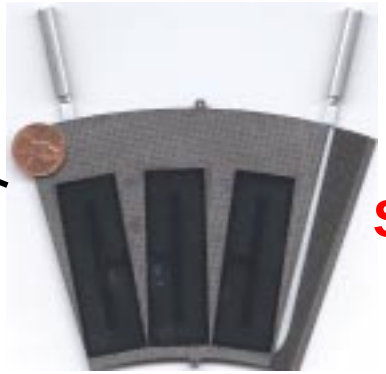
Disk with 12 Sectors



Coolant lines



Support frame



Sector- local support for modules

Sector support, cantilevered from outer edge

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WBS 1.1.1.1 Pixel Mechanics - Status

- **Sectors**
  - About one dozen prototypes tested
  - Baseline is all-carbon design fabricated by ESLI in San Diego
  - However, have developed full in-house backup to mitigate sole source and technical risk. Additional all-carbon backup also being developed via SBIR funding
  - Extensive test program
    - Thermal performance(IR and temperature measurements)
    - Mechanical stability(TV holography and optical CMM)
    - Irradiated full prototype to 22 Mrad. Nearly same performance
  - Optimizing design for final decision in Sept. 99
- **Disks**
  - Prototype design of support ring complete. Bids from fabrication vendors received. Expect ESLI to subcontract using SBIR funds.
  - ESLI is producing >12 sectors to make full disk
  - Full tests using TV holography and at LBNL

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WBS 1.1.1.1 Pixel Mechanics - Status

- **Support structure**
  - **Conceptual design completed by Hytec, Inc for Technical Design Report and was funded by US, Italy and Germany**
  - **Agreement in last few months on splitting prototype design and fabrication between US(overall frame and disk region) and Europe(barrel shells)**
  - **Full-scale prototype of one disk region designed by Hytec, Inc**
  - **Contract with fabrication vendor in place. Materials ordered. Three phase program, ending in complete prototype by end of year.**
- **Integration**
  - **Project engineer from LBNL(partly CERN supported) at CERN for last year.**
  - **Interfaces, power and signal cabling, cooling, installation ….. conceptual framework developed for all integration issues**
  - **3D modeling and multiple physical models(complete end region at LBNL and partial region in UK as part of overall ID) underway.**

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WBS 1.1.1.1 Pixel Mechanics - Issues

- **Integration**
  - Intrinsically difficult(-10 degrees C, very low mass, high stability, no space,….) but has direct impact on design of US deliverables.
  - Design at early stage. Needs much work.
  - LBNL project engineer will be replaced by Italian engineer at CERN starting next month.
  - Strong desire by pixel and ID community for us to continue integration role(reflection of quality of our engineer and need) => have accepted role in services integration and modeling. This will require some additional engineering support at LBNL.
- **Cooling**
  - Cooling is nominally a separate Inner Detector project based at CERN. Substantially under engineered at present.
  - Pixel baseline is evaporative cooling using fluorinert.
  - But common solution with silicon strips desired. Final choice of cooling fluid and operating conditions not made(review at end of May)
  - Choice can have big impact on our design. We have recently increased substantially our measurement work(pressure tests, ..) and calculations to influence decision.
  - No US construction commitment made(or will be made)

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WBS 1.1.1.2 Pixel Sensors

- Prototype 1.0 sensors fabricated(two vendors) and tested very successfully(see test beam results later)
  - Baseline design selected
  - This design has feature that allows testing(by punch-through biasing of the pixels)
  - Test beam results indicated improvement needed in implant design of baseline choice
- This improvement was implemented with minimal mask changes in prototype 1.5 round.
  - These wafers are just now available and irradiation and testing program has started.
  - Test beam starting next month
- Design of prototype 2.0 wafers is complete
  - Will look like production wafers, but explore processing variations, including oxygen-enriched to enhance radiation hardness
  - Fabrication should start in few weeks with at least 2 vendors
- Issue
  - If prototype 2.0 is successful, desire to begin preproduction before US baseline. This is not news(same as at Oct. 98 Lehman review). If this occurs, will submit BCP to add construction funding for this item.

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WBS 1.1.1.3 Pixel Electronics

- Pre-prototype program completed successfully by end 1997.
- Full-scale prototypes fabricated in rad-soft technologies in 1998 and tested extensively. Different design approaches. FE-A, FE-B, FE-C.
- FE-A(AMS -> Temic/DMILL). First delivery in February. Functional. Yield about 5%. Second run delivered in July(all CMOS version FE-C). Yield appears higher, about 80%.
- FE-B(HP -> Honeywell SoI). First delivery in April. Functional. Yield about 93%.
- MCC(AMS -> Temic/Honeywell). First delivery in July. Functional. Yield about 80%.
- Unified design approach adopted for rad-hard design FE chips => all working on same design to be implemented in the two rad-hard processes
- Largely serial effort on rad-hard design(manpower limited). DMILL prototype first(FE-D) aimed at submission next month. Then Honeywell SoI(FE-H) later this year.
- Effort is significantly behind baseline schedule, resulting from optimism in original schedule and need to proceed with largely serial development.

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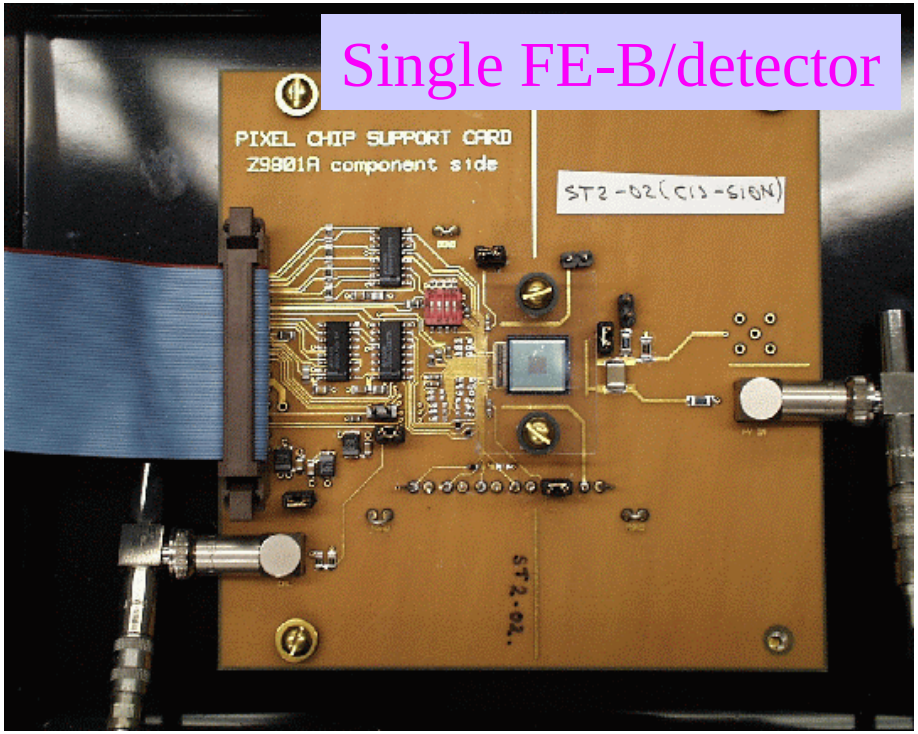
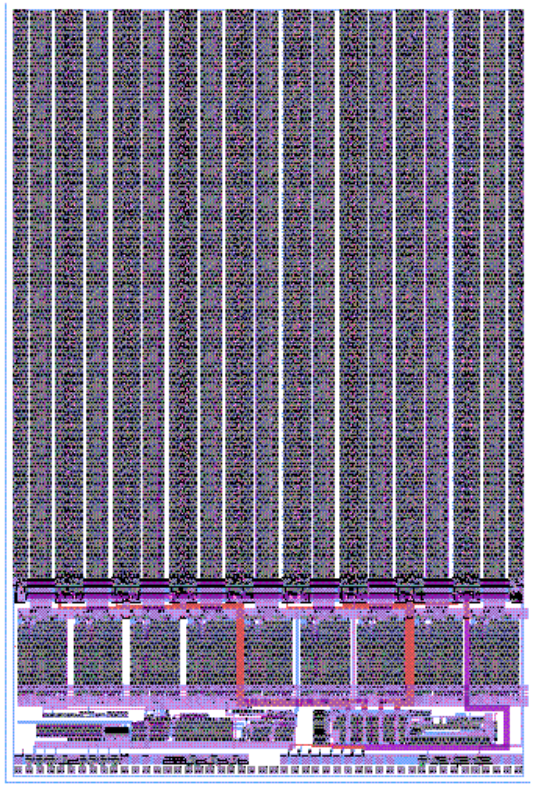
WBS 1.1.1.3 Pixel Electronics

- **FE-A/C and FE-B bonded to prototype detectors, including irradiated detectors.**
  - **18x160 pixels(50x400 micron pixel size). Complete analog and digital to ATLAS specs. Spec is 50x300 micron pixel but 400 vs 300 micron performance comparison underway**
  - **Essential requirements met(efficiency, time resolution, noise, threshold,….)**
  - **Multiple test beam runs at CERN. Extensive lab tests. Principle established.**





FE-B

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Lab and Test Beam Results - Summary

- **Extensive lab tests and three test beam runs in 1998. Very successful.**
- **Highlights**
  - **Dozens of single-chip/detectors have been operated successfully with multiple detector types and front-end ICs**
  - **16 chip modules have been operated successfully**
  - **Detectors irradiated to lifetime fluence expected at LHC(10^{15}) have been read-out in a test beam with efficiency near 100%**
  - **Operation below full depletion voltage demonstrated**
  - **Preferred detector type identified in these studies**
  - **Timing performance needed to identify bunch crossings has been demonstrated, albeit not at full system level.**
  - **Operation at thresholds 2,000-3,000 electrons demonstrated**
  - **Threshold uniformity demonstrated.**
  - **Spatial resolution as expected**
- **Conclusion**
  - **Proof-of-principle of pixel concept successful**

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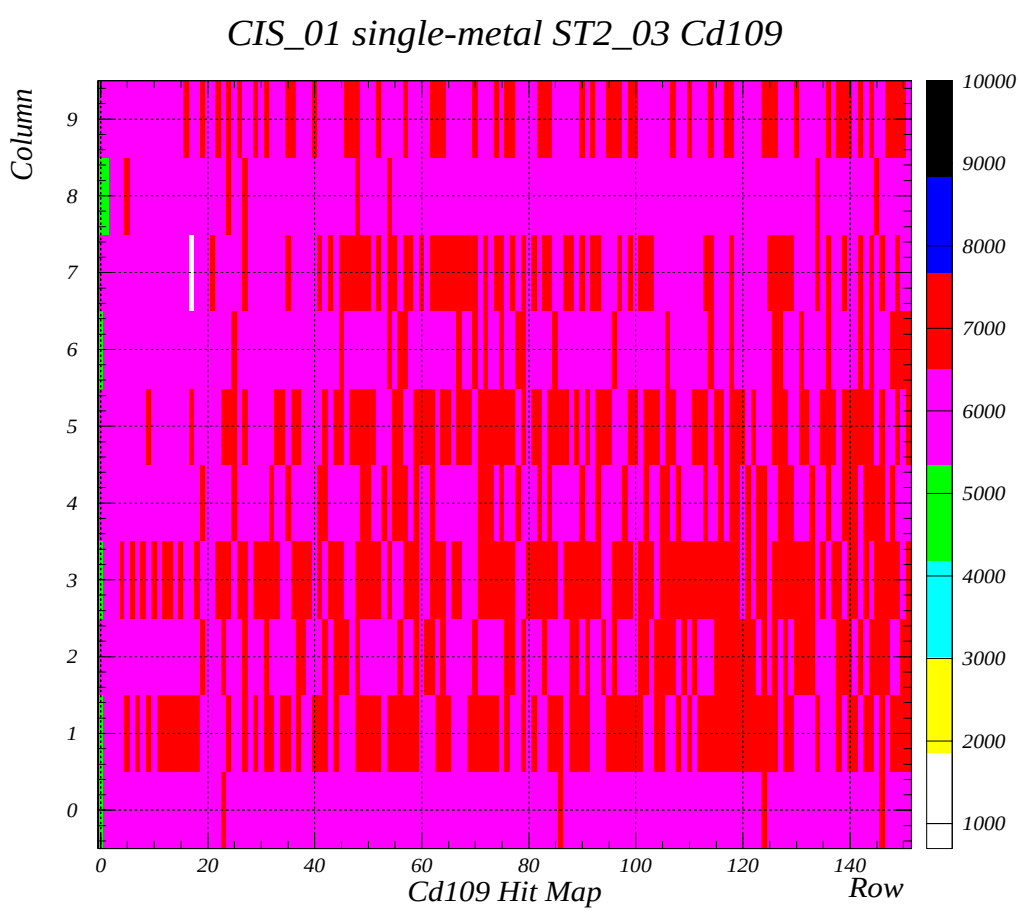
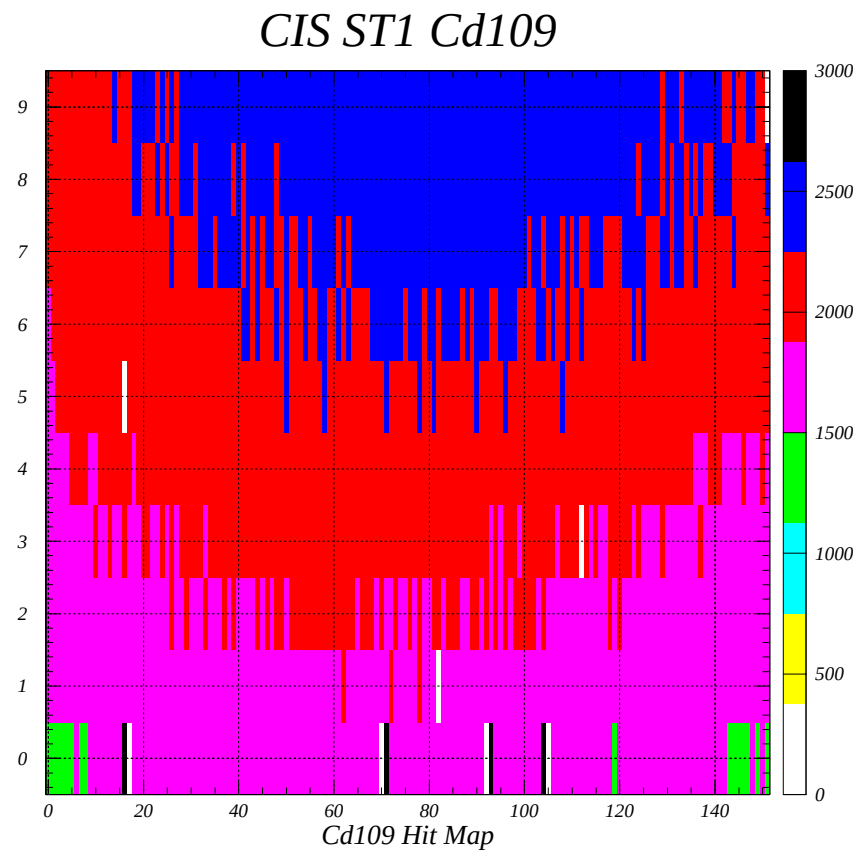
Photon Source Test of FE-B and Detectors





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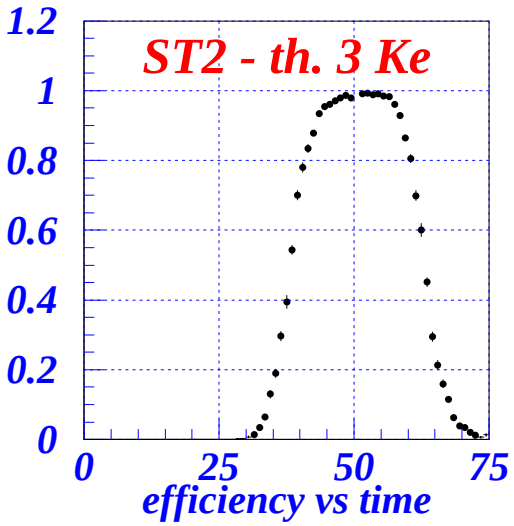
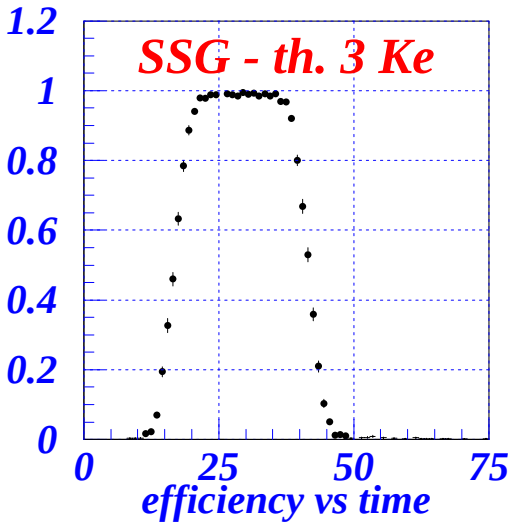
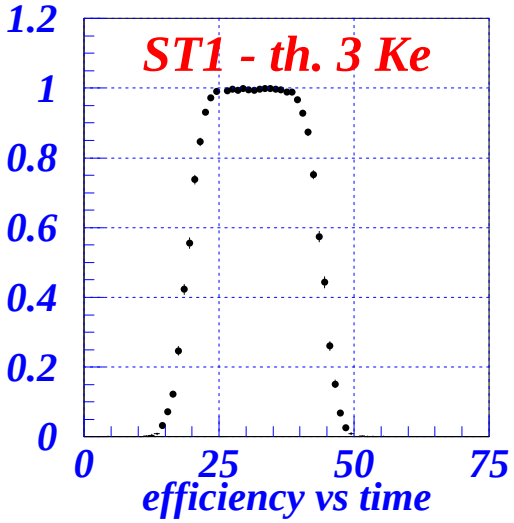
Lab and Test Beam Results - Examples







Efficiency vs time of particle passage for three different detector types before irradiation. The efficiency is near 100% in each case and there is a substantial plateau, indicating good timing performance of the electronics

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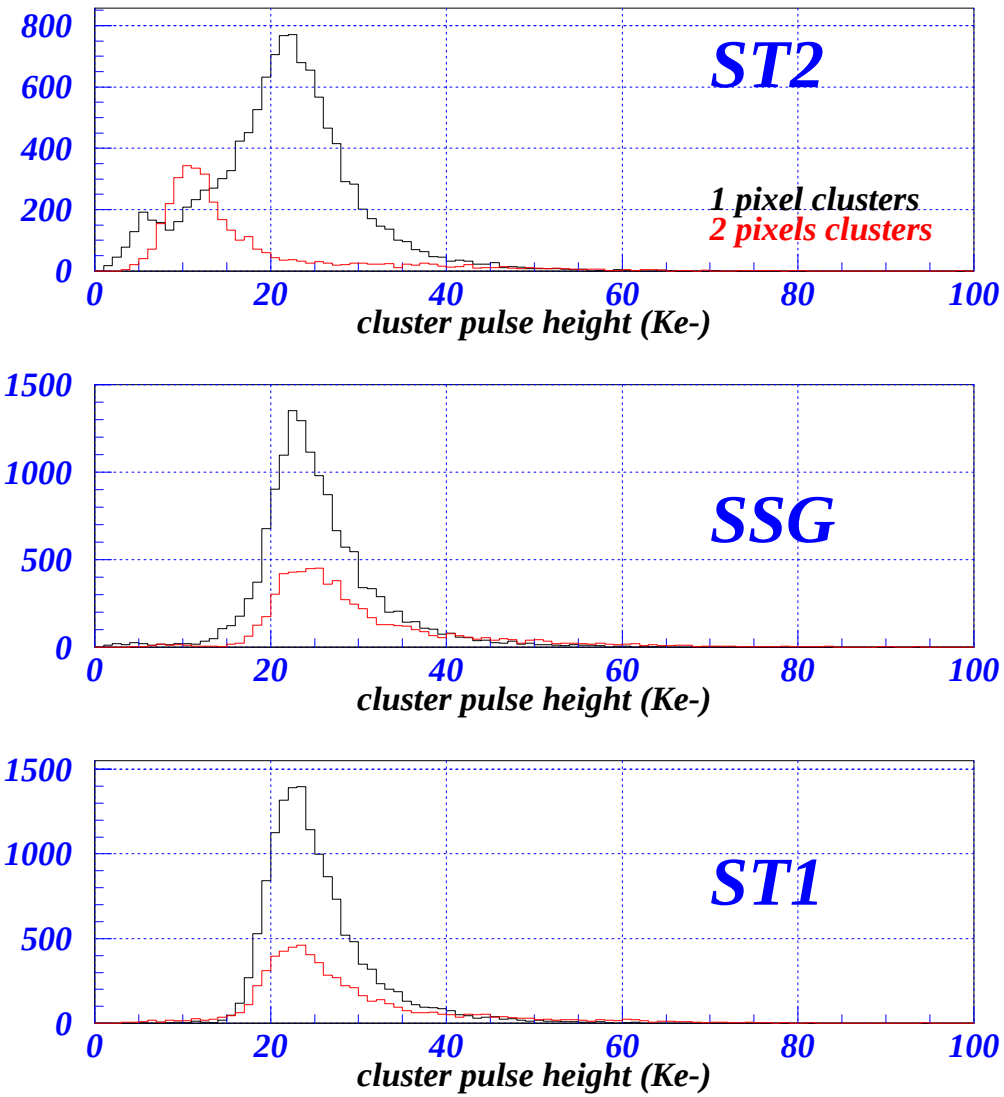
Lab and Test Beam Results - Examples



Charge distributions for three detector types. The difference between ST2 and the others is indicative of small charge losses, which has guided us in the design of additional prototype detectors under fabrication.

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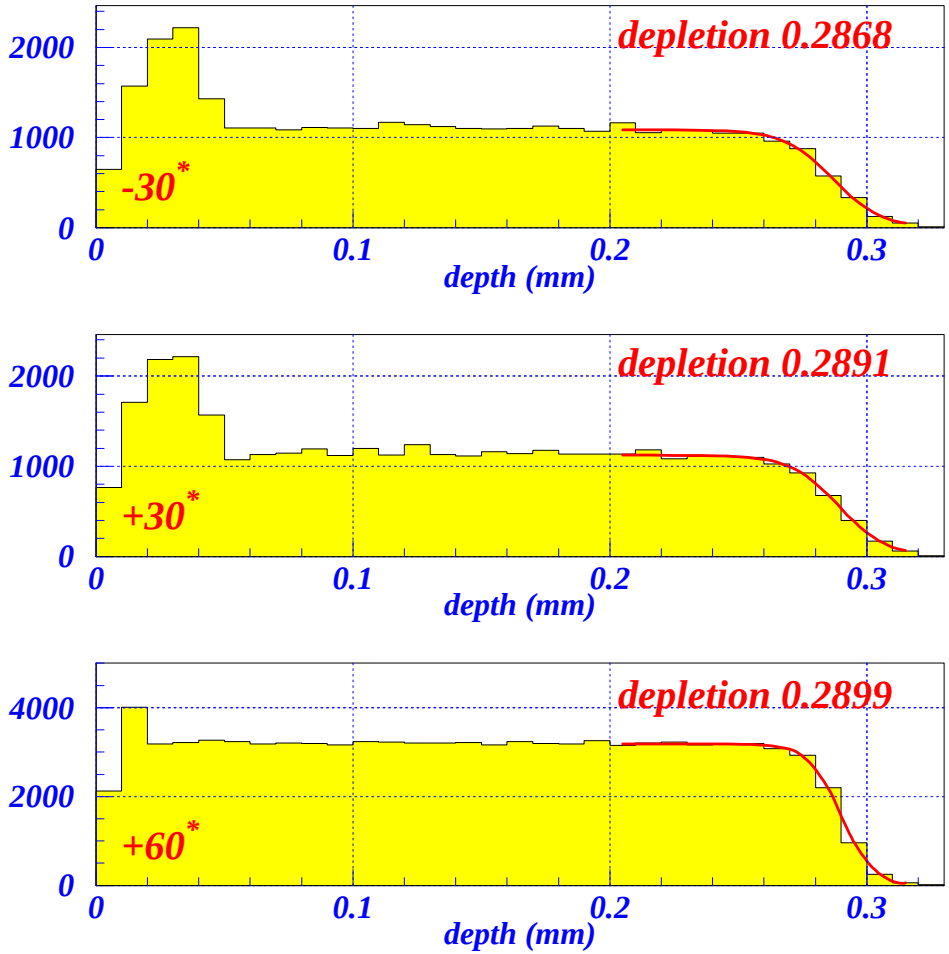
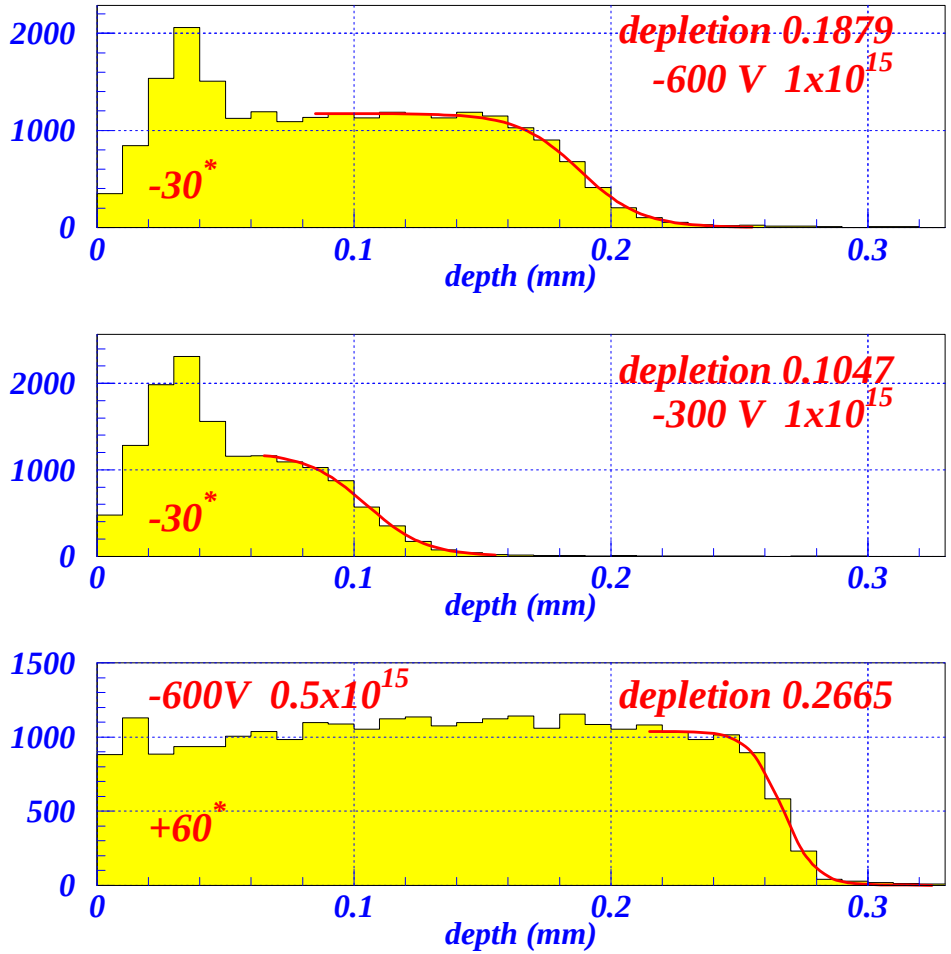
Lab and Test Beam Results - Examples

Not irradiated - depletion depth



Irradiated - depletion depth



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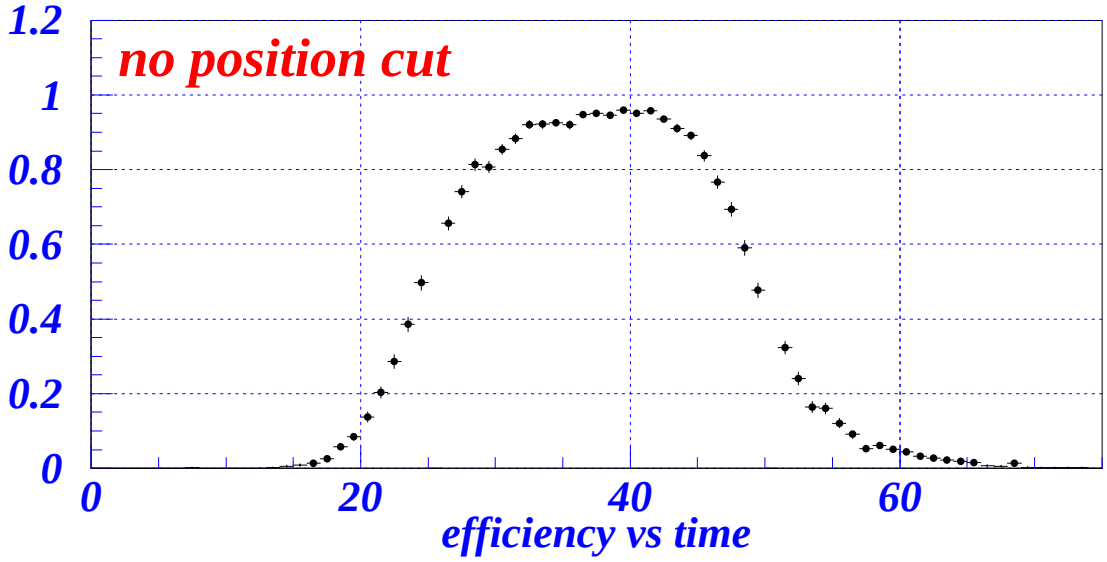
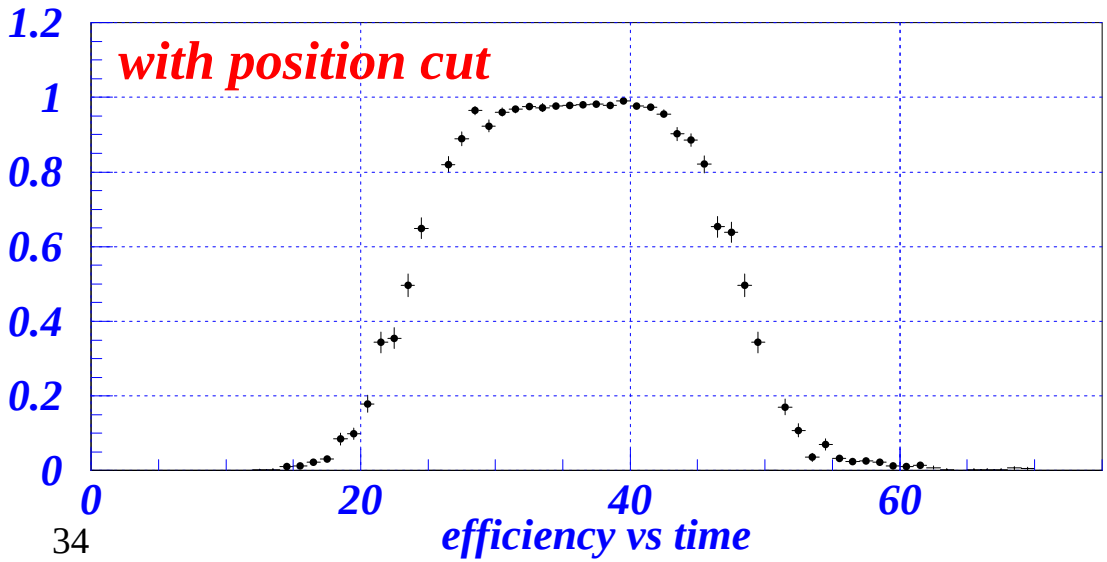
Lab and Test Beam Results - Examples



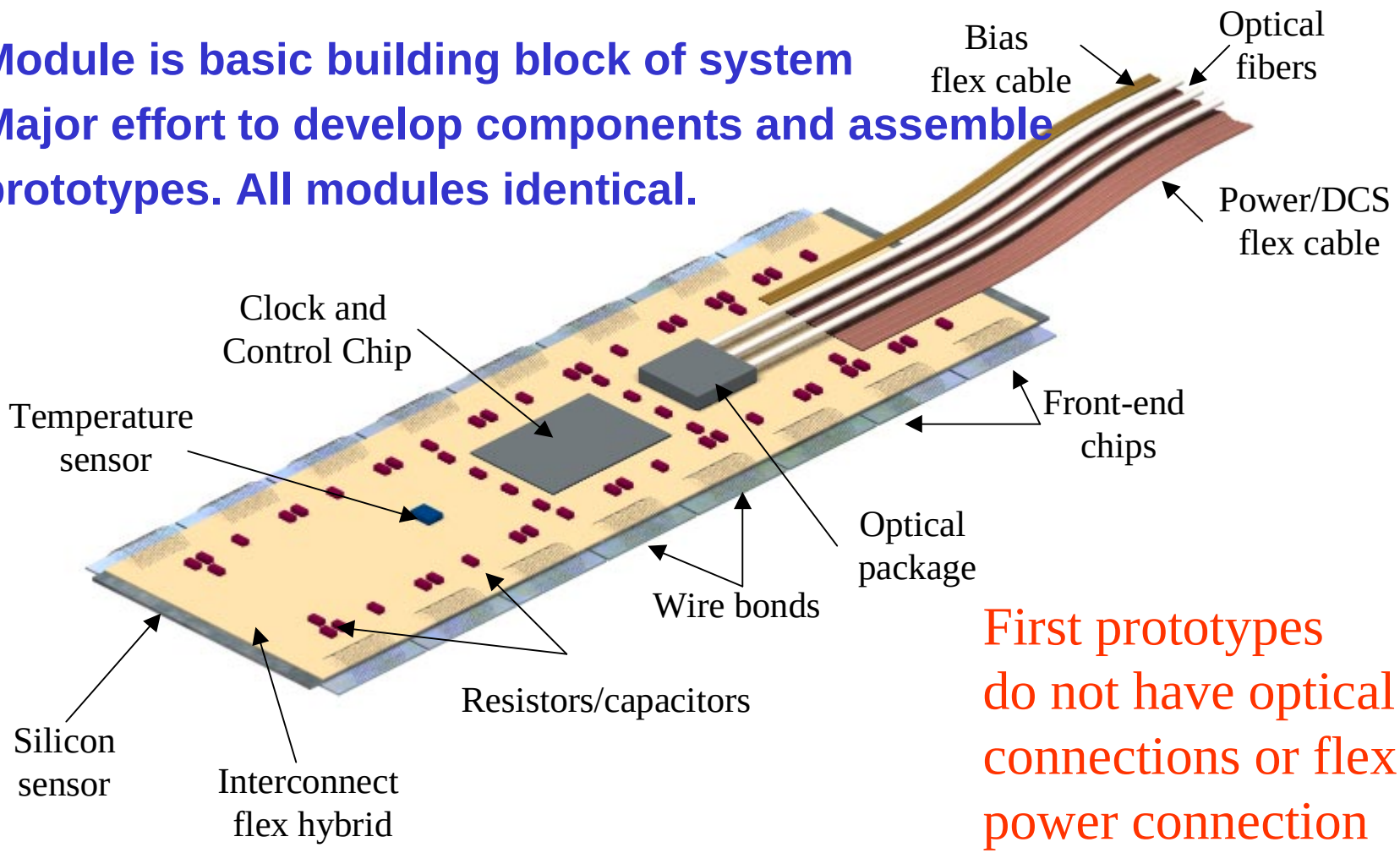


Efficiency after irradiation of $1x10^{15}$ without and with a position cut to remove tracks near the edge of the pixel.

Pixel Module

Module is basic building block of system

Major effort to develop components and assemble prototypes. All modules identical.



First prototypes do not have optical connections or flex power connection

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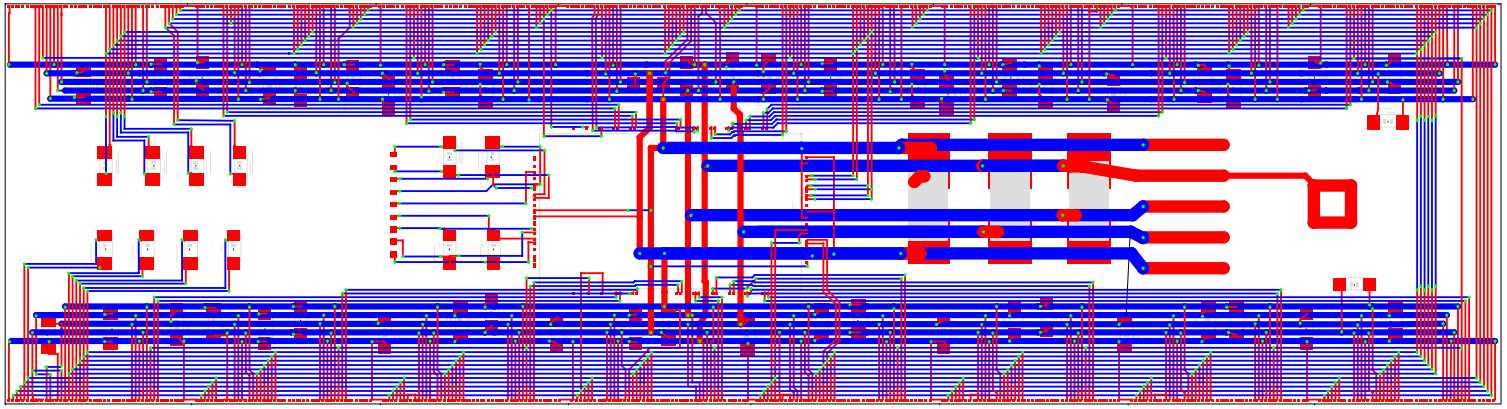
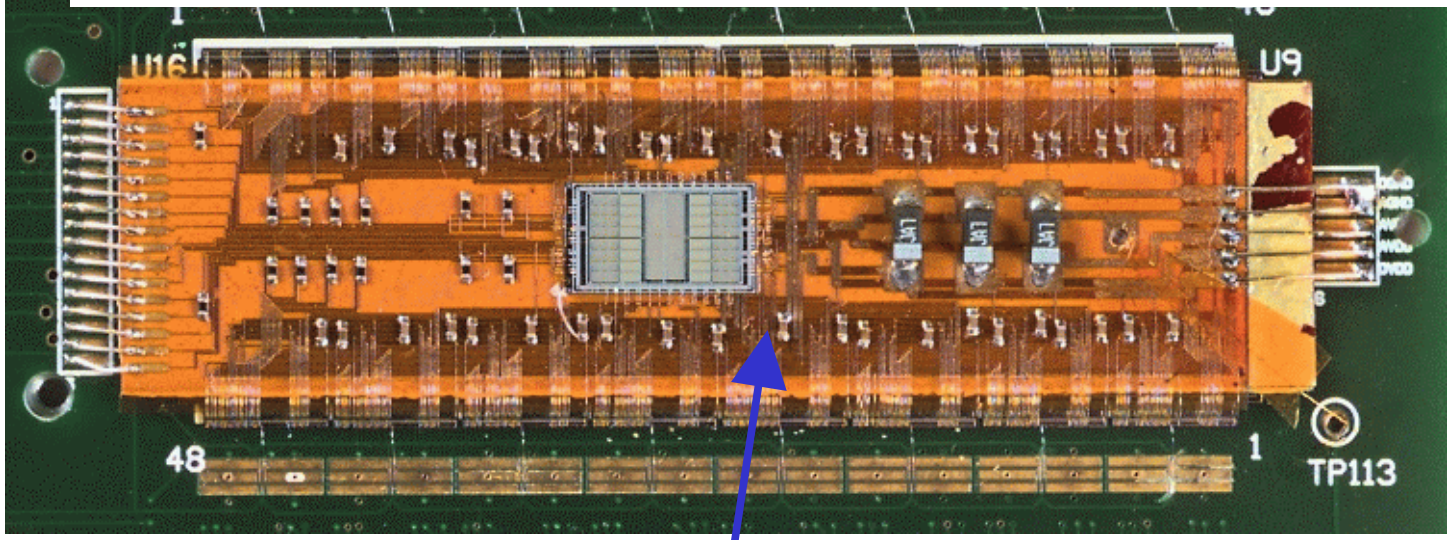
WBS 1.1.1.4 Pixel Hybrids

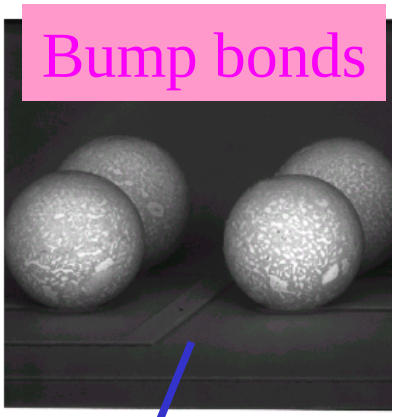
- Flex hybrid interconnect technology selected February 1999 as baseline for disks and two outer barrel layers. B-layer alternative technology(MCM-D) if it proves to be feasible, otherwise flex hybrid.
- Prototype flex hybrid(v1.0) design and fabricated at CERN succesfully
- Few modules built and tested.
- Design of revised and improved version(1.x) complete except for vendor specific items. Fabrication planned with at least two vendors in next few months.
- Issues
  - Production yield and impact on module assembly => build many more

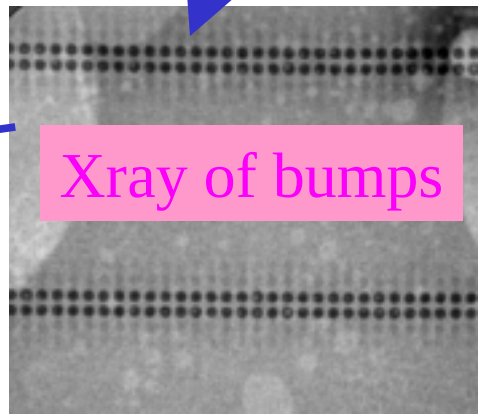


WBS 1.1.1.5 Pixel Modules

Module with flex hybrid and controller chip on PC board







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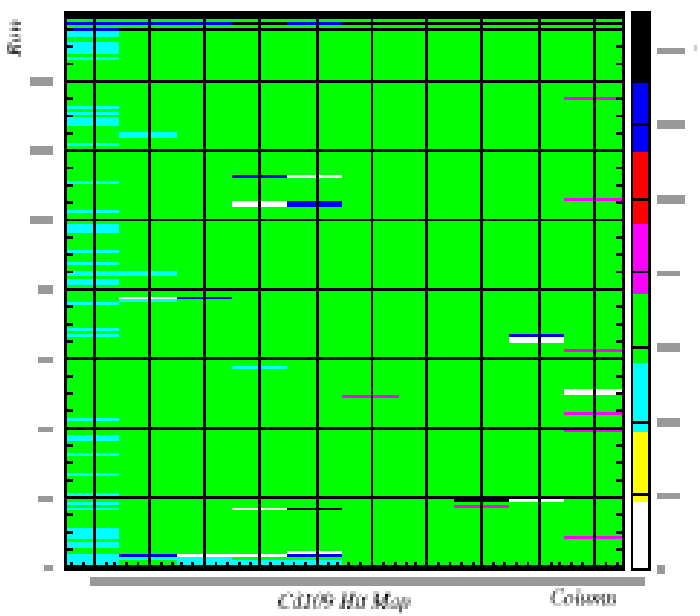
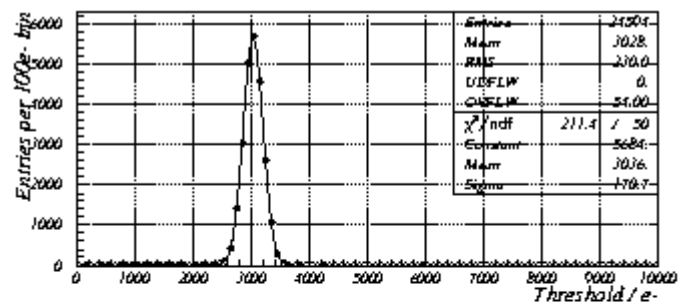
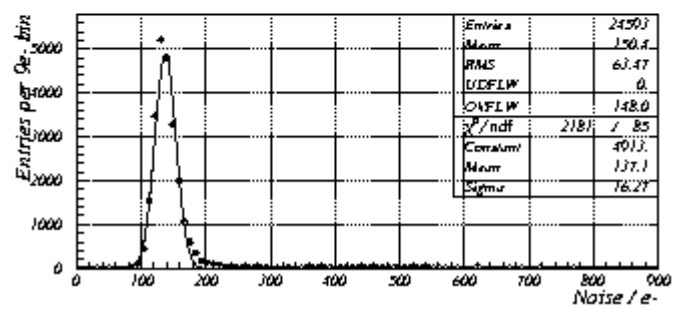
WBS 1.1.1.5 Pixel Modules

- Bump bonding under control for prototypes but much more work needed on production issues.
- A handful of modules(including bare modules) built and tested
- So far has been largely test bed for electronics and concept(can you operate 16 chips on a sensor? Yes)
- Issue - production aspects => contracts in place to build 100 module over next year.







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WBS 1.1.1 Pixel Schedule

- **Baseline schedules are on the following pages**
- **Although there are minor delays in the non-electronics elements, the critical delay is in the completion of the design of the rad-hard ICs.**
- **Currently projecting selection of rad-hard vendor after baseline date for construction review**

Milestones	Baseline	Current	Status
Compl. Design HSOI test die	16-Apr-98	1-Nov-98	Completed
Compl. Fab HSOI test die	26-Aug-98	31-Mar-99	Delayed
Compl. Design DMILL test device	15-Dec-98	15-Dec-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known
1st design review of DMILL proto	25-Jan-99	23-Feb-99	Completed
*FDR DMILL 1st prototype	25-Jan-99	TBD	TBD
*Compl. Design DMILL 1st proto.	26-Feb-99	1-May-99	Delayed
Compl. Fab DMILL test device	30-Apr-99	30-Apr-99	On schedule
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule
Compl. Eval. DMILL test device	1-Jul-99	1-Jul-99	On schedule
Compl. Eval. HSOI test die	1-Jul-99	1-Jul-99	On schedule
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Oct-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	7-Sep-99	Delayed
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	15-Feb-00	Delayed
*Compl eval. DMILL prototype	9-Dec-99	1-Jun-00	Delayed
*Compl eval HSOI prototype	15-Feb-00	1-Jun-00	Delayed
*Review design approach	19-Jan-00	15-Jun-00	Delayed
*Select rad-hard vendor	29-Jan-00	15-Jul-00	Delayed

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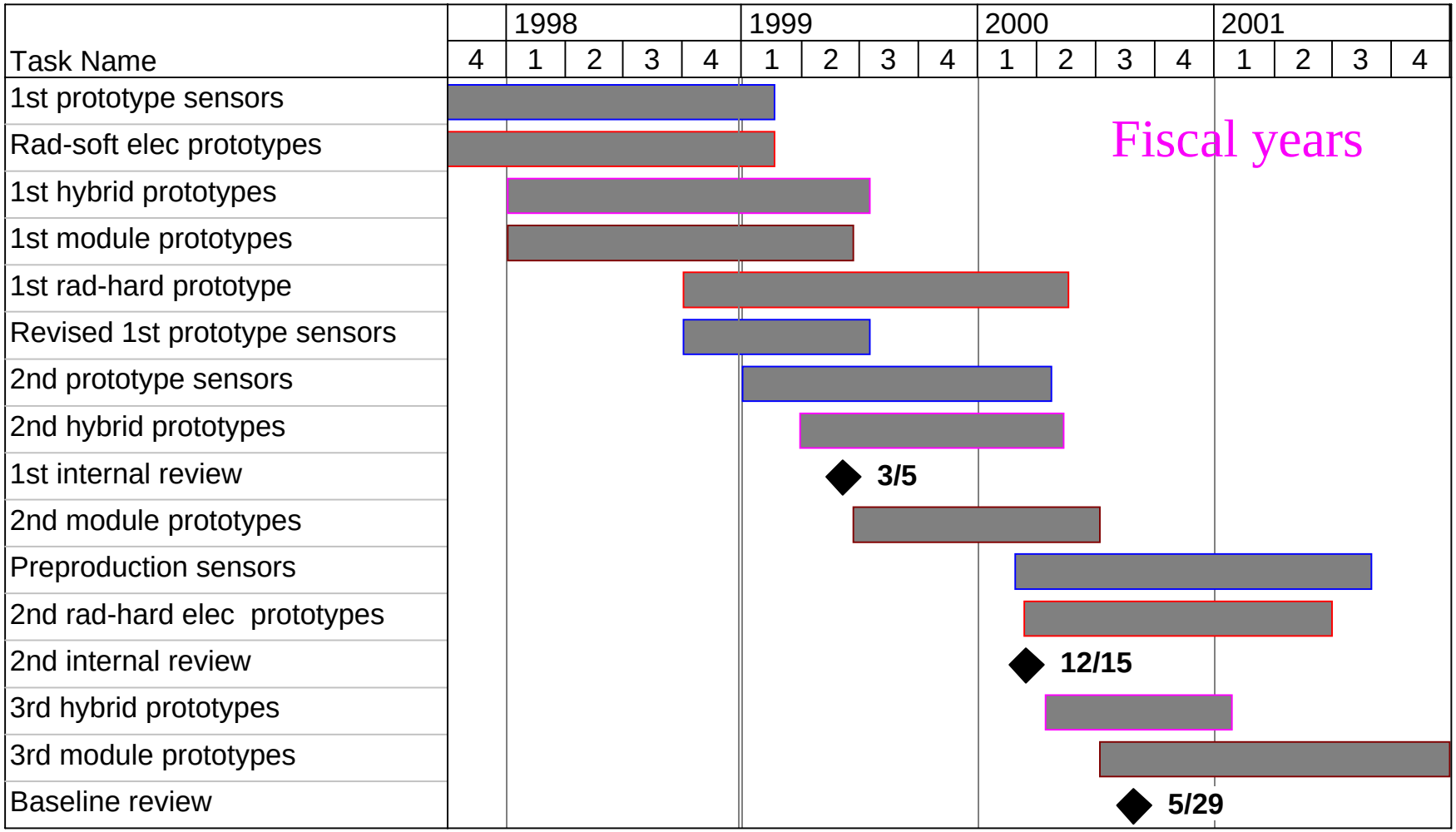
Baseline Non-Mechanics Schedule



Does not include mechanics

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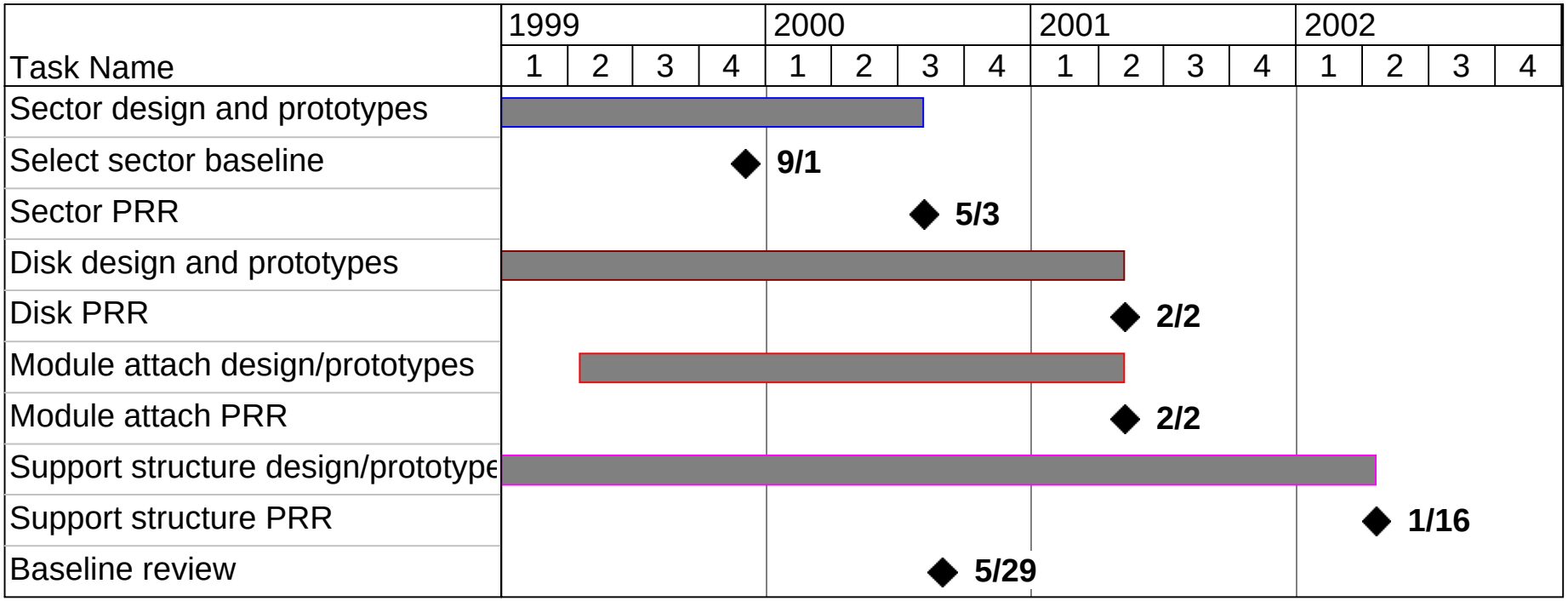
Baseline Mechanics Schedule



PRR = Production Readiness Review

Dates beyond baseline review are preliminary

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Pixel Issues

- **IC schedule**
  - **Try to improve Honeywell schedule(adding manpower from Santa Cruz)**
  - **Major problem is lack of State Dept. approval of Technical Assistance Agreements with Bonn and Marseille**
  - **Will consider selecting FE-D=DMILL(if it meets specs) without full FE-H data if required to meet schedule(except for B-layer)**
- **Baseline vs cost-to-complete**
  - **ATLAS cost-to-complete schedule precedes construction baseline review.**
  - **Pixel construction costs likely to rise(not just US problem)**
  - **Staging doesn't make sense(open heart surgery required)**
  - **B-layer is evolving into separate, and later, effort to meet technical need(higher occupancies, higher radiation,….) but is critical (as is the rest of the pixel system) for first physics operation.**
  - **Our proposal is to provide a preliminary pixel cost estimate as part of the cost-to-complete exercise - do the best job we can - and then work with ATLAS and U.S. ATLAS to define US deliverables for baseline review such that the overall project is completed.**

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Institutional Responsibilities

	ALB	LBL	UCI	UCSC	UNM	UOK	UW	OSU
1.1.1 Pixels								
1.1.1.1 Mechanics		x						
1.1.1.2 Sensors	x				x	x		
1.1.1.3 Electronics		x						x
1.1.1.4 Hybrids	x					x		
1.1.1.5 Modules	x	x		x		x		x
1.1.1.6 Common	x	x	x	x	x	x	x	x
1.1.2 Silicon Strips								
1.1.2.1 IC Electronics		x		x				
1.1.2.2 Hybrids		x		x				
1.1.2.3 Modules		x		x				
1.1.3 RODs			x				x	

OSU added - otherwise same

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WBS 1.1 Summary

- **1.1.1 Pixels**
  - **Excellent technical progress - no showstoppers yet!**
  - **Approved pre-baseline funding adequate for development through FY00 but may require some advanced construction funds**
  - **Critical issues identified and responding, but electronics schedule is major concern.**
- **1.1.2 Silicon Strips**
  - **2nd generation IC prototypes in fabrication or nearly in fabrication**
  - **Overall schedule is getting even tighter. Plan for update by end of year after 2nd IC prototypes tested.**
- **1.1.3 Read-Out Drivers(ROD)**
  - **Lab and test beam support has gone well**
  - **Selection of ROD design approach made recently but behind schedule.**