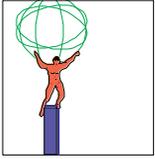


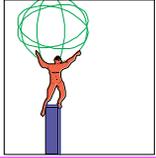
U.S. ATLAS



WBS 1.1 Silicon Subsystem

M. G. D. Gilchriese
(LBNL)

PAP Review
January 2000



WBS 1.1 Institutions

SUNY Albany

Iowa State University(new since last review)

UC Berkeley/LBNL

University of New Mexico

Ohio State University

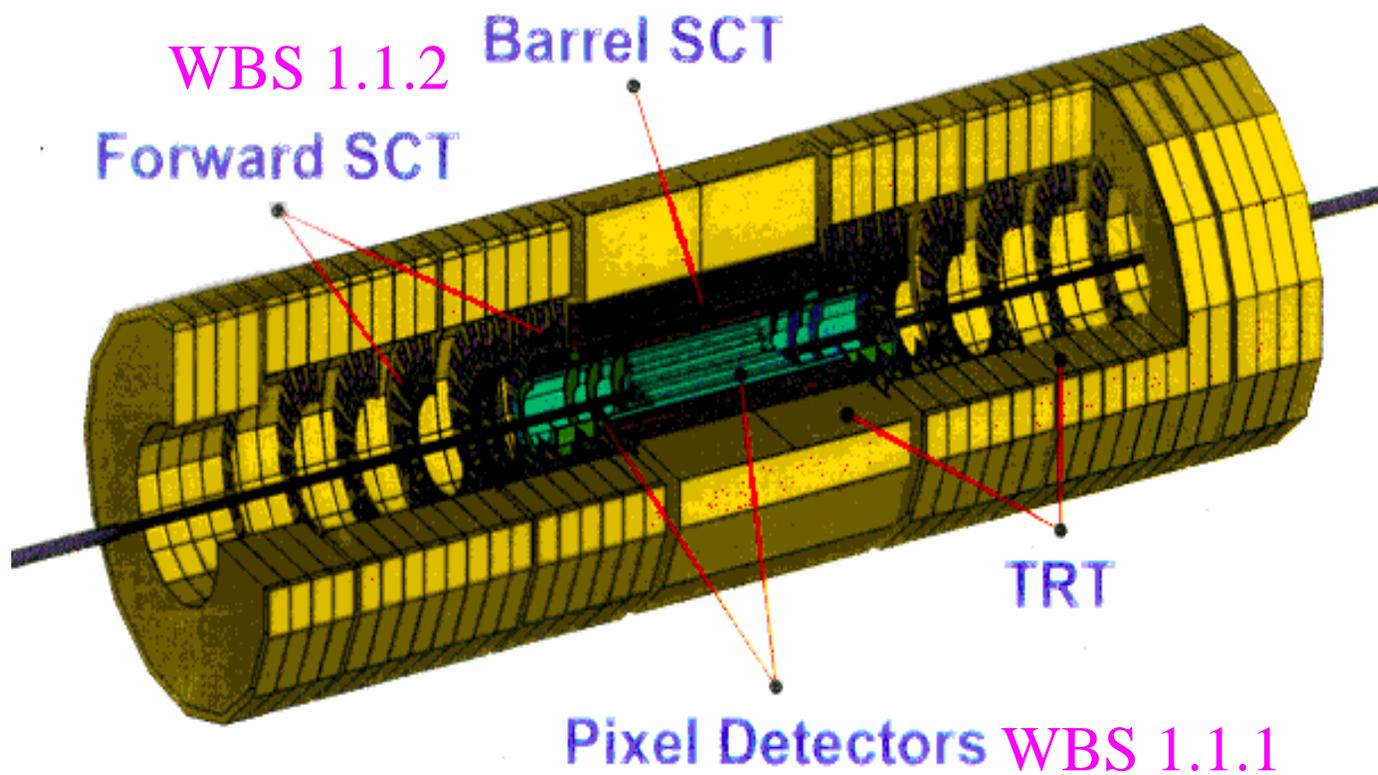
University of Oklahoma/Langston Univ.

UC Santa Cruz

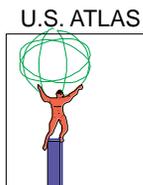
University of Wisconsin



Silicon Subsystem

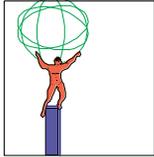


ReadOut Drivers - WBS 1.1.3

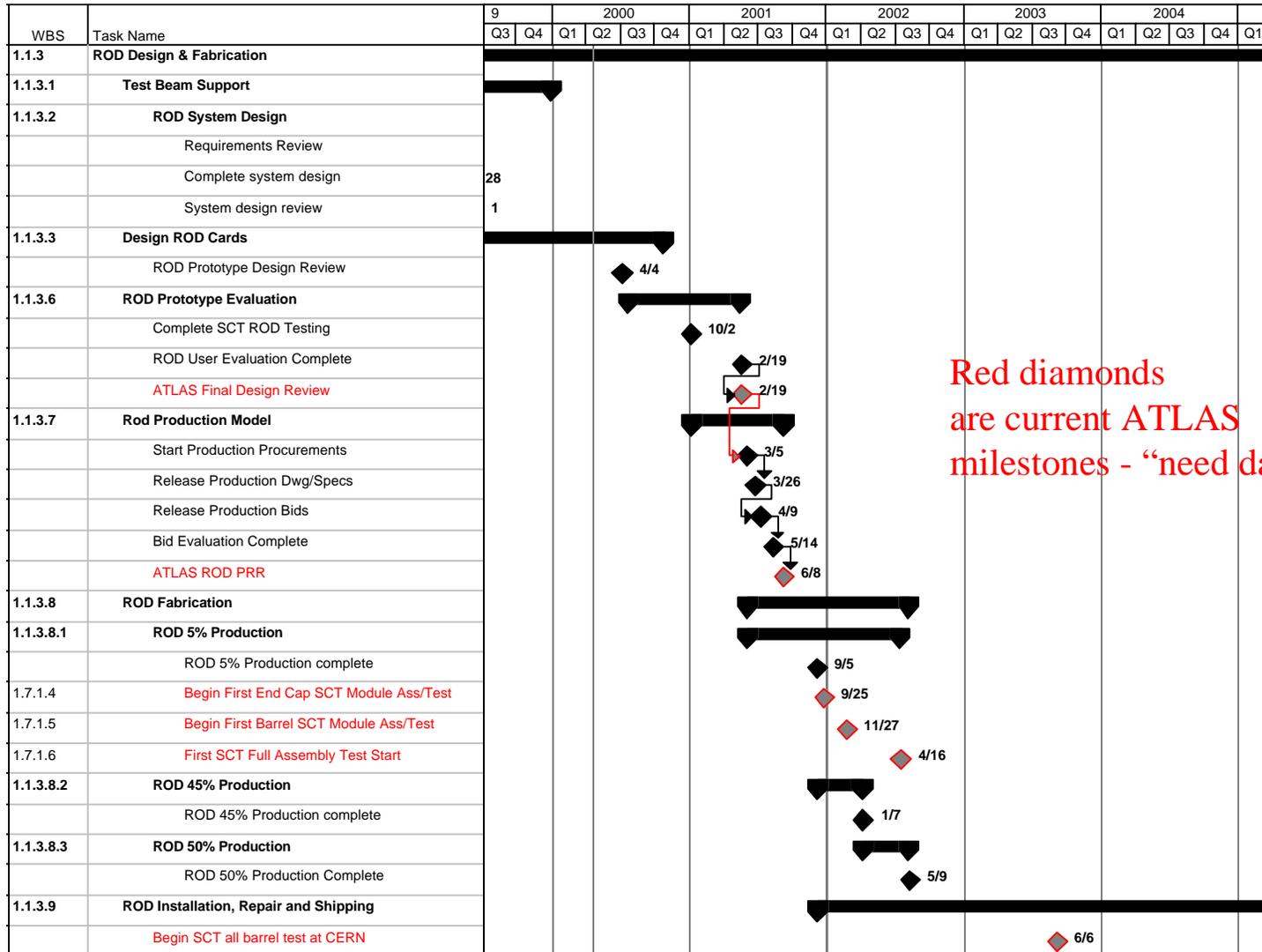


WBS 1.1.3 Read-Out Drivers

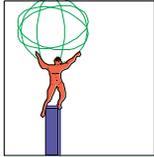
- **RODs: off-detector VME boards that receive/transmit signals from/to all pixel and SCT modules.**
- **Baseline plan: preprototype->prototype->production model->production**
 - ◆ **Design team unable to converge on common technical solution for preprototype**
 - ◆ **Review held end-March 99 to make selection**
 - ◆ **Design team changed. Irvine left. Iowa State joined. Lost time.**
- **Current plan: prototype -> production model ->production(in stages) - see milestones next page. Increased scope of prototype.**
- **Design review of status of prototype held on Dec. 17 and report included at end of this presentation. Design advancing well, follow up review scheduled just before submission for fabrication.**
- **Scope**
 - ◆ **The number of RODs needed for pixels and SCT is now much better understood compared to baseline estimate, and has gone down substantially, but obviously needs to be validated by measurements of prototype.**
 - ◆ **SCT RODs were US(75%)-UK(25%) deliverables. Pixel RODs were 100% US. Compared to baseline design assumptions from 1997, design has changed to (a) eliminate ASICs from UK and (b) shift all responsibility for optical receivers/drivers (Back-of-Crate Card) and Timing Interface Module to UK. Interface with US deliverable now much cleaner.**
 - ◆ **ETC now includes fabrication of 100% of both pixel and SCT RODs.**



WBS 1.1.3 Current Milestones



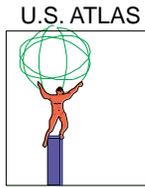
Red diamonds are current ATLAS milestones - "need dates"



WBS 1.1.3 ETC

- WBS structure simplified.
- Completely revised estimates for labor and fabrication made for ETC.
- Fabrication costs detailed by type of ROD. Although all have same basic design, pixels are different than SCT, differences within pixels(B-layer vs outer layers), etc
- Actuals + ETC nearly same as projected FY97 estimate.
- Comparison shown below includes contingencies but same if comparing base costs.

		FY97 Estimate(no BCPs)							
		FY97	FY97	FY97	FY00		FY00	Actuals	
		Base	Cont	Total	Total	AY	ETC	+	
		Cost	Cost	Cost	Cost	Actuals	Total	FY00 ETC	Difference
WBS 1.1.3		3001	695	3696	3926	540	3350	3890	-36



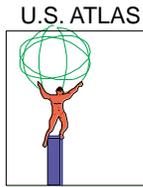
WBS 1.1.3 Risks and Issues

- **Risks**

- ◆ Continuity of design team -> go as fast as possible
- ◆ Interfaces not under US control changed -> working hard to avoid this. Have good communication with UK and pixel/SCT electronics coordinators.
- ◆ Intrinsic board complexity(SCT has 96 links) -> build prototype and see.

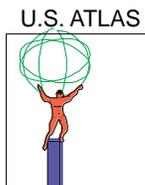
- **Issues**

- ◆ Relative role of US and UK in production testing of SCT RODs still to be sorted out. Similar issue will come along for pixels.
- ◆ Long lead-time procurement of critical parts -> after FDR and before PRR according to current schedule.
- ◆ Life-time buy of critical parts and spares not part of baseline. General ATLAS problem but exacerbated here by critical dependence on parts that rapidly will become obsolete.



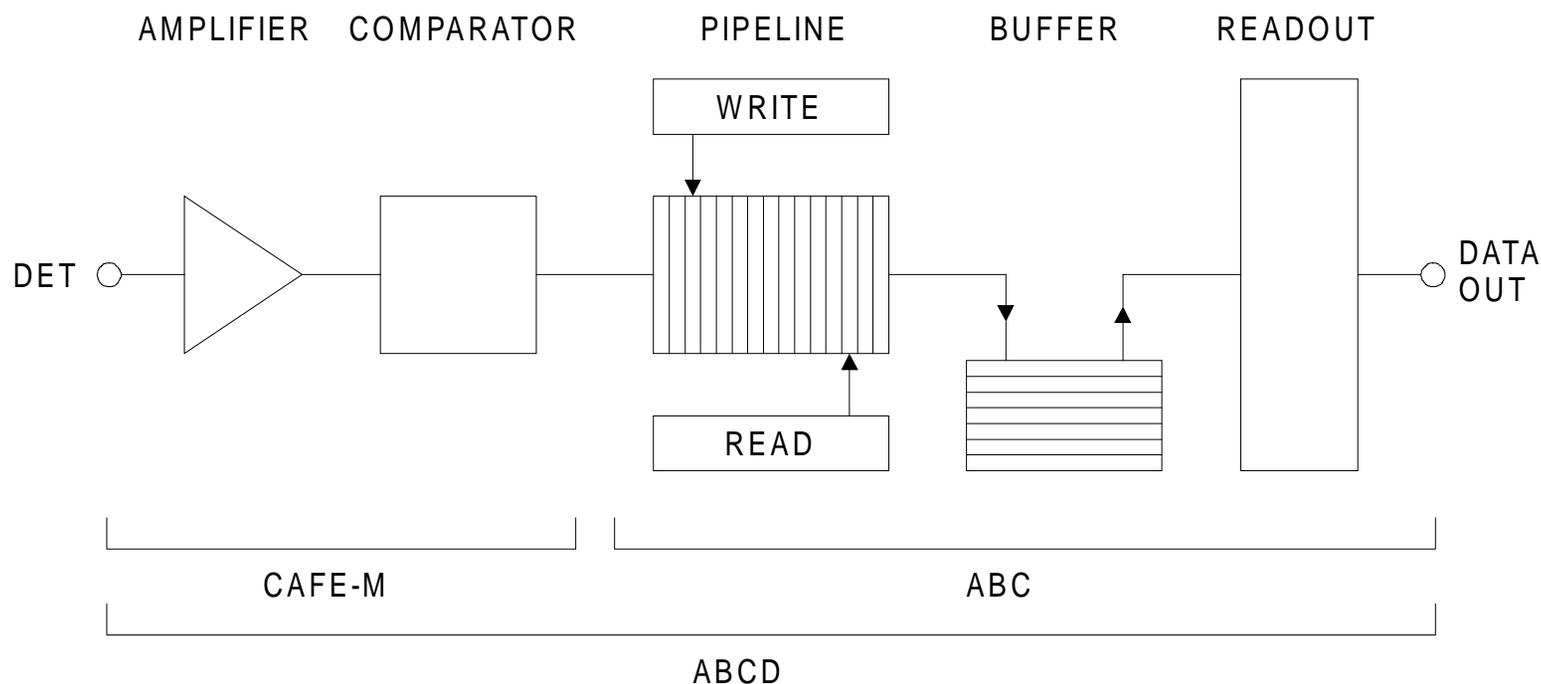
WBS 1.1.2 Silicon Strip System

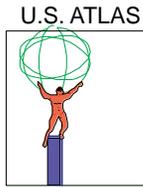
- **Scope**
 - ◆ No changes
- **Schedule**
 - ◆ US schedule and ATLAS schedule now in reasonable agreement(see comparison later). Both schedules were modified to reach consistency.
- **ETC**
 - ◆ Revised estimates of major materials (IC, hybrids, ...) complete but based on same model as in FY97(CAFÉ/ABC electronics and BeO hybrids).
 - ◆ Design decisions on electronics and hybrids optimally mistimed(eg. next few weeks) to sort out before Lehman review.



WBS 1.1.2.1 Silicon Strip IC Electronics

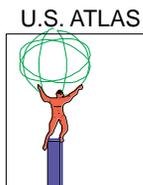
- Two rad-hard solutions under development
 - ◆ CAFÉ(bipolar from Maxim) + ABC(CMOS from Honeywell) - 2 chips. This has been and currently still is the US cost baseline.
 - ◆ ABCD(BiCMOS from Temic) - 1 chip.





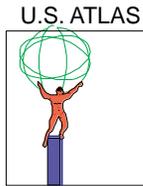
WBS 1.1.2.1 Silicon Strip IC Electronics

- Prototypes of all three ICs(CAFÉ, ABC and ABCD) were fabricated successfully and roughly on schedule last year.
- Both solutions, CAFÉ+ABC and ABCD, are functional pre-radiation with limited number of understood design errors(in ABC and ABCD). We have a preliminary but not final understanding of performance vs specifications via beam tests(at CERN and KEK) and laboratory measurements.
- The measured yields of CAFÉ/ABC are about as expected(roughly 70%) but the measured yield of ABCD is around 20%, about one-half that expected. The lower ABCD yield appears to be entirely consistent with processing(defect density).
- We have considerable but not entirely consistent measurements of the performance of both options after numerous irradiations.
- It seems apparent that neither option will meet all current specifications that were set many years ago, but will be close, and we are evaluating via simulation the effects of noise, threshold uniformity, timewalk etc as now expected to assess the impact on efficiency and tracking.
- The choice between the options, planned for early December 1999, has not been made. A coherent comparison of the two options, particularly the radiation effects and the impact on performance via simulation, is just now being completed.
- We will compile and review the data next week at CERN and have agreed to make a final decision no later than mid-February.



WBS 1.1.2.1 ETC

- Production costs have gone down relative to the FY97 estimate for the CAFÉ/ABC option but, given the measured yield of ABCD, the ABCD option will now cost more and this is reflected in the large contingency for production.
- We have added in the ETC, systems engineering(N. Spencer from Santa Cruz) and administrative support to help keep track of the ICs(import/export of controlled objects). To extent we can secure base support for Spencer, could reduce Design ETC costs by about \$350K.
- Should ABCD be selected, will have to modify(increase) base estimate and lower contingency.
- Costs for ABC and ABCD are based on response to CERN from one year ago under auspices of call for quotes on Frame Contract. This contract is not yet signed by any party and we are anxious to get it signed. Meeting at CERN with Temic arranged for Feb. 4 to finalize with them, we hope. Honeywell is more uncertain.
- Revised lower costs for CAFE are based on new estimate obtained by us.



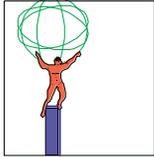
WBS 1.1.2.1 Risks and Issues

- **Risks**

- ◆ Stability of Temic and Honeywell (in principle solved by Frame Contract that specifies production into 2003 but...) -> go fast and backup solution? CAFÉ/ABC for ABCD or vice versa, deep submicron process
- ◆ Find problems that require lengthy redesign after launching preproduction submission in next few months -> not much, live with or take schedule hit.
- ◆ Systems issues not yet really addressed -> system tests (multi-module this summer)
- ◆ Low dose rate effect on bipolar front-ends -> setting up more tests but these take long time

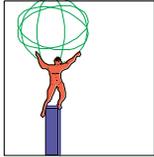
- **Issues**

- ◆ If ABCD...ability of US to participate in design if problems arise. Very limited involvement so far.
- ◆ Life-time buy and spares - see first risk item.

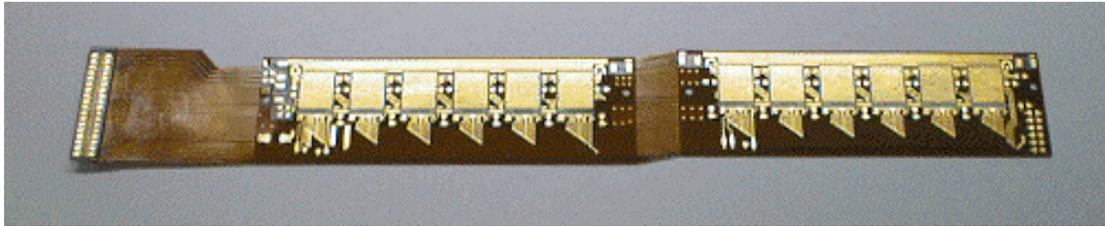


WBS 1.1.2.2 Silicon Strip Hybrids

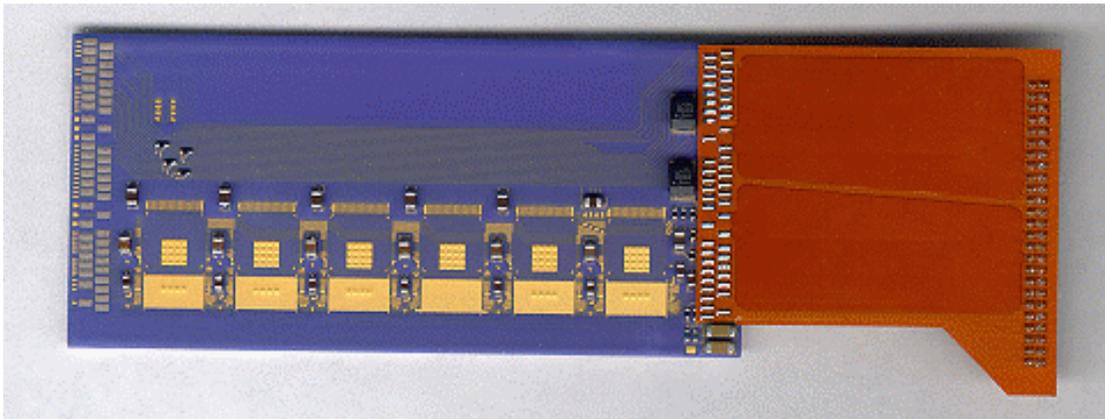
- Our baseline for barrel hybrids has been BeO hybrids and prototypes of these have been successfully manufactured and tested.
- ATLAS has considered alternative technologies: multi-layer kapton glued to a conducting (metallized carbon-carbon) mechanical support and direct deposition of traces on thermal pyrolytic graphite.
- Recently, the collaboration has proposed stopping development of the BeO hybrids but has not made a final selection of barrel hybrid type.
- We have in the last month obtained samples of the kapton hybrids and are evaluating them, and will receive samples of the TPG hybrids shortly for evaluation.
- The ETC has a revised cost for production of BeO hybrids that is slightly reduced compared to the FY97 baseline.
- We have not yet made an independent cost estimate of either the kapton or TPG hybrids. Estimates made by ATLAS suggest that either would be cheaper than BeO but this remains to be verified according to US costing rules. This will take some months since we need experience.



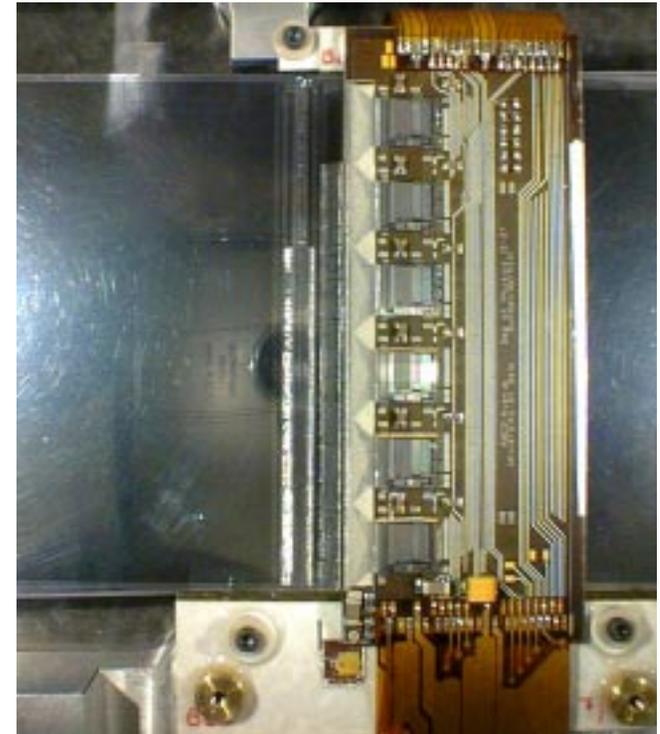
Silicon Strip Hybrids



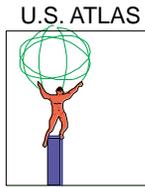
Copper on Kapton



Metal layers on beryllia



Metal layers/insulator
on pyrolytic graphite



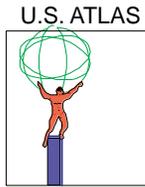
WBS 1.1.2.2 Risks and Issues

- **Risks**

- ◆ Neither kapton or certainly TPG hybrids have had use in existing silicon systems.
- ◆ Systems issues not yet really addressed -> system tests(multi-module this summer)

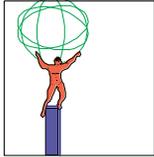
- **Issues**

- ◆ If either kapton or TPG, US role except as receiver of parts not yet clear. Minimal ability to influence schedule.



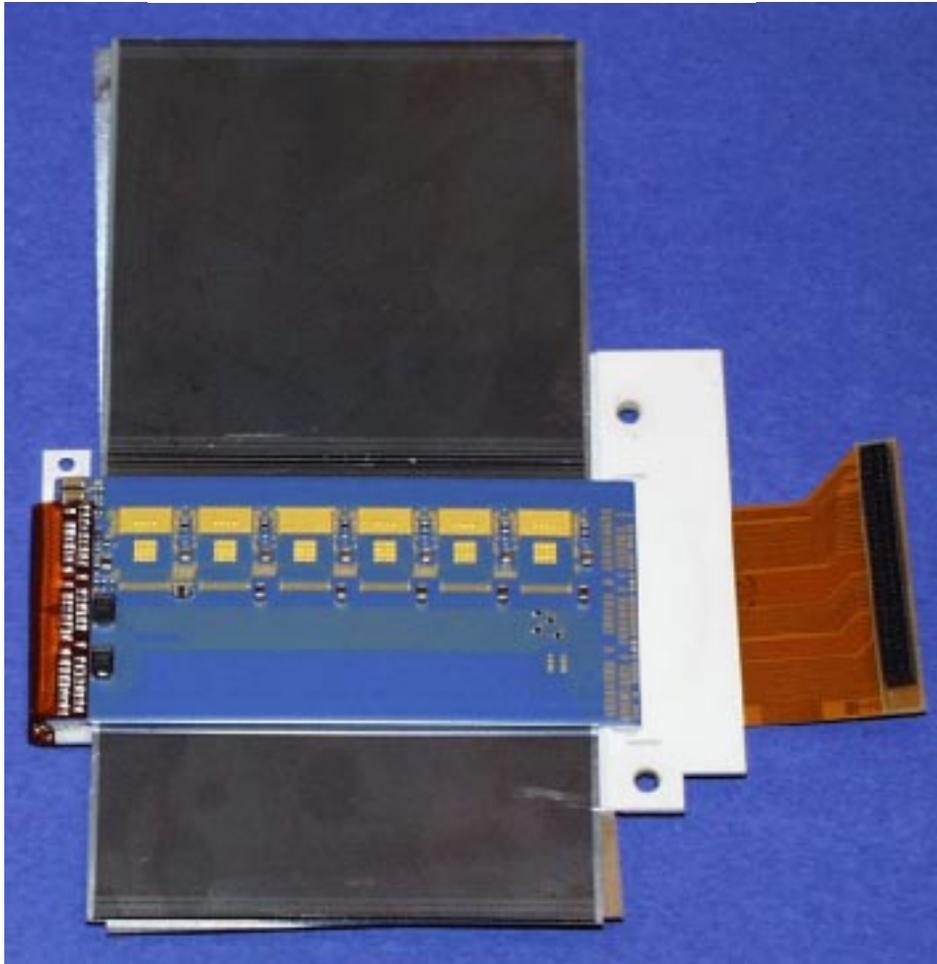
WBS 1.1.2.3 Silicon Strip Modules

- **Tooling and procedures to make prototype modules in place and operational.**
- **Clean space available for production assembly.**
- **Most of effort on modules has been to study electronics and hybrids.**
- **Are at early stage in this process(as expected from our schedule)**

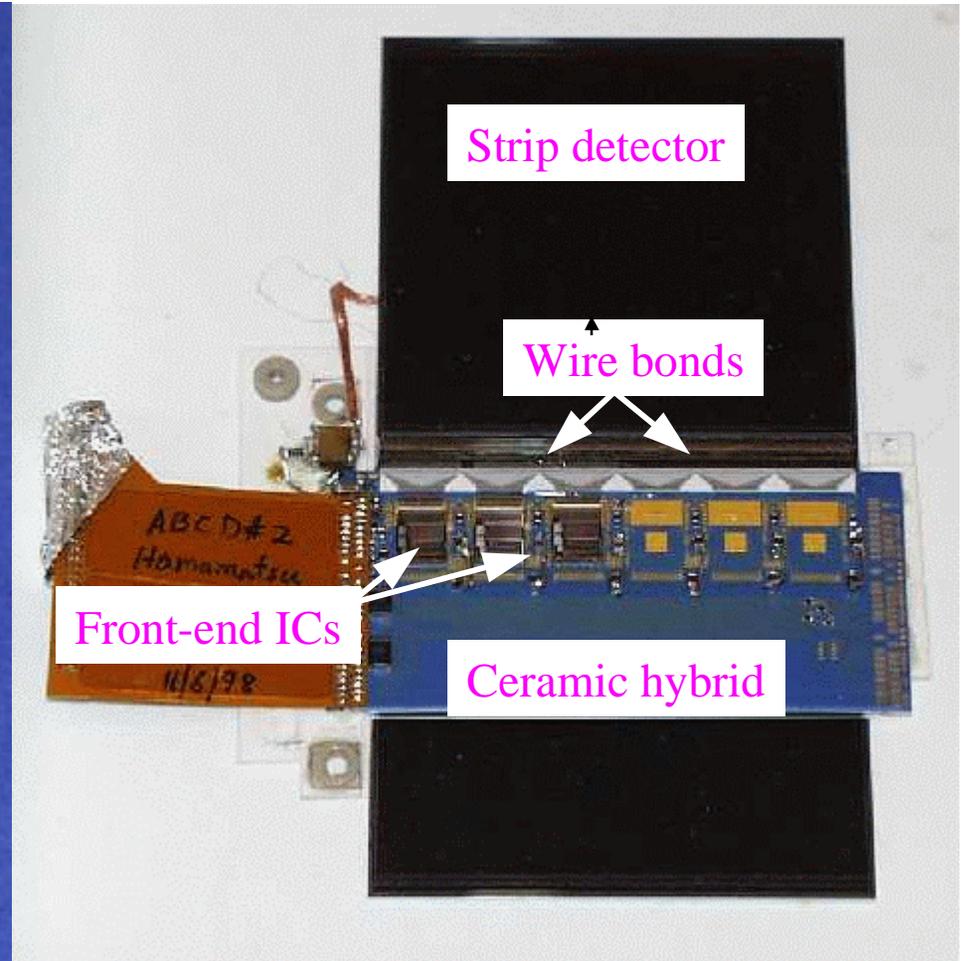


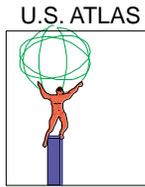
Barrel Silicon Strip Modules

Double-sided dummy module



Single-sided active module





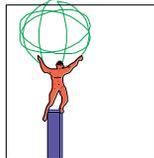
WBS 1.1.2.3 Risks and Issues

- **Risks**

- ◆ Electronics/hybrid tests, system tests will indicate substantial changes to module assembly procedures -> do these tests as fast as possible.
- ◆ Continued need for resources to understand electronics performance will slow down preparations for production -> decouple the electronics issues from proceeding with mechanical activity lead to production to extent possible - more technical manpower(expected from base support).

- **Issues**

- ◆ It's likely that all key module components - detectors, hybrids, thermal baseboards - except electronics will come from outside US. No significant ability to influence delivery schedule.

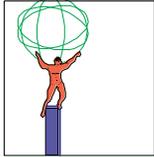


WBS 1.1.2 ETC

U.S. ATLAS E.T.C. WBS Actuals + E.T.C. Cost Estimates FY 00\$

1/25/00 10:35:53 AM

WBS Number	Description	E.T.C. Base Cost (k\$)	Cont Cost (k\$)	Cont %	E.T.C. Total Cost (k\$)	AY \$ Actual (k\$)	New	Previous	Difference (New - Old) (k\$)
							Total Cost	Estimate FY 97\$	
1.1.2	Silicon Strip System	4568	2035	45	6603	861	5429	5364	-269
1.1.2.1	IC Electronics	2622	1515	58	4137	722	3343	3210	-67
1.1.2.1.1	Design	772	51	7	823	318	1090	570	484
1.1.2.1.2	Development and Prototypes	106	8	7	114	389	495	510	-47
1.1.2.1.3	Production	1744	1456	84	3200	15	1759	2130	-504
1.1.2.2	Hybrids/Cables/Fanouts	973	209	21	1181	67	1040	1089	-117
1.1.2.2.1	Design	0	0	0	0	0	0	0	0
1.1.2.2.2	Development and prototype	32	1	3	33	67	99	81	14
1.1.2.2.3	Production	941	208	22	1148	0	941	1008	-131
1.1.2.3	Module Assembly and Test	973	311	32	1284	73	1046	1064	-85
1.1.2.3.1	Design of assembly and test	127	42	33	168	1	127	120	0
1.1.2.3.2	Development and prototypes	57	13	24	70	62	118	111	0
1.1.2.3.3	Production	790	256	32	1046	10	800	833	-85

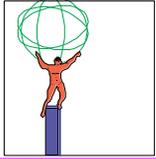


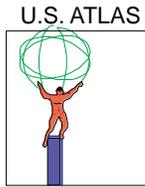
WBS 1.1.2 Schedule

ATLAS Milestones	Current ATLAS*	Baseline US	Forecast US
SCT Front end electronics			
Decision on vendor	12/3/99	12/10/99	2/28/00
Final design review	1/28/00	3/3/00	3/27/00
Front end electronics order placed (5% + 95%)	4/28/00	3/31/00	5/1/00
Front end electronics PRR	10/20/00	3/2/01	2/12/01
Release order for main production (95%)	2/26/01	3/30/01	3/5/01
Front end electronics 10% available	7/6/01	9/11/01	8/15/01
Front end electronics 25% available	9/14/01	11/22/01	10/26/01
Front end electronics production complete	8/2/02	11/21/02	8/19/02
SCT Barrel module hybrids assembly			
Hybrid choice decision	2/15/00	12/10/99	2/28/00
Final design review	4/10/00	2/11/00	5/10/00
Hybrid order placed (5% + 95%)	7/10/00	2/28/00	5/25/00
Hybrids PRR	2/16/01	4/11/01	2/15/01
Release order for main production (95%)	3/2/01	6/6/01	3/15/01
10% hybrid assembly available	10/19/01	1/15/02	8/1/01
25% hybrid assembly available	1/18/02	3/26/02	10/24/01
Barrel hybrid assembly complete	11/22/02	3/14/03	11/21/02
SCT Barrel module tooling			
Assembly tooling review	4/7/00	11/10/00	11/1/00
Tooling ready for production of modules	1/26/01	11/13/00	11/2/00
Module PRR	3/5/01	4/11/01	3/6/01
SCT Barrel modules			
Order placed silicon barrel modules (5% + 95%)	4/16/01	11/13/00	11/1/00
Release order for main production	9/17/01	6/5/01	4/12/01
Barrel silicon module 10% complete	1/7/02	11/20/01	9/18/01
Barrel silicon module 25% complete	4/15/02	2/26/02	12/25/01
Barrel silicon modules complete	4/14/03	8/26/03	4/22/03
* Current ATLAS schedule not baselined			
Level 2 US milestones			

Possible to meet US baseline if we push hard, I think

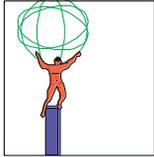
U.S. ATLAS





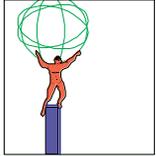
WBS 1.1.1 Pixel Project Status

- **Approved October 1998 for development through FY2000 with fixed project support - so-called Pre-Technical Baseline.**
- **Review in summer 2000 leading to construction baseline - this is still our plan, although we will not be advanced as planned on electronics items.**
- **Two internal reviews were planned before baseline review**
 - ◆ **March 1999 complete.**
 - ◆ **2nd review part of next month's Lehman exercise**
 - ◆ **In addition, have added mechanics review in April that will also cover mechanical aspects of module assembly.**

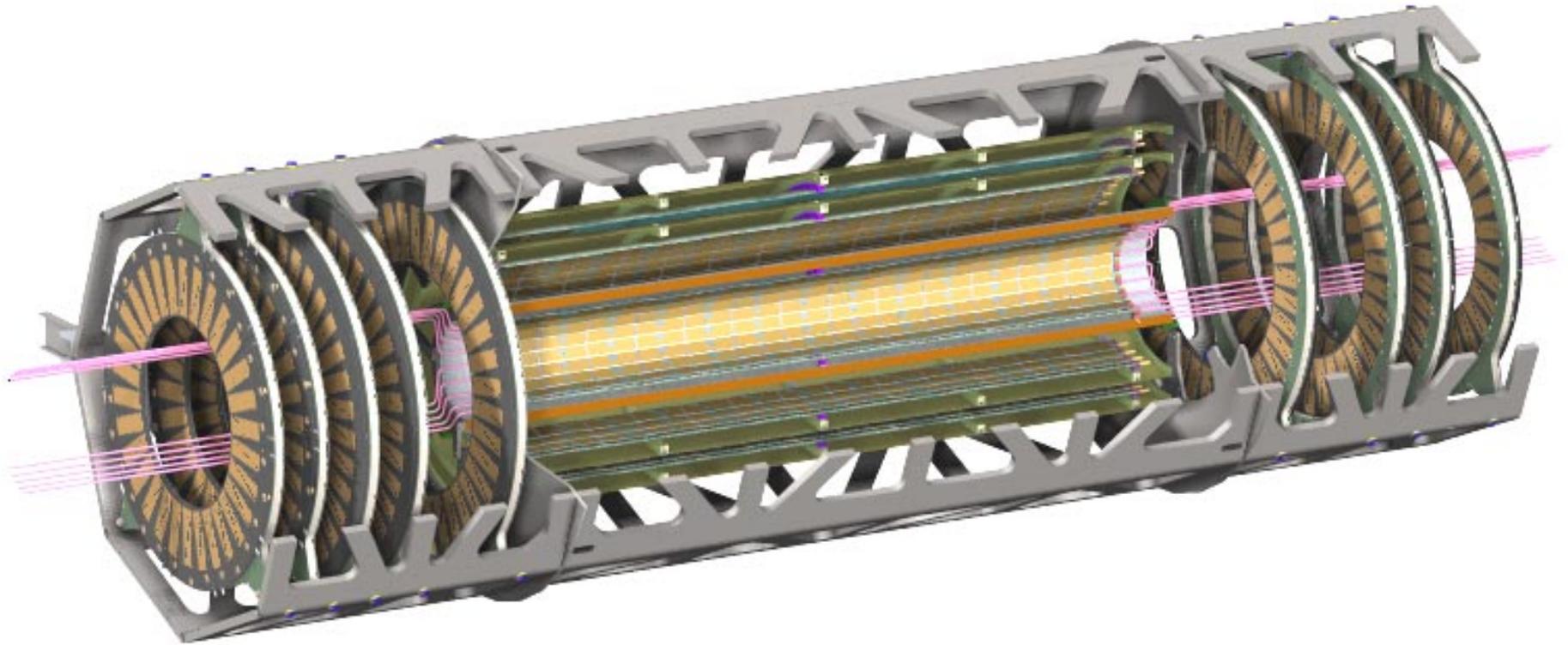


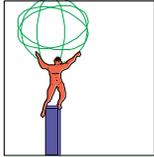
WBS 1.1.1 Technical Status Summary

- **1.1.1.1 Mechanics**
 - ◆ Prototypes of major elements fabricated and under test. Looks good so far.
 - ◆ Major technical issues: cooling system uncertainty(non - US responsibility but affects our design) and cable plant lack of design/cost(we have picked up most of this for now to advance project and control interfaces).
- **1.1.1.2 Sensors**
 - ◆ Round 1, round 1.5 prototype sensors fabricated and tested successfully. Round 2 prototypes just returned and under test. Final Design Review completed on Dec. 3.
 - ◆ Major technical issue: inadequate testing after irradiation(US opinion)
- **1.1.1.3 Electronics**
 - ◆ Full-scale, rad-soft prototype tests very successful. Proof-of principle - it can work.
 - ◆ First rad-hard fabrication complete(Temic). Design errors identified but major problem is believed to be very low yield. Honeywell design underway, but substantially late.
 - ◆ Major technical issue: Combination of design flaws and low yield likely to prevent meaningful irradiation testing until after refabrication of Temic chip.
- **1.1.1.4 Hybrids**
 - ◆ Prototype flex hybrids successfully manufactured by two sources. Few modules built, design looks OK
 - ◆ Major technical issues: detailed design verification with multiple modules and production preparations.
- **1.1.1.5 Modules**
 - ◆ Prototypes fabricated and tested but not enough built to understand systems aspects.
 - ◆ Critical bump bonding under control with limited outstanding issues with two vendors, third vendor being qualified by ATLAS and CMS working with still other vendors.
 - ◆ Major technical issues: yield of assembly process and radiation testing

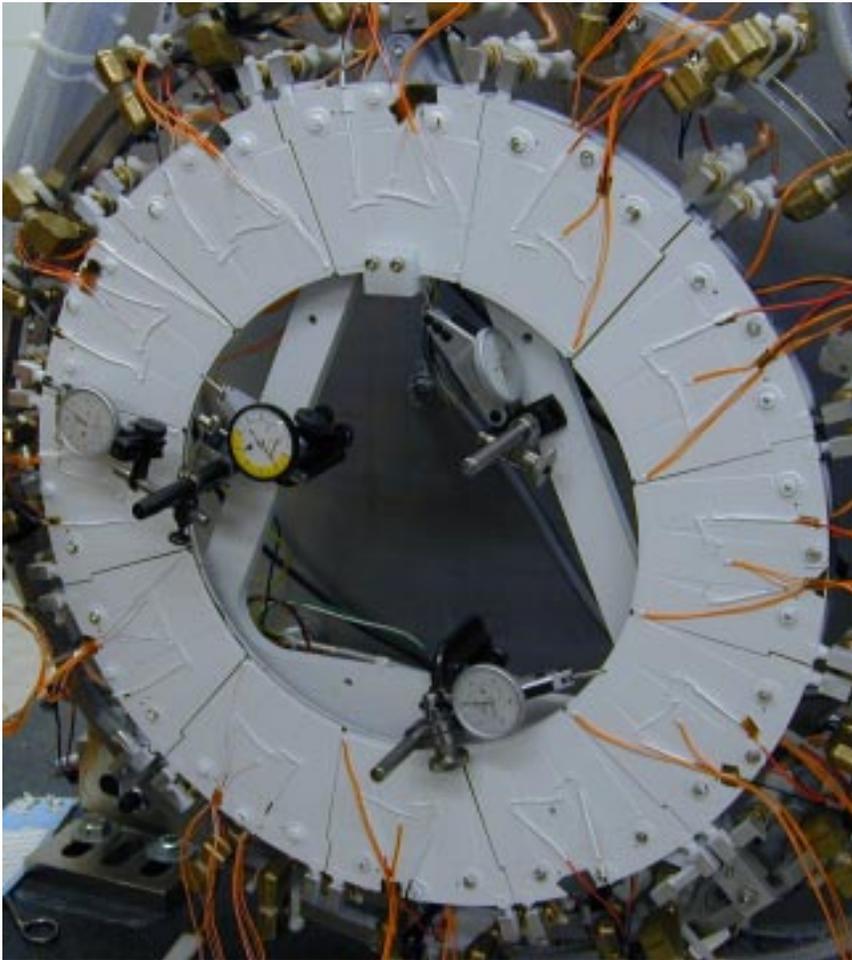


WBS 1.1.1.1 Pixel Mechanics

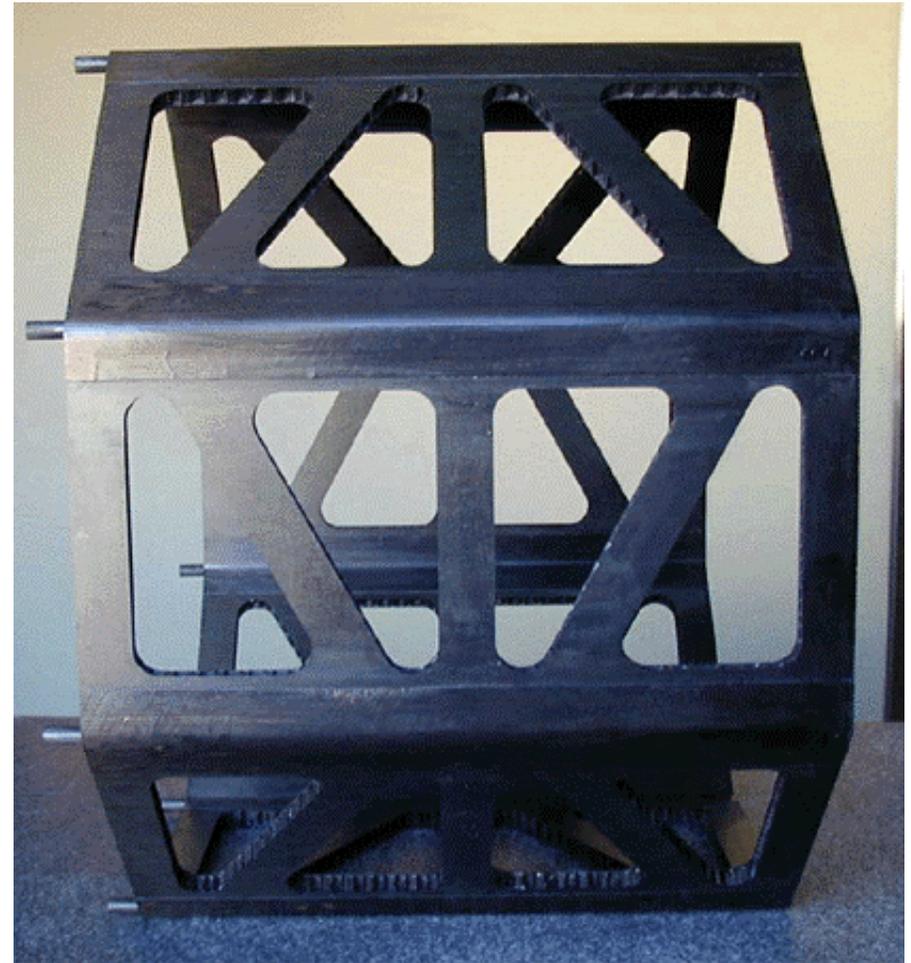




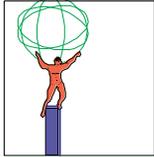
WBS 1.1.1.1 Prototypes



Prototype disk



Prototype end frame



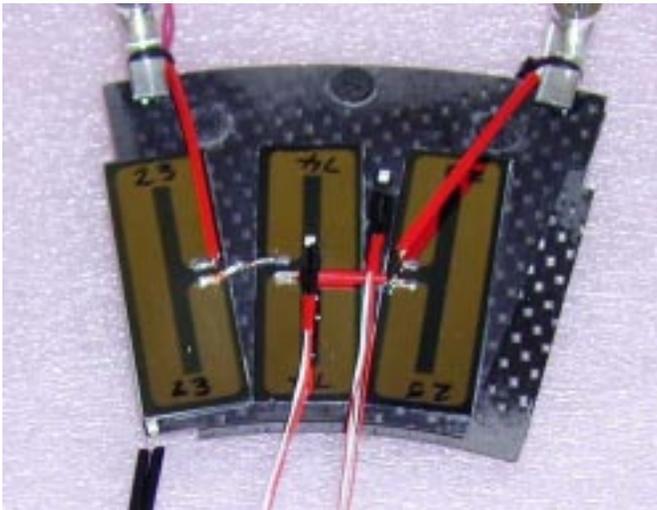
WBS 1.1.1.1 Prototypes



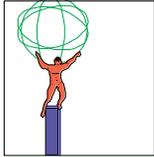
Al-tube
LBNL



ESLI, Inc
All-carbon



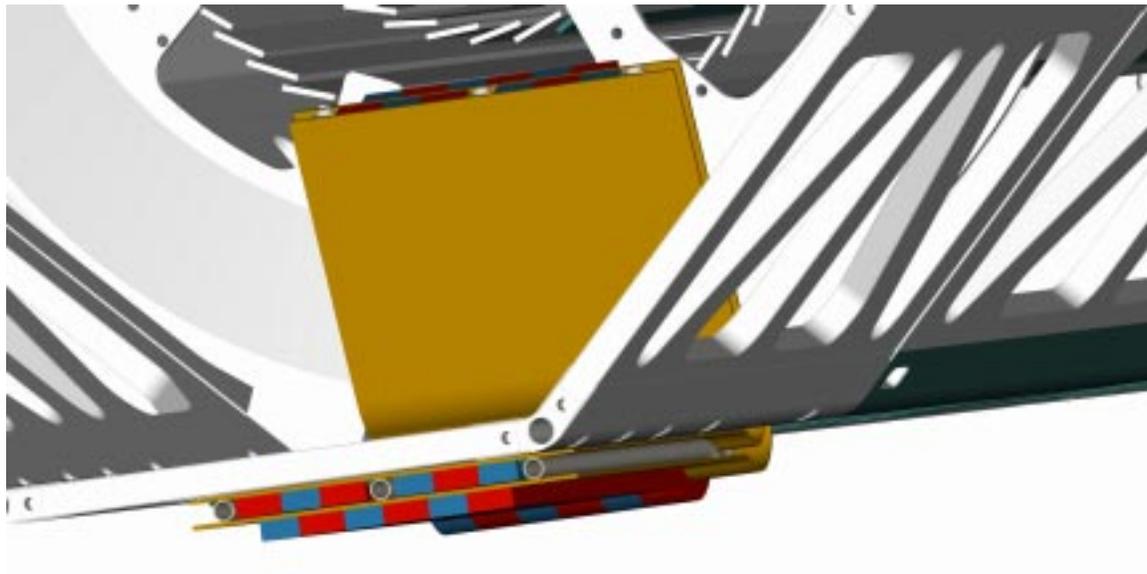
Hytec, Inc
All-carbon

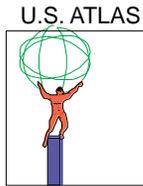


WBS 1.1.1.1 Prototypes/Design



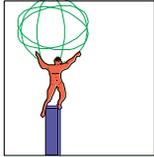
- Cable plant is major issue
 - ◆ Have set up and are just starting production of long(5 m) flex cables at LBL
 - ◆ Have taken on most of design integration, since critical interface with frame and disk region(all of the services must pass through disk region)
 - ◆ Overall cost estimates(we are nervous)





WBS 1.1.1.1 Pixel Mechanics - Status

- **Sectors**
 - ◆ Multiple sectors made and tested of all three designs.
 - ◆ Baseline was ESLI but changed to Al-tube because of coolant choice(see later) with Hytec as “fall-forward”
- **Disks**
 - ◆ First full disk(with ESLI sectors) made and under test. Learned much.
 - ◆ Second full prototype designed and planned by April.
- **Frame**
 - ◆ Real end section complete and under test. So far looks good.
- **Services**
 - ◆ Picked up much of this work to control interfaces to frame and to advance project.
 - ◆ Making prototype low mass cables and conceptual design/cost(a worry) of all cables.
 - ◆ Detailed layouts in progress. Critical to completing frame design.



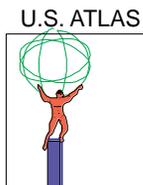
WBS 1.1.1.1 Risks and Issues

- **Risks**

- ◆ Cooling history. Binary ice -> liquid or evaporative fluorinerts -> low pressure(4-5 bar) evaporative -> high pressure(up to 10 bar) evaporative ->???. What to do? Conservative approach for design.
- ◆ Costly cable plant -> do design. Sharing with SCT?

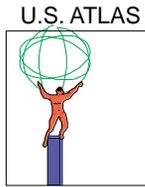
- **Issues**

- ◆ Will be ready to proceed with construction design for some items in about mid this FY. These funds were not included in Development budget -> have schedule design review April 10 as part of week long pixel mechanics meeting -> success => advanced construction funding.
- ◆ Because of cooling gyrations, need more Development funds for Al-tube sector. Also some for cable plant mockup and prototypes, not foreseen when Development budget set. Again review in April.



WBS 1.1.1.2 Pixel Sensors

- **Prototype 1.0 and 1.5 sensors fabricated and tested extensively, including with rad-soft electronics. A few irradiated sensors bonded to rad-soft electronics - work after lifetime fluence.**
- **Baseline design chosen and 2nd prototype sensors manufactured with two of the three vendors qualified to bid on production.**
 - ◆ **Wafers have been received from both vendors, CiS and IRST, and are undergoing measurement at ATLAS institutes.**
 - ◆ **CiS sensors operate well: pre-irradiation breakdown voltages typically > 600 V for the production design.**
 - ◆ **First devices from IRST show low pre-irradiation breakdown voltage (~150 V). A second batch is in progress to understand this. Its delivery is expected in mid-February.**
 - ◆ **Data are available at http://www-hep.phys.unm.edu/atlas_pixel/2_prototypes/.**
- **Final Design Review completed on December 3, 1999. Report at end of this presentation.**
- **Production Readiness Review scheduled for next week.**



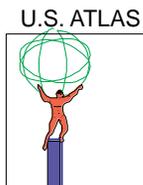
WBS 1.1.1.2 Risks and Issues

- **Risks**

- ◆ US opinion was that more irradiation testing should be done before PRR and certainly before preproduction order -> trying to do this but takes considerable beam time.
- ◆ No tests done yet with rad-hard electronics. Can imagine combined problems not seen with irradiated detectors and rad-soft electronics.
- ◆ Formally qualified vendors have limited capacity and will take some time for production -> which is why preproduction is scheduled this FY. But need to balance against item above.

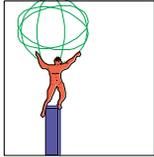
- **Issues**

- ◆ None

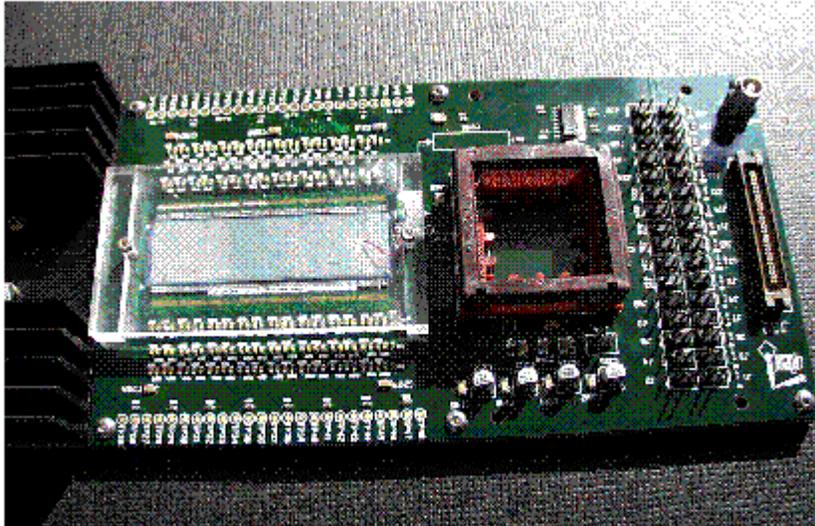


WBS 1.1.1.3 Pixel Electronics

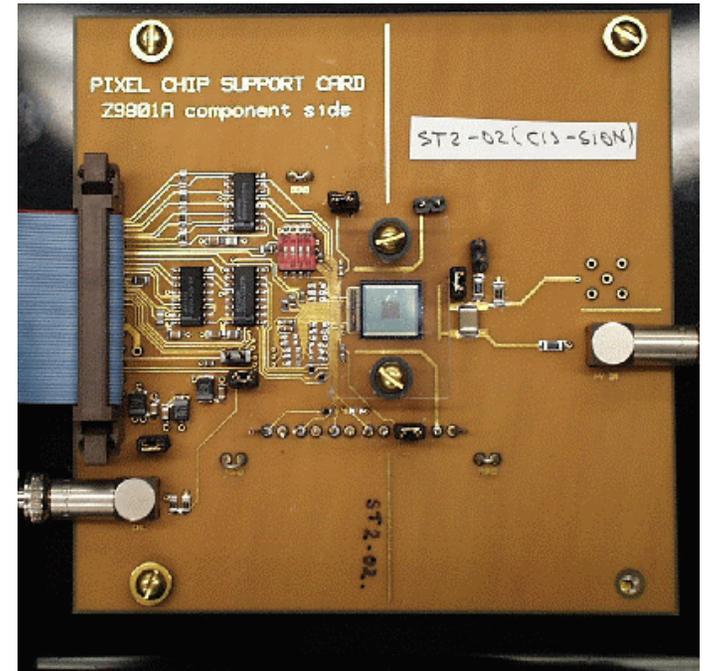
- **Critical path item.**
- **Full-scale prototypes(FE-A, FE-B and FE-C) fabricated in rad-soft technologies in 1998 and tested extensively in 1998 and 1999. Can't do justice to all of these impressive data. Bottom line - proof-of-principle demonstrated.**
- **Rad-hard status**
 - ◆ **Defacto decision to adopt Temic/DMILL for all but innermost layer of detector(B-layer). This is about 90% of detector. Why?**
 - ▲ **Cost - for same yield, apparently much less than Honeywell Sol**
 - ▲ **Inability for European members of design team to have access to Honeywell design rules. Now in place but delayed by State Department approval for roughly one year.**
 - ◆ **Honeywell Sol for B-layer. Why?**
 - ▲ **Denser process. Can do 300 long micron pixel, whereas 400 micron is DMILL limit. Even with pixel detector, confusion an issue for jets at innermost layer.**
 - ▲ **Suggestion that more rad-hard(but not proven)**
 - ▲ **Keeps both vendors in game.**
 - ▲ **Comes later.**



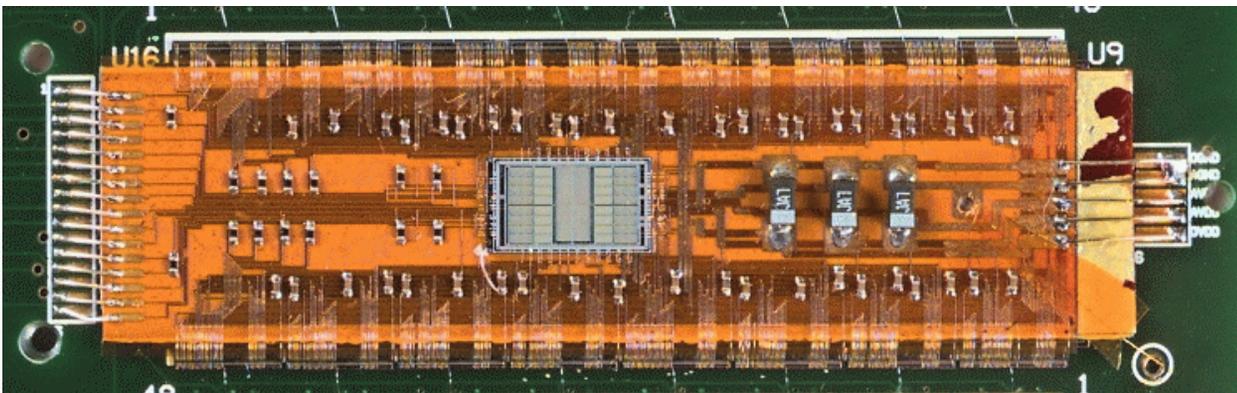
What Has Been Tested



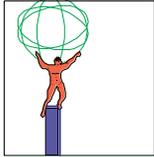
Bare 16-chip modules



Dozens of single chip/sensor assemblies of different types

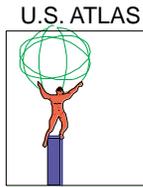


16-chip modules with flex hybrid



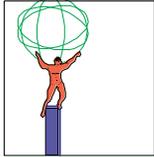
WBS 1.1.1.3 Pixel Electronics

- **Engineering run of FE-D(for DMILL) completed in October 1999**
- **Extensive testing**
 - ◆ A number of design errors identified
 - ◆ But, accounting for these errors, essential design appears to be OK but
 - ◆ Yield is very low, essentially zero for “perfect” chips - like those seen in rad-soft prototypes
 - ◆ Low yield can be attributed to particular processing problem that results in “leaky transistors”.
 - ◆ Discussions yesterday and today in France with Temic
 - ◆ Temic, so far, has not accepted full responsibility for processing difficulties.
 - ◆ Have kept 4 of 8 wafers.
 - ◆ Two wafers probed and best die(11 on each wafer) identified and simple repair fixing one error made with ion beam surgery.
 - ◆ One wafer each sent to two bump bonding vendors so that testing with detectors can be done.
 - ◆ Redesign on track for submission again in March, pending outcome of discussions with Temic.12-16 week fab time.
- **Honeywell design progressing**
 - ◆ Obviously slowed down by need to resubmit to Temic so soon
 - ◆ Most work by US so far since European groups have little familiarity with process but learning now that agreements in place
 - ◆ Weaknesses in FE-D design will be fixed in FE-H
 - ◆ But submission not likely before June(could be later) with current personnel. 23 week fab time. Have just this week hired another designer (by March) familiar with project.



WBS 1.1.1.3 Pixel Electronics

- **Electronics for optical receivers/drivers**
 - ◆ Ohio State(collaborating with Siegen) adapted SCT design for pixels and prototypes included in FE-D submission.
 - ◆ Under test now at OSU. Clearly some flaws but too soon to make final conclusion.
- **Module Clock and Control Chip**
 - ◆ Non-US effort but for completeness...also included on FE-D run. Looks OK so far.



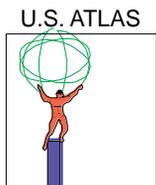
WBS 1.1.1.3 Risks and Issues

• Risks

- ◆ Obviously this is the cost and schedule risk for the Project.
- ◆ Cost risk(lower Temic yield or using HSOI for entire project) currently covered by large contingency (100% or about \$1M) but US contributes about 20% of total cost.
- ◆ Schedule
 - ▲ If FE-D2 submission has acceptable yield -> continue on our current plan
 - ▲ If FE-D2 continues to have very low yield but can be ascribed to design error -> FE-D3
 - ▲ If FE-D2 continues to have very low yield that cannot be ascribed to design -> dump Temic
 - Honeywell then becomes baseline choice but will be considerable pressure to move to deep submicron because of cost.
 - IF FE-H is success, I believe should continue with Honeywell as fast as possible ie. go into preproduction and develop deep submicron in parallel
 - ▲ If FE-H also unacceptable -> time for Plan B if ATLAS schedule remains close to mid-2005 turn on.

• Issue

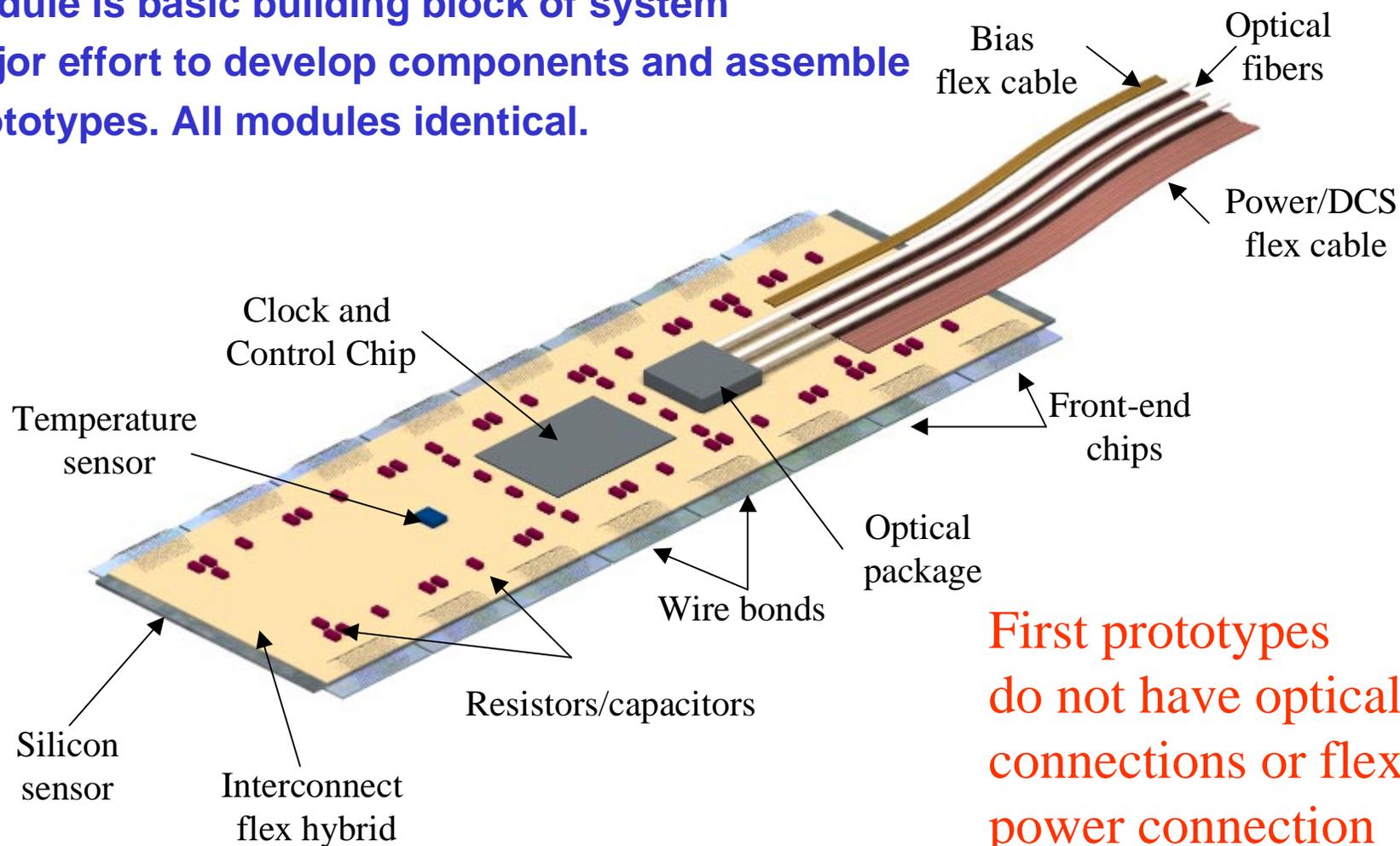
- ◆ The only way to advance the schedule is with more manpower for IC design and testing. We have been trying and are trying to do this. Finding manpower is currently issue, not money. Hopefully this will change. To really begin deep submicron roughly in parallel will require more money, if we can find the manpower.



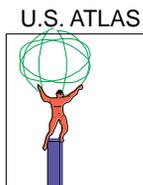
Pixel Module

Module is basic building block of system

Major effort to develop components and assemble prototypes. All modules identical.

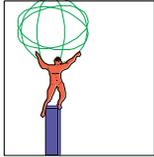


First prototypes do not have optical connections or flex power connection

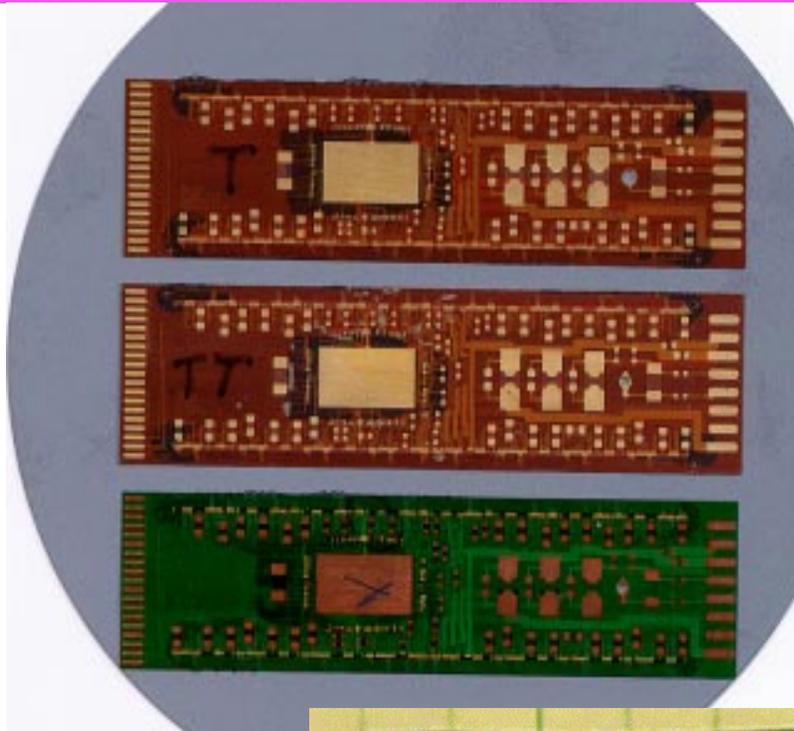


WBS 1.1.1.4 Pixel Hybrids

- This includes flex-circuit hybrids as shown on next page and local connections (“pigtail”) from these hybrids to power/control cables. Pigtails currently planned to also hold optical receivers/drivers.
- Flex hybrids v1.x manufactured at CERN(two generations) and most recently by US company(Compunetics).
- Few modules built and design looks OK but need more detailed verification with more modules
- Design of v2.x launched. Agreement reached on how, generally, to make connections to pigtails(different for barrel and disks) with identical flex hybrid. V2.x would be first to allow optical communication.
- Loading of flex hybrids so far done by hand but industry loading work just beginning in US and in Italy.
- Design of flex hybrid 100% responsibility of Oklahoma. Pigtail designs separated out: barrel in Europe and disk in US(UOK/LBL).
- In general, this has gone well but limited by availability of modules(in turn limited mostly by electronics). Recognize need to push harder now on production issues and are doing this.



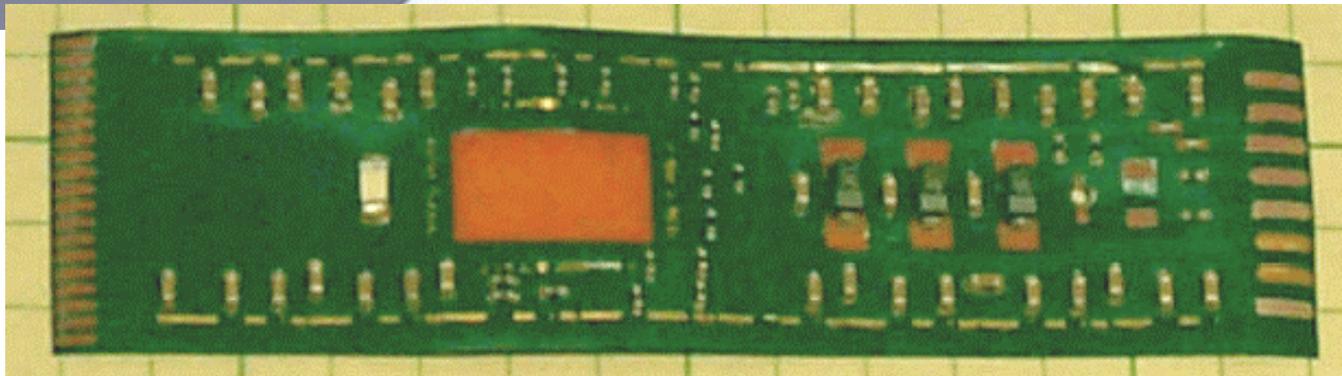
WBS 1.1.1.4 Pixel Hybrids



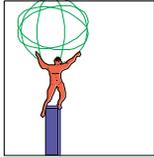
CERN - first version

CERN - second version

Compunetics

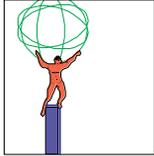


Compunetics v1.4 Flex Hybrid with passive components mounted.

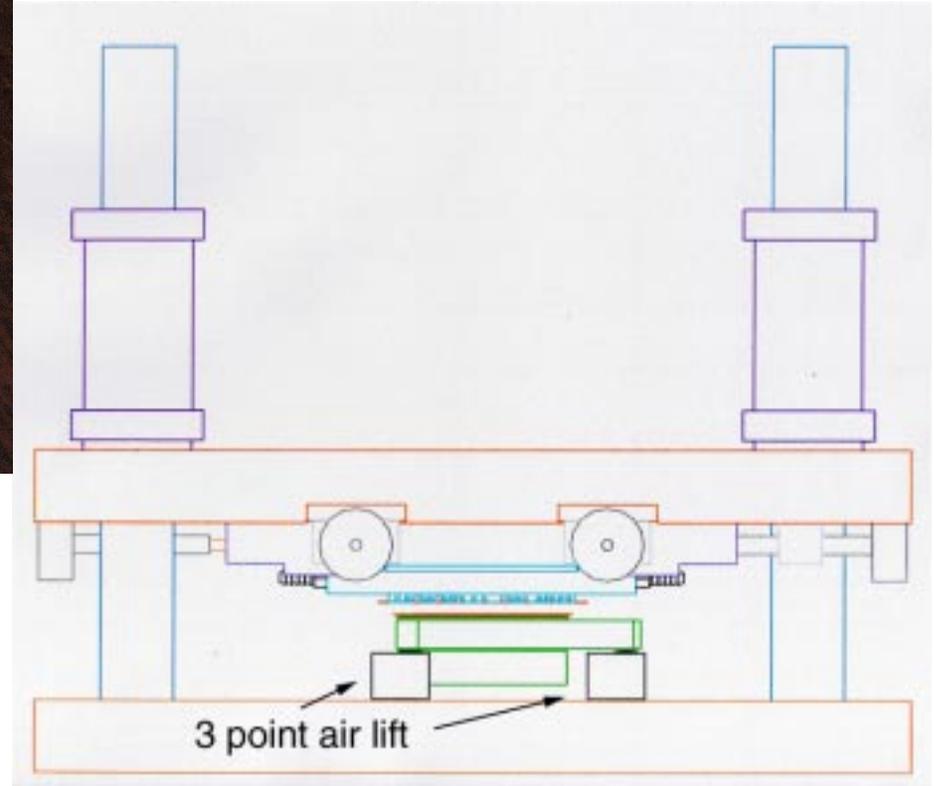
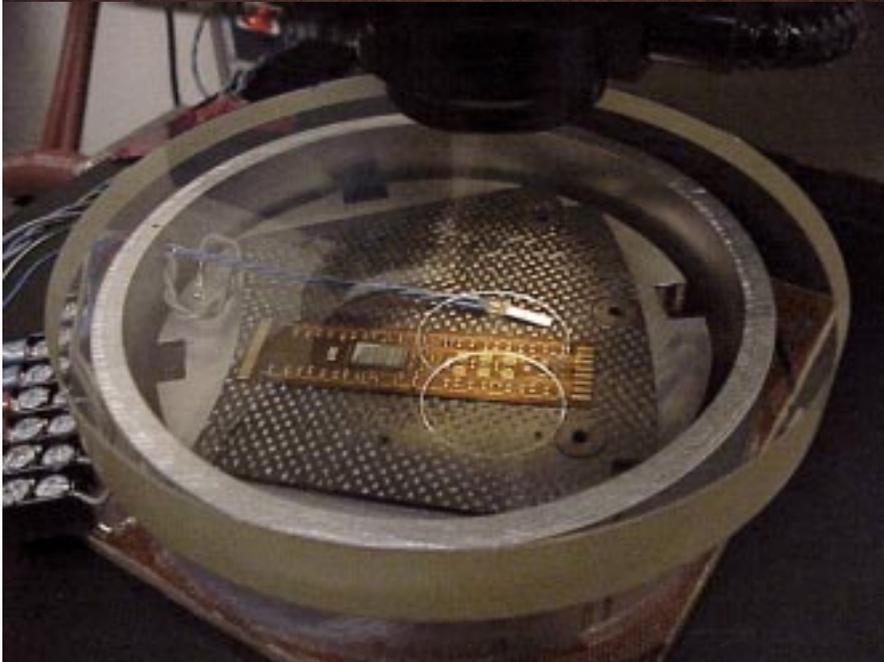
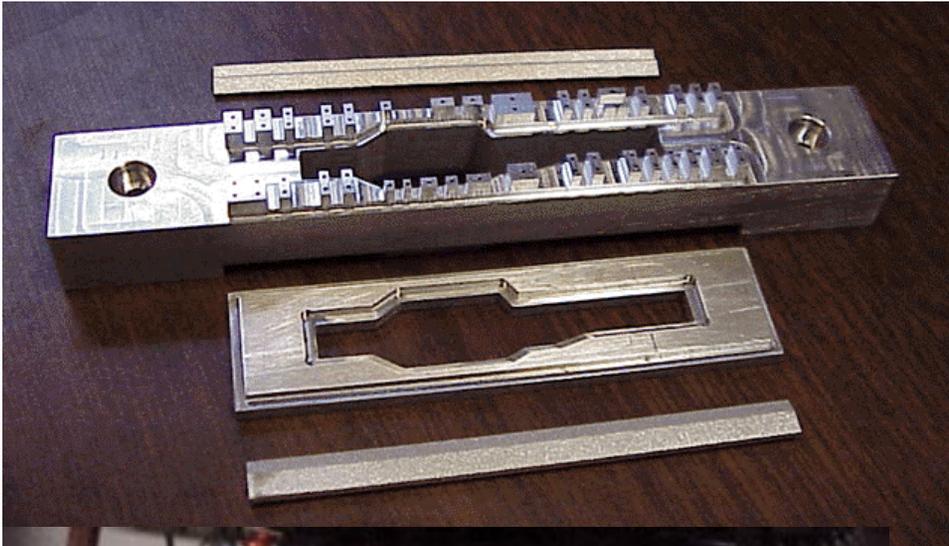


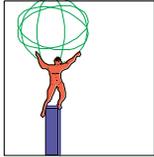
WBS 1.1.1.5 Pixel Modules

- **Modules include wafer thinning, dicing, bump bonding of ICs to sensor, attachment of flex to “bare module” and attachment of pigtailed and wire bonding and attachment of modules to mechanical support.**
- **Bump bonding status**
 - ◆ **Two vendors in Europe have demonstrated acceptable mechanical yield (low defect rate) and third European vendor started. Keep touch with CMS/B-Tev, who are working with different vendors.**
 - ◆ **Neither of two vendors wants more than 50% of job.**
 - ◆ **Site visit to one vendor (Germany) completed and other vendor (Italy) next week. Action list, mostly on QC/QA.**
 - ◆ **US role much reduced and we have dropped production responsibility, except perhaps for wafer thinning (only successes so far in US) and perhaps some X-ray inspection (Italian vendor currently lacks this capability) but are trying to shift these to Europe. Why? Practical and very large cost uncertainty.**
- **Conceptual design of module attachment procedures and tooling completed in US.**
- **Currently working on mechanical properties, wire bonding tests, gluing tests, irradiation, etc**
- **Limited by lack of modules, and until this month, flex hybrids to practice. Dummy module program started but no product yet from bump bonding vendors.**



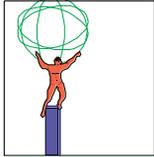
WBS 1.1.1.5 Pixel Modules





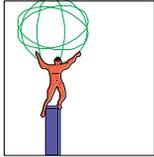
WBS 1.1.1 Scope and ETC

- The ETC has two parts. Completion of the Pre-Technical Baseline and a rough draft of proposed production. In both we have been guided by
 - ◆ need to advance the project
 - ◆ US strengths
 - ◆ and for production aiming to take on 100% of responsibilities that we can cost over next months where possible
- We are in good communication with the rest of the collaboration. The US (and perhaps Canada) are in the unique position of not being approved yet for construction.
- In general, as I have remarked in previous reviews, the production cost of the pixel subsystem has increased compared to the collaboration's estimates in 1996-97 although the physical scope has actually decreased by about 10% (as estimated from number of modules).



WBS 1.1.1 ETC and Scope - PreTechnical Baseline

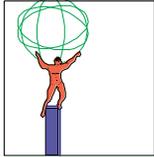
- **Mechanics: modest increase in structure prototypes and services(prototypes and mockup) -review in April before BCP made**
- **Sensors: no change(after BCPs for advancing preproduction and for engineering manpower)**
- **Electronics: no change, assuming no deep submicron**
- **Hybrids: modest increase in design(EE grad students) and prototypes. Also review about April before BCP made.**
- **Modules: no change**



WBS 1.1.1 PreTechnical Baseline ETC

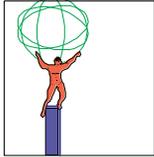
- Total cost includes contingency in both cases.
- Some small accounting problems to correct.
- BCPs approved or submitted will be 105K with expectation of about 100K more to come => use about 1/2 of contingency from FY97 estimate.

		FY97 Estimate(no BCPs)									
		FY97	FY97	FY97	FY00		FY00	Actuals			
		Base	Cont	Total	Total	AY	ETC	+			
		Cost	Cost	Cost	Cost	Actuals	Total	FY00 ETC	Difference		
WBS 1.1.1	Pre-Technical	2144	440	2583	2744	1025	1654	2679	-65		
	Baseline										
1.1.1.1	Mechanics	759	183	942	1001	476	490	966	-35		
1.1.1.1.1	Design	391	77	468	497	251	199	450	-47		
1.1.1.1.2	Development	368	106	474	504	225	291	516	12		
1.1.1.2	Sensors	159	30	189	201	104	112	216	15		
1.1.1.2.1	Design	55	5	60	64	39	54	93	29	BCP submitted	
1.1.1.2.2	Development	104	25	129	137	65	58	123	-14		
1.1.1.3	Electronics	727	94	820	871	279	499	778	-93		
1.1.1.3.1	Design	237	13	250	266	174	83	257	-9		
1.1.1.3.2	Development	490	81	570	606	105	416	521	-85		
1.1.1.4	Hybrids	186	44	229	243	107	188	295	52		
1.1.1.4.1	Design	71	9	79	84	81	31	112	28	Actuals over by 50K	
1.1.1.4.2	Development	115	35	150	159	26	157	183	24		
1.1.1.5	Modules	313	89	403	428	59	365	424	-4		
1.1.1.5.1	Design	48	13	62	66	0	60	60	-6		
1.1.1.5.2	Development	265	76	341	362	59	305	364	2		



WBS 1.1.1 ETC and Scope - Draft Production

- **Mechanics**
 - ◆ Disks, frame and cones.
 - ◆ Thermal barriers(now part of frame) and integrated B-layer insertion rails
 - ◆ Contribution to final assembly at CERN
 - ◆ Cable plant inside ID volume.
- **Sensors**
 - ◆ xxx wafers(about 20% of total) and testing of same
- **Electronics**
 - ◆ yyy wafers for outer layers and zzz wafers for B-layer(about 20% of total in each case)
 - ◆ Testing of about one-half of all wafers
 - ◆ One-half of z wafers for optical electronics
- **Hybrids**
 - ◆ All module flex hybrids and all disk pigtailed
 - ◆ Currently loading of all of these but under discussion.
- **Modules**
 - ◆ Assembly of all disk modules and attachment to disk structures and testing.
 - ◆ Currently all front-end IC wafer thinning, dicing, sorting but under discussion.
 - ◆ X-ray inspection of about one-half of bare modules but also under discussion.
- **Compared to guesses in 1996-97, mechanics has increased, sensors and electronics the same, hybrids+modules same, but have focussed on hybrids and dropped bump bonding.**

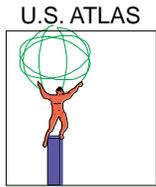


WBS 1.1.1 Total ETC

U.S. ATLAS E.T.C. WBS Actuals + E.T.C. Cost Estimates FY 00\$

1/25/00 10:24:07 AM

WBS Number	Description	E.T.C. Base Cost (k\$)	Cont Cost (k\$)	Cont %	E.T.C. Total Cost (k\$)	AY \$ Actual (k\$)	New	Previous	Difference (New - Old) (k\$)
							Total Cost	Estimate	
1.1.1	Pixels	8227	3697	45	11924	1025	9252	2134	6985
1.1.1.1	Mechanics and Final Assembly	2891	947	33	3839	476	3367	759	2561
1.1.1.1.1	Design	638	172	27	810	251	889	391	474
1.1.1.1.2	Development and Prototypes	228	63	28	291	225	453	368	61
1.1.1.1.3	Production	2026	712	35	2738	0	2026	0	2026
1.1.1.2	Sensors	675	149	22	824	104	780	225	541
1.1.1.2.1	Design/Engineering	49	5	10	54	39	88	55	30
1.1.1.2.2	Development and Prototypes	45	13	30	58	65	110	104	0
1.1.1.2.3	Production	581	131	22	712	0	581	66	511
1.1.1.3	Electronics	2596	1683	65	4279	279	2875	727	2103
1.1.1.3.1	Design/Engineering	78	5	7	83	174	252	237	1
1.1.1.3.2	Development and Prototypes	416	100	24	515	105	521	490	0
1.1.1.3.3	Production	2102	1578	75	3680	0	2102	0	2102
1.1.1.4	Hybrids, Cables and Optical	759	482	63	1241	107	866	115	743
1.1.1.4.1	Design/Engineering	29	2	6	31	81	110	0	110
1.1.1.4.2	Development and Prototypes	119	37	31	157	26	145	115	23
1.1.1.4.3	Production	611	443	72	1053	0	611	0	611
1.1.1.5	Module Assembly/Test	1193	399	33	1592	59	1251	308	924
1.1.1.5.1	Design/Engineering	47	13	28	60	0	47	44	1
1.1.1.5.2	Development and Prototypes	223	82	37	305	59	282	265	1
1.1.1.5.3	Production	923	303	33	1226	0	923	0	923
1.1.1.6	Pixel Misc Items	113	37	33	150	0	113	0	113
1.1.1.6.1	Test Support	63	21	33	83	0	63	0	63
1.1.1.6.2	Misc. Costs	50	17	33	67	0	50	0	50



Institutional Responsibilities

ALB LBL ISU UCSC UNM UOK UW OSU

1.1.1 Pixels

1.1.1.1 Mechanics

X

X

1.1.1.2 Sensors

X

X

X

1.1.1.3 Electronics

X

X

1.1.1.4 Hybrids

X

X

X

1.1.1.5 Modules

X

X

X

X

X

X

1.1.2 Silicon Strips

1.1.2.1 IC Electronics

X

X

1.1.2.2 Hybrids

X

X

1.1.2.3 Modules

X

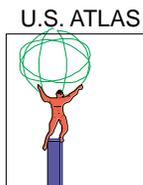
X

1.1.3 RODs

X

X

X Change since last review



WBS 1.1 Summary

- **1.1.1 Pixels**
 - ◆ Technical progress continues to be excellent, although we could have been luckier on the rad-hard electronics.
 - ◆ Electronics schedule is the critical problem.
 - ◆ Our proposal is to keep pushing hard and go for construction baseline review before end of FY. Plan for success!
- **1.1.2 Silicon Strips**
 - ◆ 2nd generation IC prototypes fabricated on schedule.
 - ◆ Final choice between IC options in next few weeks.
 - ◆ Preproduction IC submission forecast +1 month relative to baseline but possible to meet baseline schedule.
 - ◆ Rest of project driven by electronics(at present)
- **1.1.3 Read-Out Drivers(ROD)**
 - ◆ Design team in place
 - ◆ Prototype design advancing well