ATLAS PIXEL SYSTEM
MODULE ASSEMBLY

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Pixel Module

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical.

First prototypes do not have optical connections or flex power connection
Items Covered in This Talk

- Bump deposition (or receiving metal) on IC and detector wafers
- Dicing, thinning and possibly backside metallization of these wafers
- Flip chip assembly to produce what we call “bare modules”
- Probing of bare modules (not done yet - production)
- Mounting flex hybrids with components on module
- Module burn in and testing
- Principal interfaces
  - Module attachment to mechanical structure
  - Cabling (power and optical links)
## Assembly Process - Example

<table>
<thead>
<tr>
<th>Step</th>
<th>ICs</th>
<th>Yields (%)</th>
<th>Detectors</th>
<th>Yields (%)</th>
<th>Flex</th>
<th>Yields (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30.0% Fab</td>
<td>100.0% Fab</td>
<td>80.0% Fab</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>97.0% Probe</td>
<td>90.0% Probe</td>
<td>98.6% Cut (from CLEOIII)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>97.0% Bump deposition</td>
<td>97.0% Bump deposition</td>
<td>100.0% Probe</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.5% Inspection(bump yield)</td>
<td>92.3% Inspection(bump yield)</td>
<td>95.0% Mount components</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>95.0% Thin and metallize</td>
<td>97.0% Dice</td>
<td>99.9% Wire bond MCC (from CLEOIII)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td>99.0% Sort</td>
<td>97.0% Probe/burn-in</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>97.0% Dice</td>
<td>99.9% Ship</td>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>97.0% Sort</td>
<td>99.0% Inspect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>99.9% Ship</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>97.0% Bump deposition</td>
<td>100.0% Probe</td>
</tr>
<tr>
<td>99.0% Inspect</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>97.0% Sort</td>
<td>99.9% Ship</td>
</tr>
<tr>
<td>Yield (%)</td>
<td>25% per die</td>
<td>76% per tile</td>
<td>72% per flex</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module Assembly</th>
<th>Yields (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flip chip/die</td>
<td>99.0%</td>
</tr>
<tr>
<td>Flip chip/module</td>
<td>85.1%</td>
</tr>
<tr>
<td>Ship</td>
<td>99.9%</td>
</tr>
<tr>
<td>Inspect</td>
<td>99.9%</td>
</tr>
<tr>
<td>Probe bare module</td>
<td>99.0%</td>
</tr>
<tr>
<td>Ship</td>
<td>99.9%</td>
</tr>
<tr>
<td>Attach flex</td>
<td>98.0%</td>
</tr>
<tr>
<td>Wire bond FE's (with repair)</td>
<td>95.0%</td>
</tr>
<tr>
<td>Attach pwr/optics</td>
<td>98.0%</td>
</tr>
<tr>
<td>Ship</td>
<td>99.9%</td>
</tr>
<tr>
<td>Test/burn in</td>
<td>95.0%</td>
</tr>
<tr>
<td>Ship</td>
<td>99.9%</td>
</tr>
<tr>
<td>71% per module</td>
<td></td>
</tr>
</tbody>
</table>

M. Gilchriese
U.S. ATLAS Internal Review March 1999
Pixel Modules

Module with flex hybrid and controller chip on PC board

16 chips with 46,000 bump bonds

Sensor

ICs

Bump bonds

Xray of bumps

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U.S. ATLAS Internal Review March 1999
Bump Bonding

- Solder or indium bumps have been used so far in our prototype program.
- Different process flow for solder and indium and some small variations for fixed metal between vendors.

Vendors
- AIT(indium)$^1$
- Alenia(indium)$^2$
- Boeing(indium)$^{2,3}$
- GEC(solder)$^1$
- IZM(solder)$^2$
- Sofradir(indium)$^4$

IZM

Flip Chip Assembly

- Solder Bumping
  - Read out chip
- Inspection
- Dicing
- Cleaning & Inspection

- Loading Substrate
- Loading Chip
- Alignment
  - 4 µm 3σ accuracy
- Placement
- Unload Module / Single Tile
- Reflow Soldering
  - $240^\circ$ C peak temperature, activated atmosphere

$^1$ Used by others
$^2$ ATLAS parts made
$^3$ No longer active
$^4$ Contacts in process
Bump Bonding- What Do We Know?

- Both indium and solder successful for prototypes but some concerns about indium (high resistance from oxides?)
- Defect rate for bump deposition is roughly $10^{-5} - 10^{-4}$ for both metals
- Visual inspection appears to be adequate to measure this
- Defect rate for flip chip assembly has varied greatly for prototypes and between vendors from about $10^{-4} - 10^{-2}$
- X-ray inspection established with two vendors (IZM and here in Bay Area) and is adequate to measure flip-chip yield
- Thinning of bumped IC wafers to 150 microns and subsequent flip chip assembly has been demonstrated (on one 16 chip module) for indium only at the moment.
- Dicing of bumped wafers demonstrated with multiple vendors.
- Irradiated bumped (indium) detectors work. Bumping does not appear to affect detector properties adversely
- Tensile and shear strength measured. Creep studied. But all with low statistics.
- Preliminary price enquiry made to many vendors. Large differences in price (factor of 2)
Examples

Flip-chip assembly of single detector to IC

X-ray inspection of solder bump 16 chip module from IZM
Bump Bonding - What Don’t We Know?

- Should we choose one technology - solder or indium? Or should we allow both (equivalent to having two vendors?)
- Irradiated detectors with solder bumps OK?
- Yield with good confidence for all steps
- Impact of possible need for backside IC metallization on process steps
- Strength of bonds with good statistics
- Production rate for both wafer bump deposition or flip-chip assembly.
- Do we need more than one vendor for schedule reasons? Clearly desirable to reduce risk.
- QA program must exist but we haven’t come close to implementing this with vendors. Are agreed that substantial collaboration involvement is required.
Bump Bonding Program

- Build many more modules - as many as we can afford
- Goal is to build 50+ active modules with prototype 2 sensors and FE-B and later FE-D/H chips by early 2000.
- This will be done at IZM and Alenia. Third vendor under consideration but not decided yet.
- 2nd generation dummy module program not yet fixed. Decide in June.
- Stay in touch with other programs (ALICE, FNAL pixels)
- Detailed schedule up to production is (just) under development (primarily by me) following selection of flex module baseline 3 weeks ago
Module Assembly

- Only two flex modules have been assembled to date, one at Oklahoma and one at LBL.
- A few more with flex v1.0 will be made in Europe shortly.
- These have been and will be made to address electronics performance issues not module assembly.
- Production aspects of module assembly simply have not yet been addressed.
- Will begin to address these issues in about June of this year in preparation to prototype assembly tooling and procedures with modules made from 2\textsuperscript{nd} prototype sensors and FE-B(first) and then FE-D chips.
Module Assembly Plan

- Within the U.S., LBNL is responsible for module assembly but this relies on delivery of tested parts.
- We plan to have either direct responsibility in US or defined point of contact for all aspects during the development phase (through about mid-2000). We expect every step to also occur in Europe so coordination is important.
  - IC wafer probing (Einsweiler, Richardson, + labor)
  - Sensor wafer testing (Seidel, Hoeferkamp, UNM postdoc)
  - Bump deposition and inspection (Gilchriese)
  - Dicing, thinning and metallization (Gilchriese, Palaio)
  - Flex production and testing (Skubic, Boyd, Timm, + labor)
  - Flip-chip assembly and inspection (X-ray) (Gilchriese + labor)
  - Bare module probing (Einsweiler, Richardson, LBL postdoc, LBNL engineering)
  - Module assembly tooling (Goozen, Zizka)
  - Module assembly (Goozen, Zizka + labor)
  - Assembled module testing (Einsweiler, Richardson, LBL postdoc, LBNL engineering initially, but migrates to other groups)
  - PPL upgrades and software (Richardson, Fasching, UW supported engineering)
  - Optical interface/tests (when relevant) (Gan, Kagan, OSU engineering)
  - Power cable interface/tests (Anderssen + testing group)
  - Module attachment interface (Anderssen)
  - Overall coordination (Gilchriese)