Bump Bonding Plan

Draft of March 30, 1999

Scope

- Planning leading up to selection of production vendor(s) - about the next year
- Address both fundamental measurements(does it work - meet requirements) and production issues(suitable for ATLAS production)
- Next steps
  - Define individual responsibilities for carrying out the elements of the plan
  - Finances - what is feasible?
  - Need to be in place by June Pixel Week
  - Visits to major vendors must be scheduled soon to go over aspects of this plan, particularly QA
  - More regular contact among participants is needed

Fundamental Issues

Issue	How Addressed
• Electronics noise and stablity difference between solder and indium or between different vendors?	• Single-chip assemblies, modules tested at Bonn, LBL and Genoa
• Functionality after irradiation, including ICs after high temp. from bumping.	• Boeing indium demonstrated. Alenia indium irradiated March at LBL and tested at Genoa(test beam?). Solder must wait for rad-hard chips in Fall. Temperature effect on ICs needs study.
• Feasibility/reliability of thinned IC die with thinned detectors. Is deformation of thinned items so much that it's not possible. Solder indium difference?	• Assembly of 150 microns with Boeing indium demonstrated to some level. Thinned die flatness measurements in progress at LBL. Need to measure all components. When with solder? When with Alenia?

Electronics Interactions

- Experience with below summarized on next page for noise
  - Boeing indium
  - IZM solder
  - Alenia indium
- IZM single-chip and module noise is similar
- Clear difference in noise between Boeing indium and IZM solder with FE-B that is believed to be attributed in part to noisy regions from bad flip chip(tails) and apparent high resistance of Boeing bumps.
- Alenia measurement with FE-B showing high noise is not understood => need more measurements. Need to X-ray bare assemblies to show not a flip chip problem and then measure.
- Alenia and IZM comparison with FE-C shows ???

Noise Measurements

DEVICE	FRONT-END	DETECTOR TYPE	BUMP TYPE	NOISE
Bare module	FE-C	P1 Seiko Tile 2	IZM	137
Bare module	FE-B	P1 CIS Tile 2	Boeing	225
Bare module	FE-B	P1 Seiko Tile 1	Boeing	191
Bare module	FE-B	P1 CIS Tile 1	IZM	140-150
Flex module	FE-B	P1 CIS Tile 1	Boeing	270-314
Single chip	FE-C	P1 CIS ST1	IZM	106
Single chip	FE-B	P1 CIS ST1	IZM	83
Single chip	FE-C	P1 CIS ST1	IZM	136
Single chip	FE-C	P1 CIS ST2	IZM	75
Single chip	FE-C	P1 CIS SSG	IZM	191
Single chip	FE-A	P1 CIS SXT	Boeing	396
Single chip	FE-C	P1 Seiko ST2	IZM	109
Single chip	FE-C	P1 CIS ST1	IZM	164
Single chip	FE-C	P1 Seiko ST2	IZM	149
Single chip	FE-B	P1 CIS ST1	IZM	116
Single chip	FE-B	P1 CIS ST2	IZM	105
Single chip	FE-B	P1 CIS SSG	IZM	171
Single chip	FE-B	P1 CIS S7O	IZM	173
Single chip	FE-B	P1 CIS S8O	Boeing	100-600
Single chip	FE-B	P1 CIS SBR	Boeing	100-400
Single chip	FE-B	P1 CIS ST2 SiON	IZM	114
Single chip	FE-B	P1 CIS ST2 SiON	IZM	112
Single chip	FE-B	P1 CIS ST1 SiON	IZM	122
Single chip	FE-B	P1 CIS ST1 SiON	IZM	106
Single chip	FE-B	P1 CIS ST1 SiON	IZM	107
Single chip	FE-B	P1 S7O	Boeing	150-800
Single chip	FE-B	P1 SXT	Boeing	200-500
Single chip	FE-B	P1 ST1 MCMD	IZM	104
Single chip	FE-B	P1 ST2 MCMD	IZM	109
Single chip	FE-B		Alenia	high
Single chip	FE-C		Alenia	??

Measurements are done in different places with different procedures.
Module noise values are in general increased from flip chip problems

Production Issues(I)

Issue	How Addressed
• Demonstrate feasibility of backside metallization for solder bumping	• Underway now at IZM. Issue for Alenia?
• Demonstrate feasibility of backside metallization for thin wafers(150 microns?) followed by bump deposition and/or metallization after bumping and thinning.	• Not clear. Should be done first with dummy wafers. Thin 2 FE-B wafers, metallize in US and send 1 to IZM and 1 to Alenia? Metallize bumped wafers possible(vendor says yes, but haven't done it)
• Bumping 200 micron detector wafers in both indium and solder	• Dummy 200 micron wafers done by AIT successfully. 2nd prototype detectors(200 micron) to be done at IZM and Alenia.

Production Issues(II)

Issue	How Addressed
• Shear and tensile strength, and creep, with better statistics	• Initial LBL work but not with relevant vendors.Indium at Milano? Solder? Need more detailed plan
• Wire bonding tests after bumping. Have had problems. What do we know about Alenia items?	• Bonn-LBL differences with IZM items. Why? Experience at Genoa?
• Flip chip with Alenia	• Transition from Genoa to Alenia. By Summer 1999.
• Develop and test QA plan to measure yield during prototype phase	• See later. Overlap of collaborators with vendor?

Production Issues(III)

Issue	How Addressed
• Rework feasibility	• Underway now with indium in Genoa. Solder how?
• Vendor reporting	• Prototype
• Assess production rate	• Prototype. But may not be sufficient. Should be part of contract
• Packaging and shipping	• Prototype

Component Availability - ICs

- FE-B wafers
  - One wafer diced for tests
  - 2 wafers were done at Boeing
  - 1 wafer for AIT
  - Potentially 16 wafers either at IZM or Alenia or not yet probed => about 1120 good die => <70 modules worth
- FE-C wafers
  - ???
- FE-D wafers
  - 8 wafers delivered. If 30% yield, about 200 good die => <12 modules
- FE-H wafers
  - 5 wafers delivered. If 30% yield, about 125 good die => < 7 modules

Component Availability - Sensors

- Prototype 1b/1.5
  - Fabrication complete at CIS
  - First delivery of 16 wafers, of which 8 our out of spec
  - Second batch of 11 280 micron wafers and 5 200 micron wafers
  - => 48 possible modules
- Prototype 2.0
  - Depends on number of firms
  - 20 wafers minimum from each firm
  - 2 firms minimum => 120 possible modules
- Summary
  - ICs > 90 modules possible
  - Sensors > 168 modules possible

Current IZM Plan

- Now - July 1999
  - with existing sensor wafers(3): 21 SCs, 4 bare modules, 2 MCM-D modules
  - with prototype 1.5 sensor wafers(7): 5 SCs, 8 bare modules, 5 MCM-D modules
  - ?? FE-B wafers and ?? FE-C wafers
- Aug. 99- Feb. 00
  - with sensor 2.0 wafers(>17): 30 SCs, 40 bare modules, 10 MCM-D modules
  - ?? FE-B wafers, ?? FE-C wafers, 3 FE-D wafers
- Feb. 00 - Jul. 00
  - with sensor 2.0 wafers
  - 1 FE-D wafer, 2 FE-H wafers
- Wafer thinning in Germany(CISCO) to be investigated by end April

	Single chip	Bare modules	MCM-D modules	Components
Now - July 1999	26	12	7	1.5, FE-B, C
Aug. 99 - Feb. 00	30	40	10	2.0, FE-B,D
Feb. 00 - Jul. 00	?	30	6	2.0, FE-D,H

Proposed QA with IZM

Outline of QA Plan	Responsibilities
Visual inspection IC wafers(after probe)	Bonn
Visual inspection sensor wafers(after probe)	Dortmund
Visual inspection IC after thinning	Not relevant
Mask coordination	IZM/?
Record all bumping process parameters	IZM
Visual inspection after bumping or UBM	IZM/Bonn
Thinning	CISCO?/?
Visual inspection after thinning if bumped	IZM
Visual inspection after dicing	IZM
Inspection just before flip chip	IZM
Record flip chip parameters	IZM
X-ray inspection after flip chip	IZM
Mechanical(flatness) after flip chip?	IZM? Dortmund?
Travelers and database coordination	Dortmund
Regular reports to collaboration	Bonn

Current Alenia Plan

- Now - July 1999
  - with existing sensor wafers(?): ?? SCs, ? bare modules, ? MCM-D modules
  - with prototype 1.5 sensor wafers(?): ? SCs, ? bare modules, ? MCM-D modules
  - ?? FE-B wafers and ?? FE-C wafers
  - flip chip done at Genoa
- Aug. 99- Feb. 00
  - with sensor 2.0 wafers(??): ?? SCs, ?? bare modules, ?? MCM-D modules
  - ?? FE-B wafers, ?? FE-C wafers, 3 FE-D wafers
  - flip chip done at Alenia from now on
- Feb. 00 - Jul. 00
  - with sensor 2.0 wafers(??)
  - 1 FE-D wafer, 2 FE-H wafers
- Wafer thinning possible at Alenia but prefer outside supplier(TBD)

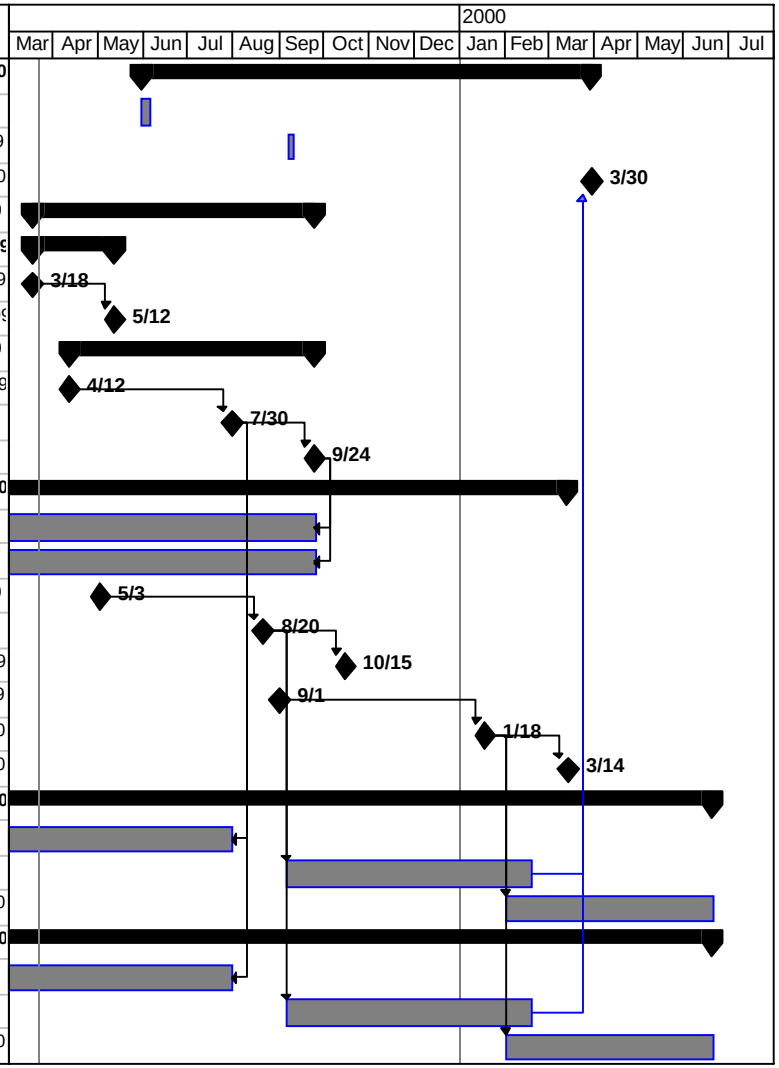
	Single chip	Bare modules	MCM-D modules	Components
Now - July 1999				1.5, FE-B, C
Aug. 99 - Feb. 00				2.0, FE-B,D
Feb. 00 - Jul. 00				2.0, FE-D,H

Proposed QA with Alenia

Outline of QA Plan	Responsibilities
Visual inspection IC wafers(after probe)	?
Visual inspection sensor wafers(after probe)	?
Visual inspection IC after thinning	TBD
Mask coordination	Alenia/?
Record all bumping process parameters	Alenia
Visual inspection after bumping or UBM	Alenia/?
Thinning	US? Or
Visual inspection after thinning if bumped	US? Or ?
Visual inspection after dicing	Alenia
Inspection just before flip chip	Alenia
Record flip chip parameters	Alenia
X-ray inspection after flip chip	?? US?
Mechanical(flatness) after flip chip?	Genoa/Milano
Travelers and database coordination	?
Regular reports to collaboration	?

Other Vendors and Summary

- AIT(indium)
  - One FE-B wafer to be done(under diamond program)
  - One Prototype I Seiko wafer to be done(under BTeV program)
  - Inspection results available
  - Three assemblies(ST1, ST2, SSG) to be made for ATLAS to compare noise with Boeing indium and IZM
  - Timescale: tentatively end of May
- Sofradir(indium)
  - In progress with dummy wafers
  - Need to understand better process
- Summary
  - Sum of Alenia + IZM plans exceeds supply of parts from sensor prototypes 1b/1.5 +2.0 and FE-B/C+FE-D/H wafers

Overall Schedule

ID	Task Name	Duration	Start	Finish
1	**ATLAS events/milestones**	**219 days**	**Mon 5/31/99**	**Thu 3/30/00**
2	Pixel week(Prague)	5 days	Mon 5/31/99	Fri 6/4/99
3	Pixel week(CERN)	4 days	Tue 9/7/99	Sat 9/11/99
4	Select bumping vendors	0 days	Thu 3/30/00	Thu 3/30/00
5	**Sensors**	**137 days**	**Thu 3/18/99**	**Fri 9/24/99**
6	**Prototype 1.5**	**40 days**	**Thu 3/18/99**	**Wed 5/12/99**
7	First wafers delivered	0 days	Thu 3/18/99	Thu 3/18/99
8	Last wafer probed	0 days	Wed 5/12/99	Wed 5/12/99
9	**Prototype 2.0**	**120 days**	**Mon 4/12/99**	**Fri 9/24/99**
10	Submit for fabrication	0 days	Mon 4/12/99	Mon 4/12/99
11	First wafers delivered	0 days	Fri 7/30/99	Fri 7/30/99
12	Last wafer probed	0 days	Fri 9/24/99	Fri 9/24/99
13	**Front-end Electronics**	**272 days**	**Mon 3/1/99**	**Tue 3/14/00**
14	FE-B probing	150 days	Mon 3/1/99	Fri 9/24/99
15	FE-C probing	150 days	Mon 3/1/99	Fri 9/24/99
16	FE-D submit	0 days	Mon 5/3/99	Mon 5/3/99
17	FE-D wafers arrive	0 days	Fri 8/20/99	Fri 8/20/99
18	FE-D wafers probed	0 days	Fri 10/15/99	Fri 10/15/99
19	FE-H submit	0 days	Wed 9/1/99	Wed 9/1/99
20	FE-D wafers arrive	0 days	Tue 1/18/00	Tue 1/18/00
21	FE-D wafers probed	0 days	Tue 3/14/00	Tue 3/14/00
22	**IZM**	**342 days**	**Mon 3/1/99**	**Tue 6/20/00**
23	1/1b/1.5+FE-B,C	110 days	Mon 3/1/99	Fri 7/30/99
24	2.0+FE-B,C,D	120 days	Mon 9/6/99	Fri 2/18/00
25	2.0+FE-D,H	100 days	Wed 2/2/00	Tue 6/20/00
26	**Alenia**	**342 days**	**Mon 3/1/99**	**Tue 6/20/00**
27	1/1b/1.5+FE-B,C	110 days	Mon 3/1/99	Fri 7/30/99
28	2.0+FE-B,C,D	120 days	Mon 9/6/99	Fri 2/18/00
29	2.0+FE-D,H	100 days	Wed 2/2/00	Tue 6/20/00