The ATLAS Pixel B-Layer Replacement Program

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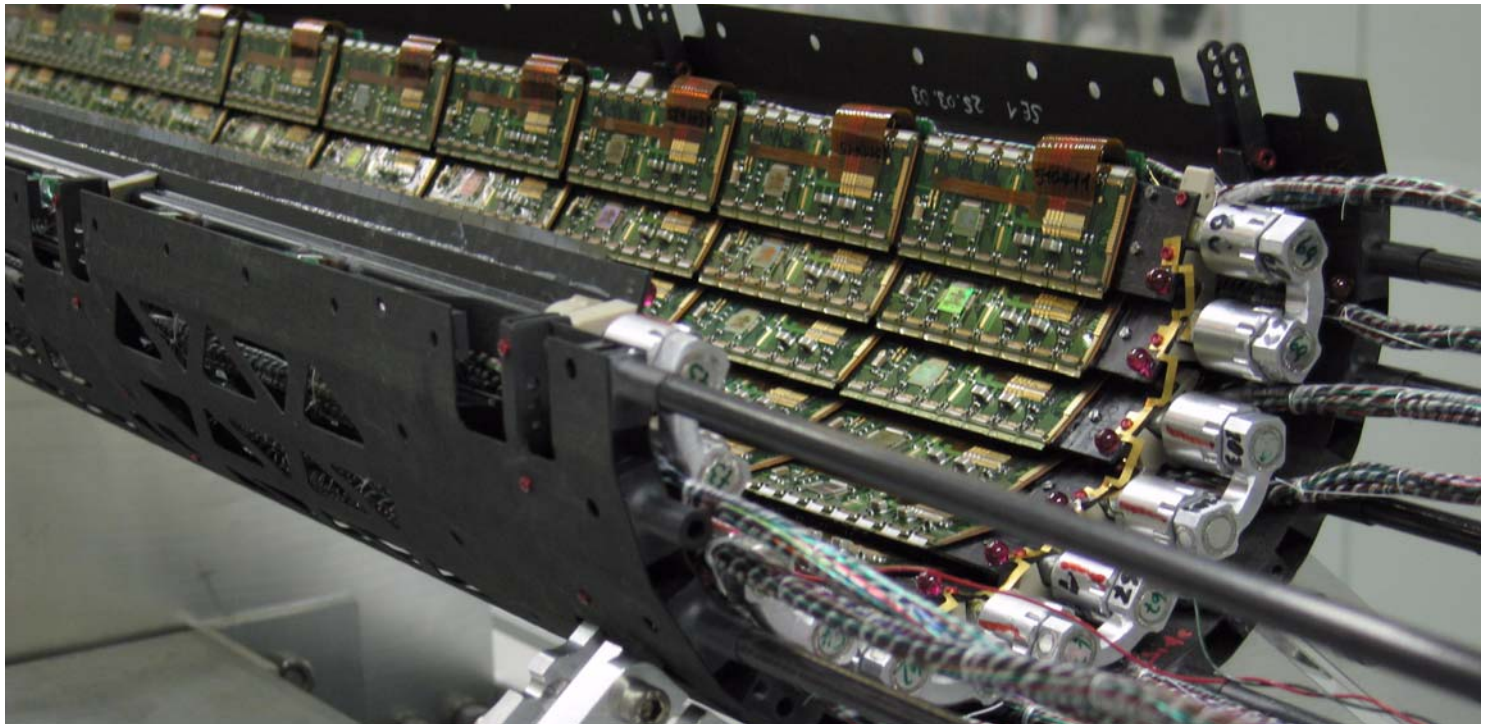
Goals for the ATLAS B-Layer Replacement:

- Early version of this was presented in ATL-IP-ER-0015, which is now more than two years old, but contained much of the material presented here.
- Present current overview, with warning that it is very much a work in progress. Too early to make many implementation decisions before we have operational experience, therefore concentrate on “core technologies” in near future.
- The integration of the present detector has taught us that the replacement of the B-Layer will not be a simple undertaking...

Present ATLAS Pixel B-Layer

Innermost layer of the ATLAS Pixel Detector:

- Historically called B-layer. Sensor radius is 50mm, and layer consists of 22 carbon-carbon staves (11 evaporative cooling circuits), each supporting 13 modules:



- Total of 286 modules (16%) with 20 degree tilt angle, 13.2M channels, active area roughly 0.29 m^2, worst-case end-of-lifetime power load as high as 2.4kW.
- Features: two data fibers/module at 80Mbit/s each, all cooling connections on C-side (historical), operation to 10^{34} luminosity with 99% single hit efficiency.
- Staves are mounted inside carbon-fiber half-shells, which clamp to form the layer.

B-Layer Replacement Concept:

Justification:

- With nominal luminosity profile, expect B-layer performance to start degrading after 2-3 years at LHC design luminosity or about 300 fb^{-1} (10^{15} NIEL dose, 50MRad ionizing dose). Expect reduced efficiency and modest reduction in point resolution.
- The performance of the B-Layer has a large impact on ATLAS physics performance, particularly for B-tagging. On the timescale of next several years, expect that improvements in technology should allow construction of a B-Layer with improved segmentation, greater radiation hardness, and reduced material.
- Propose to prepare an upgraded B-Layer for installation during the Winter 2012/ 2013 shutdown, after roughly 4 full years of ATLAS operation.

Alternatives:

- Minimal “upgrade” would be to build essentially identical modules and staves. Expect to acquire enough 0.25µ wafers for FE/MCC to do this if necessary.
- Preferred scenario involves improvements to sensor/electronics design, to module and mechanics geometry, and operations with greater occupancy and total dose.
- Hope for beampipe radius reduction from 29mm to something in the range of 17-25mm (R. Veness, Liverpool meeting). With corresponding reduction in clearances, could optimistically achieve a 30mm B-layer radius.
- Consider either single small R layer, or double layer with R about 30mm and 55mm.

Goals for B-Layer Replacement Program

Principal goals are:

- **Reduction of material**, required to take full advantage of point resolution. This could use a combination of improved power distribution (reduced electrical services) and improved active fraction for the basic modules (closer to 90% rather than the present 71%). Present best estimate for pixel layer now is 2.5% X_0 per layer. Would like to target between 1.5% X_0 and 2.0% X_0 per layer.
- **Improvement of segmentation**, useful to cope with higher occupancy and provide improved point resolution in one or both measurement coordinates. Ideally, would like to reduce pixel area by a factor 2-3. What is the optimal aspect ratio ?
- **Increased radiation tolerance**, both for higher instantaneous luminosity and for higher total dose tolerance. Set nominal goal of a factor 3 increase, leading to instantaneous rate of $1x10^8$ $cm^{-2}s^{-1}$, and a total dose of $3x10^{15}$ neutron equivalent. This is an intermediate step to SLHC, and would be consistent with operation at 30mm radius and the present LHC design luminosity up to SLHC (2016) period.
- **Improved layout geometry:** consider an ambitious geometry upgrade, with an inner measurement at 30mm and an outer measurement at roughly the present B-layer location, based on a highly-integrated double layer.

Possible Implementation Scenarios

Minimal degradation of B-Layer:

- Present estimates of B-Layer lifetime should be conservative, with a number of safety factors. Perhaps as nominal time for B-Layer replacement approaches, very little actual degradation in performance is seen.
- Consider a “low risk” upgrade, involving the insertion of a new fourth layer inside the existing B-layer. Would need to work on new “mini service panels” and develop a model for sharing existing services. This is similar to the CDF “L00” upgrade.

Significant degradation of B-Layer:

- Present estimates of B-Layer exposure or lifetime are optimistic, and the performance of the detector degrades more rapidly than expected.
- In this case, the nominal “higher risk” upgrade would make sense, involving replacement of inner layer, and potential rebuilding of parts of Service Panels.

Significant degradation of other parts of Pixel Detector:

- The infrastructure integrated into the Service Panels is complex, and many scenarios for failures could be imagined, including opto-link failures, electrical connection failures, or cooling problems related to fitting leaks or radiation effects.
- Such failures could significantly reduce the performance of the Pixel Detector, and necessitate replacement of all of the Service Panels.

Corresponding Technical Issues and R&D

Services (11 cooling circuits and 286 module connections):

The B-Layer replacement should be compatible with existing services at the PP1 interface (end of pixel package at +/- 3.5m). **Need to evaluate the real limitations.**

- **HV bias distribution:** limited to about 1KV maximum. However, silicon sensor performance after high doses is limited by trapping, and improvements saturate at about 2-3 V/μ, so the services are well-matched to this limit.
- **LV distribution:** currents cannot be significantly increased with present services and linear regulator approach at PP2. However, implementation of a DC-DC converter approach on-detector could allow providing significantly more current at the 1.2V that will be typical of next generation micro-electronics designs.
- **Cooling infrastructure:** will act as a constraint on any changes. Maximum pressure and mass flow constraints down to PP1 need to be evaluated. Ideally, run colder to limit leakage currents, but evaporative systems with lower temperatures imply higher worst-case pressures (C2F6 about 30bar, CO2 about 60bar).
- **Fiber infrastructure:** all multi-mode, and a mixture of rad-hard SIMM and commercial GRIN fiber. Tests indicate bandwidth is OK to above 1Gbit/s.
- **From PP1 inwards:** should change service panels and/or opto-boards ? Not trivial since the 2-hit staging re-design placed the “staged” parts (middle disk and L1) on the ISP, instead of the B-layer as originally designed. Parts that would need changing are distributed, so disassembly/re-assembly of Service Panels needed !

Near-term Workplan: develop "core technologies" needed

Sensors:

- Assume n+ on n as baseline technology, but 3D offers much better signal above 10^{15} doses, and "active edge" design for improved integration. Push commercial production, assess performance with present FE-I3 electronics, and explore impact of higher capacitance on new FE design (mainly a power/current issue).

Micro-electronics:

- Develop new FE design in 130nm IBM CMOS that addresses a number of key issues. These include: larger FE array, larger fraction of die area as active pixels, more functional integration to simplify services, optimization of analog FE and readout architecture for higher dose and higher occupancy.

Integration:

- Explore integration of either single-chip modules, or 4-chip modules onto highly integrated stave structure. In this case, all interconnections and services would be integrated into mechanical structure, supporting advanced power distribution.

Opto-links:

- Explore more highly integrated, and higher bandwidth, optical links. These are needed to deal with higher occupancies, but could also be tailored to highly integrated stave concept, and next generation TTC/Data architecture (GBT).

Power distribution:

- Explore engineered solutions involving either serial power approaches or DC-DC converters. Build prototype electronics blocks to evaluate use in stave.

Logistics:

- Carry out detailed studies of different scenarios for removing and replacing components of the Pixel Detector. Emphasize activation issues and schedule/risk issues of disassembly/assembly operations. Use this information to drive scope and planning for replacement conceptual design.

Mechanics:

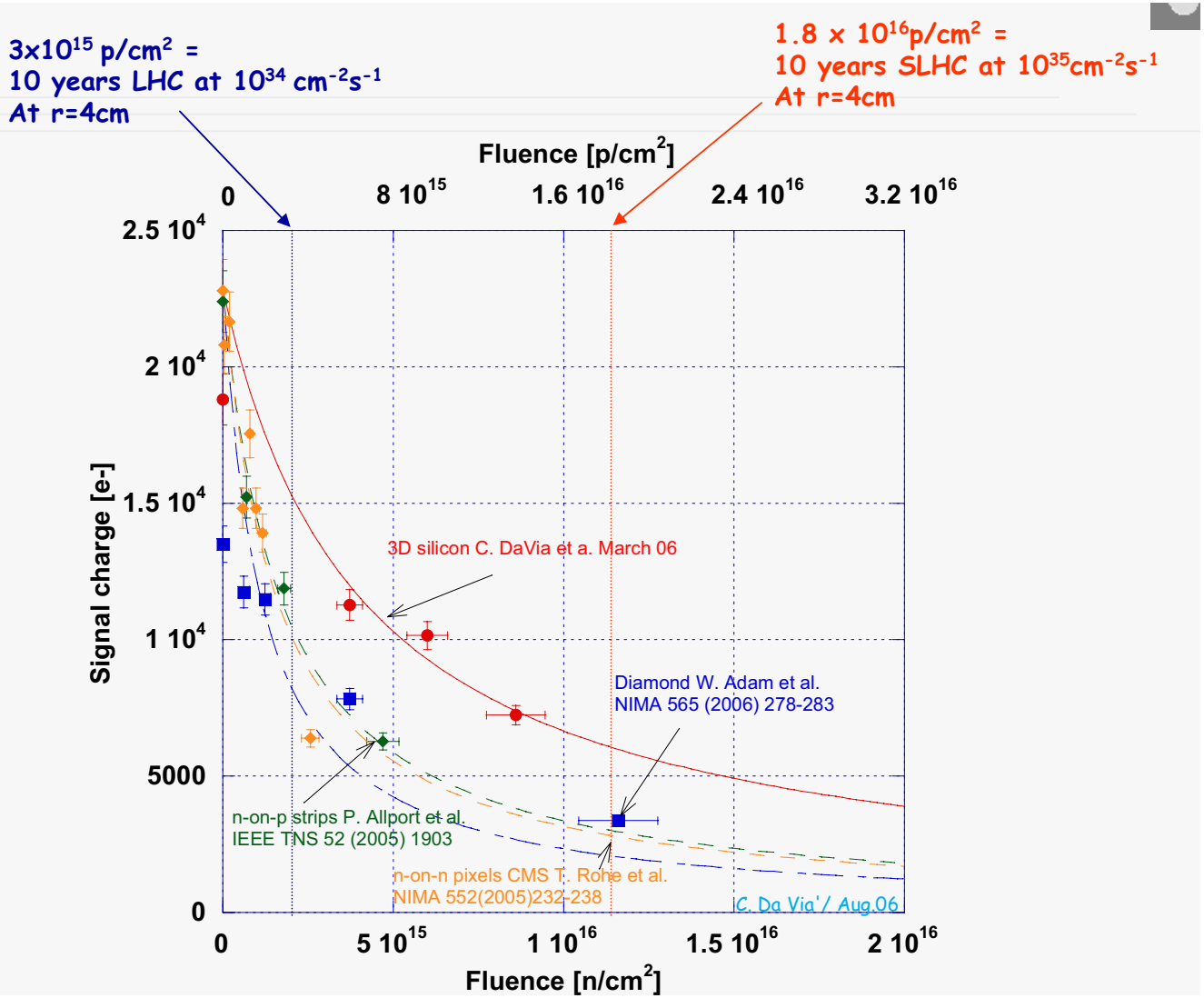
- Explore issues related to highly integrated stave, as well as integration with smaller radius beampipe.
- Note that final decision on minimum beampipe radius would probably not be taken before 2009, so it is critical that we have a flexible concept.

Initial Strategy:

- All of the above efforts are initially rather independent of the detailed design of the B-layer replacement. Progress can therefore be made in 2008 and even 2009 in these core areas while the overall design of the replacement continues to evolve.

Sensor Development Plan:

- Basic goal: **increase total dose tolerance by a factor 3**. Baseline would use present sensor design, but its marginal (sensors limit present B-layer lifetime):



Compilation: C. Da Via.

Predicts 15Ke signal after 10^{15} NIEL for n+ on n sensors (agrees with our irradiations).

Same sensors would have only about 7Ke signal left after dose of $3x10^{15}$ NIEL.

Note 3D sensors (70µ gap) predicted to have 13Ke after same dose, and 7Ke after 10^{16} NIEL!

ATLAS 3D group working with SINTEF and IRST

- Noise and Timing measurements with FE-I3 are ongoing and interesting.

FE Development Plan:

- **Fix geometry of FE chip:** assume 50μ pixel pitch, and pixel length is 200-250μ. Size the chip for the present module dimensions, but use 4 FE chips to cover one module. This gives a die of roughly 16mm width and 19mm height, with approximately 64-80 columns and 320 rows of pixels, for 20-25K pixels/FE chip).
- Could foresee single-die modules with active edges as natural 3D implementation, or four-die modules with present 10 cm^2 active area for planar sensors (which require large guardring structures for HV operation). A single chip would work for both using metalization to alter input transistor and biassing range (done in FE-I3).
- **Develop new analog FE design:** already well underway with most recent LBL submission, with further areas of development in minimizing power, optimizing space, and evaluating cost/benefit for charge measurement.
- **Develop new Readout Architecture:** for higher occupancy, and larger column length, a new readout approach is needed. Expect this to require distribution of functionality in present EOC buffers in a heirarchical manner throughout the pixel array. A complex integration challenge. Present chip is limited above about $3x10^7$ hits/cm^2, and uses one buffer for every 5 pixels. Scaling to new architecture not yet clear, but will surely require more buffering per pixel.
- **Optimize layout rules:** try to avoid full “gate all around” approach, in particular to allow use of commercial standard cells, and to improve storage cell density. This is risky for the highest doses, so requires extensive validation with irradiations.

Overall System Design and Prototyping:

- Need to define functional blocks and their interfaces in overall system (FE chips, controller/optolink chips, power distribution chips) to allow development of useful prototypes.
- **Power distribution:** efforts on Serial Powering and on DC-DC converters are critical, and need to converge to a useful power distribution architecture. Ideally, the required infrastructure would naturally integrate with stave electrical bussing and cooling. DC-DC converter approach fits naturally with the present PP2 system and grounding scheme, but serial powering potentially offers greater reductions in services burden.
- **Clock/control/data distribution:** efforts on next generation optical interfaces are proceeding. Need to define clock distribution (40 MHz, or much higher ?), TTC protocol, and data transmission protocol. Link bandwidth will determine amount of "data concentration" required. Ideally, would collaborate with common developments for SLHC, using B-Layer replacement as "first generation prototype". Again, look to integrate this infrastructure naturally into stave.

Schedule

Overall Schedule:

- Began development in 2004, after completing existing FE-I3 production pixel chip.
- Model for B-Layer Replacement assumes a lifetime of about 300 fb-1, after which significant signal loss in sensors begins to have an impact.
- Assume such luminosities could be accumulated over high-luminosity runs in 2010-2012, and therefore natural schedule is to replace in 2012/2013 shutdown.
- The replacement operation is complex, and will involve significant work around highly activated components (and risk of damage to other elements of detector).
- Minimum estimated replacement time is about 6 months, and realistically, it could be closer to 8 months. This is probably not a standard “annual” shut-down.

Provisional Milestones (in collaboration with ATLAS PO):

- Define key parameters by Oct 07 (pixel and FE chip geometry), hold R&D Review
- Test submissions in early 07 and 08, and finalize sensor choices (e.g. planar versus 3D), then build engineering run of full-scale chip by early 09.
- Evaluate modules built with prototype FE chips and sensors in 09.
- Overall B-Layer Replacement TDR in July 09, FE Electronics PRR in Mar 10.
- Already an aggressive schedule for significant development, so fall-back is always to go ahead with something quite close to the present B-layer design.

Funding Plan

General concept:

- The B-Layer has a moderate lifetime due to its proximity to the beam. It is therefore a “consumable” in ATLAS, and its replacement is part of the M&O B line for pixels.
- This means that the replacement “project” remains under the Pixel Collaboration, and that the corresponding funding should come from Pixel FAs, including new members of the Pixel Collaboration.
- This plan was built into the M&O B profiles for ATLAS, that presently extend through 2010. However, there have been a number of developments since then, including extra costs within ID and Pixels, which will also need to be “paid back” on a similar timescale. There is no detailed plan for operations requirements for pixel M&O B in the period 2009 - 2012, so the integral of all needs is not well-known.
- It was also assumed that there would be modest amounts of R&D (emphasis on D) before starting construction. Construction would start with the equivalent of “Module 0” in ATLAS, meaning pre-production fabrication runs for sensors and micro-electronics.

Tentative Scope and Profile:

- Cost for present Pixel Detector was 15.5 MCHF CORE (which eventually became a more complex mixture of CORE and deferrals due to “staging” of pixel system).
- B-Layer replacement estimated in the range of about 3-4 MCHF CORE-like cost with initial scope, assuming no major rework or replacement of Service Panels.
- Schedule Plan just described would start the flow of M&O B funding in 2009, with expenses extending over a 4 year period through 2012, at about 1 MCHF per year.
- Meanwhile, R&D funding is already supporting significant progress in 3D sensors and in 130nm CMOS FE development. Based on present technical progress, it should be possible to make pre-production fabrication runs in early 2009.

Major Question:

- Given that the schedule is somewhat compressed, and the cost is somewhat increased, does this replacement plan fit inside of the Pixel M&O B line ?
- Expect that the answer to this question may depend on the FA involved, and the other calls on M&O funding in the same timeframe.

Possible CORE-like Funding Profile (no SQP fabrication):

(units = 2008 CHF)	2009	2010	2011	2012
Sensors	150K	500K	500K	
Electronics	550K	275K	275K	
Modules	100K	200K	500K	300K
Off-detector and Opto-links	50K	100K	200K	200K
Mechanics	100K	150K	200K	
Service Panels				
Total = 4.35MCHF	950K	1225K	1675K	500K

- Sensors assumes pre-production run in 2009 and 500 wafer production run in 2010/2011 at 2K/wafer and 33% yield (double cost and half of yield).
- Electronics assumes 12 wafer engineering run in 2009 and 150 wafer production run in 2010/2011. Prices are 2008 8M, and production assumes yield of 20%.
- Modules assumes initial pre-production bumping in 2009/2010, and bumping cost of 2K/module for 500 modules in production.

Roles played by US in Current Pixel Project:

- Sets the stage for expected roles in upgrades, and possible priorities for US group contributions as seen from ATLAS side.

Sensors:

- US played a contributing role in sensor testing, but development was done in Europe. This looks likely to continue in the future.
- Critical role played in early prototyping by close collaboration between sensor designers and FE designers. This is now underway with LBNL and 3D groups.

Electronics:

- US (LBNL) played lead role in FE chip design and integration, as well as providing test system for all lab and production testing. No other pixel institution has a real IC design team, so this remains an essential role for upgrades.
- US (LBNL) played lead role in off-detector electronics (design of major blocks was either done by LBNL/Wisc or UK-SCT groups). Again, no other institute has equivalent board-level capability to that of LBNL. Also, Pixels relied heavily on SCT for BOC (off-detector opto), so additional help would be needed for upgrading.
- US (OSU) played leading role in on-detector opto-links. Not clear how to proceed with this in the future - non-pixel US collaborators like SMU could play a role, or CERN opto group could play a role. Investigating using B-Layer replacement as a “prototype” for common opto design centered at CERN - architecture is interesting.

Modules and services:

- US (LBNL and OU) played a large role in developing module and electrical services concepts. Would be natural for this to continue for upgrades. Note this could be largely a development role, and would be tightly coupled to the stave concept.

Local Mechanical Supports:

- US (LBNL) led this area for the disks. European development for barrel was more complex and problematic, involving joint development by CPPM, Genova, and Wuppertal, under leadership of M. Olcese. Major re-build required due to pipes.
- At the present time, the European effort is very weak in engineering, but new groups like NIKHEF or Geneva could change this.
- An improved module/stave effort would be natural collaboration between experts at LBNL and European groups. Leverages ongoing large-R stave effort at LBNL. Very skeptical of success without the US (LBNL) as an anchor of competence.

Global Supports:

- For barrel, this work was done under contract to IVW in Germany. For overall support, this work was done under contract to Hytec in US.
- In the future, it might be most natural for this work to be taken up by the ID Project Engineer (Andrea Cattinacio) and a team at CERN, more tightly coupled to the machine and the overall ID engineering.
- This would require transfer of integration and installation knowledge to CERN.

Next Steps:

- Pixel Collaboration setting up an Upgrade organization to oversee both B-Layer replacement, and SLHC upgrade R&D. Initial overall coordinator expected to be Giovanni Darbo. Need to begin work on overall architecture, create working groups, and work on proposals.
- Sensor effort on 3D now organizing under Cinzia Da Via and Giovanni Darbo. This is targeted at SLHC, but with the B-layer replacement as an initial goal.
- Specific effort on new FE chip for B-layer replacement is starting up under Darbo, myself, and Maurice. Contributing groups outside of LBL expected to include Bonn/ Mannheim, CPPM, Genova, and NIKHEF. First mapping of roles is proposed and will be discussed in a general phone meeting next week.
- First draft workplan for the FE chip effort is almost ready for distribution, with Maurice as editor. Will use this document to organize efforts at contributing institutes.
- Next document to work on will be overall conceptual design of electronics, functional blocks, and system architecture.
- This effort will gain more momentum once the present detector is installed and into a commissioning phase by later this year.