Introduction

- Welcome to Berkeley Lab
- The purpose of this meeting is to:
  - Review the US stave based tracker R&D program
  - Discuss mechanical support issues
  - Discuss R&D plans for the near future
  - Organize efforts on DAQ to enable stave testing
  - Order lunch
- Participants
  - Berkeley: stave R&D electrical, mechanical, DAQ
  - BNL: mechanical support and testing, DAQ, sensors
  - Yale: new effort, interest in assembly
  - Santa Cruz: electronics, DAQ
  - SMU: optical data transmission

Introduction cont.

- Tuesday:
  - Mechanical discussion
  - DAQ discussion, in parallel, in the lab
- Wednesday
  - DAQ discussion

Tuesday Agenda

• Intro	Carl Haber	45 + 15	60	8:30
• Project Office + Layout	Dave Lissauer	35 + 10	45	9:30
• *Break*				10:15
• Stave Engineering	Bill Miller	60 + 20	80	10:30
• Local Plans and Status	Gil	20 + 10	30	12:00
• BNL Stave Study	Margareta	10+5	15	12:30
• Lorentz Angle Issue	Anatoli	15	15	12:45
• *Working Lunch*				1:00
• Space Frame	Anatoli	45+15	60	1:30
• Stave Attachment	Anatoli	30 + 15	45	2:30
• BNL Measuring System	Dave Lynn	15+5	20	3:15
• *Break*				3:45
• Visit to AAR Composites	Dave Lynn	15	15	4:00
• Robotics	Paul	30	30	4:15
• Discussion				

Wednesday Agenda

• Intro	Carl	45 + 15
• LBL effort	Tim	45 + 15
• BNL effort	Hucheng	
• Yale effort	Paul	
• Report on Tues discussion	Tim / Hucheng / Andrew	
• Opto	Jingbo	

Liverpool Meeting and Beyond

- Dec 6-8 Tracker Upgrade meeting held in Liverpool - review
- Early 2007 new developments in occupancy calculations
- Lead to strawman for tracker layer configurations being the most aggressive choice


ATLAS High Luminosity
Upgrade
Tracker
Workshop
Conference Coordinator
Mrs Jackie Sharp
j.sharp@liverpool.ac.uk
Tel: (0044)151-794-3363
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High Energy Physics Group
Department of Physics
University of Liverpool
Liverpool L69 7ZE UK
Liverpool
6th – 8th December 2006
Web page: http://www.liv.ac.uk/physics/AHLUTW

Sessions

- Working groups
- Organization
- Layout and Simulation
- Module Integration
- Engineering
- Sensors and Electronics
- Services Irradiation and Wrap Up

Working Groups

- ATLAS has established a set of working groups to look at specific tracking issues
- 3D Sensors (Darbo)
- Thermal management (Viehauser)
- Electronics (Farthouat)
- Modules (Allport)

Organisation (14:00->15:30)			Chairperson: Marzio Nessi (*CERN*) Location:
14:00	Welcome and Introduction (10') (Slides)		Phil Allport (*U. of Liverpool*)
14:10	Summary of LHC Proposals (20') (Slides)		Per Grafstrom (*CERN*)
14:30	Project Office Report (25') (Slides)		David Lissauer (*Department of Physics*)
14:55	Review Office (15') (Slides)		Mike Tyndel (*Particle Physics*)
15:10	Steering Group Report (20') (Slides; Slides - original; Slides - ppt)		Nigel Hessey (*NIKHEF*)

Important Milestones - ID

- Ready for beam: 1/1/2016
- Beam off – start decommissioning 7/1/2014 (18 month for installation)

- Straw man Layout - 12/31/2006
  - → (Modification/changes to be made in term of performance /Risk/Cost etc.)
- **TDR - Feb/2010**
- Cooling PRR April/2010
- Mechanical Support Design complete Oct/2010
- Sensor PRR July/2010
- FE-electronics Sept/2010
- Surface Assembly March/2012
- Ready for Installation August/2014
- Barrel Installation Feb/2015
- B-layer/beam pipe August/2015

Conceptual Design R&D

Prototypes

Pre-series

Production

Assembly& Installation

ID Layout

- Layout Advisory Committee has been set up
  - Tasks:
    - Develop list of performance goals, "Straw man" layout with list of options, and evolve it to "Baseline layout"
    - Advise USG and PO on layout matters
  - Membership
    - Chaired by me
    - Representatives of different parts of ATLAS detector, experience, funding, geography
- Layout Group
  - Anyone working on layout matters
  - Simulation etc.
- Developed a document on performance goals, definition of straw man, and options

Nigel Hessey

Advisory Committee:

Phil Allport
Allan Clark
Mogens Dam
Nanni Darbo
Juan Fuster Verdu
Mauricio Garcia-Sciveres
Nigel Hessey
David Lissauer
Marzio Nessi
Pavel Nevski
Richard Nisius
Ulrich Parzefall
Leonardo Rossi
Steinar Stapnes
Jeffrey Tseng
Mike Tyndel
Yoshinobu Unno
Dirk Zerwas
Alexander Rozanov
Abe Seiden
Norbert Wermes

Tracker R&D Proposals

- Approved by EB:
  - Opto-electronics, ABC-Next, Radiation background
- Approved by USG and to be sent to CB:
  - Staves, Strip detectors, SiGe
- Expressions of Intent received:
  - 3D sensors, Modules, Powering, Gossip, High-rate Straw Tracker, Thin 3D pixels, Silicon-on-Sapphire

Parameters of the SLHC

- Key issues are
  - Luminosity ~3000 fb-1
  - Bunch structure
    - Timing 12.5, 25, 50 ns
    - Technical feasibility in LHC
    - Lengths
    - Total and peak L
    - Interactions per crossing
    - LHC Magnetic elements
    - Effect on machine operation, RF

Heat load

zoom on heat load

parameter	symbol	nominal	ultimate	12.5 ns	25 ns, smaller β*	50 ns, long
SR heat load 4.6-20 K	P_{SR} [W/m]	0.17	0.25	0.5	0.25	0.36
image current heat	P_{IC} [W/m]	0.15	0.33	1.87	0.33	0.78
total BS heat load w/o e-cloud	$P_{SR} + P_{IC}$ [W/m]	0.32	0.58	2.37	0.58	1.14
local cooling limit*	P_{cool} [W/m]	2.4	2.4	2.4	2.4	2.4
cooling remaining for e-cloud	$P_{cool,\ rest}$ [W/m]	2.08	1.82	0.03	1.82	1.26
simulated e-c heat for SEY=1.4 (1.3)	P [W/m]	1.07 (0.44)	1.04 (0.6)	13.34 (7.85)	1.04 (0.59)	0.36 (0.1)

* L. Tavian, LUMI'06

Not feasible **OK**

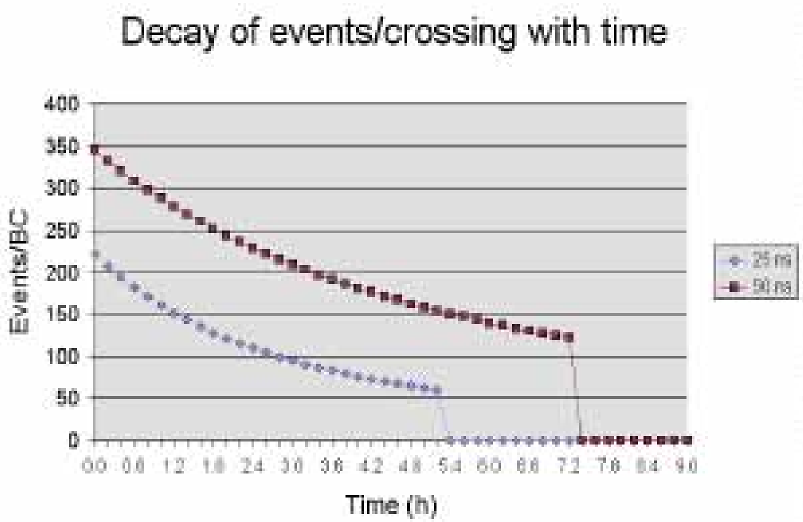
P.Grafstrom

Hardware needed for these two scenarios

- 25 ns small ß (8 cm)
  - New triplet with bigger aperture (L* =23m)
  - Small angle crab cavity (~100 m from IP)
  - D0 needed
  - If NbTi technology Qo is needed
  - If Nb_3Sn technology no Qo needed
- 50 ns long bunch
  - New triplet with bigger aperture (L*=23 m)
  - No D0 needed
  - Both NbTi and Nb_3Sn possible without need for Qo
  - Wire compensation needed (~100 m from IP)

Further comparison (Nigel Hessey)

	25 ns small ß	50 ns long bunch	25 ns small ß'
Peak lumi:	$15.5\ 10^{34}$	$8.9\ 10^{34}$	$11.7\ 10^{34}$
Events crossing:	296	340	223
Lumi. Life time:	2.1 h	5.3 h	2.8 h
Effective lumi:	$3.6\ 10^{34}$	$3.1\ 10^{34}$	$3.1\ 10^{34}$



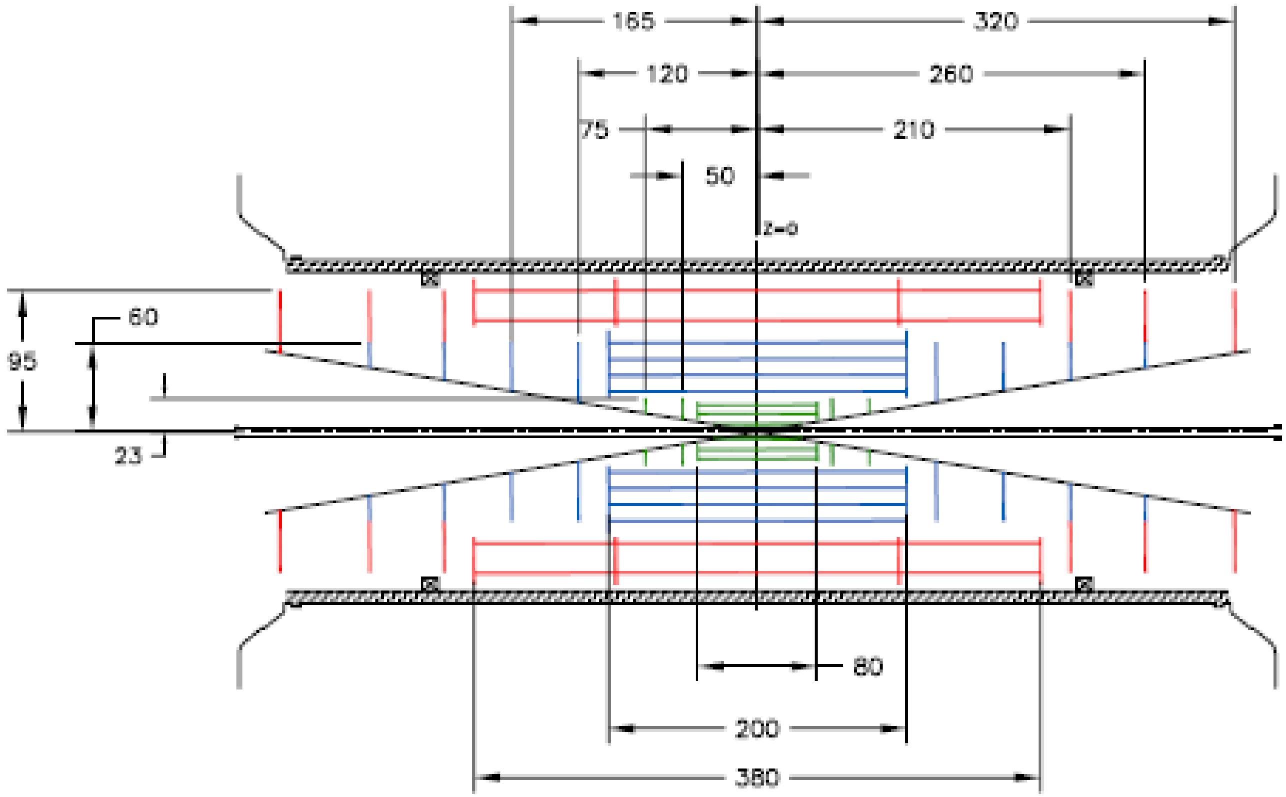
Nigel version for "honest" comparison
ß from 8 cm to 11 cm
(turnaround 5 h)

Layout and Simulation (16:00->17:45)

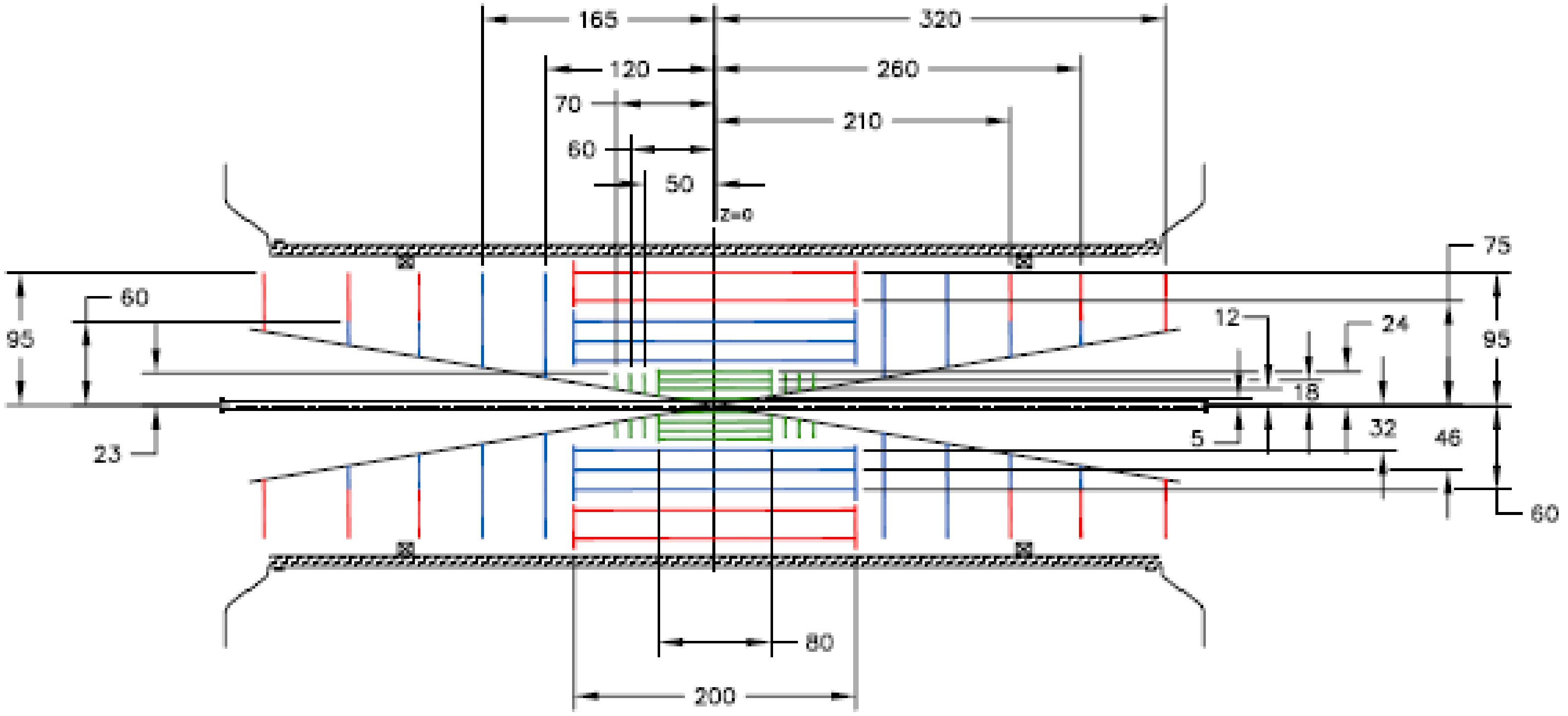
Chairperson: Nigel Hessey (*NIKHEF*)
Location:

16:00	**Layout Options** (25') (Slides)	Abraham Seiden (*University of California*)
16:25	**Layout Software Update** (15') (Slides)	Jeffrey Tseng (*Nuclear Physics Laboratory*)
16:40	**Lessons from b-tagging Performance of ATLAS Pixel Layout** (15') (Slides)	Alexandre Rozanov (*Faculte des Sciences de Luminy*)
16:55	**Vertexing with Inner Detector** (15') (Slides)	Vadim Kostyukhin (*Istituto Nazionale di Fisica Nucleare (INFN)*)
17:10	**ATLAS Inner Tracker Layout Studies for the SLHC Based on FATRAS** (15') (Slides)	Oliver Kortner (*Max-Planck-Institut für Physik München*)
17:25	**EndCap Layout** (20') (Slides)	Carmen Garcia (*Instituto de Fisica Corpuscular (IFIC) UV-CSIC*)

ID Strawman Layout 3+4+2 (P+SS+LS)



SS/LS FIXED LENGTH



Layout Issues

- Overall configuration
- Long/short barrels
  - Projectivity
  - Assembly and integration
- Disposition of layers – Key issue for specific R&D on tracker concepts

Module Integration Session (08:30->13:00)

Chairperson: Phil Allport (*U. of Liverpool*)
Location:

08:30	**Multi-Chip-Modules Deposited Experiences Made in the R&D Phase of the ATLAS Pixel Detector** (20') (Slides)	Tobias Flick (*Bergische Universitaet Wuppertal*)
08:50	**Wafer Level System Integration** (30') (Slides)	Ehrmann
09:20	**Pixel Module Concepts** (20') (Slides)	Mauricio Garcia-Sciveres (*Physics Division*)
09:40	**R&D for a Novel Pixel Detector for the SLHC** (25') (Slides)	Hans-Günther Moser (*Max-Planck-Institut*)
10:05	**GOSSIP: A New and Potentially Better Vertex Detector for ATLAS** (25') (Slides)	Harry Van Der Graaf (*NIKHEF*)

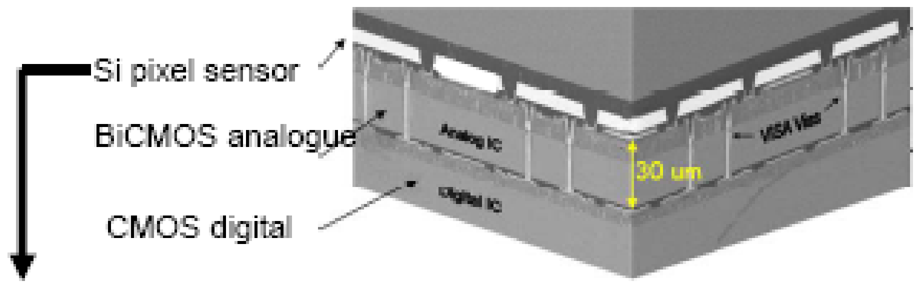
Implication for advanced strip layer designs as well

H.-G. Moser
Semiconductor
Laboratory
MPI for Physics,
Munich

R&D for a novel pixel detector for SLHC

3D interconnection (sensor – electronics; electronics – electronics):

Alternative to bump bonding (fine pitch, potentially low cost?).
New possibilities for ASIC architecture (multilayer, size reduction).
Optimization of rad. hardness, speed, power.
Impact on module design (ultra thin ASICs, top contact, 4-side buttable).



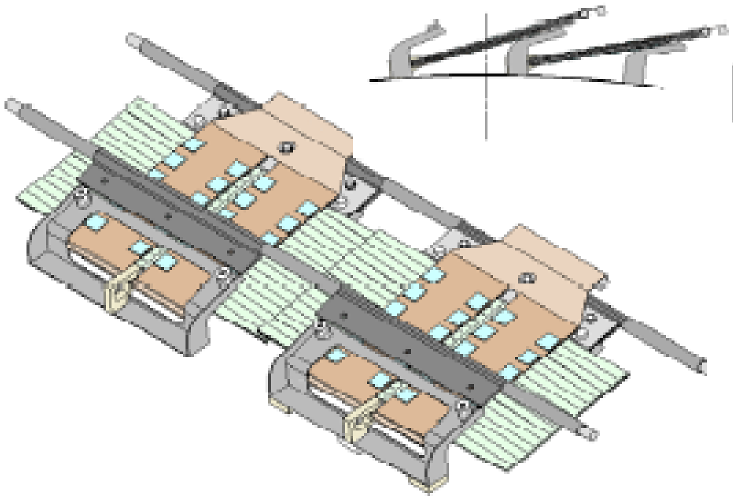
R&D on thin (O(50µm) FZ silicon detectors:
Based on well known pixel sensor technology.
Can be operated at 10^{16} n/cm^2 (V_{dep}, I_{leak}, CCE).

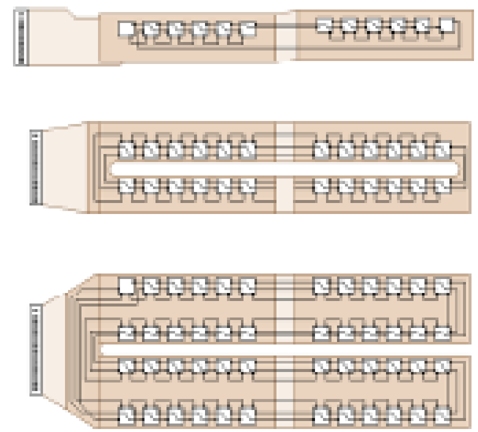
Can lead to an advanced module design: rad hard with low material budget

ATLAS High Luminosity Tracker Upgrade Workshop, Liverpool, 6-8 Dec 2006

Module Integration Session (08:30->13:00)		Chairperson: Phil Allport (*U. of Liverpool*) Location:
11:00	Module Development for ATLAS/SLHC (25') (Slides)	Yoshinobu Unno (*KEK*)
11:25	Stave Concept (25') (Slides)	Carl Haber (*Lawrence Berkeley National Laboratory (LBNL)*)
11:50	Negative Charge Measurements with ATLAS SCT Readout (15') (Slides)	Peter Kodys (*Charles University*)
12:05	Interconnects, Packaging and Power (25') (Slides)	Marc Weber (*Rutherford Appleton Laboratory*)
12:30	Serial Powering R&D for Pixels: Status and Plan (15') (Slides)	Markus Cristinziani (*Physikalisches Institut*)
12:45	Power Delivery of Low Voltage and High Currents for the SLHC ATLAS Tracker (15') (Slides)	Satish Dhawan (*Yale University*)

SLHC Module - A Proposal

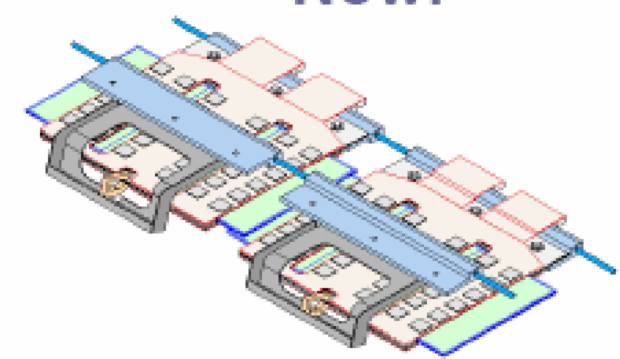


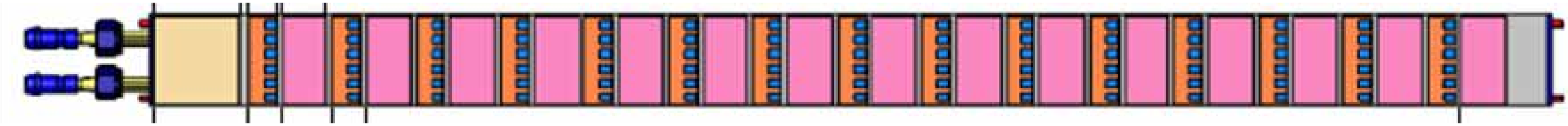


- Presented at the Oct. workshop at CERN
- One module with 124x64mm² sensor
  - Segmented into 1, 2, and 4 striplets
  - Wrap-around hybrids with 1, 2, and 4 rows of ASIC's

Y. Unno, ATLAS Tracker Upgrade Workshop@Liverpool

Now:





Integrated Structures

- Alternative to individual rigid modules on a rigid support: "super-modules" (or "staves") plus end-plates*.
- Minimize heat flow path lengths
- Eliminate mechanical redundancy
- Integrate support, cooling, electrical services
  - Increased integration implies decreased material
- Assembly sites build, test, & deliver these units
  - Final assembly is simplified
- Include alternative powering schemes – reduce services
- Create higher-value elements & assume greater risk

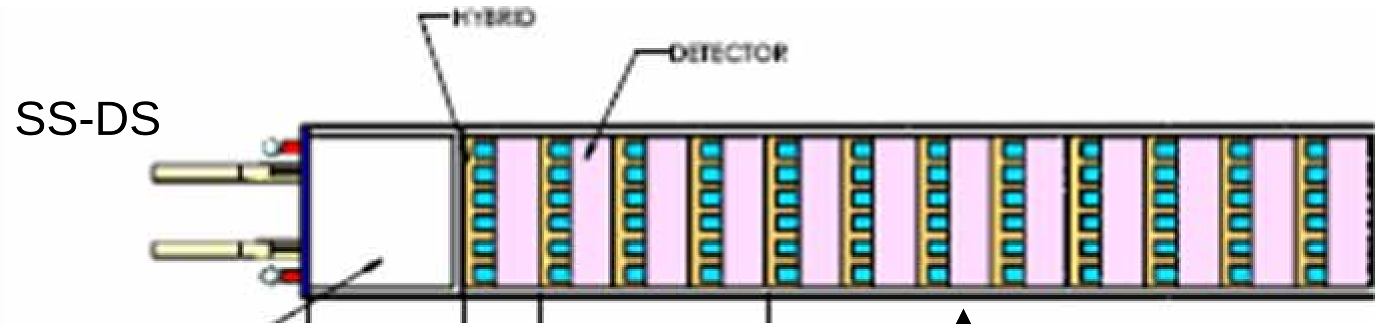
*see presentation of D.Lynn and other layout discussions

General Point

- The basic ideas
  - Eliminate mechanical redundancy—no standalone modules
  - Minimize cooling paths
  - Less rework/repair capability
  - More common use of electrical services

Are not wed to long structures (which are natural only in the barrel). In the forward perhaps a more natural variant are <u>super disks or sectors</u>

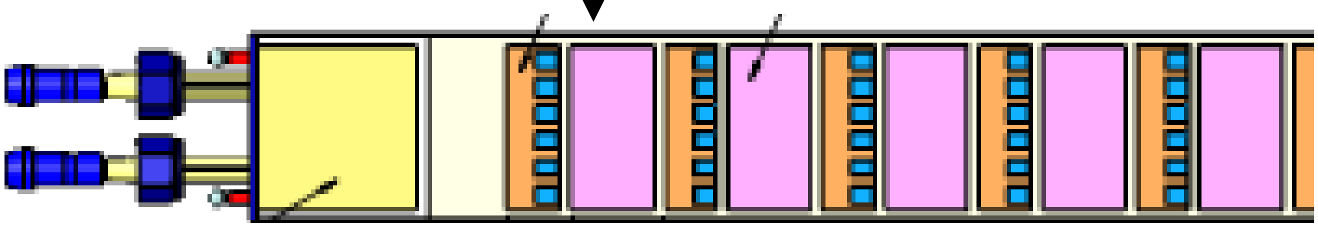
SS-DS



1 meter,
<u>Double sided</u>,
3 cm strip,
32 modules/side
192 Watts
2.5 % Xo

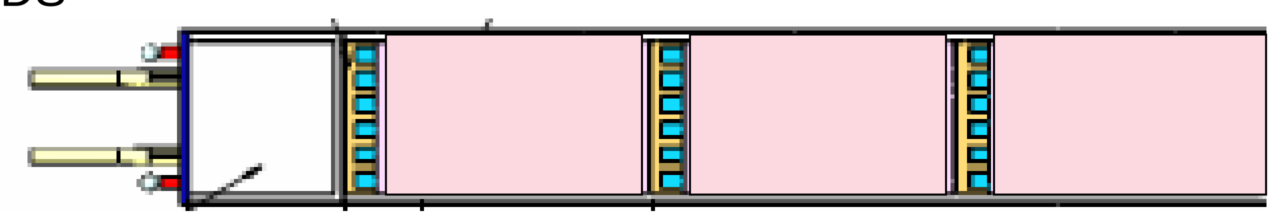
Naturally accommodate double sided (stereo) or singled sided short sensors

SS-SS



1 meter,
<u>Effective single sided,</u>
3 cm strip,
15 modules/side
108 Watts
1.7 % Xo

LS-DS



2 meter,
<u>Outer tracker,</u>
<u>Double sided,</u>
12 cm strip,
8 modules/side
1.7 % Xo

Mechanical Support for Barrel Staves

D. Lynn, BNL

BNL Mech Group

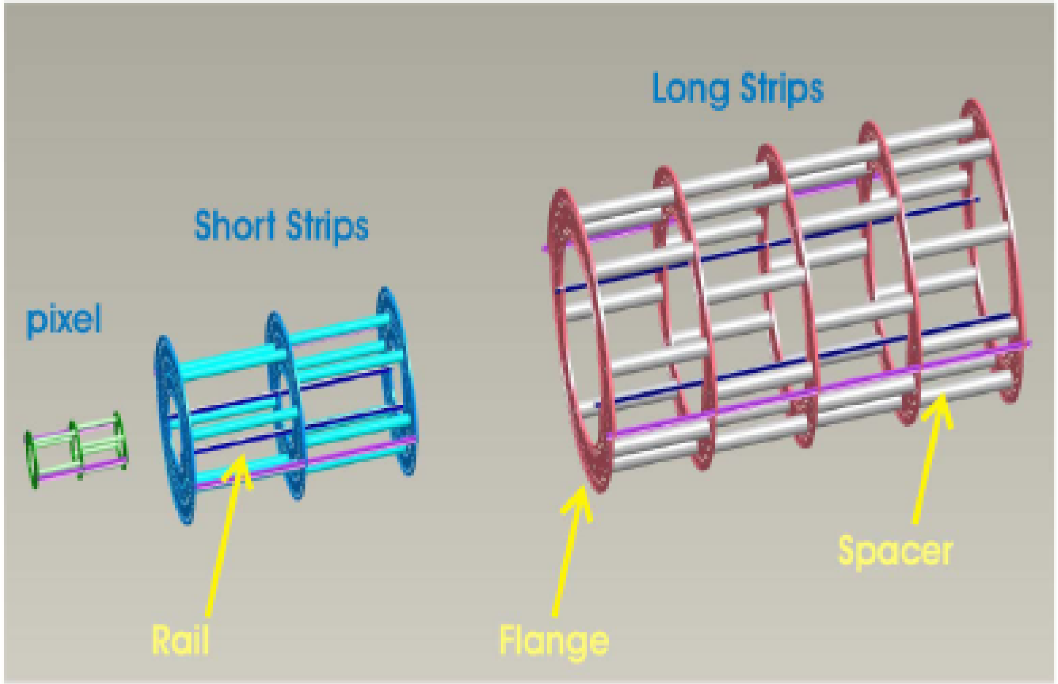
Burns, R., Duffin, D., Gordeev, A., Farrel, J., Hoffman, A., Lissauer, D., Rahm, D., Rehak, M., Semertzidis, Y., Sexton, K., Sondericker, J.

In Collab with LBNL

Gilchriese, M., Haber, C., Miller, B.

Currently Investigating a "Space Frame Approach"

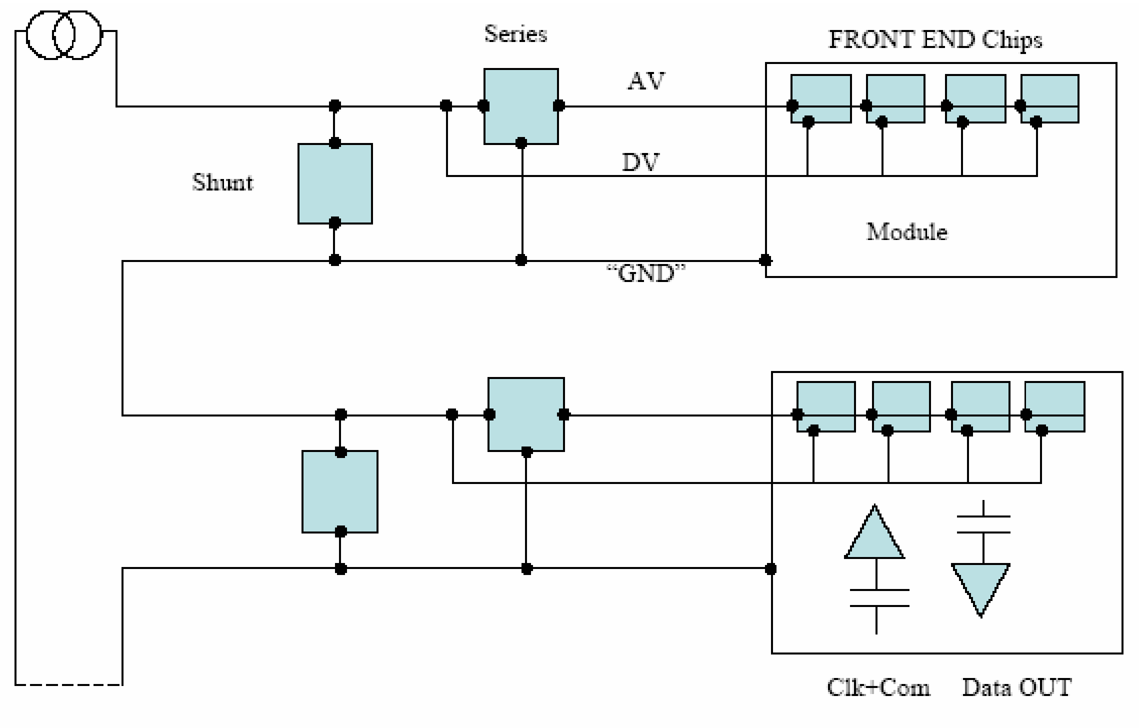
- Short strip and Long strip flanges spaced 1 meter apart
- Pixel Flanges 40 cm apart
- Each sub-frame allows independent assembly of LS/SS/Pixel Barrels

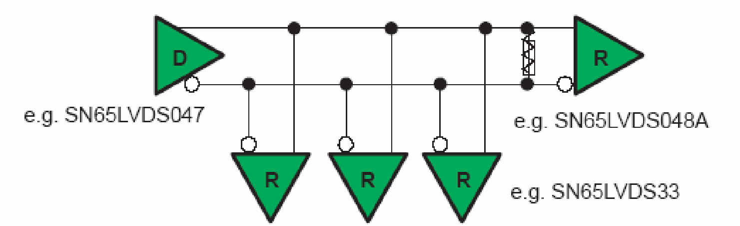


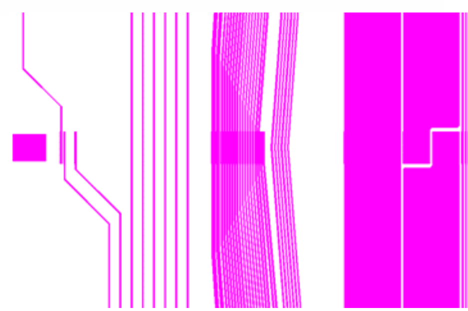
Powering

- Serial and DC-DC conversion powering schemes promise to reduce services dramatically
- See talk of M.Weber for quantitative comparisons
- Active R&D in pixel community, here, RAL,Yale on these issues
- Serial powered stave under test at LBL

Serial Powering Configuration







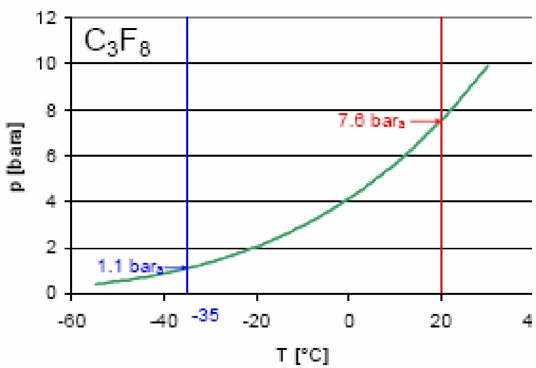
Engineering (14:00->17:40)		Chairperson: David Lissauer (*Department of Physics*) Location:
14:00	**Beampipe Radius for the ATLAS B-Layer Upgrade** (20') (Slides)	Raymond Veness (*CERN*)
14:20	**An R&D Proposal for New Carbon Fibre Concepts to Simplify and Optimize the Thermal Management and Mechanical Design in the SLHC Pixel Detector** (20') (Slides)	Peter Mattig (*Physikalisches Institut*)
14:40	**ATLAS - Barrel Constructions - Lessons** (25') (Slides)	Eric Perrin (*Section de Physique*)
15:05	**EC - Mechanical Constructions** (25') (Slides)	Patrick Werneke (*NIKHEF*)
15:30	TEA	
16:00	**Mechanical Support for Barrel Staves** (20') (Slides)	David Lynn
16:20	**Summary of Thermal Management Working Group Meeting** (30') (Introduction to Coolants)	Georg Viehhauser
16:50	**Assembly, Integration, Safety and Risk Management** (30') (Paper)	Heinz Pernegger (*CERN*)
17:20	**Development of Involute Laminates for Integrated Module Support and Thermal Management** (20') (Slides)	Eric Anderssen (*Lawrence Berkeley National Laboratory (LBNL)*)

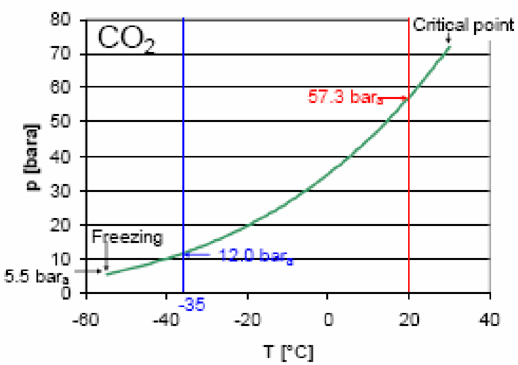
Cooling

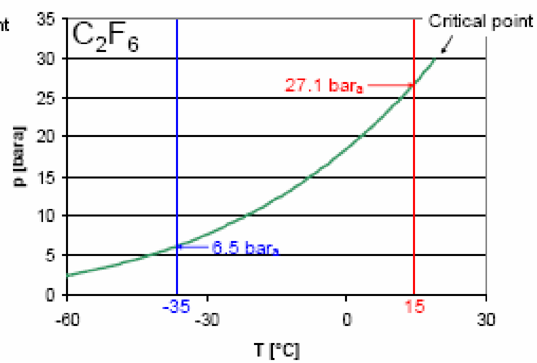
- Lower temperature operation required
  - T silicon SCT would be -25 C
  - Coolant is how much colder?
- Need to reuse much of existing pipes
- Present coolant C3F8 is very very marginal at SLHC – pressure to low
- Prime candidate is CO_2 with very high pressure operation

Possible candidates

- C_3F_8:
  - Used in existing system → experience,
  - Low pressure.
- C_2F_6:
  - Similar, but allows to cover low temperatures.
- CO_2:
  - Low temperatures.
  - High pressure.
  - Low mass flows.
  - Experience in LHCb, AMS, industry.







Jumping the gun…

Two (maybe 3) candidate fluids: C_2F_6, CO_2 & (maybe still) C_3F_8

A few pros and cons:

C_2F_6: Enthalpy ~ 100J/g, P_{evap}~ 4 bar_a @ -45°C, T_{crit} ~ 20°C
Liquid delivery pressure in warm zones ≥ 30 bar

CO_2: Enthalpy ~ 280J/g P_{evap} ~ 7 bar_a @ -45°C, T_{crit} ~ 30°C
Higher evaporation pressure → higher HTC
Triple point temperature ~ -56°C (dry ice formation)
Liquid delivery pressure in warm zones ≥ 70 bar

C_3F_8: Enthalpy~100J/g, P_{evap} < 1 bar_a*@ -45°C, T_{crit} ~ 60°C
* low evaporation pressure needs special treatment

Critical point issues

CO_2: T_{crit} = 31.1°C, C_2F_6: T_{crit} = 19.7°C.
Non-isolated feed lines → in contact with warmer temperature source.

Two possible issues:

- Compressible bubbles in feed line.
- Around critical temperature (in particular above) large $(dh/dT)_p$ → less cooling power after expansion (without pre-cooling).

G.Viehhauser

Sensors and Electronics (08:30->13:00)

Chairperson: Nanni Darbo (*Universita degli Studi di Genova Dipart. di Fisica*)
Location:

08:30	**Summary of FE Electronics** (30')	Philippe Farthouat (*CERN*)
09:05	**Towards a Next Generation Pixel FE Chip** (30') (Slides)	Kevin Einsweiler (*Lawrence Berkeley National Laboratory (LBNL)*)
09:35	**ABC - Next Status Report** (30') (Slides)	Wladyslaw Dabrowski (*AGH Univ. of Science & Technology Phys.&Appl.Comp.Sc.*)
10:05	**Radiation Hardness Evaluation of the Silicon on Sapphire Technology and the Design of the Link-on-Chip** (25') (Slides)	Jingbo Ye, Ping Gui (*SMU*)
10:30	COFFEE	
11:00	**3D Status and Summary** (30')	Cinzia Da Via' (*Brunel University*)
11:30	**Preliminary Results with Miniature Microstrip p-type Detectors after Neutron Irradiation to SLHC Doses** (15') (Slides)	Gianluigi Casse (*Department of Physics*)
11:45	**P-type Sensor Development and Irradiation** (15')	Kazuhiko Hara (*Institute of Physics*)
12:00	**Development of Non-inverting Silicon Strip Detectors for the ATLAS ID Upgrade** (30')	Hartmut Sadrozinski
12:30	**CMS Perspectives for a Tracker Upgrade** (30') (Slides)	Tilman Rohe (*Nuclear and Particle Physics Department*)

On-going R&D in ATLAS

- Radiation test of opto-electronics devices
- ABC-Next (including a 130 nm chapter)
- SiGe evaluation (tracker + calorimeter)
- Power distribution (EoI)
- Kevin also reported on starting (re-starting) 0.13 um work for a PIXEL chip (part of B-layer proposal to come)
- Missing:
  - Architecture
  - "Controllers"
  - Protocols (data, control and timing)
  - ***Needed before final ABC-Next or Pixel chip design start***

S.Stapnes, Summary ID upgrade WS 71

Next

- CMS is facing the same kind of problems
- There will be a common workshop ATLAS-CMS devoted to electronics
  - 19-21 March 2007 at CERN
  - Announcement and program before Xmas
    - **Introduction - Machine, ATLAS plans, CMS plans**
    - **Power systems, opto-links, services**
    - **Tracker read-out architectures**
      - **On-going R&D**
      - **Triggering with trackers**
    - **Calorimeters, muons, trigger/DAQ**
    - **Identify/plan potential common building blocks**

S.Stapnes, Summary ID upgrade WS 72

Electronics Summary

- NRE costs for new ASICs push us to minimise the number of different designs and to try and find common solutions
- ATLAS to organise itself to make sure that all R&D needs in electronics are covered and that we get what's needed from non purely ATLAS R&D efforts
- Several R&D on electronics started. Missing work on architecture, controllers, …

S.Stapnes, Summary ID upgrade WS 73

SSD Development for ATLAS Upgrade Tracker

Institution	P-type SSD	Strip Isolation	HV design	Modules constr.	Mech. Structures cooling	Hybrids,Readout	Electr. Char.	Laser CCE	CCE	Trapping	Oper. Param.
KEK	x	x	x	x	x	x	x	x	x	x	
Tsukuba						x	x	x	x	x	x
Liverpool	x	x		x	x		x	x	x	x	
Lancaster							x		x		x
Glasgow				x			x	x?	x	x?	
Sheffield					x	x	x		x		
Cambridge						x	x		x		
QML				x			x				
Freiburg				x		x		x	x		
MPI	x	x	x				x				
Ljubljana							x	x	x	x	
Prague							x	x	x		
Barcelona	x	x	x	x		x	x		x		
Valencia	x	x		x		x	x		x		
Santa Cruz									x	x	x
BNL	x	x	x								
PTI	x	x					x	x		x	

S.Stapnes, Summary ID upgrade WS 80

After Liverpool

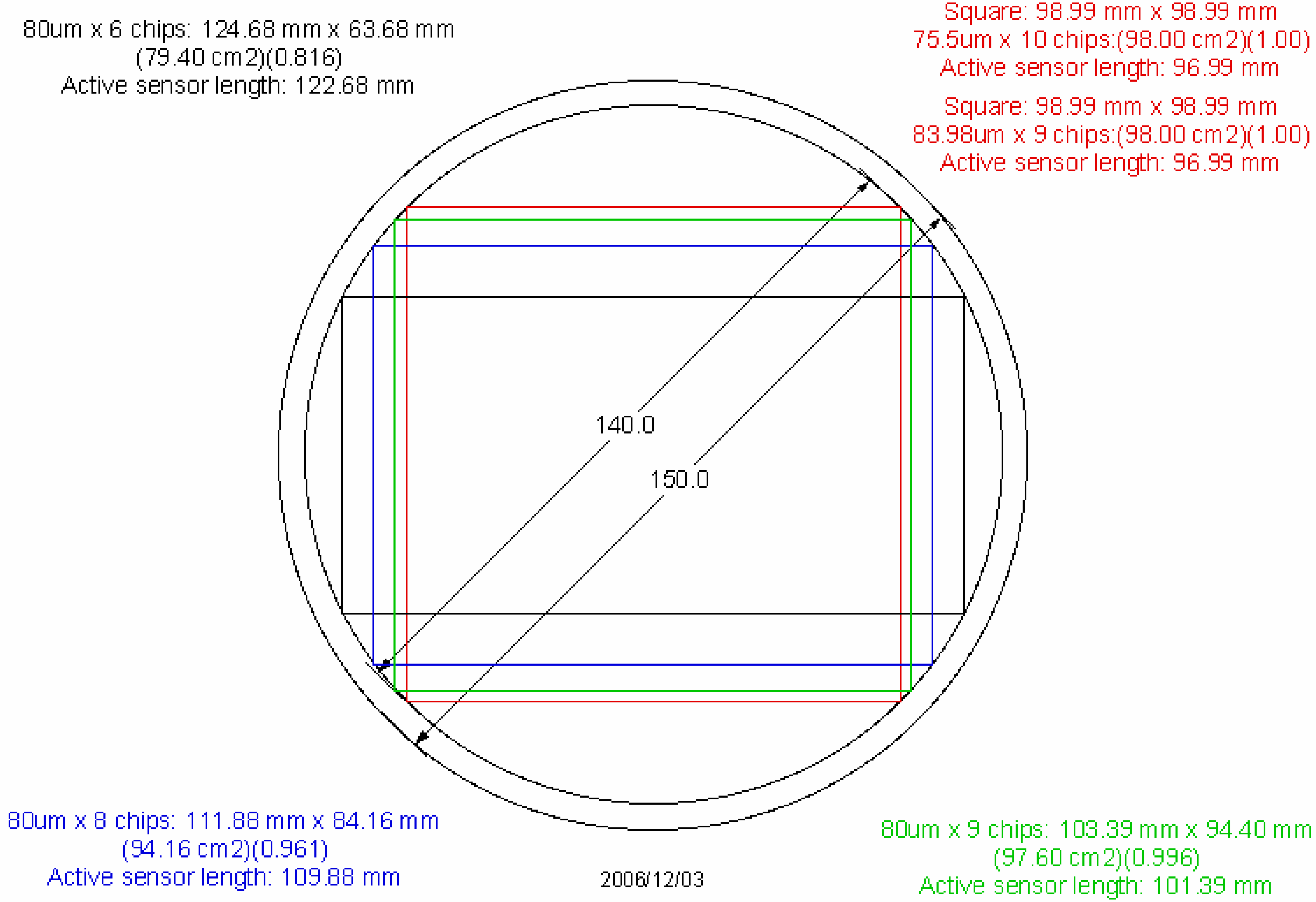
- New assessment of occupancy
- Module integration group
- Baseline inner layer design
  - Inner layers are double sided
  - Sensor is 10 x 10 cm, 2.5 cm x 75 um segment
  - Leads to 10 chips per "module"

Machine parameter update

	25 ns small ß	50 ns long bunch
• Bunch spacing	25 ns	50 ns
• Rms bunch length	7.55 cm	14.4 cm
• Long. Profile	Gauss	Flat
• Luminous region	2.5 cm	3.5 cm
• Peak lumi	15.5 10^{34}	8.9 10^{34}
• **Events crossing**	**296**	**400**
• Lumi. Life time	2.1 h	5.3 h
• Effective lumi (10 h turn around)	2.4×10^{34}	2.3×10^{34}
• Effective lumi (5 h turn around)	3.6×10^{34}	3.6×10^{34}

– 340 ev/50ns was a mistake

Sensor sizes in 150 mm wafer



Implications of sensor size

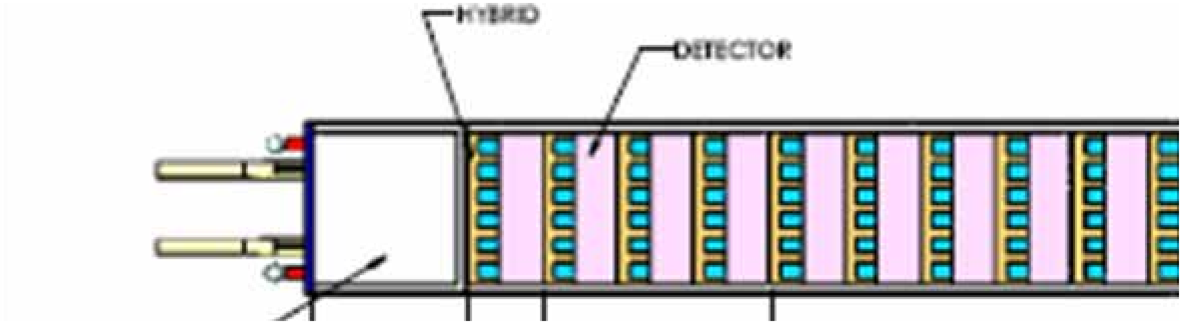
- 12cmx6cm-6chips

								symmetry				Pileup	400					
												a1	3E-04					
								4				a2	1.7	16				
Layer	Radius [mm]	dR [mm]	Incident angle(P) [rad]	Overlap for min. m [mm]	Opening angle [rad]	Arc [mm]	Sectors	Int((Sectors+0.99)/4)*4	chi2	ArcIntSect [mm]	phi-overlap [mm]	No. striplets	Occupancy [%]	No. mods/row	D/S	No. modules	No. sensors	No. chips
B4	364	139	0.10942	1.856748	0.162	59.039	39.996	40	1.3E-05	57.177	1.862	4	1.554	16	2	640	1280	30720
B5	503	136	0.15148	2.584022	0.117	59.086	55.936	56	0.00416	56.436	2.649	4	0.954	16	2	896	1792	43008
B6	639	164	0.19289	3.308584	0.092	59.105	71.957	72	0.00183	55.763	3.342	2	1.406	16	2	1152	2304	27648
																2688	5376	101376
																1.24444	1.24444	0.7543
B7	803	128	0.24329	4.206095	0.074	59.117	91.884	92	0.01349	54.841	4.275	2	1.106	16	1	1472	1472	17664
B8	931		0.28307	4.929955	0.064	59.122	107.943	108	0.00323	54.163	4.958	2	0.974	16	1	1728	1728	20736
																3200	3200	38400
																1.25	1.25	0.75

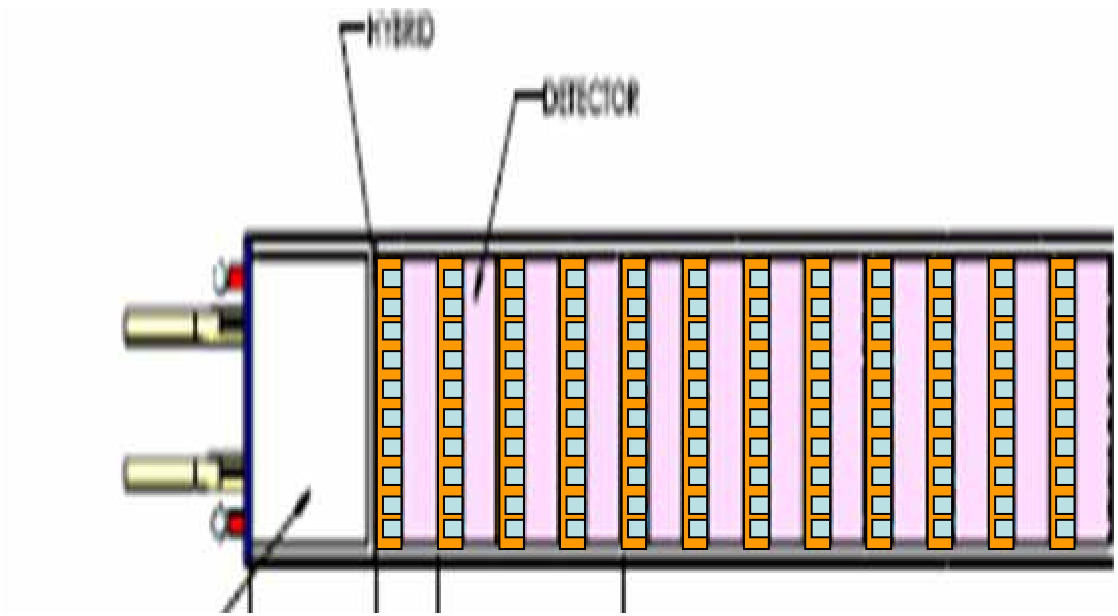
- 10cmx10cm-10chips

square400p

								symmetry				Pileup	400					
												a1	3E-04					
								4				a2	1.7	20				
Layer	Radius [mm]	dR [mm]	Incident angle(P) [rad]	Overlap for min. m [mm]	Opening angle [rad]	Arc [mm]	Sectors	Int((Sectors+0.99)/4)*4	chi2	ArcIntSect [mm]	phi-overlap [mm]	No. striplets	Occupancy [%]	No. mods/row	D/S	No. modules	No. sensors	No. chips
B4	343	165	0.10308	2.736324	0.270	92.663	23.965	24	0.00119	89.797	2.866	4	1.28	20	2	480	960	38400
B5	508	160	0.153	4.099022	0.183	92.896	35.946	36	0.00297	88.663	4.233	4	0.703	20	2	720	1440	57600
B6	668	155	0.20177	5.446972	0.139	92.979	47.950	48	0.00247	87.441	5.538	2	0.999	20	2	960	1920	38400
																2160	4320	134400
																1	1	1
B7	823	100	0.24948	6.790384	0.113	93.017	59.970	60	0.00088	86.184	6.833	2	0.808	20	1	1200	1200	24000
B8	923		0.28057	7.682502	0.101	93.033	67.948	68	0.00269	85.285	7.748	2	0.733	20	1	1360	1360	27200
																2560	2560	51200
																1	1	1



1 meter,
<u>Double sided</u>,
6 x 12 cm sensor
3 cm strip,
32 modules/side
192+65 Watts



1 meter,
<u>Double sided</u>,
10 x 10 cm sensor
2.5 cm strip,
40 modules/side
400+110 Watts

Significant increase in power

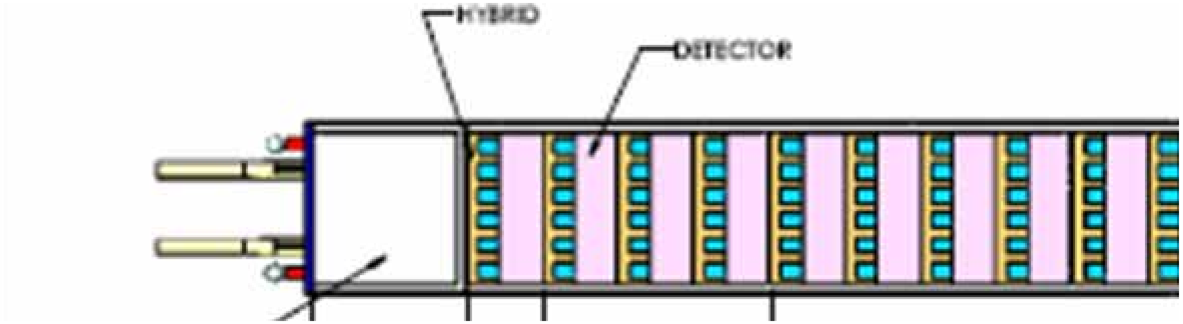
Local Activities

Research Program to USG

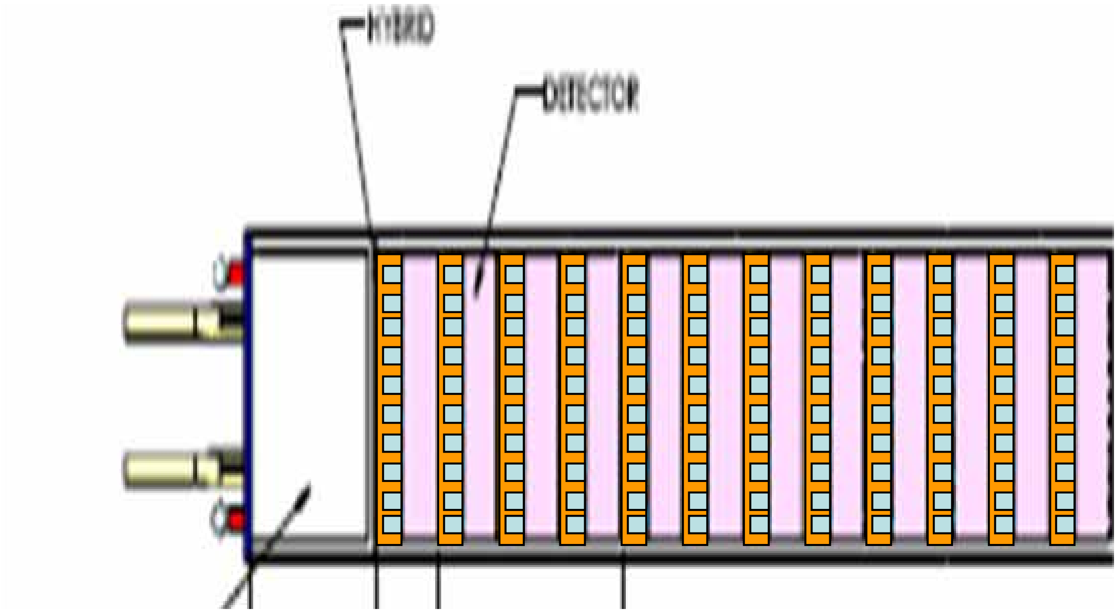
- Push technical limits and assumptions
- Emphasis on early test results
- Develop test-beds for a range of ideas which may be of use
- Mechanical/thermal study
  - Study mechanical/thermal issues in long integrated structure
  - Design structures meeting sLHC specifications
  - Develop prototype assembly tooling and processes
- Electrical study
  - Prototyping a simplified structure with long strips
  - Study powering options (DC-DC, series)
  - Prototyping and measurements of full scale structures
  - Development of DAQ tools for parallel module tests
  - Develop commercial sources for components

Broad Specifications

- Temperature
  - -25C at the silicon, uniformity (thermal run-away), minimize cooling paths
- Build and mechanical tolerances
  - Use precision survey and database where possible
  - Design for minimal sag (~60 microns) unless rad-hard monitoring can be established
- Geometry
  - Short (3 cm) Single and Double sided (stereo) for intermediate region and long Double sided (~12 cm) configuration for outer regions.
- Reliability + Services
  - Use passive redundancy
  - Common clock/com, individual data lines, some common HV
  - Alternative powering schemes
  - Accommodate the loss of some super-modules



1 meter,
Double sided,
6 x 12 cm sensor
3 cm strip,
32 modules/side
192+65 Watts



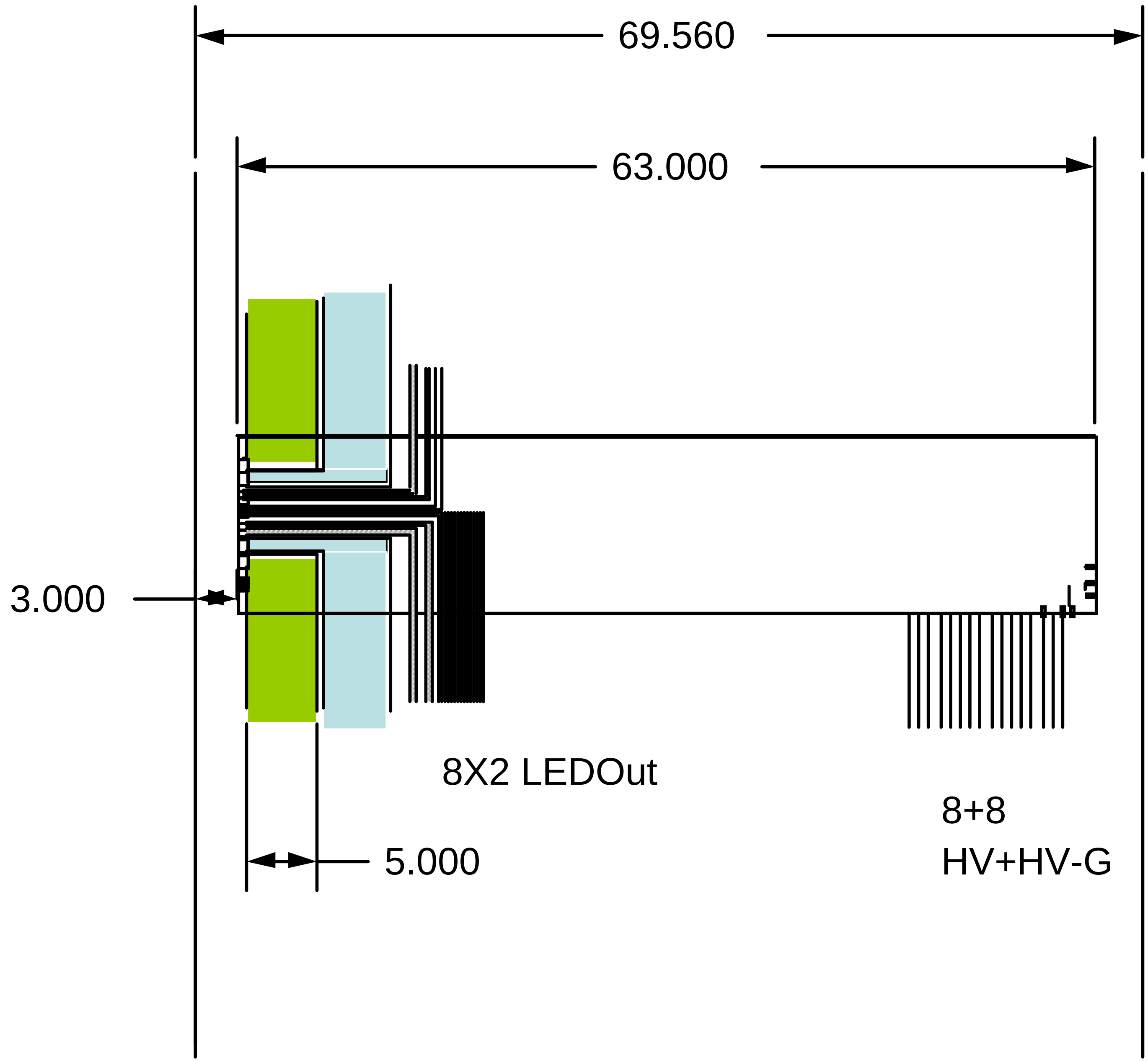
1 meter,
Double sided,
10 x 10 cm sensor
2.5 cm strip,
40 modules/side
400+110 Watts

Significant increase in power

1 crystal cell 4 x 3 cm strip segments

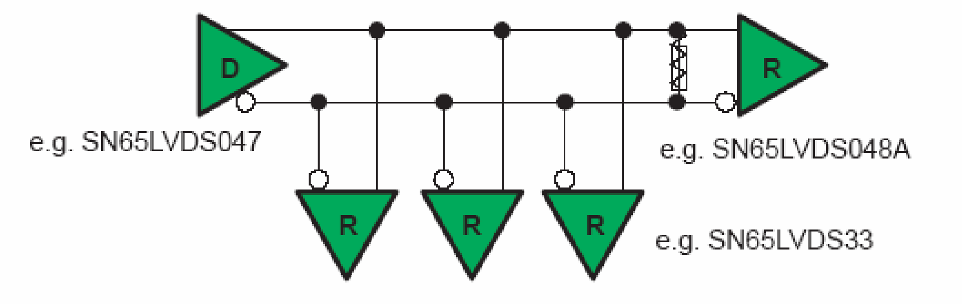
This is a schematic not a physical layout of the stave

Traces shown are underneath the detectors


69.560
63.000
3.000
8X2 LEDOut
8+8
HV+HV-G
5.000

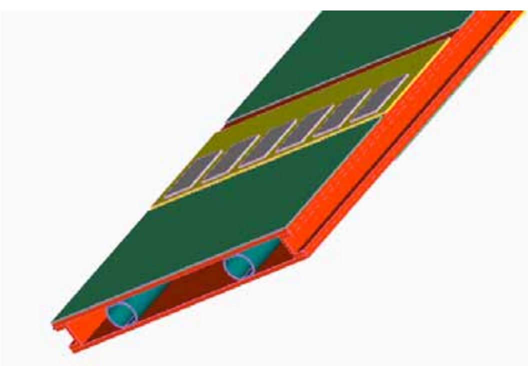
Clock/Command Distribution

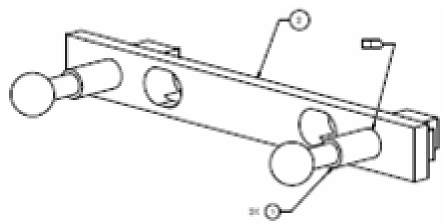
- ATLAS SCT and Phase 1 stave had individual clock/com to each of 6 modules
- This was at the edge of practicality (layout) for Phase 1
- Long staves with $N \rightarrow \infty$ modules
- Prefer to use a multi-drop configuration
  - Implications for ABCD-Next design, etc.
  - Timing
  - Receiver capacitance

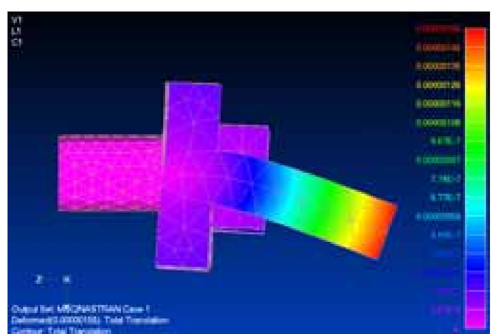


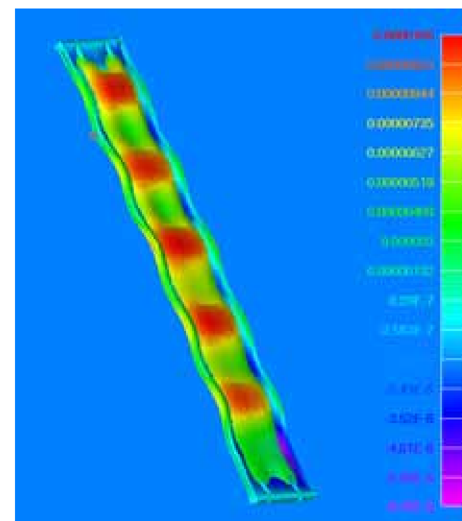
Mechanical Design & Simulations

- Layout and tooling design
- Determine material properties: High conductivity, high modulus CF 4:1 facings, Honeycomb core, Al cooling line
- Rigid pin support at ends
- Max gravitational sag over 1 meter < 75 microns
- Max deformation from Room Temperature = 11 microns
- Radiation length contribution 0.75% for support and coolant (about half the mass)



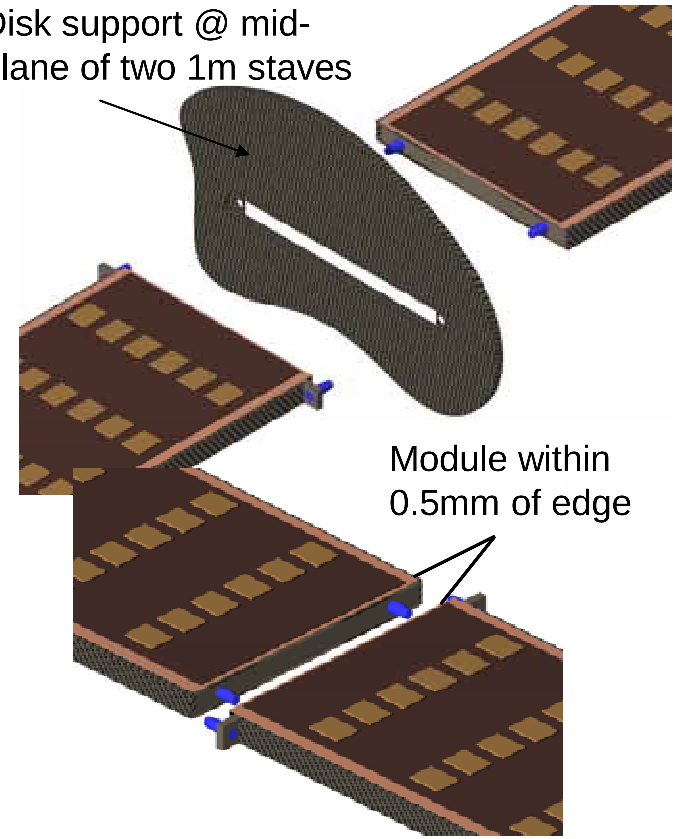






Mid Stave Support

- Objective
  - Minimize dead space between two staves, which butt together
    - No module overhang
    - Maintains uniform wafer cooling
- Approach
  - 1st stave installed is supported by the mid-plane disk
  - 2nd stave is supported by 1st stave, using precision tapered pins
    - Taper is to facilitate assembly
    - Use pin and slot concept to avoid thermal strain issue
  - Pin engagement length and external pin frame sized to achieve rigidity, minimizing pin deflections



Thermal Studies

- Temperature Distributions
- Thermal distortions
- FEA stress in cooling pipes
- Coolant pressure drop and heat transfer

Thermal Property Parameters

FEA Model Properties

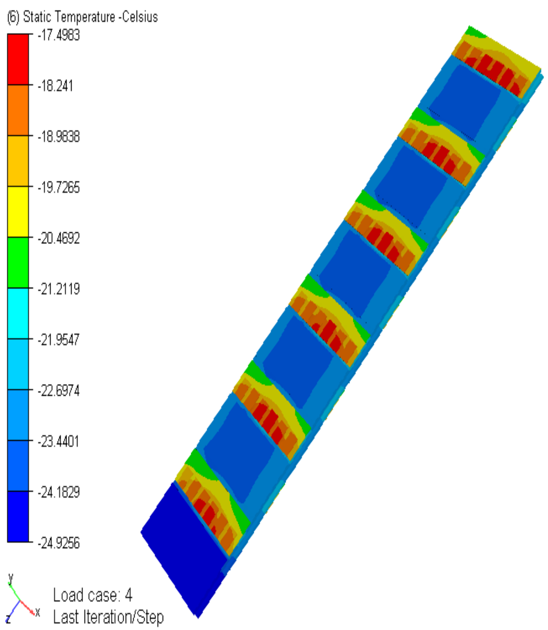
!!

Material	K- (W/mK)	Thickness (mm)
Silicon Wafer	148	0.28
Silver-Adhesive	1.55	0.0508
Dielectric/BeO Hybrid	8	0.38
Cable Bus	0.12	0.125
Composite Facing		0.75
Stave axis	384	
Transverse	97	
Through thickness	1.44	
Coolant tube (Al)	204	0.3048
CGL Adhesive	1	0.0762

Need to understand cable bus and dielectric TC and design options for possible improvements here.

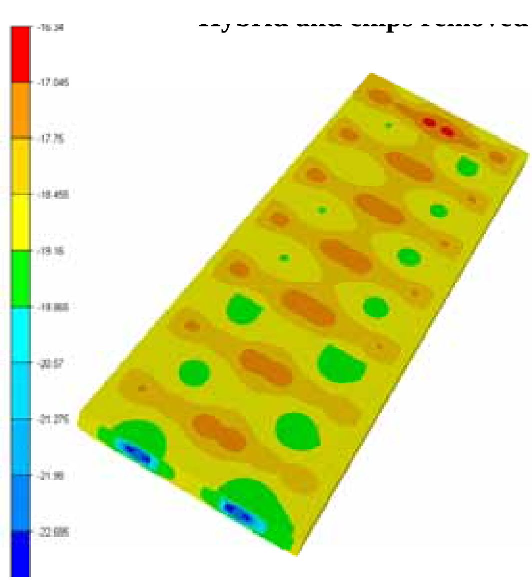
Temperature Distributions

Single sided



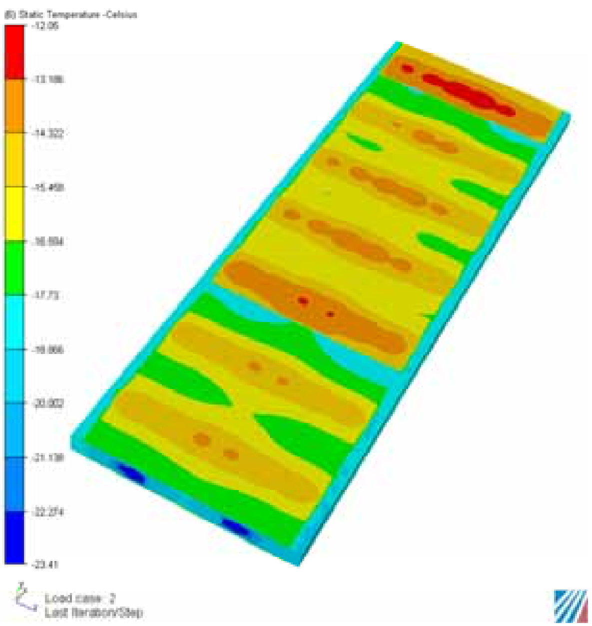
-17.5 C Chip/Silicon -23.5 C

DS low cable TC



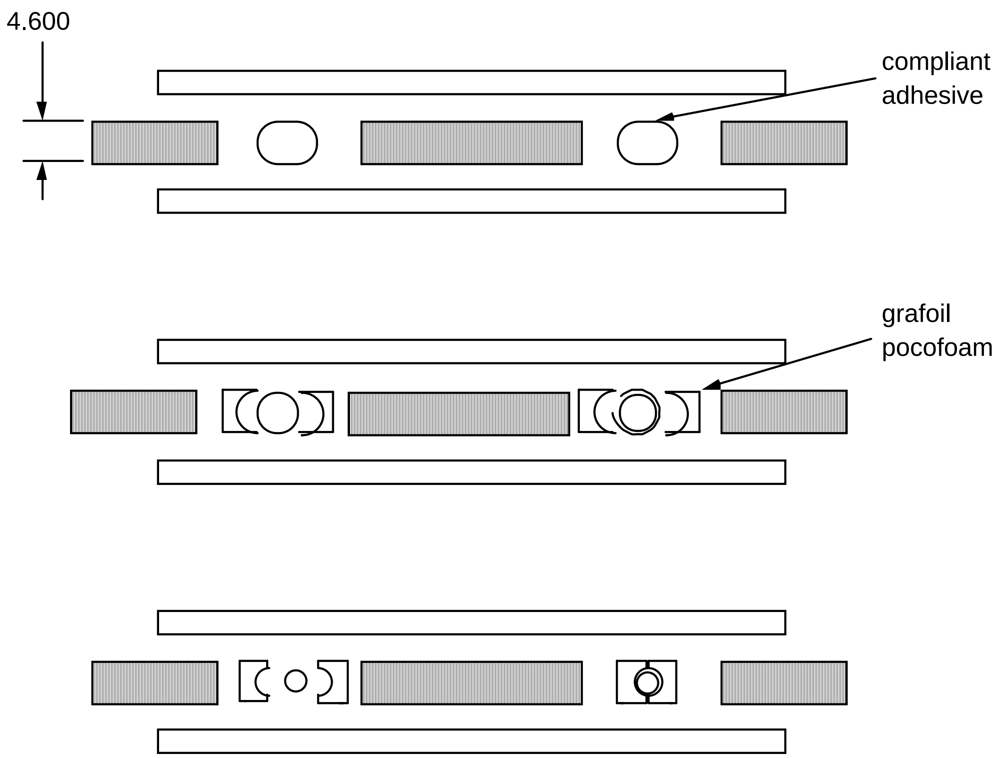
-12.6 C Chip/Silicon -13.6 C

DS high cable TC



-16.7 C Chip/Silicon -17.4 C

Coolant Variants



Lower pressure

High pressure

Very high pressure

Special Materials

- Al cooling tubes
  - Extensive experience from pixels with flattened tubes and compliant adhesives CGL7018 LV
- Grafoil
  - A compliant layered graphite foil which can be used as a cladding on cooling pipes (TC 100/5 in/out)
- Pocofoam
  - High thermal conductivity (TC 45/135 in/out) machine-able carbon foam

Comparison Overview
Doubled Sided Stave

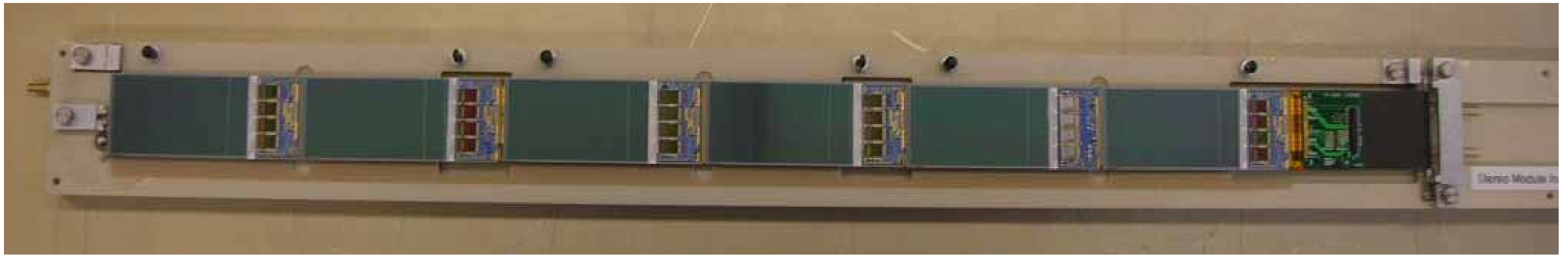
Sag	Tube	ΔT Si	Interface	Max Pressure Limit	Coolant
<75 u	Flat Aluminum 6 mm → 4.6 mm	~10	Compliant adhesive	15 bar	C_3F_8 or C_3F_8 /C_2F_6
"	Round Aluminum 4.6 mm	~11	Grafoil	150 bar	C_3F_8 barely $C0_2$
"	Round Ni Cu 2 mm	~11-12	Grafoil	Big	$C0_2$

Implications for 10 x 10

- Thermal drops will increase
- Wider cable means more space available
- Investigate the use of high thermal conductivity inserts into the bus cable dead space

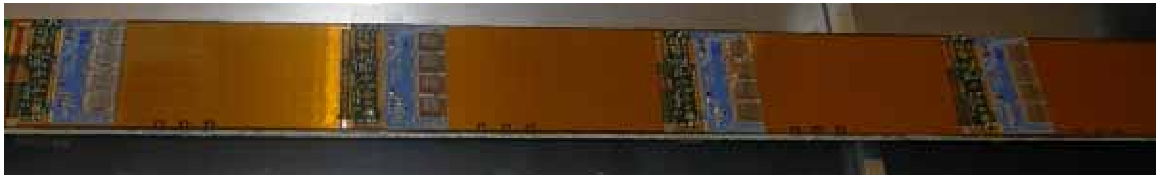
Electrical Tests

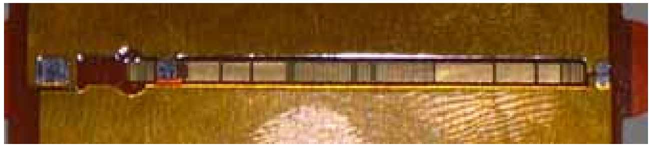
- Develop ATLAS hybrid specific for multi-module use
- 1 sensor + hybrid = 1 module (hybrid glued to Si); 6 modules per side
- Modules linked by **embedded bus cable**
- Total length 66 cm, 6144 channels
- Built around carbon fiber/foam laminate



- Measure multi-module performance with ATLAS electronics
- Compare individual and serial powering
- A concrete stave example

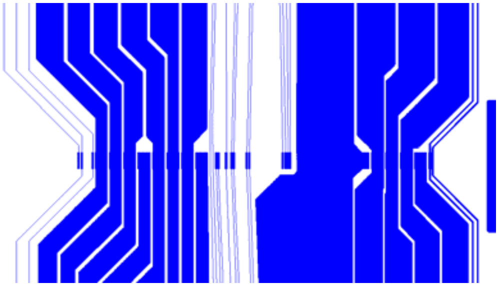
Core + Bus Cable + Module



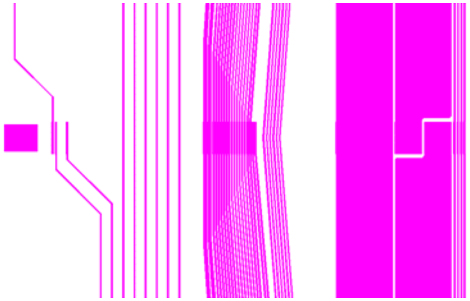


75 Ω differential stripline

Individual

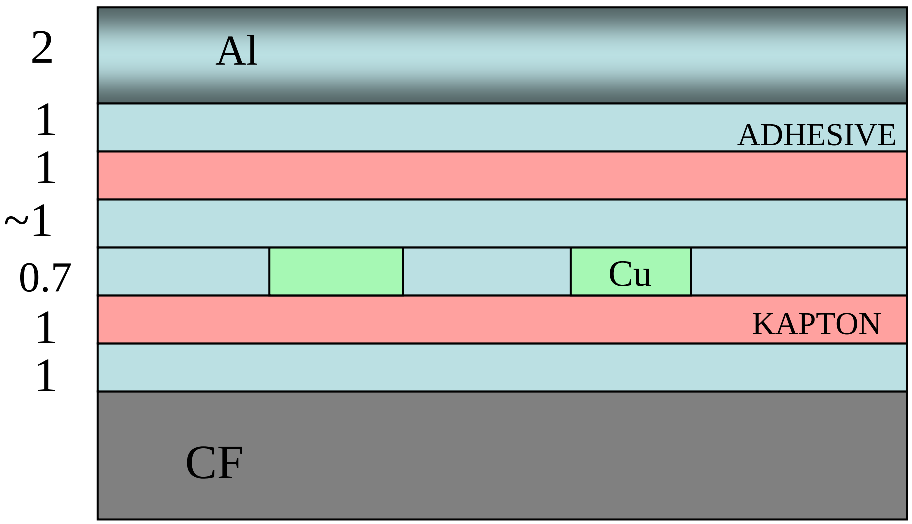


Serial

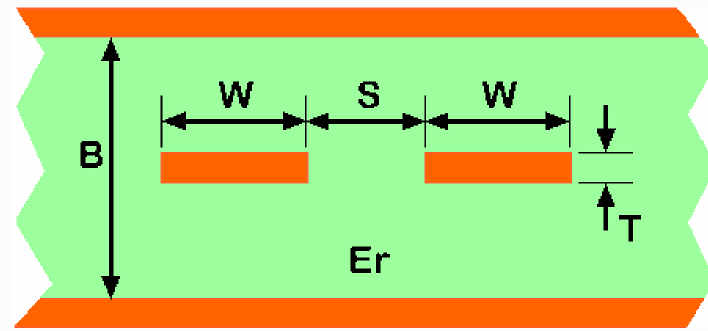


Bus Cable Geometry and Impedance

Materials: Al foil 2mil, Dupont LF0100, Shinetsu CA333 2 mils, Cu 18 um, Kapton 1 mil, Adhesive



Differential Stripline Impedance Calculator



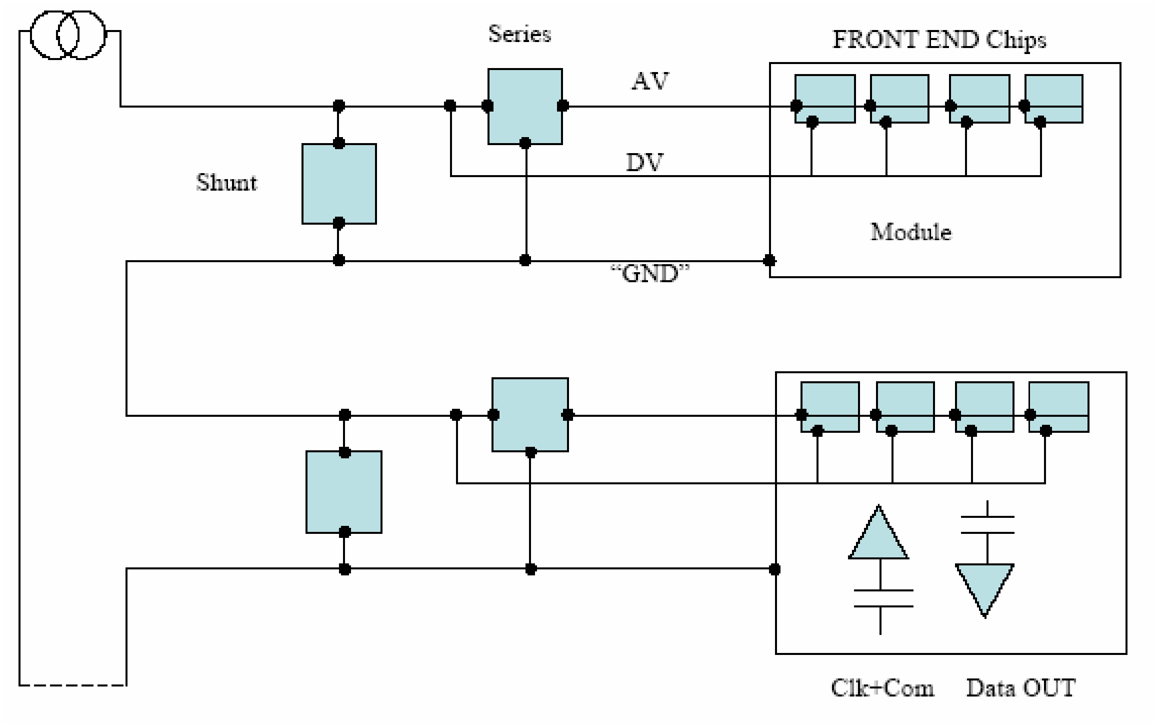
Notes:
1) Calculation assumes traces are centered vertically.
2) S/T > 5.0

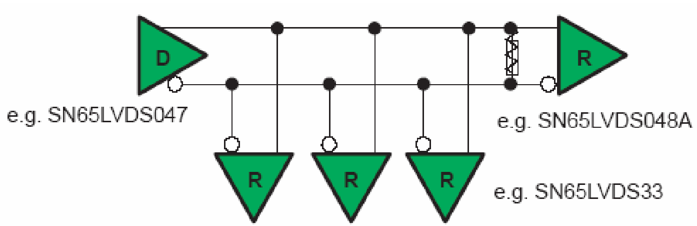
Enter dimensions:

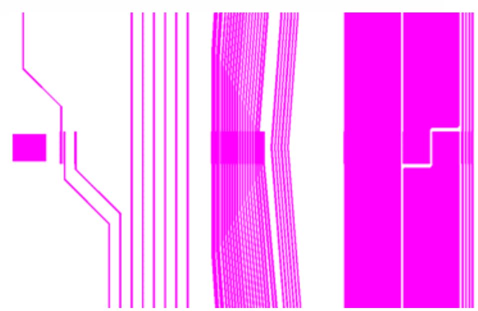
Trace width (W)	3	mils
Trace thickness (T)	.7	mils
Trace spacing (S)	4	mils
Distance between planes (B)	5	mils
Relative Dielectric constant (Er)	3.6	
Compute Z		
Differential Trace Impedance	72.9	ohms

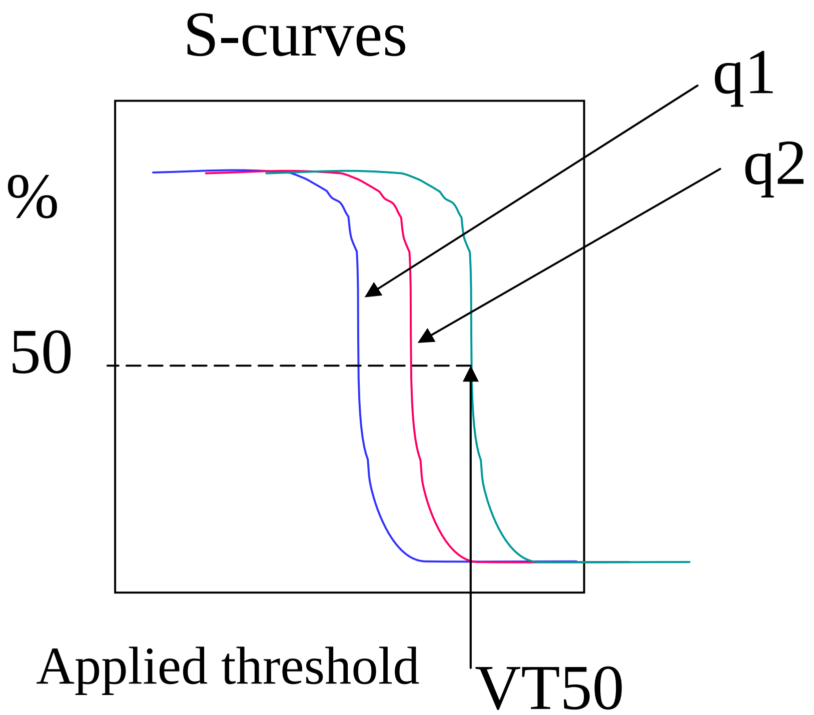
>>Matches measured impedance

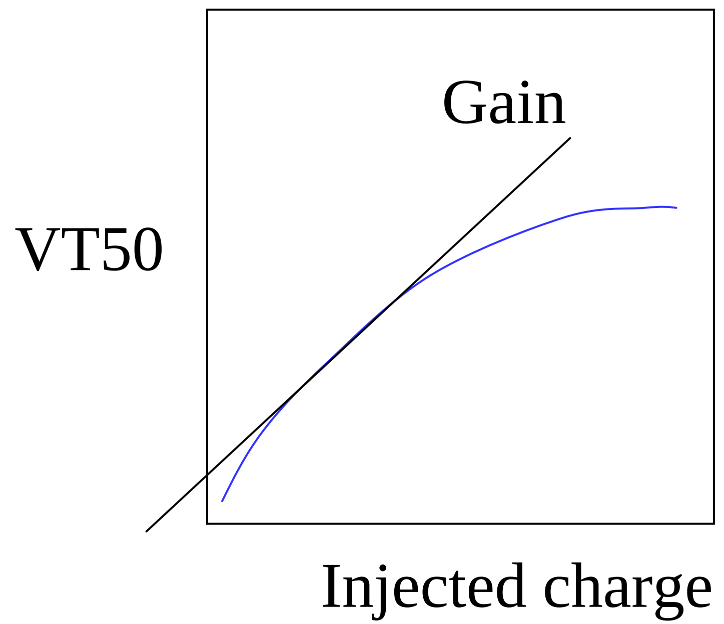
Serial Powering Configuration



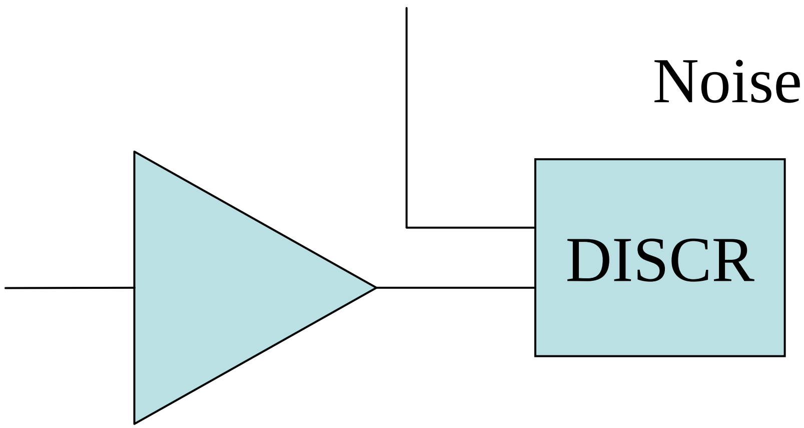






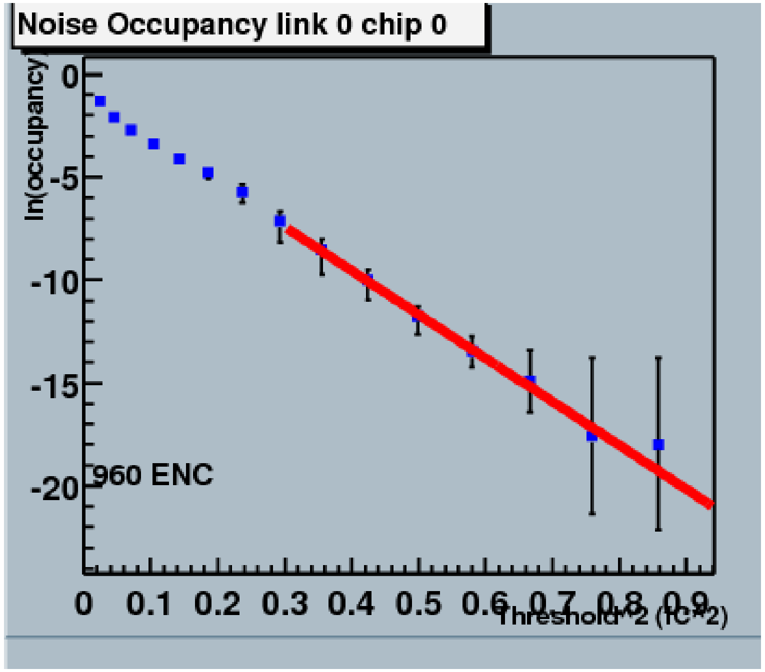


Noise given by width of underlying Gaussian



Studies

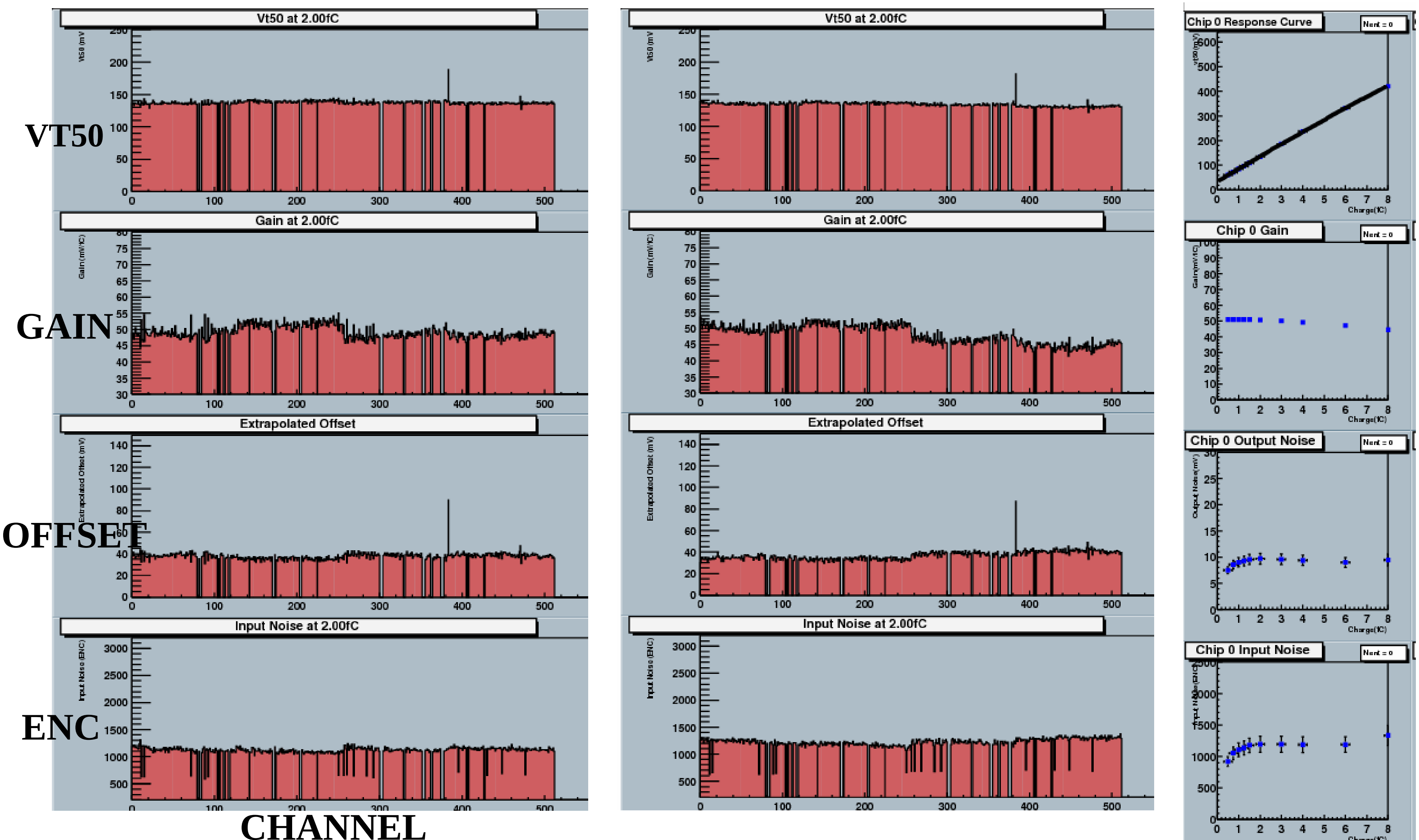
- Multi-modules with individual powering
  - Analog performance on and off stave, consistent
- Multi-modules with serial powering
  - Power distribution, voltage drops OK
  - Multi-drop AC coupled LVDS system, OK
  - Good digital data transmission
  - Analog performance on and off stave, consistent



With serial powering

Individual Power

Module in Test Box   Module On Stave



Serial powered modules on stave + 4 hybrids

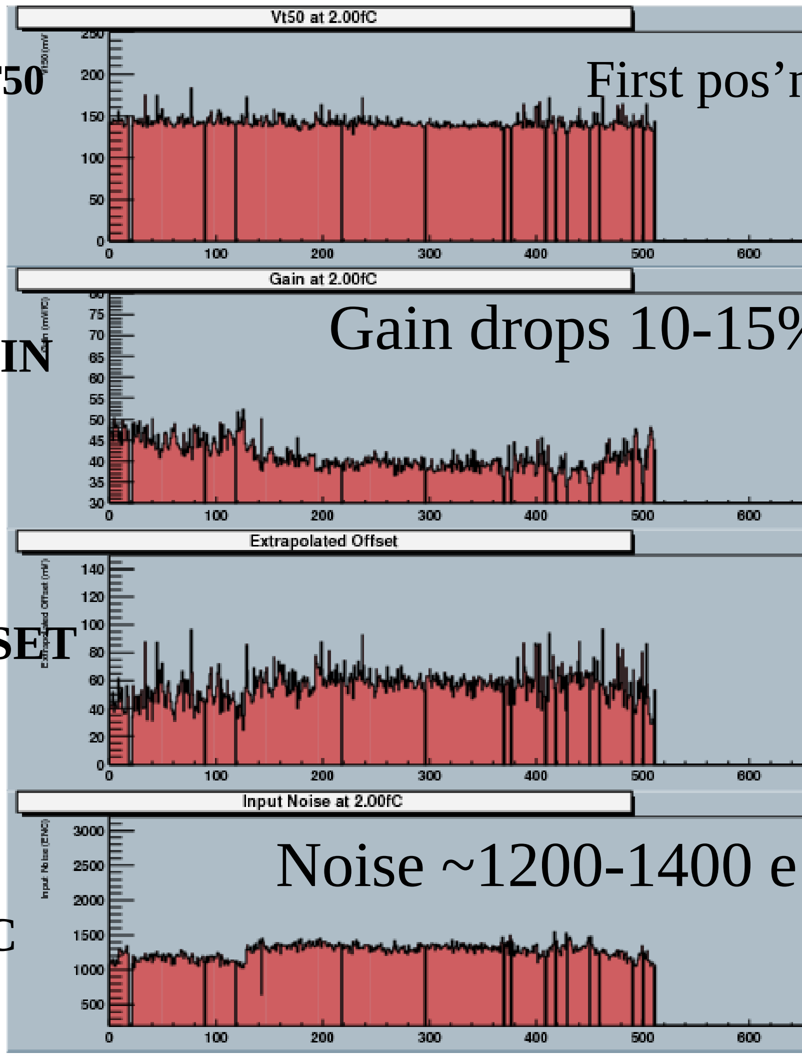
Last pos’n

VT50

GAIN

OFFSET

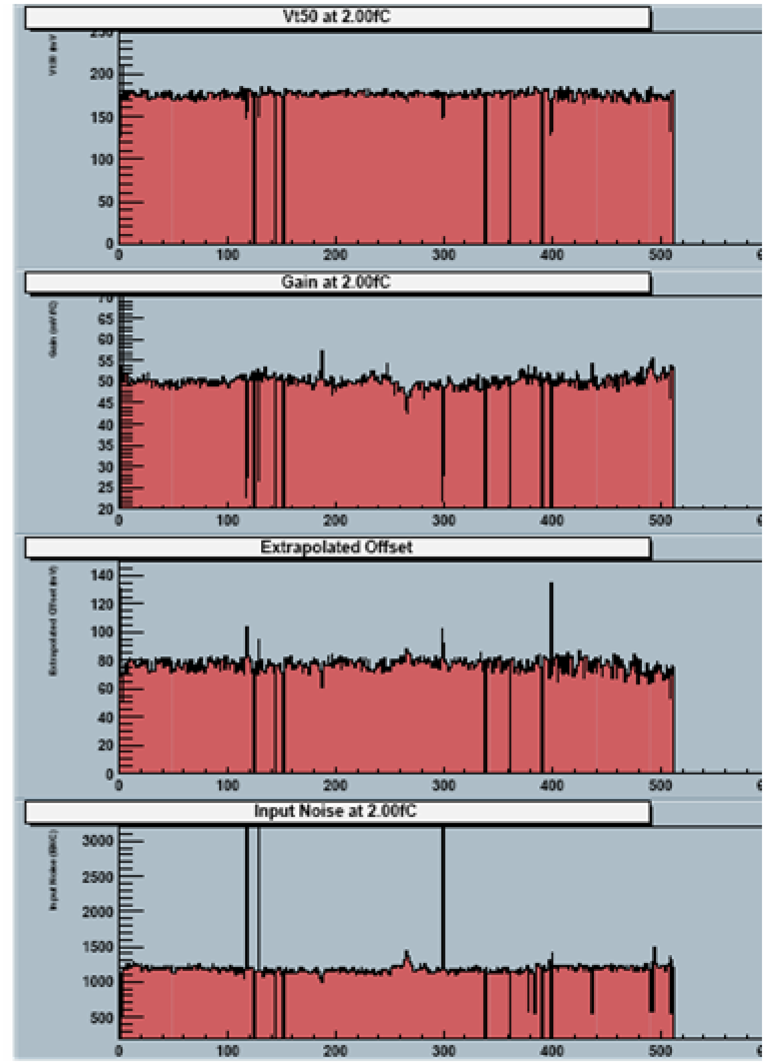
ENC



First pos’n

Gain drops 10-15%

Noise ~1200-1400 e



DAQ

- Present electrical studies are based upon the existing MUSTARD/CLOAC VME system.
- Recognize that for multi-module tests this is not very convenient.
- Pursue a development project based upon National Instruments High Speed Digital IO technology – 16 channel PXI card
- Considerable software development is now underway (talk of Tim Phung and others on Wed)
- Aim to organize and broaden this activity across the R&D collaboration.

Property	**Short stave**	**Long Stave**
Width	6.4 cm	12.8 cm
length (nominal)	98 cm	192 cm
detector width	6.4 cm	12.8 cm
detector length	3 cm	10-12 cm
detectors per side*	15 / 32	12-16
gap between detector along the stave	2.4 cm / 1 mm	3 mm
detector thickness	280 microns	300 microns
number of strips/module	768	768
strip pitch	80 microns	160 microns
Power in front end chips (per hybrid)	3 watts	3 watts
Power in silicon – no dose (per crystal)	1 milliwatt	2 milliwatt
Power in silicon – high dose (per crystal)	1 watt	2 watt
Maximum temperature at silicon	-25 C	-10 C
Maximum temperature variation	<5 C	<5C
Max detector position shift from nom Dy	30 microns	30 microns
Max detector position shift from nom Dx	30 microns	30 microns
Survey accuracy Sy	5 microns	5 microns
Survey accuracy Sx	10 microns	5 microns
Survey accuracy Sq	0.13 mRad	0,13 mRad
Ladder sag maximum**	~75 microns	~75 microns
Ladder sag stability***	25 microns	25 microns

Plans and Prototyping Activity

- Given the instability in layer configurations we have tried to remain consistent with multiple alternatives.
- Need to build a test a fully double sided stave (SS-DS)
- Unfortunately could not forsee 10 x 10 cm as an option. (Will it survive? Power x2)
- Need to redo all the thermal and mechanical simulations for the 10 x 10 configuration.
- Hopefully this will not leave too many questions unanswered…

Continued

- Gil will present schedule and more details
- Procure mechanical components
- Fabricate mechanical asssembly fixtures
- Design and fabrication of electrical components
  - Hybrid
  - Bus cable
  - Interface card
- Design and fabrication of electrical assembly fixtures
- Plan to use new DAQ for stave characterizations