R&D Plans for R > 20 cm

Parameters LHC, SLHC

	LHC	SLHC
$\sqrt{s}$	14 TeV	14 TeV
L	10^{34}	10^{35}
Bunch spacing Δt	25 ns	12.5 ns
σ_{pp} (inelastic)	~ 80 mb	~ 80 mb
N. interactions/x-ing ($N=L\ \sigma_{pp}\ \Delta t$)	~ 20	~ 100
$dN_{ch}/d\eta$ per x-ing	~ 150	~ 750
$\langle E_T \rangle$ charge particles	~ 450 MeV	~ 450 MeV
Track density	1	10
Pile-up noise in cal	1	~3
Dose central region	1	10

Occupancy

- At 10^{34} the mean pile-up occupancy in an SCT module is ~40% of that due to b-jets from Higgs (layer 1@ 30 cm)
- Assume this is an acceptable target
- (At 10^{35} the pile-up occupancy in an existing SCT module will be 2-4x that due to b-jets from Higgs)

Occupancy (2)

- At 30 cm an SCT module covers 0.25% of the barrel surface area.
- For present SCT region, modules will have to be modified to meet old occupancy and merged cluster targets
  - Increased segmentation
    - Finer pitch (increases channel count per module)
    - Shorter strips (increases number of modules)
    - Re-visit binary vs multi-bit front ends for cluster merging?
- For TRT region need guidelines for width x length, extrapolate from SCT, scale to 10^{35}

Occupancy (3)

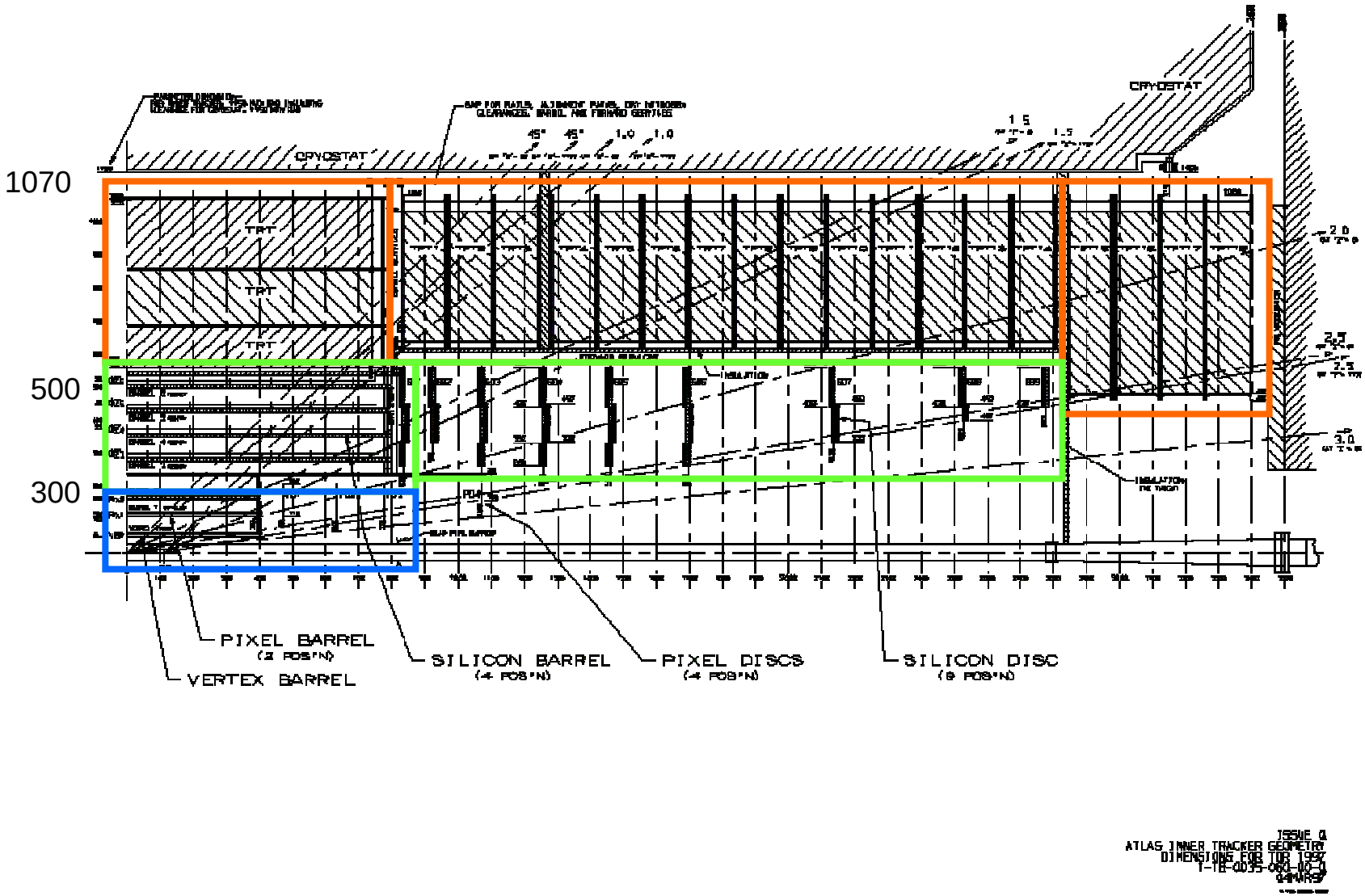
- Even at large radius will need considerably shorter strip lengths to meet low occupancy specifications
- Need to optimize module width vs length with concerns for
  - Material
  - Signal/power distribution, reliability
  - Cooling
- Typical “Outer (TRT) Region” module size could be 4 cm (wide) by 6 cm (long)
- Single module design model still valid at all radii?

Cluster Merging

- At 10^{34} the fraction of merged clusters in an SCT module is 1% due pile-up and 2% due to b-jets from Higgs (layer 1@ 30 cm)
- Assume this is an acceptable target
- (At 10^{35} the fraction of merged clusters due to pile-up in an existing SCT module will be 10%)

Elements of an SLHC Tracker

- < 20 *cm*: inner, dose:10^{16} /cm^2
  - new technology
- 20 < r < 50 *cm*: intermediate, dose: 10^{14}-10^{15} /cm^2
  - pixels, short strips, strip-pixels
  - modularity, mass, reliability, system issues
  - 60 m^2, 4K “SCT modules”
- > 50 *cm*: outer 10^{12}-10^{13} /cm^2
  - strips
  - modularity, mass, construction logistics
  - 140 m^2, 16K “SCT modules”

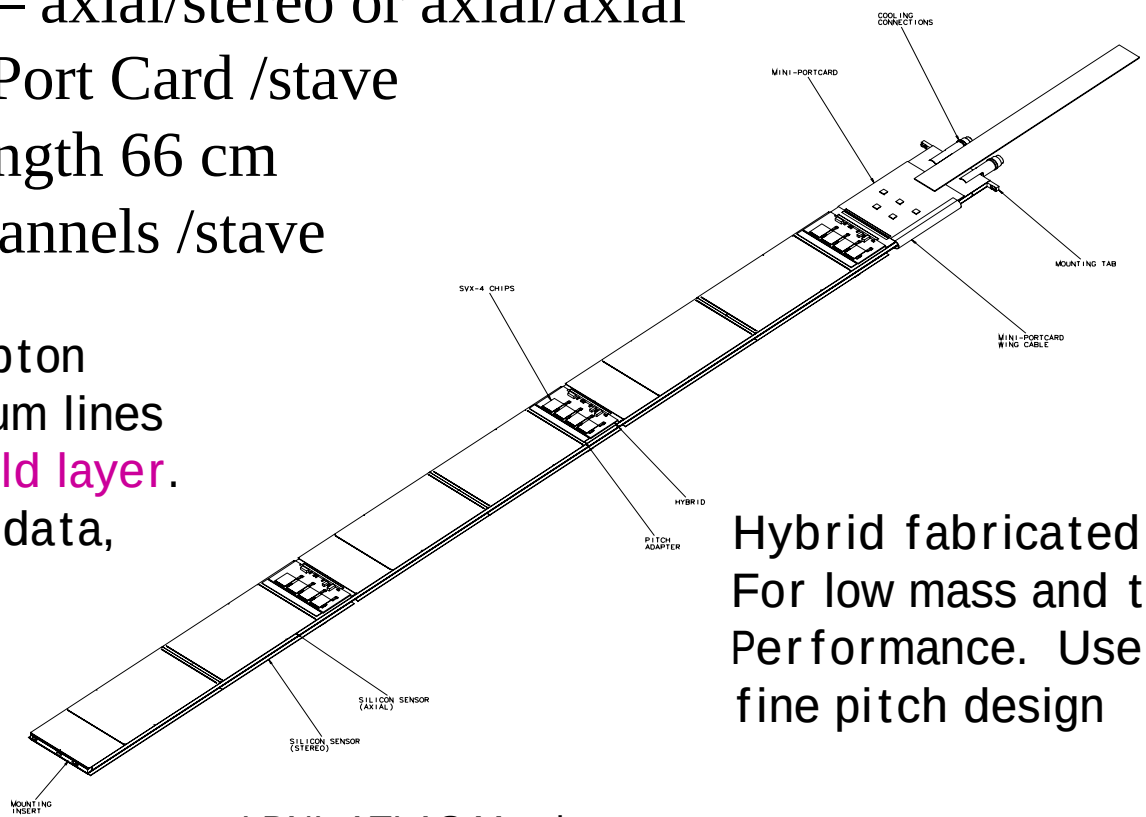

1070
500
300
CRYOSTAT
CRYOSTAT
TRT
TRT
TRT
PIXEL BARREL
(3 POS'N)
VERTEX BARREL
SILICON BARREL
(4 POS'N)
PIXEL DISCS
(4 POS'N)
SILICON DISC
(9 POS'N)

Development of Tracking Structures

- Address here the SCT region and the replacement of the TRT with silicon strip modules. Precise long term focus unclear.
- Pursue certain generic or basic R&D to flesh out eventual direction(s).
- The modularity required or adopted will be effected by a number of factors
  - Experience from present SCT effort
  - Radius, occupancy, simulations
  - Material
  - Assembly logistics, cost, and schedule
- Starting concept is a stave (multi-module) structure as was studied for Run2b

Stave Conceptual View

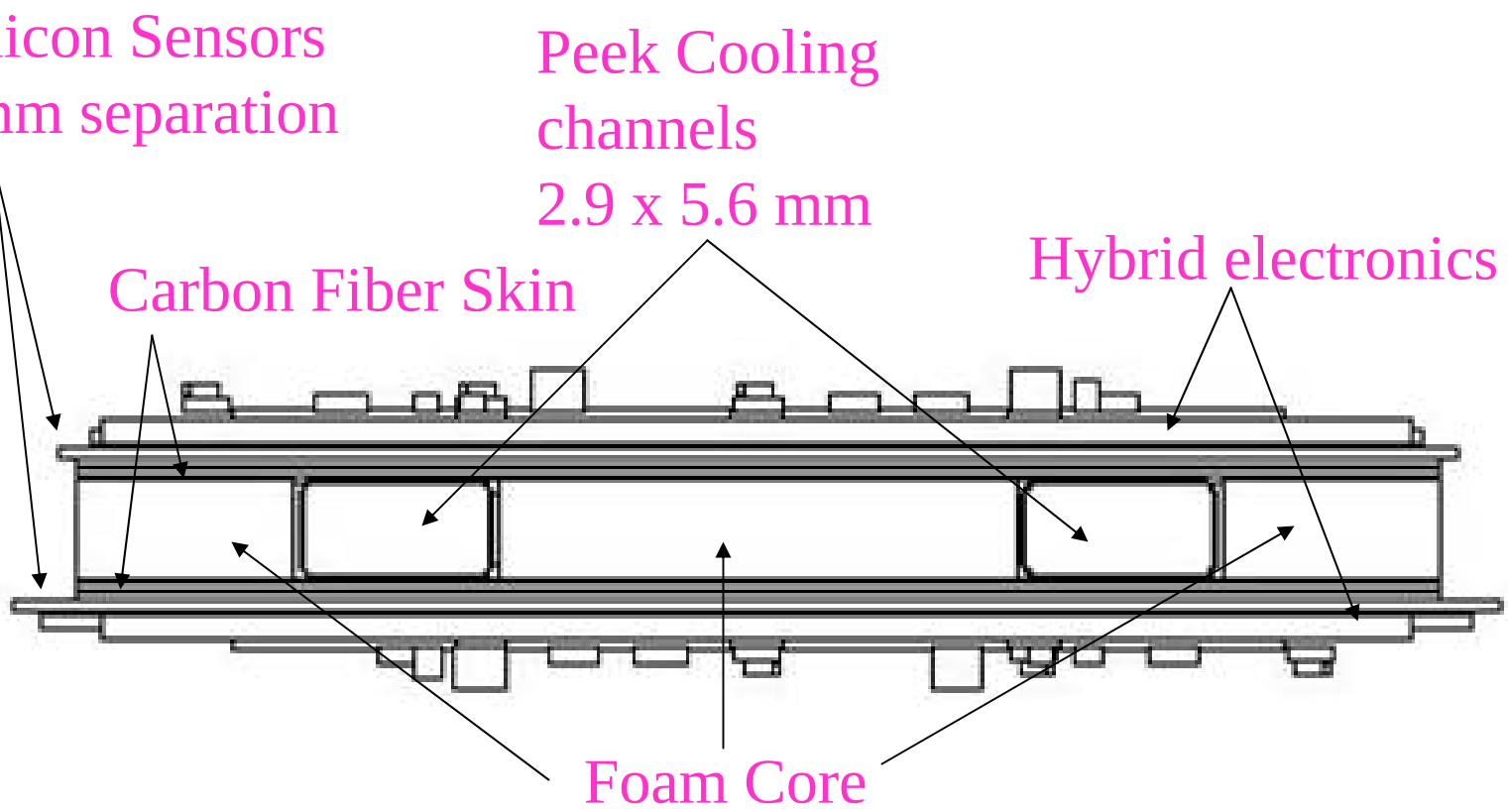
- 2 sensors + hybrid = 1 module (ladder)
- 3 modules per side
- Modules linked by **embedded bus cable** and readout token passing scheme
- 2 sided – axial/stereo or axial/axial
- 1 Mini-Port Card /stave
- Total length 66 cm
- 3072 channels /stave



Bus cable is Cu/Kapton laminate with 100 um lines and spaces, Al shield layer. Distribute signals, data, power, HV

Hybrid fabricated on BeO For low mass and thermal Performance. Use advanced fine pitch design

Stave End View

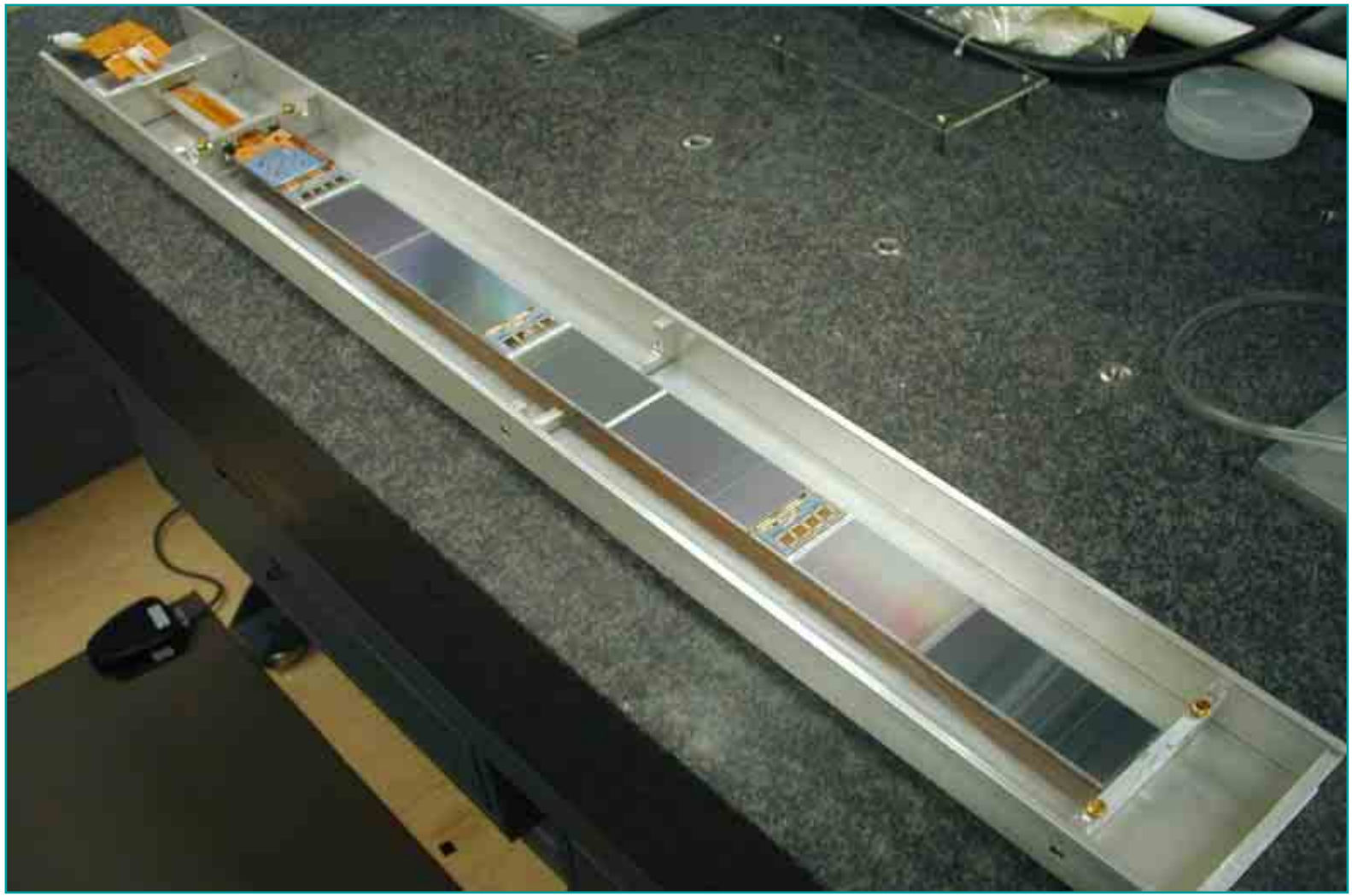


Material/stave:

- 1.8% RL
- (compare 2.5% ATLAS)
- 124 grams

Fraction of Total RL:

- Hybrids 13%
- Sensors 39%
- Bus Cable 17%
- CF/Coolant 29%

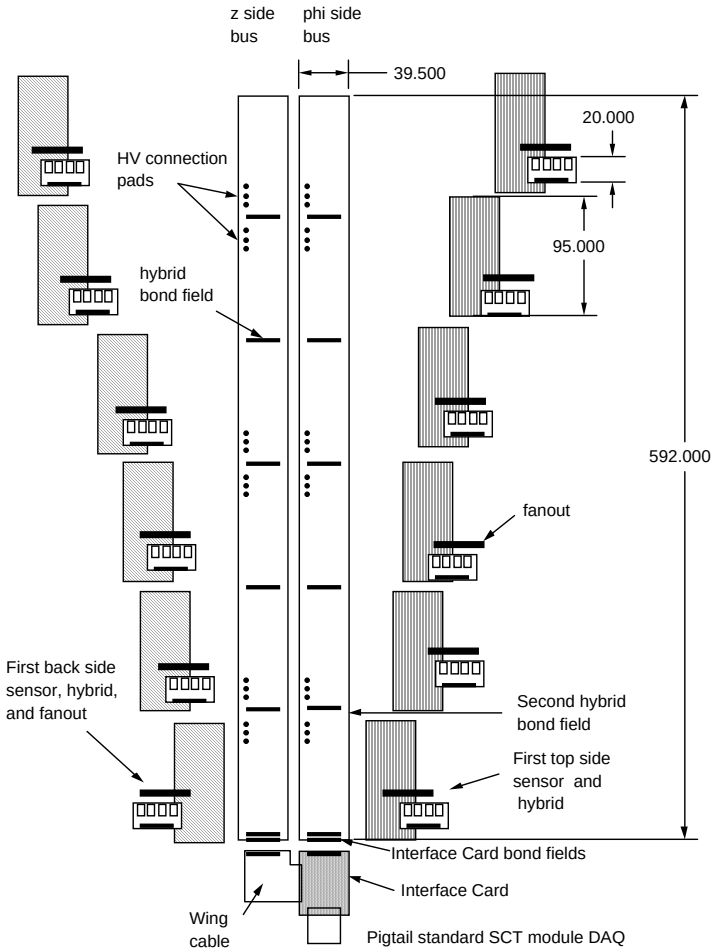


- Proposal submitted 8/2004 to A.Seiden
- Effort is a collaboration
  - LBL
  - Brookhaven
    - David Lynn
    - David Lissauer
    - Instrumentation: Vejlko Radeka, Zheng Li, Paul O' Connor
  - Hampton University
    - Ken MacFarlane
    - Keith Baker
- BNL and Hampton have interest in eventual large scale assembly.

3 Phases + Related Project

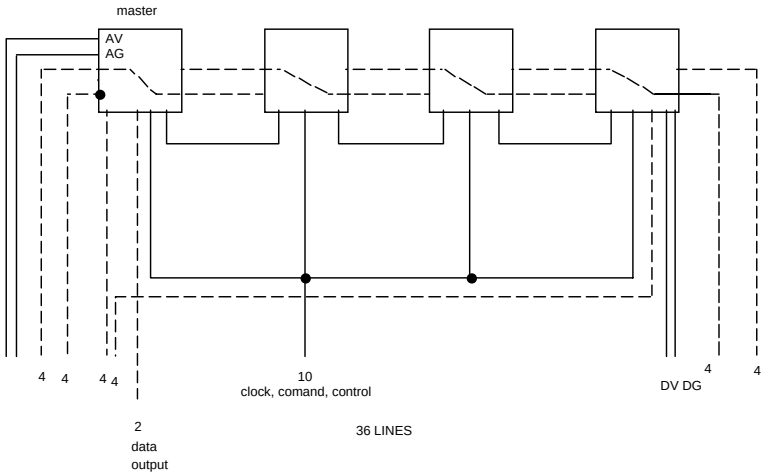
- Phase 1: (FY05) Explore behavior of ATLAS electronics on a stave, leverage Run2b experience.
  - Assemble mock and real staves at LBNL and then BNL
- BNL Strip-pixel project: (FY05) Development of an ATLAS specific single-sided 2D detector.
- Phase 2: (FY05)Test of strip-pixel detector with analog and ATLAS binary readout at BNL.
- Phase 3: (FY06) Development of new ATLAS specific stave with strip-pixel or other appropriate readout.

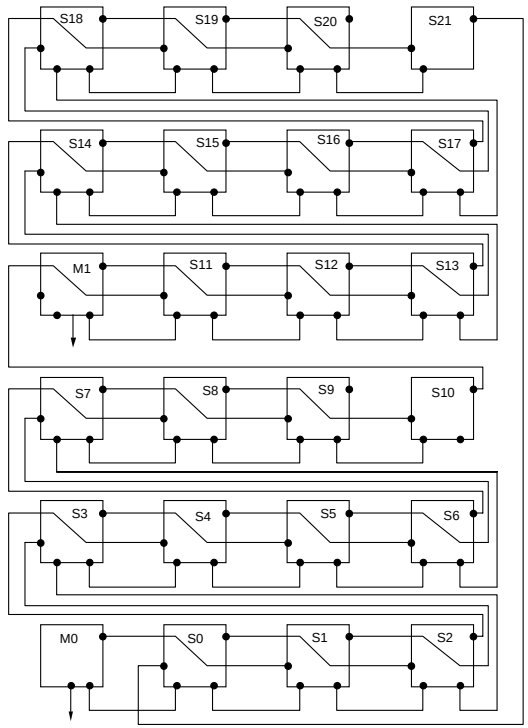
ATLAS Stave (Outer Region)

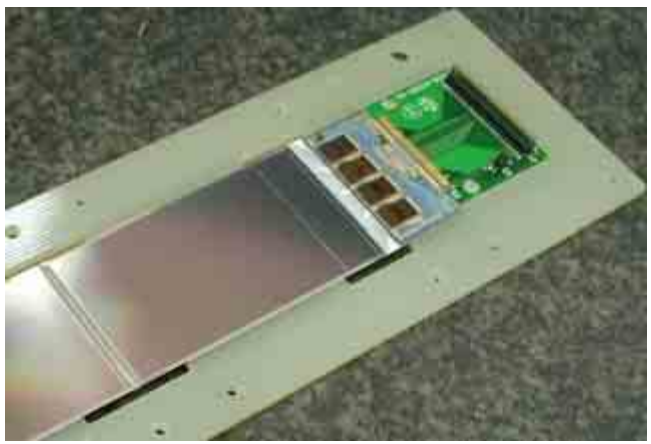


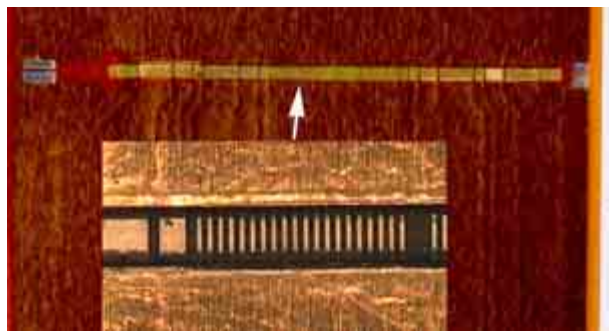
Hybrid and Interconnections

Key initial task is the design of a hybrid and bus cable for the ABCD chips









Stave Assembly Fixtures from FNAL

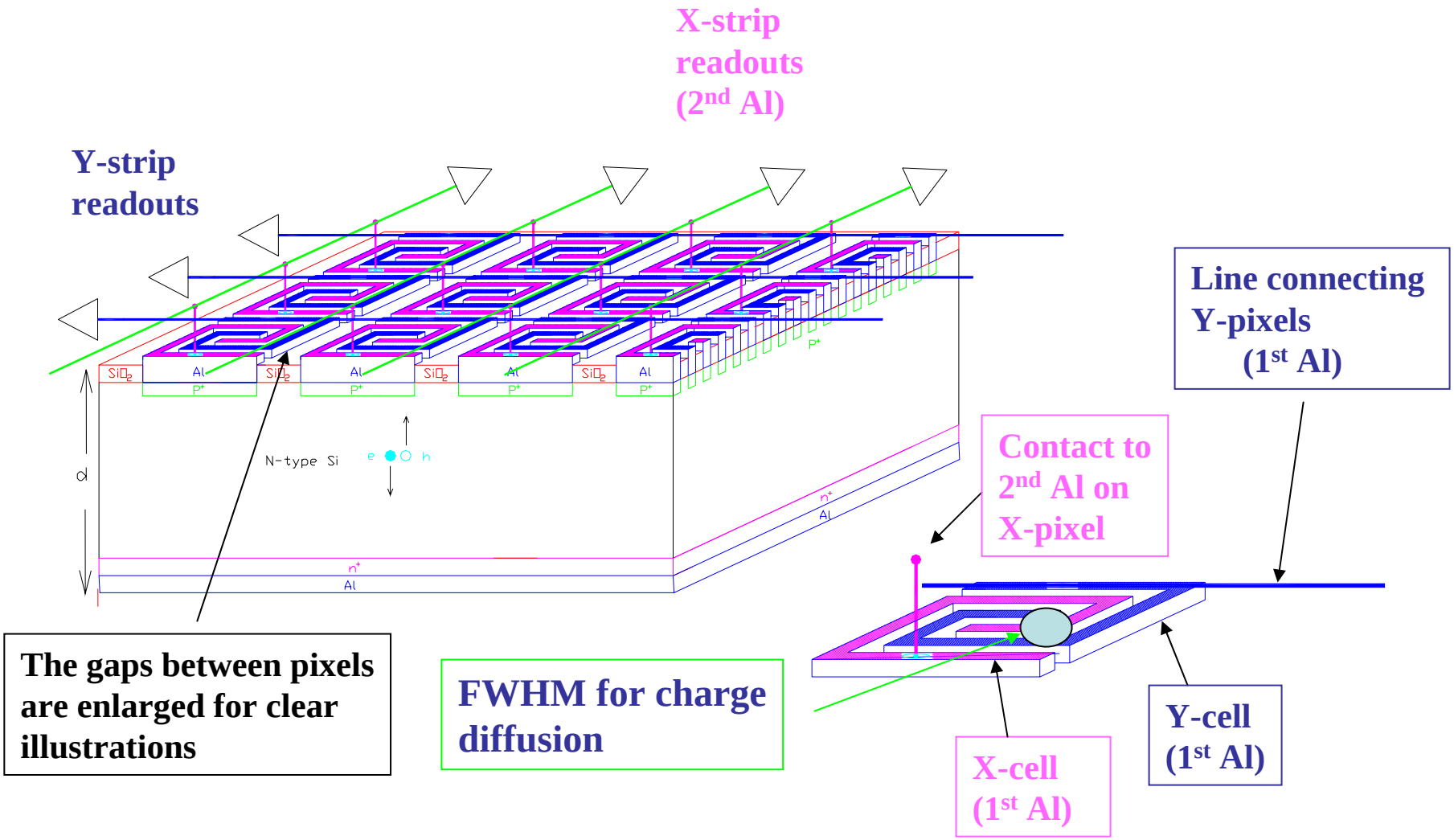
Phase 1 Milestones (completion dates given)

full electrical specification and schematic for Phase 1 stave	10/04
establishment of test stands at LBNL, BNL, and Hampton	11/04
validation of test stand operation on test parts	12/04
design and layout of Phase 1 hybrid	12/04
fabrication of hybrid	03/05
assembly and test of hybrid	04/05
re-commission and tests with existing fixtures	03/05
assembly of ATLAS staves	06/05
initial test of ATLAS staves at LBNL	07/05
transfer to and test of staves at BNL/Hampton	08/05
irradiation studies of staves	10/05
transfer of assembly methods to BN	07/05

Phase 2 + BNL effort

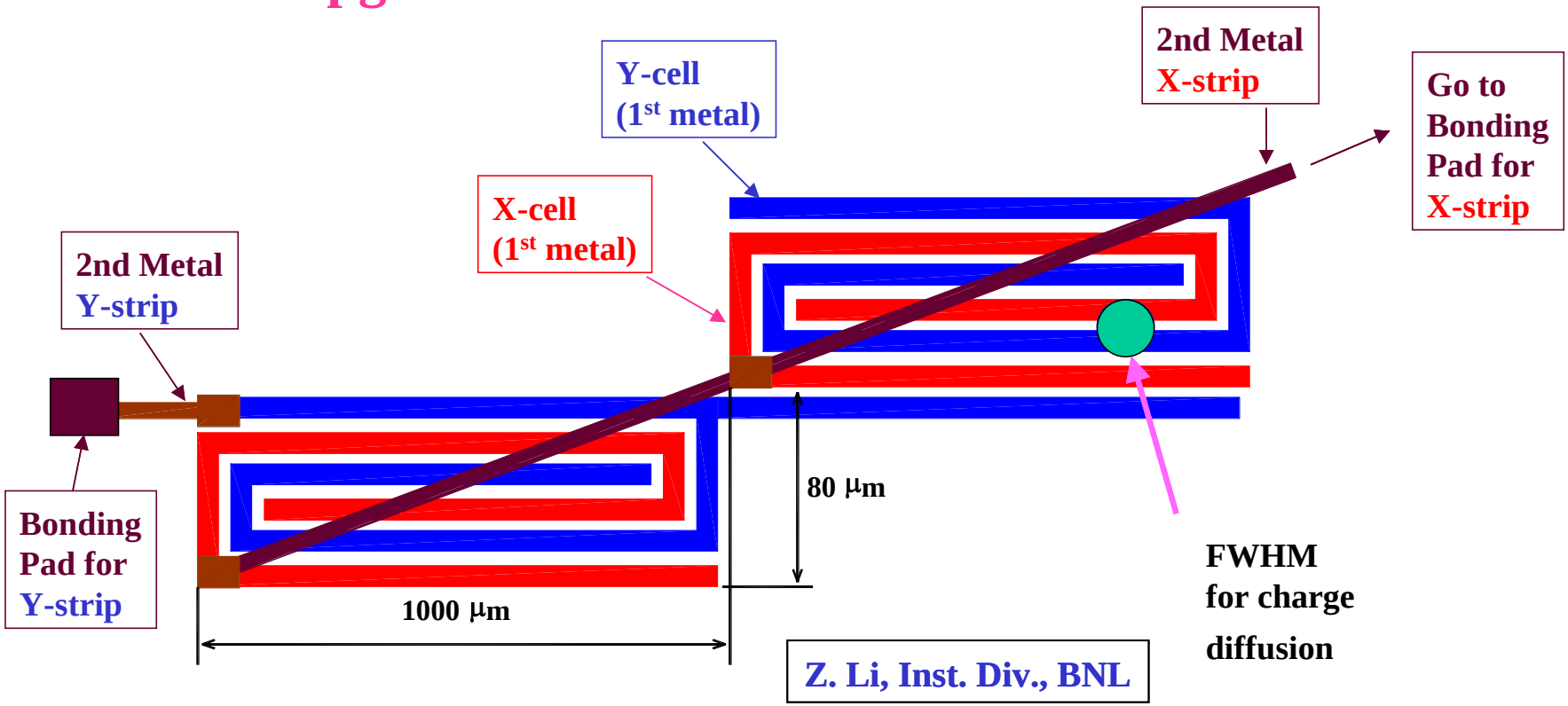
BNL slide

Schematic of a spiral interleaving scheme for ISD



Schematic of the Prototype Stripixel Detector

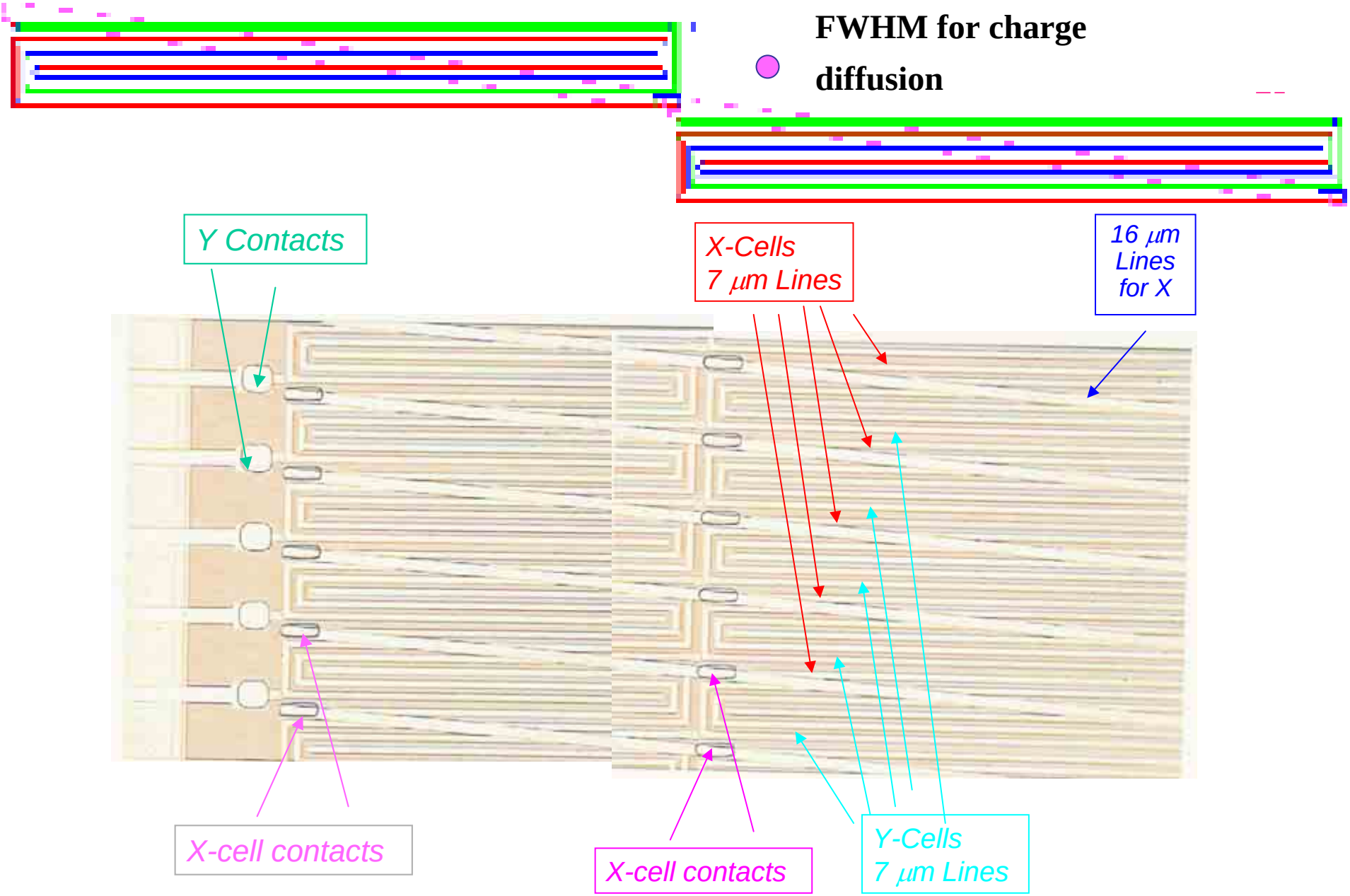
PHENIX Upgrade



Pixel pitches: 1000 μm in X, and 80 μm in Y

Pixel arrays: 30x384

4.6° stereo angle between X and Y strips


FWHM for charge diffusion
Y Contacts
X-Cells 7 μm Lines
16 μm Lines for X
X-cell contacts
X-cell contacts
Y-Cells 7 μm Lines

Issues

- Serious concern about signal to noise due to sharing and increased capacitance
- Only appropriate at certain radii?
- As strip length decreases density of readout electronics may become excessive
- Crossover point with long pixel structures

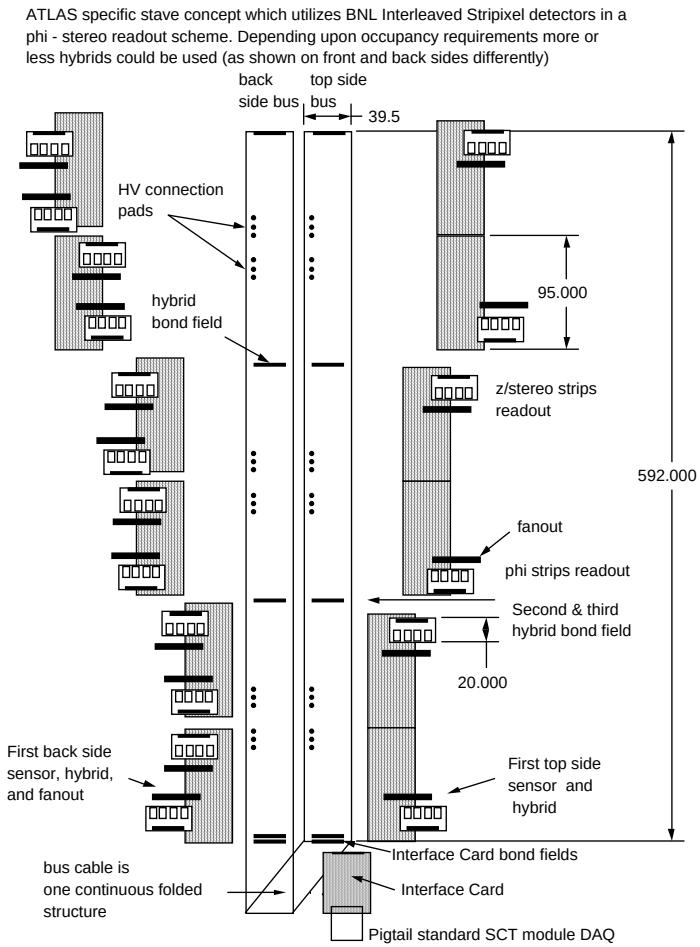
Phase 2. Milestones:

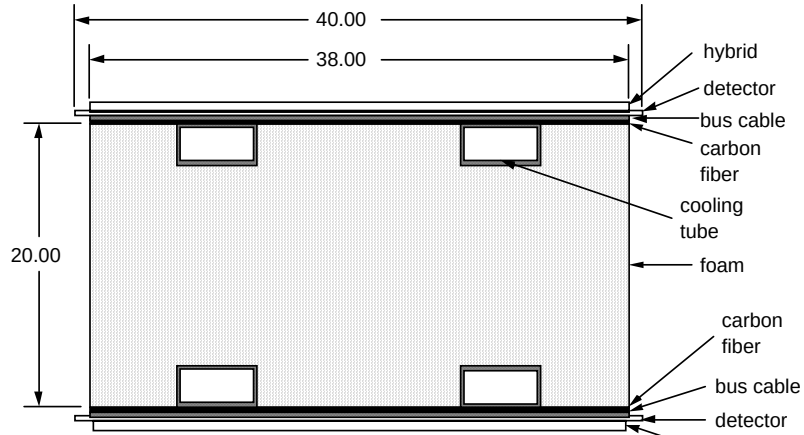
Simulations establish detector size/granularity; detector design started	03/05
Detector submitted for fabrication	04/05
Printed circuit board design begins	04/05
Circuit boards submitted for fabrication	06/05
Circuit board and detectors arrive at BNL; testing begins	08/05
Testing of detectors completed	11/05

Phase 3

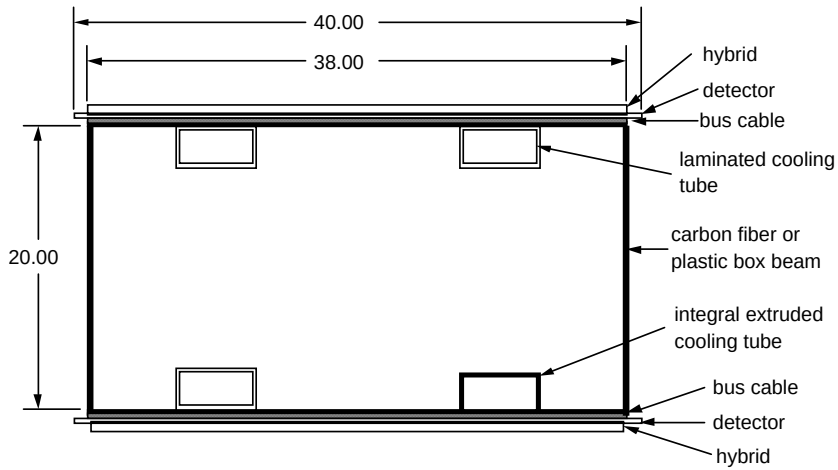
- This is an out-year effort FY06
- Configuration, region, radii to be determined from earlier phase work and simulations
- Considerable component and fixture development will be required.

Strip-pixel staves (Phase 3)





End view concept for thick stave structure based upon laminated structure



End view concept for thick stave structure based upon box beam core

For strip-pixel layer two sides Independent, therefore thicker stave is more appropriate

Budget

- Phase 1
  - LBNL $90K for hybrid development and component fabrication
  - BNL $20K for technical labor to learn assembly process
  - Hampton $20K to establish test stands
- Phase 2: BNL $35K
- Phase 3: rough estimate of $300K
- Strip-pixel development ~$50K