First Steps towards Pixel Upgrades

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Near-term (next 6-9 months):

Work on 0.13μ test chip:

- Simple 5mm^2 Test chip submitted May 10 to MOSIS

Work with 3D sensor collaboration:

- Working closely with Sherwood and Chris to evaluate 3D sensors

Longer-term (05/06):

- Continue on micro-electronics R&D and follow sensor R&D closely.

Why Now ???

- This is the last year for some time where there will be any significant irradiation or testbeam activity possible at CERN. We have on-going irradiation and testbeam plans in Oct/Nov, try to “piggyback” on this to gain basic knowledge.
- Try to make basic evaluations to help set initial directions for B-layer upgrade

Overview of Pixel Upgrades

Phased Approach:

- First phase would be a B-layer replacement after about 3-4 years of operation (2011-2012 ?). The goal would be improved performance (reduced material, improved point resolution, improved segmentation and design for higher luminosity, and design improvements for better total dose and SEU tolerance).
- Second phase would be a total ID replacement for nominal SLHC conditions of 10^{35} luminosity, perhaps after about 6-8 years of operation (2014-2016 ?). This would most probably be an “all silicon” system with improved pixels for small radii, very short strips/long pixels for intermediate radii, and low cost strips for large radii.

Comments:

- First phase is close enough that it requires significant R&D in the near future. However, it also provides an intermediate step to evaluate new concepts and take smaller evolutionary steps.
- Second phase, particularly at small radii, requires extraordinary performance. Total dose tolerance of up to 500 MRad and about 5-10 x 10^{15} n-equivalent sensor dose. Must cope with hit occupancies of several hundred MHz per cm^2, and transmit about 1Gbit/s of data per module.

Test Chip in 0.13μ IBM CMOS

Comments:

- Expect Hybrid Pixel design to remain the best approach for ATLAS. On-detector electronics needs smallest feature size CMOS process with acceptable analog performance. Present information suggests that 130nm IBM CMOS8RF_LM is good compromise. Moving to 90nm or even 65nm processes looks problematic.

Goals:

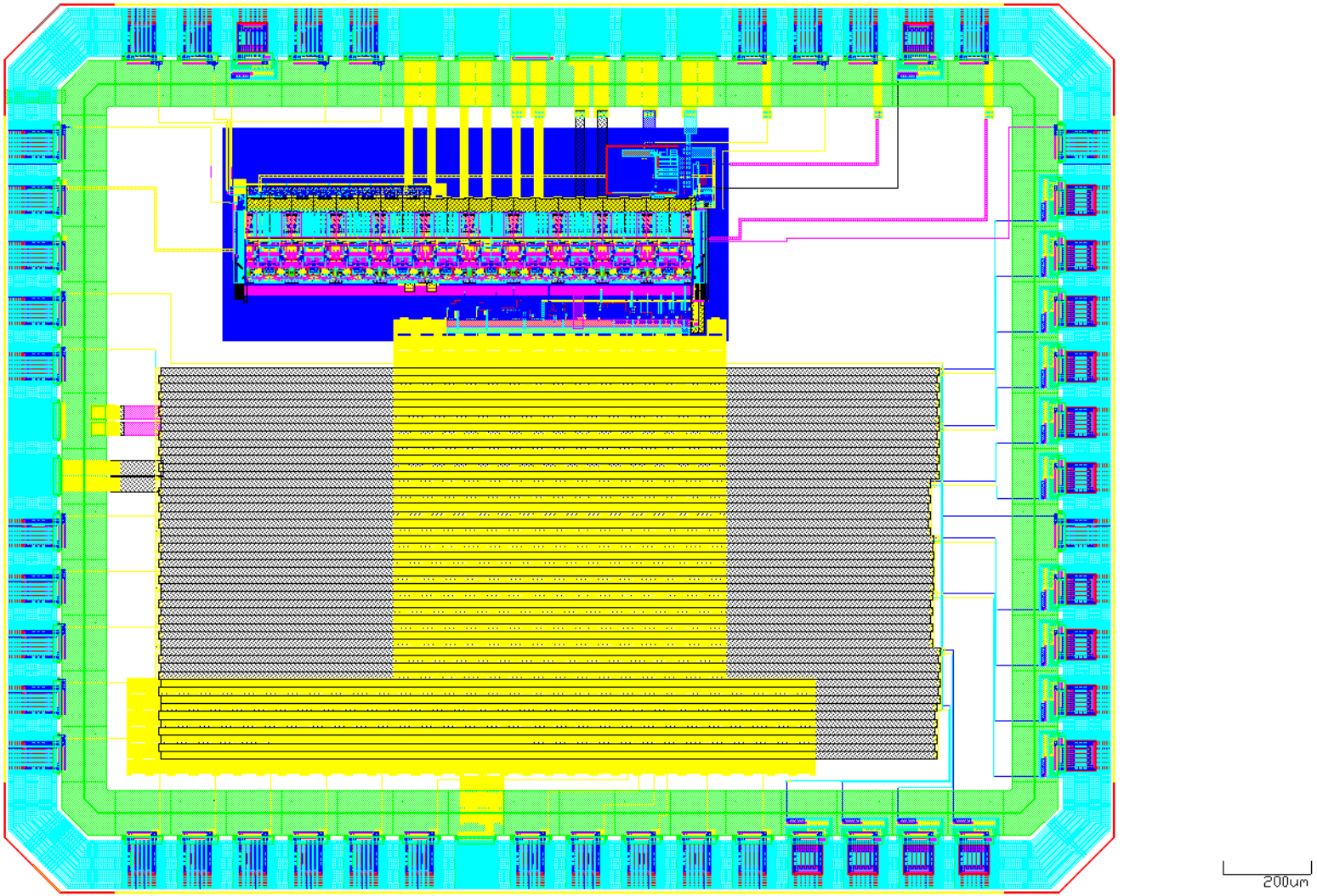
- CERN is in the process of preparing a tender for a new frame contract for DSM processes of feature size 0.13μ and beyond.
- First indications from simple test chips made by CERN MIC group are that 0.13μ is much more radiation hard than 0.25μ. It may be possible to use linear NMOS instead of annular NMOS, and the threshold shifts at large doses (50MRad) are much smaller than for 0.25μ (10's of mV).
- For now, only simple access to 0.13μ is through MOSIS (US MPW broker). They are IBMs standard MPW vendor. After discussions among interested institutes, decided that four groups wanted to prepare test chips for May 10 MOSIS submission. These groups are: CERN (basic devices and standard circuits), FNAL (pixel R&D), LBL (ATLAS pixels), and NIKHEF (general R&D).
- We defined set of modest goals in January, and worked on this in March and April, with E. Mandelli (analog) and G. Meddeler (digital) from the pixel design team.

Scope of submission:

- **Analog:** transfer elements of existing FE-I3 pixel front-end design to 0.13µ in order to gain some first experience with analog design issues in this process, and look at agreement between simulation and silicon for typical pixel circuitry.
- Approach: start with layout for FE-I3 analog front-end and control block. Remove bias compensation and auto-tuning circuitry. Modify device sizes and types to get reasonable performance in simulation. No attempt was made to improve or re-design the front-end, and the basic device sizes were left unchanged.
- A column of 20 pixel front-ends implemented, including control circuitry (pixel register and pixel latches). Readout uses Hitbus. No capacitive loads or leakage current injection available. No DACs, only individual bias mirrors and pads.
- **Digital:** transfer elements of SEU-tolerant storage cells into 0.13µ and study SEU-tolerance issues versus design, layout, and cell size.
- First, use SKIL scripts to shrink 0.25µ LBL standard cell library from FE-I3 to 0.13µ version, then remove DRC errors by hand.
- Implement structures like FE-I3 Global Register (DFF shift register with latches for storage, write/readback capability available) for several different cell designs.
- All cells are triply redundant with logic used in FE-I3 (running parity and bitflip calculations). roughly 100 bits of each type implemented.
- Cell types include Artisan latch (3µ x 4µ, linear devices), as well as Bonn pixel latch and standard cell version of pixel latch (all annular layout).

Pixel Test chip in 0.13μ IBM Process:

- Chip is 2mm x 2.5mm with 56 pads:



- MOSIS offers 8-metal CMOS8RF process with two thick metals (we use “LM version” of the process).

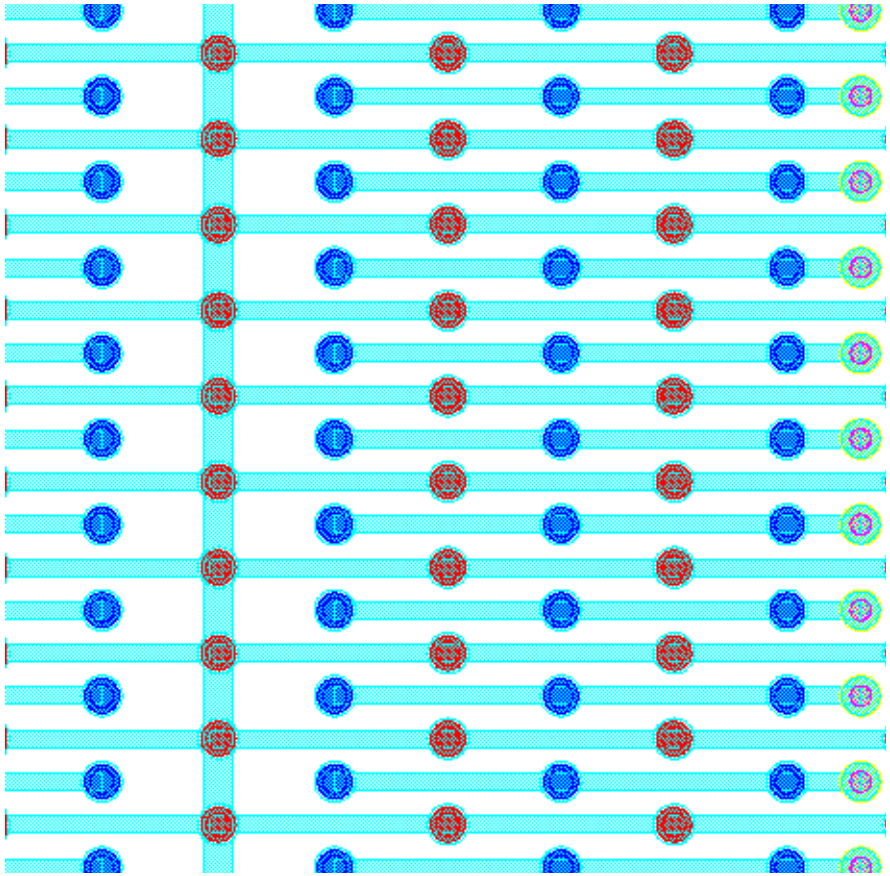
Plans:

- MOSIS has nominal delivery date for 40 die as Oct 15. Working on simple readout board for this test chip. Previous test chips used NI I/O Register to allow a laptop to act as a programmable sequencer and control and evaluate the performance. Unfortunately, with the loss of John Richardson, much of this capability must be re-created.
- Could try to evaluate the chip for total dose and SEU effects during the Oct/Nov PS irradiation (the last one before 2006 at the earliest). However, given the lack of manpower, this will be almost impossible to achieve.
- If the CERN window closes, will explore LBL 88” Cyclotron (55MeV protons, not closed yet), and Indiana Cyclotron (200 MeV protons, better for SEU studies, and used by FNAL, but charges by the hour).
- Expect to learn enough from this run so that a next test chip could contain useful new analog designs. Also expect that we should learn enough that we could choose a direction to follow for SEU-hardening of next generation FE chip.

Program to evaluate 3D sensor designs

- Sherwood Parker and Chris Kenney have been working on novel sensor design for several years, reported at pixel weeks in the past.
- The basic idea is to use an-isotropic etching to drill vertical holes through silicon wafers, and implant them with doped poly to form vertical p+ and n+ electrodes.
- This allows decoupling the charge deposition (vertical, determined by silicon wafer thickness) from charge collection (horizontal, determined by column spacing).
- In addition, they have developed an “edge-less” technology for terminating the boundary of the active sensor volume so that charge collection works well out to within a few microns of the edge (afterwards, the devices are plasma-diced).
- We have been urging them to build prototypes for us, appropriate for use with single-chip bump-bonded assemblies, so that we could evaluate the performance of this novel approach.
- Our concerns include high capacitance of the design (perhaps as high as 1pF per pixel), and in-efficient charge collection in some areas (near and inside columns).
- They have received enough support from NIH (interested primarily in edge-less techniques) to be able to carry out a small wafer-scale prototype run. This run is on 4” standard FZ material, and includes 15 ATLAS pixel compatible sensors. Two different designs have been implemented, using either 2 n+ columns per pixel or 3 n+ columns per pixel.

Region of 3 column design (GDS file for masks):



- Bias-grid region of present design is used to connect HV bias to p+ columns. These are brought to the edge of the device for wire-bond connections (awkward, but possible). Bumping pattern is identical to FE-I3. Distance between nearest p+ and n+ columns is roughly 80μ (1/3 of depletion depth required for production sensor).

Status and Plan:

- We had an extended visit in June to the Stanford Micro-systems facility where the work is being done, and discussed technical issues.
- All non-masked processing has been done (p-spray implant, field oxidation, and bonding to support wafer). Should have now completed lithography for n-type holes, but having problems with STS etcher.
- We are running out of time for evaluation during final SPS testbeam run at CERN and irradiation during final PS irradiation at CERN.

Will follow two paths for testing:

- First, provide good single FE-I3 die with AMS bumps to Chris. He will do Indium bump deposition and plasma dicing, followed by flip-chip at Stanford to produce a few samples as quickly as possible.
- Second, provide 1-2 wafers to IZM for bump deposition, dicing of one wafer quadrant (contains 10 ATLAS sensors), and flip-chip to FE-I3 single die. GDS file delivered to IZM for mask making. Probably close to 1 month turn-around once wafers are received, so only a few weeks are left before the CERN window closes.
- These tests would give us some first indications of the problems with this interesting approach. Could imagine that it would gain a factor of 3-4 in radiation tolerance compared to the present production sensor design, which could be quite interesting for a new B-layer, particularly if we are allowed to consider smaller radii at some future time !

Future Plans

- In the process of submitting proposals for R&D in micro-electronics and 3D sensors to cover the years 2005/2006. Expect that during this period, must move from basic R&D and proof-of-principle, into designs which would be optimized for a B-layer upgrade. Microelectronics R&D budget requires about 300K$/year in this scenario.
- Unfortunately, with such a schedule in mind, some key decisions/directions would be taken in the absence of actual operational experience in ATLAS with the present pixel detector.
- Goals for this period include a first pass at an optimized front-end design and readout architecture for a new FE chip, along with a well-characterized and very SEU-tolerant standard cell library for IBM 0.13μ CMOS. At this stage, it is also quite critical to have approximate sensor parameters in mind (capacitance, signal size, unit cell geometry).
- If LHC and ATLAS proceed well, could hope that by 2007, would be ready to start the upgrade project. Several years of dedicated prototyping would lead into production of the new designs on a timescale of 2009-2010, with roughly 2 years to build and test the new B-layer.
- Must also start additional R&D in power distribution (initial ideas based on small feature size SOI Power CMOS process for regulator design) and optical data transmission (much higher data rates required with minimal power increase).