MAREBO, A FULL RADHARD PIXEL DETECTOR PROTOTYPE FOR ATLAS

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ABSTRACT*: MAREBO is a radhard pixel front-end chip for ATLAS designed in the DMILL radhard BiCMOS technology. The chip is the latest generation of the ATLAS pixel chips of the FE-A prototyping programme. It has been submitted in June 1997 and received in November 1997. It contains 12 columns of 63 pixels each. The main goal of this chip is to reach LHC requirements in terms of electrical specifications and radiation tolerance. The pixel size has been extended in order to fit with existing n^+/n and diamond detectors. MAREBO has been intensively measured in lab with and without n+/n sensors and has been successfully tested in beam before and after irradiation. All these results have demonstrated that the chip meets analog electrical requirements for the ATLAS pixel detector at LHC. Irradiation measurements of the analog section are also discussed.*

I. INTRODUCTION

For many experiments, silicon pixel detectors, featuring high spatial resolution and real two-dimensional reconstruction, are of considerable interest. This interest has been recently focussed by the successful implementations of the CERN Omega [1,2] experiment and the DELPHI [3,4] detector at LEP.

In the foreseen ATLAS[5] and CMS[6] detectors at the future CERN collider (LHC), a high radiation level [7] is expected. Electronics for vertex detectors, especially for the pixel detectors which can be placed very close to the interaction point (4cm, 11cm and 14cm), requires radhard technologies. DMILL is a new radhard technology developed at CEA-LETI (Grenoble, France) and industrialized since mid 1997[8] at TEMIC/MHS (Nantes, France). It can accomodate these very severe constraints along with high speed operation, mixed analog-digital implementation and low noise needs[9,10]. It integrates monolithically PJFET, vertical NPN and CMOS devices on a thick silicon film on insulator (SIMOX plus epitaxy). The SOI substrate, along with insulating trenches, ensures complete dielectric isolation.

The very encouraging results obtained with the ATLAS pixel prototypes during the development of the DMILL technology[11,12,13] have demonstrated that the severe demanding LHC requirements can be reached. In parallel, in order to optimize the learning, time and financial contraints, 2 Front-End designs have been submitted in the AMS BiCMOS 0.8u technology: Beer&Pastis[14,15] and the real scale FE-A demonstrator (PIRATE)[15].

The MAREBO chip is the latest generation of the ATLAS pixel chips of the FE-A prototyping programme. The main goal of this chip is to meet the ATLAS pixel requirements for the analog section in a radiation hard technology. It has been designed in the DMILL rad-hard BiCMOS process and was submitted in the first Multi-Project run (MPW) offered by TEMIC/MHS in 1997. MAREBO has been successfully bump-bonded to n^+/n and diamond sensors and has been tested in the lab as well as in beam at CERN before and after irradiation.

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II. THE MAREBO CHIP

The chip has a size of 7.3mm*5.5mm with an active area of 5.2mm*3.2mm. It contains 12 columns of 63 pixels each with a layout area of 50um*397um. The actual pixel pitch is slightly larger (433.4um) in order to fit existing n^+/n as well as diamond detectors. Every pixel cell contains an analog part with a preamplifier/comparator circuit for negative input polarity, a 3-bit DAC for threshold fine adjust, a readout section for time tagging and analog information using the Time-Over-Threshold technique[16], and a control section which allows to inject and mask pixels, load DAC values and to monitor the discriminator signals through the hitbus (fastOR).

The circuits of the analog part and of the control section are nearly identical to the circuits implemented in the ATLAS pixel FE-A demonstrator (PIRATE) such that a comparison of the level of integration in DMILL and the AMS BiCMOS 0.8u technology (Austria Mikro Systeme) is possible: the size of the analog parts is almost identical (144 µm for DMILL and 141 µm for AMS including the bump bond pad) while the control logic takes 20% more space in DMILL. Every transistor is isolated by insulating trenches in DMILL but the «trench to trench» rule is half as stringent as the «well to well» or «active to well» rules in a standard technology. The transfer to DMILL has nearly no impact on the analog layout size because transistors in analog designs have usually dedicated substrate connections. In digital layouts, which are principally larger in DMILL than in AMS, the wells can be merged to avoid the «well to well» rule so that they can be shrunk by about 20% with respect to standard DMILL layouts. Nevertheless the size of the DMILL design is only slightly larger than the present AMS design.

The Fig. 1. depicts the layout of the pixel cell.

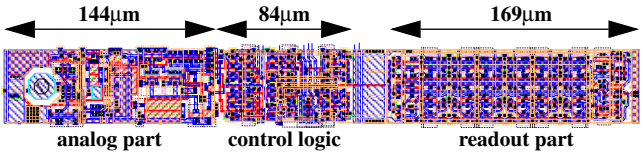

Fig. 1. layout of the pixel cell

The nomimal power consumption is 40µW per cell.

III. CHIP PERFORMANCE

The amplifier is a folded cascode charge sensitive amplifier with a feedback capacitance of 3 fF buffered by a nMOS source follower. These two full-CMOS stages are fed back by an improved version of the DC feedback circuit already proven in the previous chips[13]. Special attention has been paid to simulate the cell with worst case models which include process variation and parameter shifts after high levels of irradiation.

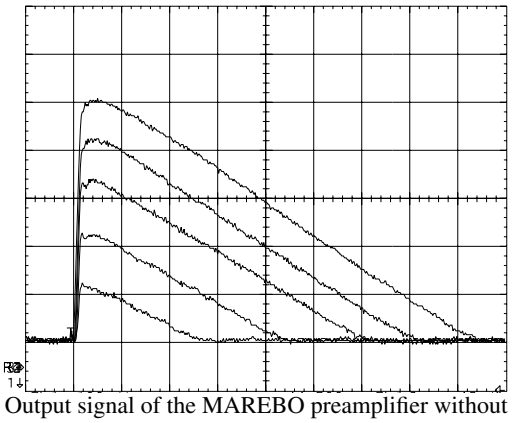

Fig. 2. Output signal of the MAREBO preamplifier without detector: Input charges of 5, 10, 15, 20 and 25 ke (horiz. scale: 200 ns per div., vert. scale: 200 mV per div.).

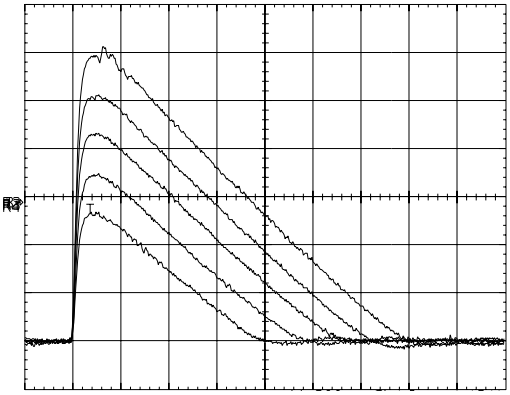

Fig. 3. Output signal of the MAREBO preamplifier with detector: Input charges of 6, 8, 10, 12 and 14 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).

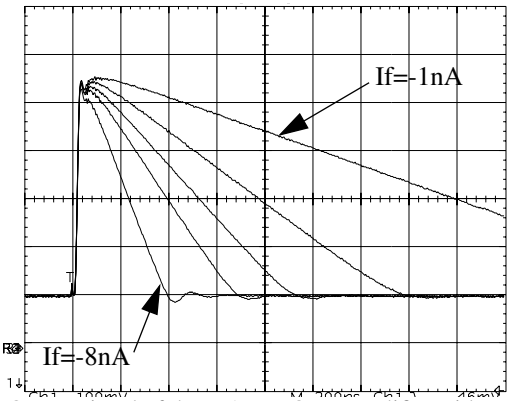

Fig. 4. Output signal of the MAREBO preamplifier without detector: Feedback current of 1, 2, 3, 4 and 8 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).

Fig. 2 to Fig. 5. show the output of the MAREBO charge sensitive amplifier monitored through an on-chip buffer with a gain of about 0.95 for various input charges, feedback currents with and without detector. Charge is injected by applying a voltage step to a capacitor in the pixel cell. All measurements are taken at the nominal power consumption of 40 μW for the analog part of the pixel.

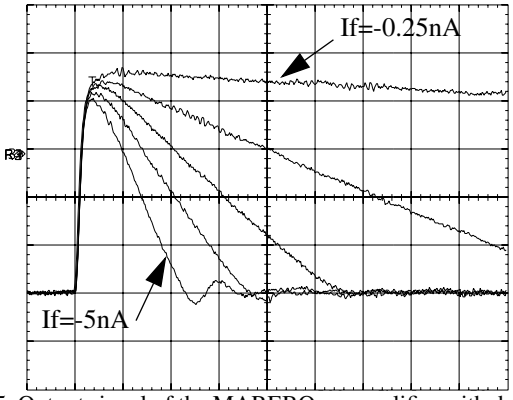

Fig. 5. Output signal of the MAREBO preamplifier with detector: Feedback current of 0.25, 1, 2, 3 and 5 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.).

Fig. 2. shows the response to various input charges without detector. The slope of the recovery period (fixed by the feedback current) remains constant at different input charges and the gain ($1/C_f$) corresponds well to the value expected by simulation. Fig. 3. shows a similar measurement with detector. The rise time increases insignificantly due to the extra input capacitance presented by the sensor diode and no significant reduction of signal amplitude is observed. Fig. 4. depicts the response for different feedback currents for constant input charge without detector. The amplifier remains stable even for shaping times in the range of the rise time. The ballistic deficit is small even for very fast shaping. Fig. 5. shows a similar measurement with detector. Also in this case, there is only a very small ballistic deficit. All these measurements demonstrate that the additional input capacitance due to connected sensor diode (which in this case is even 50% larger than planned for ATLAS) does not significantly degrade the transient performance and the stability of the preamplifier.

The discriminator is AC coupled to the amplifier. Its input stage is implemented with a differentiel pair of bipolar transistors for speed and matching purposes. A fast response of the preamplifier/discriminator system is needed for ATLAS in order to correctly associate a hit to a 25ns wide bunch crossing interval. Special attention has therefore been paid to reduce the minimum charge above threshold that can be tagged within a window of 25 ns relatively to a very large signal. This goal was achieved by forcing the input bipolar transistor going into its linear region and, consequently, slow down the discriminator for input charges above a MIP. Fig. 6. and 7, depict the response time of the pixel cell versus the injected charge above the threshold for 3 different input loads measured at threshold settings between 2000 e and 2900 e. The slowing down of the discriminator for large charges is clearly visible such that the

response time is minimal already for charges around 24 ke.

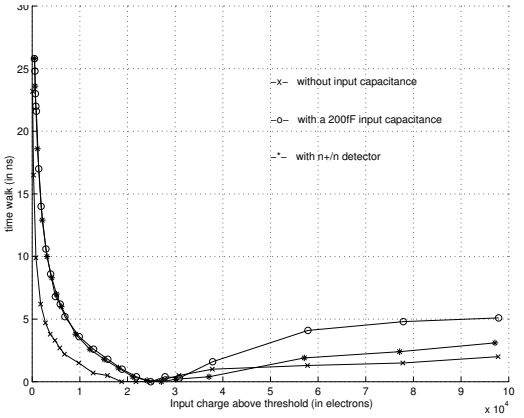

Fig. 6. Response of the pixel cell as a function of the injected charge above a threshold of 2200 e for an amplifier without input capacitance, a threshold of 2200 e for an amplifier whose input has been connected to a 200 fF test capacitor and a threshold of 2900 e for an amplifier connected to a sensor diode.

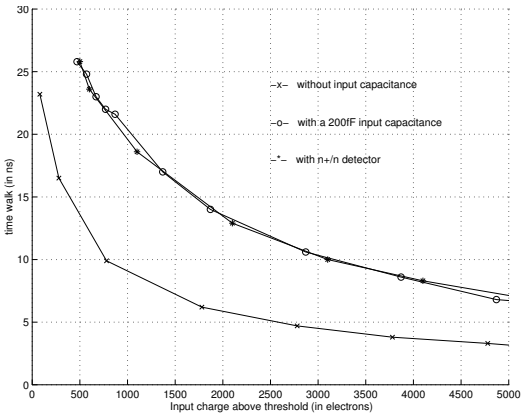

Fig. 7. Zoom-in of Fig. 6.

This technique allows the minimum charge to be reduced to 500-600 electrons above the threshold for a pixel cell with detector. The time walk decreases even further at higher thresholds. The width of the discriminator output signal increases linearly (within a certain range) with the input charge due to the very linear falling edge of the preamplifier output signal so that a TOT amplitude information can be obtained with 4-5 bits resolution.

The leakage current tolerance of the preamplifier/feedback configuration (the sensor is DC coupled) is one of the most critical points in reaching the LHC specification. Fig. 8. shows that the variation in pixel threshold remains in a range of a few hundred electrons even for leakage currents as high as 100 nA, which is more than expected after 10 years of LHC operation. As depicted in Fig. 9., the behavior of the charge sensitive amplifier at leakage currents of 0 nA, 25 nA, 50 nA, 75 nA and 100 nA shows that the shaping time is slightly decreased but tends to saturate after 50 nA. This effect is clearly demonstrated when very high leakage currents are injected, and tests show that the threshold is only slightly increased even after values greater than 200 nA.

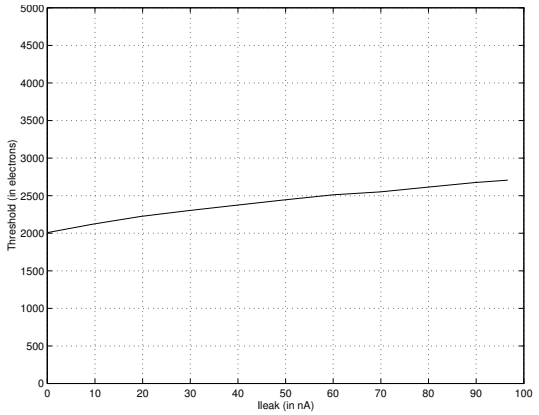

Fig. 8. Measured threshold of a pixel cell versus leakage current (measured on a test structure with additional leakage current source)

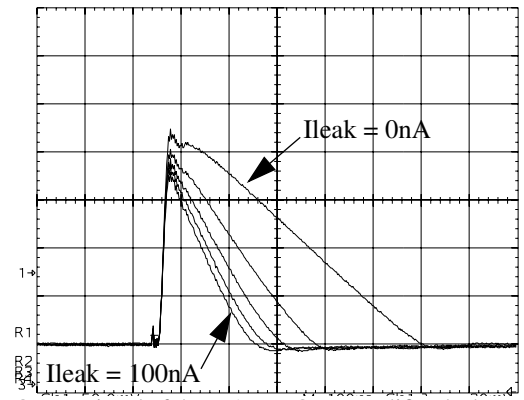

Fig. 9. Output signal of the MAREBO preamplifier, leakage current of 0, 25, 50, 75 and 100 nA with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.)

The cell-to-cell threshold mismatch is a crucial point for realizing an accurate pixel detector. In particular, it determines the minimum threshold that can be set. Pixels with thresholds much lower than the avarage value would produce too many noise hits. Although good dispersion results were obtained without independent pixel adjust on the previous Beer&Pastis chip (σ = 90e, [14,15]) and on the MAREBO chip (σ = 93e, see Fig. 10.), a 3-bit DAC for threshold fine tuning has been implemented in each cell in order to eliminate tails in the dispersion distribution and to adjust the thresholds after high level of irradiation when random parameter shifts of detector and electronics may occur and the available charge will be smaller. This fine-tuned threshold is based on a network of switched pMOS resistors which locally control the comparator bias system. The 3 bits are statically stored in registers in the control logic part of every pixel. They are loaded via a shift register which runs across all pixel cells. A control current I_{trim} is used to set the range of thresholds covered by the DAC, i.e. the threshold shift per LSB (least significant bit). Fig. 11 shows the response of the same pixel for increasing input charges for the 8 possible DAC settings. The threshold change by about 100 e per LSB for I_{trim}= 1μA is in accordance with the simulation. The threshold change per LSB is a linear function of I_{trim} and the DAC itself has a differential non-linearity of 14% which is better

than required for this application. No extra noise is induced by the adjustment circuit. Fig. 10. depicts the distribution of the thresholds of a complete chip before and after threshold tuning. The tuning is performed in a two step operation, First, the I_{trim} value is determined by searching for the largest variations, second the DAC bits are calculated. The spread after adjustment is reduced to 40 e.

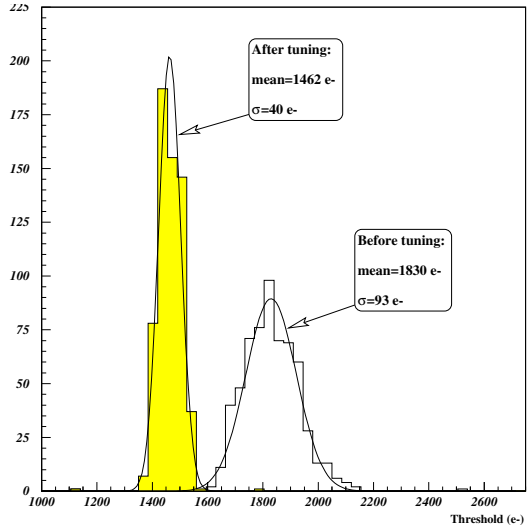

Fig. 10. Distribution of the array threshold before and after adjustment

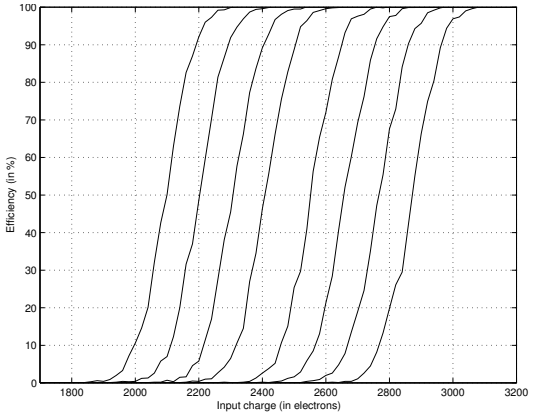

Fig. 11. Discriminator response for increasing input charge for the 8 possible DAC settings for I_{trim} = 1µA.

The cross-coupling between pixels with bump bonded sensor is defined as the ratio of the signal induced on one neighbour and the signal on the central pixel. Note that the pixels of the MAREBO chip have a length of 433.4 µm so that an increased cross coupling compared to 300 µm is expected. The method for measuring crosscoupling is described below. Using the on-chip injection circuitry, the threshold of an arbitrary pixel is determined. The pixel is then pulsed together with one or two neighbours. Due to cross coupling, a smaller injected charge is enough to fire the central pixel in 50% of the injections so that effectively, a threshold reduction is observed. For threholds of typically 3000 e, 5000 e and 9000 e, shifts are observed when one neighbour is also injected. This leads to a cross coupling of 2%.

IV. IRRADIATION OF MAREBO

MAREBO has been irradiated in a 24 GeV proton beam at PS (CERN). The maximum flux was 2.00 10^{13} p $cm^{-2}h^{-1}$ (note that this flux was reached by performing a complete beam

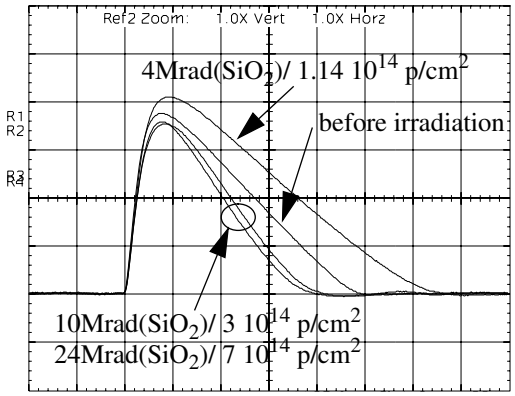

Fig. 12. Output signal of the MAREBO preamplifier after dose/ fluence of 0, 4Mrad(SiO_2)/1.1410^{14}p/cm^2, 10Mrad(SiO_2)/3 10^{14}p/ cm^2 and 24Mrad(SiO_2)/7 10^{14}p/cm^2 with constant input charge of 10 ke (horiz. scale: 200 ns per div., vert. scale: 100 mV per div.) The peaking time is increased due to extra-load presented during irradiation

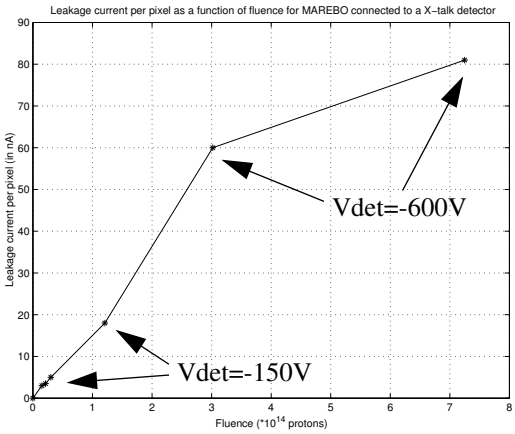

Fig. 13. Measured leakage current of the sensor versus the fluence (the detector voltage has been increased from -150V to -600V during irradiation).

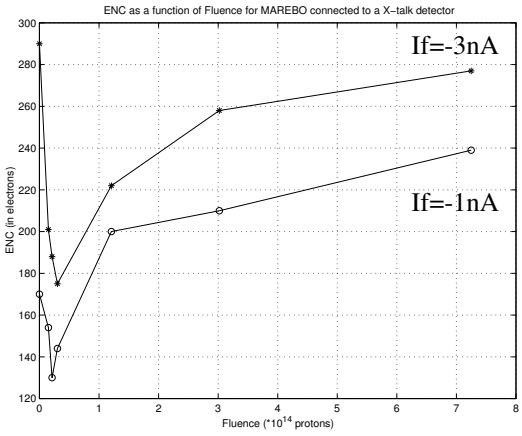

Fig. 14. Measured Equivalent Noise Charge versus fluence for 2 different feedback current, i.e. 2 different recovery time.

profile using one pixel of a MAREBO chip connected to a sensor) and the nominal temperature during and after irradiation was -7°C. In total, 4 MAREBO chips connected to a sensor and 2 MAREBO chips without detector have been irradiated and out of these 6, one MAREBO chip with detector and one without detector have been tested on-line.

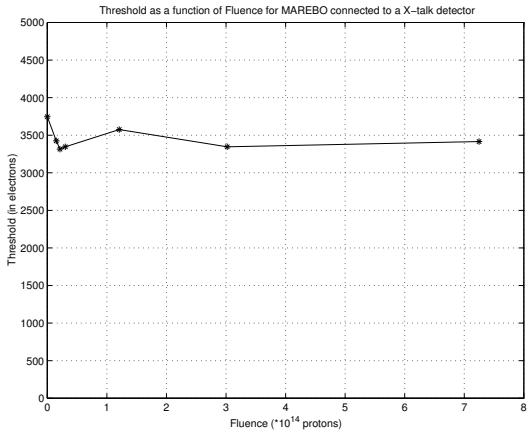

Fig. 15. Measured threshold variation of the pixel cell versus fluence.

Fig. 12. to 15. show different on-line measurements performed on the MAREBO chip connected to a detector. The different steps during irradiation are for cumulated dose/fluence: before irradiation, 0.5Mrad(SiO_2)/1.48 10^{13}p.cm^{-2}, 1Mrad(SiO_2)/2.83 10^{13}p.cm^{-2}, 4Mrad(SiO_2)/1.14 10^{14}p.cm^{-2}, 10Mrad(SiO_2)/3 10^{14}p.cm^{-2}, 24Mrad(SiO_2)/7 10^{14}p.cm^{-2}.

Fig. 12. depicts the preamplifier output signal before irradiation, after 4 Mrad, after 10 Mrad and after 24 Mrad. First, an increase of the signal amplitude is observed between 0 and 4 Mrad due to a large decrease of the sensor inter-pixel capacitance, which is the main part of the capacitor presented at the input of each pixel cell. This behaviour is clearly confirmed in Fig. 14. which shows the Equivalent Noise Charge (ENC) decreased in a factor of 2 (note that this kind of detector presents before irradiation a capacitor 50% higher than the one given by the standard ATLAS sensor). This effect occurs around the type inversion fluence of the sensor substrate (8.7 10^{13}p.cm^{-2}) where the quite intrinsic silicon substrate changes the detector properties. At this point, the leakage current plays no role (see Fig. 13.) and the serial noise is the dominant contribution in the ENC. Secondly, the preamplifier output signal presents a faster return to baseline at doses of 10 Mrad and 24 Mrad, showing a consequent increase of sensor leakage current (-60nA to -80nA as indicated in Fig. 13.). This is also confirmed by the higher values of the ENC (see Fig. 14.) demonstrating a larger contribution of the parallel noise.

Fig. 15 shows that the threshold remains in a range of a few hundred electrons even after very high dose. Only minor changes have been applied to the bias system (At 24Mrad, the voltage that controls the threshold has been increased of 0.1V as well as the analog power supply).

These results demonstrate that the analog part along with the n$^+$/n sensor remain fully functional even after level of irradiation as high as the one expected at the first ATLAS pixel layer (11cm from the beam pipe).

V. TEST BEAM BEFORE AND AFTER IRRADIATION

MAREBO has been tested in beam at H8 (CERN). As several chips were tested before irradiation during the May-June 1998 programme, the August-September 1998 period was used to test irradiated chips (kept at -7°C). The threshold was 3500e.

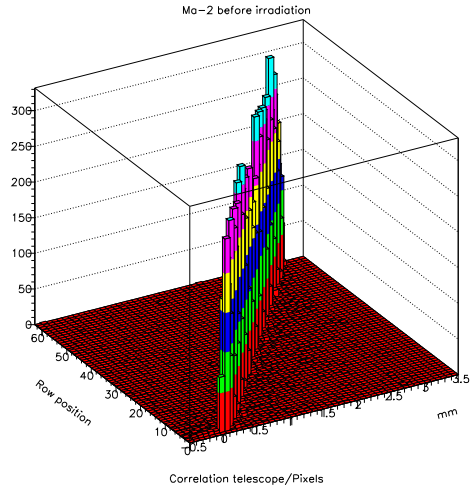

Fig. 16. Correlation between pixel position and telescope prediction for MAREBO 2 before irradiation.

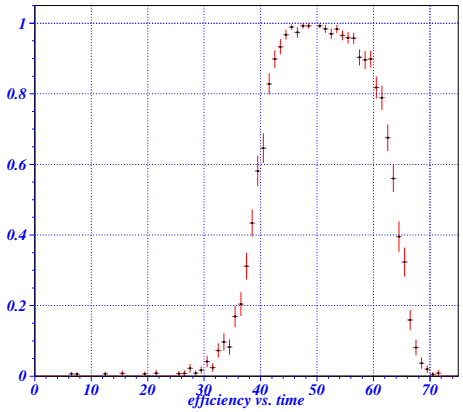

Fig. 17. Efficiency versus trigger delay for MAREBO 2 before irradiation.

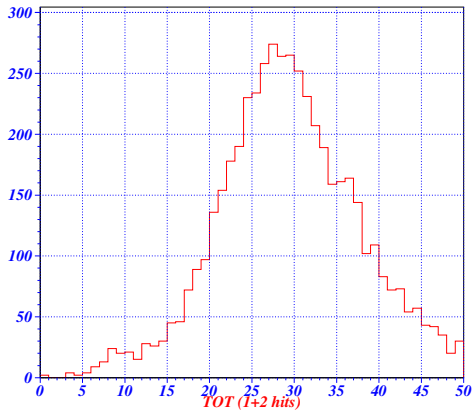

Fig. 18. Analog information using the TOT technique for MAREBO 2 before irradiation (for a single hit pixel or 2 adjacent hit pixels).

Fig. 16. to 18. are issued from data taken on MAREBO before irradiation. Fig. 16. shows the perfect correlation between telescope prediction and pixel position for one of the MAREBO chip. Fig. 17. depicts its efficiency versus trigger delay. As the incoming particule is not synchronized to the 40MHz clock used to transfer data out the chip, the «In-Time» efficiency depends on the delay between the generated trigger with respect to the rising edge of the clock signal[17]. Fig. 17. has been reconstructed using a Time to Digital Convertor (TDC) and shows an efficiency of more than 99% along with a large plateau (which will drastically ease the tune of the trigger delay for a huge number of chips at LHC). Fig.18. shows the analog information and the MIP is clearly visible (typ. 27 bunch crossing periods).

Fig. 19. to 21. depicts the same measurements on the same MAREBO chip after 24Mrad(SiO_2)/7 10^{14}p.cm^{-2}. A perfect correlation between telescope prediction and pixel position is observed (Fig. 19.) as well as an efficiency of more than 95% (Fig. 20.). The change (before and after irradiation) between the absolute trigger delay is due to different Lemo cables. A time reduction of the TOT is observed (Fig. 21.) after high level of irradiation. This effect is due to the faster shaping time of the preamplifier output signal (see chapter IV.) and the reduction of created charges in the sensor (At this point, the detector is partially depleted).

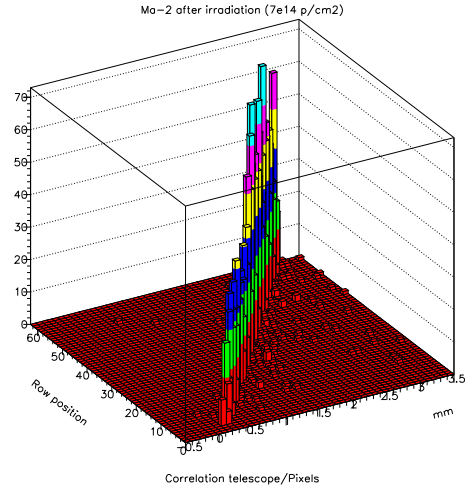

Fig. 19. Correlation between pixel position and telescope prediction for MAREBO 2 after 24Mrad(SiO_2)/7 10^{14}p.cm^{-2}.

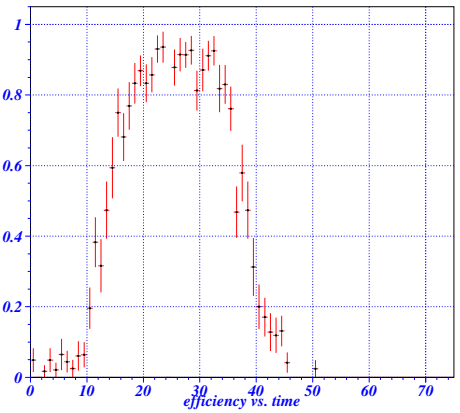

Fig. 20. Efficiency versus trigger delay for MAREBO 2 after 24Mrad(SiO_2)/7 10^{14}p.cm^{-2}.

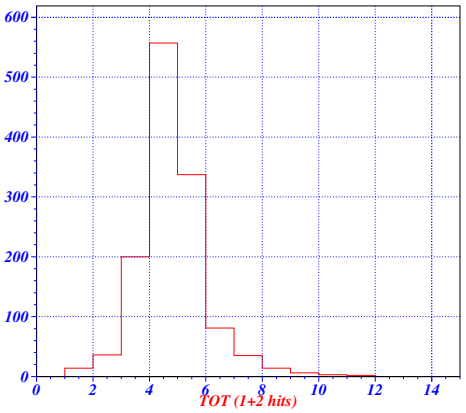

Fig. 21. Analog information using the TOT technique for MAREBO 2 after 24Mrad(SiO_2)/7 10^{14}p.cm^{-2} (for a single hit pixel or 2 adjacent hit pixels).

VI. CONCLUSION

Lab tests as well as beam tests before and after irradiation have demonstrated that the MAREBO chip meets the demanding LHC requirements for the analog section in a radiation hard technology. This is the first radhard package (electronics+sensor) for the ATLAS pixel detector which remains fully functional in beam after very high level of irradiation.

The analog front-end of the MAREBO chip will be implemented in the DMILL full scale demonstrator by the beginning of 1999.

MAREBO chips connected to diamond detector are currently under test and will be tested in beam in the very near future.

VII. ACKNOWLEDGMENT

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