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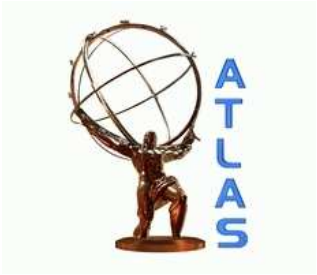

ATLAS NOTE

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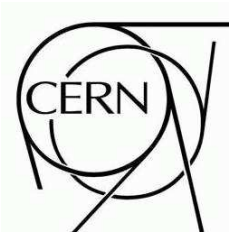

The ATLAS Pixel Detector

The Pixel Collaboration

Abstract

4 Electronics Systems

Ref. [1, 2] Inner Detector and Pixel TDR.

4.1 Overview

4.1.1 System Architecture

expand

4.2 Front End Integrated Circuit

Description of the bibliography for the FE chip. For editor use, to delete in the paper.

Ref. [3]

Ref. [4] Beam test results from M72b and Bier&Pastis. Bierr & Pastis description with measurements.

Ref. [5] Description of the CPPM/Bonn Analog/Digital architecture. Measurements of the Bear&Pastis.

Ref. [6] FE-B. Description of the dual threshold discriminator. Simulations of behaviour.

Ref. [7] Describes FE-B architecture. No measurements.

Ref. [8] Paper describing FE-A/B/C and evolution to FE-D.

Ref. [9] Description of the analog FE-I1 cell. New DC feed-back.

Ref. [10] Description and measurements of FE-I2

Ref. [11] Good article with FE-I3 Architecture description. Describes analog and digital architectures. Limited results reported (basically only threshold curves)

Ref. [12] Measurements and irradiation results on FE-I3

4.2.1 Front-end Chip History

ATLAS Pixel front-end design comes from the joint effort of 3 collaborating institutes: Bonn [1)], CPPM[2)] and LBNL[3)]. Small scale chips to demonstrate analog and digital architecture have been developed in the second half of '90: "M72b" at LBL, Lepton at CPPM, Marebo and Bier & Pastis at Bonn/CPPM. The first rad-soft functional prototypes of full size chips where submitted in '98: FE-B al LBNL, FE-A/C (Pirate) at Bonn/CPPM. FE-B was designed using $0.8\mu m$ HP[4)] CMOS technology and had the same basic readout architecture that will be used in the final chips. FE-B charge amplifier uses a direct cascode and source follower, feedback capacitance of 4 fF, DC feedback based on Marebo design. Discriminator uses a dual threshold, low threshold for precise timing, high threshold for validate the hit. FE-A was made on $0.8\mu m$ BiCMOS technology from AMS[5)], whereas FE-C was a full CMOS version. The charge amplifier uses a folded cascode input stage with feedback capacitance of 3 fF and a new improved DC feedback. Discriminator is AC coupled, with an input fully differential bipolar pair in

[1)] Physics Department of the Bonn University
[2)] Centre de Physique des Particules de Marseille
[3)] Lawrence Berkeley National Laboratory
[4)] reference HP
[5)] reference AMS

the A version and CMOS in the C. Column readout architecture uses an always running shift register to transport the hit address to the bottom of the chip. Hits are associated to the level 1 trigger (L1) by counting the number of clock cycles needed to hit to reach the column bottom. FE-A/B/C demonstrated all basic ATLAS pixel performance goals in lab and testbeam. The chip from now on were developed using the basic concept of the amplifier/discriminator from FE-A/C and the column readout architecture from FE-C. The European and LBNL front-end design efforts joined forces to combine all of the experience gained with radiation-soft chips into a common layout for the DMILL[6)] technology (known as FE-D). FE-D1 was submitted in July '99 together with DORIC and VDC chips and prototype MCC-D0. A new production run was submitted in Aug '00 with two versions of FE-D2: one with dynamic and the other with static memory cells. Run included full MCC-D2 and new DORIC and VDC chips as well. Yield on both FE and MCC was unacceptable and work with this vendor was terminated. Work on FE-H began in Dec '99 [7]. Chip was almost ready but was never submitted also because of massive cost increases from Honeywell. The failure of both traditional rad-hard vendors left the collaboration with Deep Sub-micron (DSM) approach, based on commercial process $0.25\mu m$ CMOS process and rad-tolerant layout. Major effort started in Sep '00. Three version were submitted using an IBM silicon foundry. Final chip (FE-I3) was available in late '03. Table 1 is a summary of front-end designs developed for the ATLAS Pixel detector.

Chip	Year	Cell size (μm^2)	Col × Row	# Trans.	Technology	References
M72b	??	50×536	12×64	??	HP $0.8\mu m$ CMOS, 2M ??	[4]
Marebo	??	??	12×63	??	DMILL $0.8\mu m$ BiCMOS 2M	–
Beer & Pastis	??	50×436	12×63	??	AMS $0.8\mu m$ BiCMOS, 2M	[4, 5]
FE-B	1998	50×400	18×160	??	HP $0.8\mu m$ CMOS, 2M ??	[6–8]
FE-A/C	1998 (?)	50×400	18×160	??	AMS $0.8\mu m$ BiCMOS, 2M	[5, 8]
FE-D1	1999	50×400	18×160	??	DMILL $0.8\mu m$ BiCMOS 2M	[8]
FE-D2	2000	50×400	18×160	??	DMILL $0.8\mu m$ BiCMOS 2M	–
FE-I1	200x	50×400	18×160	??	IBM $0.25\mu m$ CMOS, 6M, 1P	[9]
FE-I2/I2.1	2003	50×400	18×160	2.5 M	IBM $0.25\mu m$ CMOS, 6M	[10]
FE-I3	2003	50×400	18×160	3.5 M	IBM $0.25\mu m$ CMOS, 6M	[11, 12]

Table 1: Summary of the ATLAS Pixel front-end chips.

4.2.2 Current Design

Chip Architecture.
The readout chip for the ATLAS pixel detector [11] shown in Fig. 1 contains 2880 readout cells of $50\mu m \times 400\mu m$ size arranged in a 18×160 matrix. Each readout cell contains an analogue block where the sensor charge signal is amplified and compared to a programmable threshold by a discriminator. The digital readout part transfers the hit pixel address, a hit time stamp and a digitized amplitude information, the time over threshold (ToT) to buffers at the chip periphery. These hit buffers monitor the age of each stored hit by inspecting the associated time stamp. When a hit becomes older than the latency of the Level 1 trigger (3.2 μ s) and no trigger signal has occurred, the hit information is deleted. Hits which are marked by trigger signals are selected for readout. Triggered hit data are transmitted serially out of the chip in the same order of trigger arrival.

Charge Sensitive Preamplifier.
The charge sensitive amplifier uses a single-ended folded-cascode topology, which is a common choice

[6)] reference DMILL

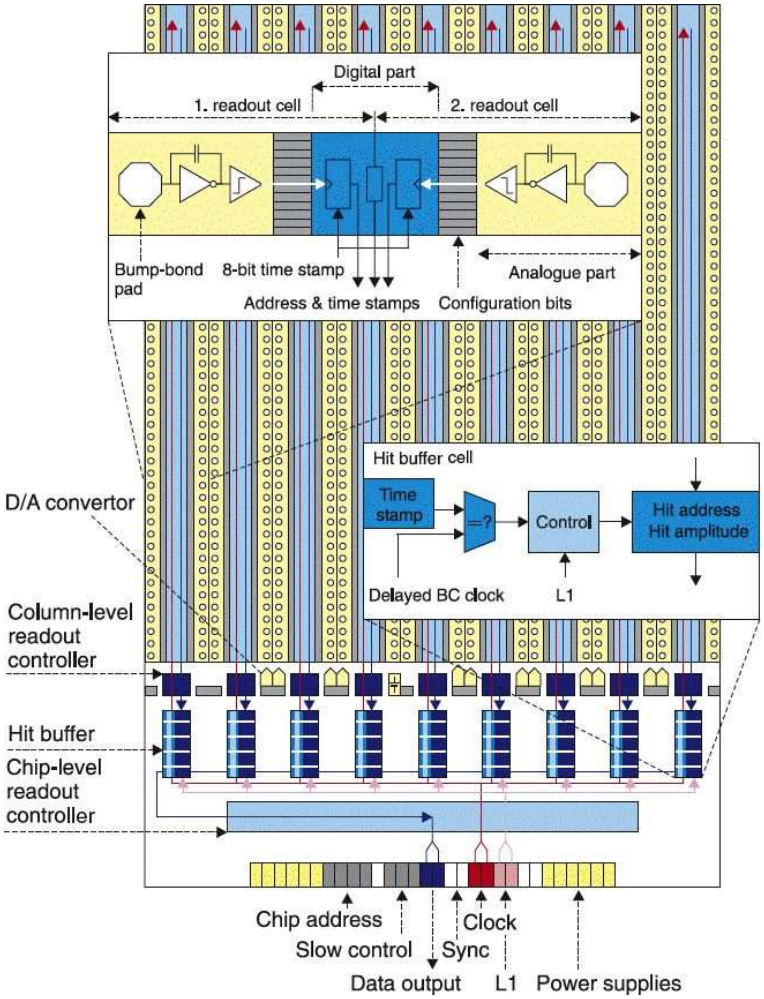

Figure 1: Simplified floorplan of the front-end chip (FE-I3) with main functional elements.

for low-voltage and high gain amplifiers. The amplifier is optimised for a nominal capacitive load of 400 fF and designed for negative signal expected from $n^+ - on - n - bulk$ detectors. Special attention was put in the design of the charge amplifier to the requirement of irradiated sensors, where the leakage current (50 nA) is two order of magnitude bigger than the signal (5000 e), which is reduced by carrier trapping inside the silicon. The preamplifier has roughly $5fF$ DC feedback design, $15ns$ risetime and operates at about $8\mu A$ bias. To fulfil the above requirements of sensor leakage current, a compensation circuit is implemented which drains the leakage current and prevents it to influence the bias current of the fast feedback circuit used to discharge the feedback capacitor. The feedback system, shown in Fig. 2 uses two PMOS devices, one (M2) providing leakage current compensation and the other (M1) continuous reset of the feedback capacitor. An important property of this feedback circuit is that the discharge current pro-

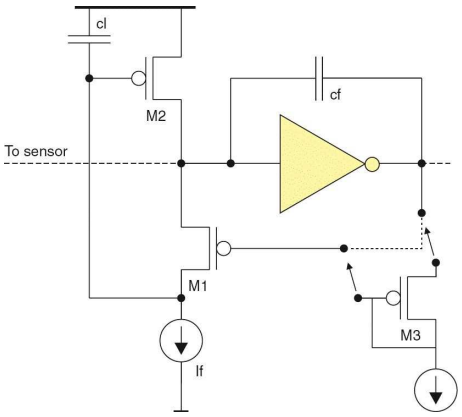

Figure 2: Charge preamplifier: feedback circuit.

vided by the reset device saturates for high output signal amplitudes. The return to baseline is therefore nearly linear and a pulse width proportional to the input charge is obtained. The width of the discriminator output, Time-over-Threshold (ToT), can therefore be used to measure the signal amplitude. Feedback current is $4nA$ for $1\mu s$ return to baseline and $20ke$ input. The feedback circuit used in FE-I3 has an additional diode-connected transistor M3, which acts as a level shifter so that the DC levels of input and output nodes are nearly equal. It also simplifies the DC coupling between amplifier and the following comparator.

Comparator.
Signal discrimination is made by a two stage-circuit: a fully differential low gain amplifier, where threshold control operates by modifying the input offset, and a DC-coupled differential comparator. The first stage has a bias of about $4\mu A$ whereas the second uses a current of about $5\mu A$. In order to make the threshold independent of the local VDDREF and on the amplifier bias current I_f, a local threshold generator is integrated in every pixel. 7-bits are used in each pixel to adjust the discriminator threshold.

Pixel Cell Control Logic.
A complete block diagram of the analogue part with several additional circuit blocks is shown in Fig. **??**. Each pixel has several parameter that can be tuned through a 14-bit control register. Those bits are:

- *FDAC 0-2:* 3-bits to trim the feedback I_f current for tuning the ToT response.
- *TDAC 0-6:* 7-bits to trim the threshold in each pixel.
- *MASK:* the digital output of the analogue part can be switched off locally by setting this bit.

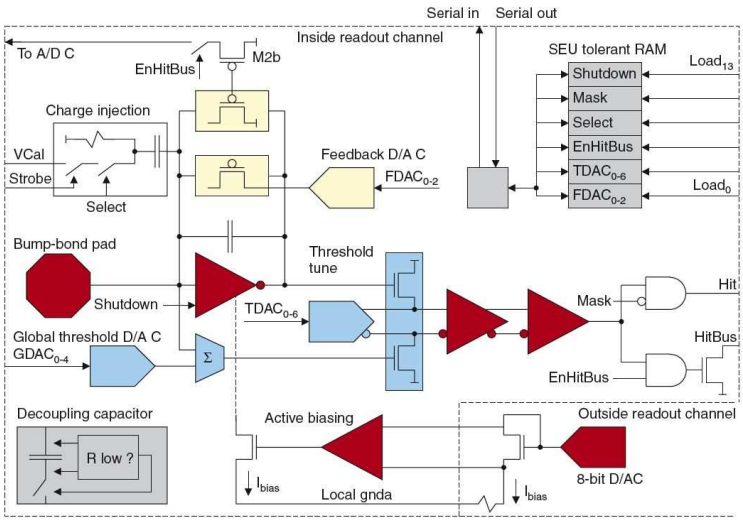

Figure 3: Pixel cell block diagram.

- *EnHitBus:* the digital outputs of all readout channels can be directly observed using a wired OR which is locally enabled with this bit. This bit bit also controls, through transistor M2b, the summing of a current proportional to the feedback plus leakage current in the preamp, allowing the monitoring of the feedback current and of the leakage current from the sensor.

- *Select:* enables the pixel for test charge injection. Amplitude is generated from *VCal* whereas timing comes from an external *Strobe* signal.

- Shutdown: disables the charge amplifier therefore no output is generated from the pixel.

Pixel Cell Readout Logic.
A block diagram of the column-pair readout is shown in Fig. 4. The digital circuitry in the readout cells generates hit information: time of leading edge (LE), time of trailing edge (TE) for ToT calculation, row address. All of this information is temporarily stored in local memories before being transferred to the hit buffers at the chip periphery. A digital circuitry generates two short (1*ns*) strobes at the LE and TE discriminator signals, respectively. These signals are used to store the 8-bit Gray-coded time stamp into two memories. The time stamps, generated at the chip periphery, running at 40 MHz are distributed differentially, in order to decrease the digital crosstalk, to analogue circuits and sensor electrodes. The complete hit information is available after the TE of the comparator signal and data transfer can start. Time stamp of the LE (8-bits) of the TE (8-bits) and the row number (8-bits) are transferred to the end-of-column (EoC) buffers. Transfer happens by a priority mechanism that selects cells with data starting from the top row. The top most cell with a hit puts the data on the bus and all the cell below it are inhibit. When the cell is readout, it releases the priority encoder bus and the next coming hit is selected and put on the readout bus. The readout speed is limited by the time the priority logic needs to ripple down. Hits can ripple through at programmable speed that is obtained from the 40 MHz clock division. In the actual chip, the maximum speed to transfer a single hit to the EoC is 20 MHz.

Column Readout Controller.
Readout is column based, and two columns are readout from the same controller. The first task of the controller is the generation of the readout sequence to transfer hit information: LE and TE timestamp, plus pixel row address into an EoC buffer. This operation begins when data is complete, which is after dis-

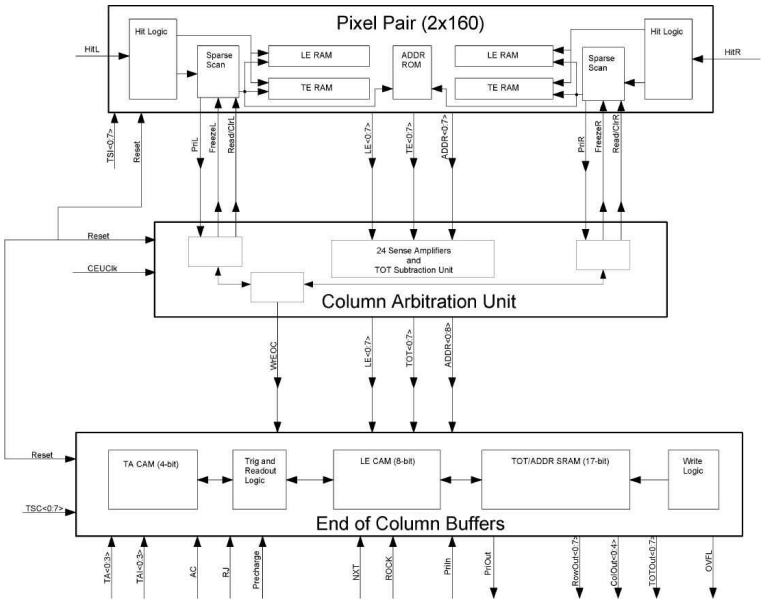

Figure 4: Block diagram of the column-pair readout (picture must be redrawn and simplified).

criminator TE. The transfer of hits from a column pair is synchronized by the Controller end-of-columnn Unit (CEU), which operates at a speed of 5, 10, or 20 MHz. A total of 64-hit buffers are available for each double-column.

The second task is some digital processing of the hit data. Hit information is formatted by the CEU. Formatting includes ToT calculation: subtraction of TE time stamp from LE timestamp. Optionally, a digital threshold may be applied to ToT, a timewalk correction may be applied (write hit twice if below correction threshold, once with LE and once with LE-1), or both. These operation are pipelined to minimize deadtime, but EoC writes cannot occur faster than 20MHz Hit information is written to the EoC buffer, and waits there for a corresponding L1 trigger. If a trigger arrives at the correct time, checked using LE timestamp of hit, the data is flagged as belonging to a particular 4-bit trigger number. Otherwise it is reset and the buffer is freed. Once the chip has received L1 triggers, the trigger FIFO will no longer be empty. This initiates a readout sequence in which the EoC buffers are scanned for the presence of hits belonging to a particular trigger number. If hits are found, they are transmitted to the serializer. After all hits for a given trigger number have been sent, an End-of-Event (EoE) word is appended to the data stream. All of these operations occur concurrently and without deadtime, with all column pairs operating independently and in parallel.

Event readout from the EoC buffers happen concurrently to the column readout. When the chip-level readout controller starts processing of a particular L1 event, it first broadcasts the correspond-ing L1 readout address to all buffers. All cells with hits waiting for readout compare their stored L1 address with the request value. The readout of the selected L1 hits is controlled by a priority network.

Chip Level Readout Controller.

The chip-level readout controller collects hit data from the EoC buffers and sends them out of the chip serially. All the hits belonging to the same L1 are grouped together into a single event and events are transmitted out of the chip into consecutive trigger order. When a L1 trigger arrives, the current bunch crossing time and a buffer overflow bit are stored in a 16 locations deep FIFO memory. This allows the chip to keep track of 16 pending L1 signals. The write pointer of the FIFO is used as the L1 identification sent to the hit buffers. The readout sequence is started as soon as the FIFO is not empty. If the

L1 priority scan in the hit buffers flags cells with matching trigger numbers, the data of the first cell in the hierarchy is sent to a global data bus from where the information is copied to a shift register. The content of the shift register is then transmitted serially. This is repeated until the priority scan shows no more hits. An End-of-Event (EoE) data word, which includes error flags, is then added to the event.

Chip Configuration.
FE-I3 has 231 global configuration bits plus 14 local bits for each of the 2880 readout channels. The global bits are the settings for eleven 8-bit bias current DACs and for one 10-bit calibration voltage DAC, global threshold bits, the L1 latency, ToT filter thresholds, column enable bits, and others. Loading of configuration in the chips happen by a very simple serial protocol running at 5 MHz. The protocol to shift-in configuration data uses three chip pins: data input, clock and load. The 16 chips in the module are selected using their geographical address (four wire-bonded pins to VDD/GND of each chip) that is sent serially at the beginning of each read or write operation.

4.2.3 Requirements and Measured Performance

Design requirements comes from operation of the pixel detector at high radiation dose, from the time resolution of 25 ns to separate two contiguous bunch crossings, from noise, from minimum operation threshold and dispersion and from the overall power budget. Measurements give a typical threshold dispersion across a module of 60 $e \div 70$ e with an operation value of 4000 e, a noise of 160 e and an in-time threshold of 1500 e above the discriminator threshold [12]. Measurements made on few modules irradiated to the full LHC-life dose (60 MRad) show negligible threshold variation (after re-tunind) and a 20% increase in the noise. During irradiation modules were continuously readout and, from measurement of Single Event Upset (SEU), we can predict a very stable operation at LHC without a significant lost of configuration data due to bit-flip in the memory elements. For a configured chip the typical digital current is 45 mA at 2 V and the analogue current is 75 mA at 1.6 V for a total power of 220 mW. Chip production was made in batches of 48 wafers. There are 288 chips on each 12-inch wafer. 6 production batches have been bought that with the 6 wafers from the engineering production run sum up 294 wafers. Average yield was about 80%[7)]. 27904 front-end chips are inside the ATLAS pixel detector.

4.3 Module Control Chip

expand

Ref. [13] Article describing MCC architecture for the AMS version. SimPix. Performance of the chip obtained from SimPix for the AMS and DSM version.

4.3.1 Prototype History

4.3.2 Current Design

4.3.3 Performance

4.3.4 Production

4.4 Optical Communication

Ref. [14] Description of the optolink system for (mainly) SCT and Pixel. Good overall system description. Describes VCSEL and Pin diodes. Describes BOC with DRX and BPM. Measurements of BER. Measurements for the SCT system.

[7)] editor note: value from Bonn, check with LBL

Ref. [15] Main article describing the Pixel optolink system. VDC, DORIC, Opto Boards, Irradiation.

Ref. [16] Description of the Pixel System. BOC. Measurement of BER.

Ref. [17] Short article describing DORIC, VDC with additional information on irradiation results.

Ref. [18] DORIC and VDC. Irradiation studies. Very similar to previus reference. Decide if give additional info.

Ref. [19] Description of the BOC. Measurements made on system.

4.4.1 Optolink Architecture

Expand In this section goes the description of DORIC/VDC, VCSEL/Pin Diode, Optocard and BOC.

4.4.2 Performance

Expand Put here measurements and irradiation results

4.4.3 Production

4.5 Data Acquisition System

Ref. [20] Describes ROD hardware for both Pixel and SCT. Describes operation modes.

4.5.1 Architecture

Expand Describe briefly DAQ architecture, with focus on ROD.

4.5.2 ROD

4.5.3 Software

Note:

system test goes to a separate section.

4.6 Detector Control System

Ref. [21] Main article on DCS. Describes the PS, ELMB, Interlock, Opto-link. On software side the overall architecture: OPC, PVSS, FIT, DAQ-DCS comunications (DDC).

Ref. [22] Description of the DCS system.

Ref. [23] Describes the architecture chosen for the pixel DCS, the interfaces to hardware devices, the interfaces to the users and the performance of the DCS system. Describes the combined test beam setup and its communication with the DAQ.

Ref. [24] Describes the PS and PP2 system.

4.6.1 Architecture

4.6.2 Hardware

4.6.3 Software

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