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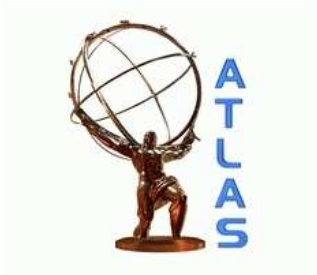

ATLAS NOTE

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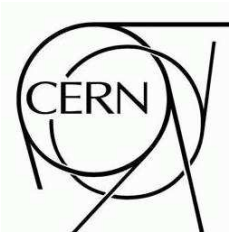

The ATLAS Pixel Detector

The Pixel Collaboration

Abstract

4 Electronics Systems

Ref. [1, 2] Inner Detector and Pixel TDR.

4.1 Overview

4.1.1 System Architecture

expand

4.1.2 Front-end Chip History

ATLAS Pixel front-end design comes from the joint effort of 3 collaborating institutes: Bonn [1)], CPPM[2)] and LBNL[3)]. Small scale chips to demonstrate analog and digital architecture have been developed in the second half of '90: "M72b" at LBL, Lepton at CPPM, Marebo and Bier & Pastis at Bonn/CPPM. The first rad-soft functional prototypes of full size chips where submitted in '98: FE-B al LBNL, FE-A/C (Pirate) at Bonn/CPPM. FE-B was designed using $0.8\mu m$ HP[4)] CMOS technology and had the same basic readout architecture that will be used in the final chips. FE-B charge amplifier uses a direct cascode and source follower, feedback capacitance of 4 fF, DC feedback based on Marebo design. Discriminator uses a dual threshold, low threshold for precise timing, high threshold for validate the hit. FE-A was made on $0.8\mu m$ BiCMOS technology from AMS[5)], whereas FE-C was a full CMOS version. The charge amplifier uses a folded cascode input stage with feedback capacitance of 3 fF and a new improved DC feedback. Discriminator is AC coupled, with an input fully differential bipolar pair in the A version and CMOS in the C. Column readout architecture uses an always running shift register to transport the hit address to the bottom of the chip. Hits are associated to the level 1 trigger (L1) by counting the number of clock cycles needed to hit to reach the column bottom. FE-A/B/C demonstrated all basic ATLAS pixel performance goals in lab and testbeam. The chip from now on were developed using the basic concept of the amplifier/discriminator from FE-A/C and the column readout architecture from FE-C. The European and LBNL front-end design efforts joined forces to combine all of the experience gained with radiation-soft chips into a common layout for the DMILL[6)] technology (known as FE-D). FE-D1 was submitted in July '99 together with DORIC and VDC chips and prototype MCC-D0. A new production run was submitted in Aug '00 with two versions of FE-D2: one with dynamic and the other with static memory cells. Run included full MCC-D2 and new DORIC and VDC chips as well. Yield on both FE and MCC was unacceptable and work with this vendor was terminated. Work on FE-H began in Dec '99 [3]. Chip was almost ready but was never submitted also because of massive cost increases from Honeywell. The failure of both traditional rad-hard vendors left the collaboration with Deep Sub-micron (DSM) approach, based on commercial process $0.25\mu m$ CMOS process and rad-tolerant layout. Major effort started in Sep '00. Three version were submitted using an IBM silicon foundry. Final chip (FE-I3) was available in late '03. Table 1 is a summary of front-end designs developed for the ATLAS Pixel detector.

[1)] Physics Department of the Bonn University
[2)] Centre de Physique des Particules de Marseille
[3)] Lawrence Berkeley National Laboratory
[4)] Hewlett-Packard Company, Palo Alto, California, United States
[5)] Austria Micro Systems AG, Premstätten, Austria
[6)] DMILL technology was developed by CEA, France, and then produced under license by TEMIC Matra MHS

Chip	Year	Cell size (μm^2)	Col × Row	Trans.	Technology	References
M72b	??	50×536	12×64	??	HP 0.8μm CMOS, 2M ??	[4]
Marebo	??	??	12×63	??	DMILL 0.8μm BiCMOS 2M	–
Beer & Pastis	??	50×436	12×63	??	AMS 0.8μm BiCMOS, 2M	[4, 5]
FE-B	1998	50×400	18×160	??	HP 0.8μm CMOS, 2M ??	[3, 6, 7]
FE-A/C	1998 ?	50×400	18×160	??	AMS 0.8μm BiCMOS, 2M	[5, 7]
FE-D1	1999	50×400	18×160	??	DMILL 0.8μm BiCMOS 2M	[7]
FE-D2	2000	50×400	18×160	??	DMILL 0.8μm BiCMOS 2M	–
FE-I1	200x	50×400	18×160	??	IBM 0.25μm CMOS, 6M, 1P	[8]
FE-I2/I2.1	2003	50×400	18×160	2.5 M	IBM 0.25μm CMOS, 6M	[9]
FE-I3	2003	50×400	18×160	3.5 M	IBM 0.25μm CMOS, 6M	[10, 11]

Table 1: Summary of the ATLAS Pixel front-end chips.

4.1.3 Current Design

Chip Architecture.
The readout chip for the ATLAS pixel detector [10] shown in Fig. 1 contains 2880 readout cells of $50\mu m \times 400\mu m$ size arranged in a 18×160 matrix. Each readout cell contains an analogue block where the sensor charge signal is amplified and compared to a programmable threshold by a discriminator. The digital readout part transfers the hit pixel address, a hit time stamp and a digitized amplitude information, the time over threshold (ToT) to buffers at the chip periphery. These hit buffers monitor the age of each stored hit by inspecting the associated time stamp. When a hit becomes older than the latency of the Level 1 trigger (3.2 μ s) and no trigger signal has occurred, the hit information is deleted. Hits which are marked by trigger signals are selected for readout. Triggered hit data are transmitted serially out of the chip in the same order of trigger arrival.

Charge Sensitive Preamplifier.
The charge sensitive amplifier uses a single-ended folded-cascode topology, which is a common choice for low-voltage and high gain amplifiers. The amplifier is optimised for a nominal capacitive load of 400 fF and designed for negative signal expected from $n^+ - on - n - bulk$ detectors. Special attention was put in the design of the charge amplifier to the requirement of irradiated sensors, where the leakage current (50 nA) is two order of magnitude bigger than the signal (5000 e), which is reduced by carrier trapping inside the silicon. The preamplifier has roughly $5fF$ DC feedback design, $15ns$ risetime and operates at about $8\mu A$ bias. To fulfil the above requirements of sensor leakage current, a compensation circuit is implemented which drains the leakage current and prevents it to influence the bias current of the fast feedback circuit used to discharge the feedback capacitor. The feedback system, shown in Fig. 2 uses two PMOS devices, one (M2) providing leakage current compensation and the other (M1) continuous reset of the feedback capacitor. An important property of this feedback circuit is that the discharge current provided by the reset device saturates for high output signal amplitudes. The return to baseline is therefore nearly linear and a pulse width proportional to the input charge is obtained. The width of the discriminator output, Time-over-Threshold (ToT), can therefore be used to measure the signal amplitude. Feedback current is $4nA$ for $1\mu s$ return to baseline and $20ke$ input. The feedback circuit used in FE-I3 has an additional diode-connected transistor M3, which acts as a level shifter so that the DC levels of input and output nodes are nearly equal. It also simplifies the DC coupling between amplifier and the following comparator.

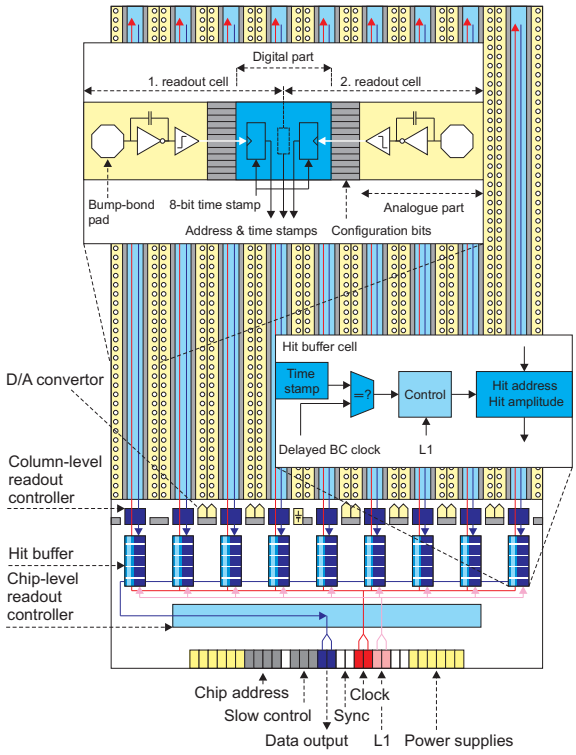

Figure 1: Simplified floorplan of the front-end chip (FE-I3) with main functional elements.

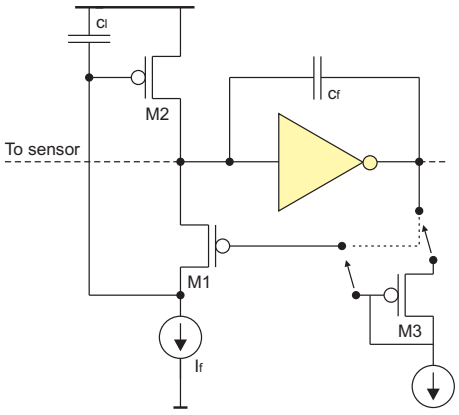

Figure 2: Charge preamplifier: feedback circuit.

Comparator.
Signal discrimination is made by a two stage-circuit: a fully differential low gain amplifier, where threshold control operates by modifying the input offset, and a DC-coupled differential comparator. The first stage has a bias of about $4\mu A$ whereas the second uses a current of about $5\mu A$. In order to make the threshold independent of the local VDDREF and on the amplifier bias current I_f, a local threshold generator is integrated in every pixel. 7-bits are used in each pixel to adjust the discriminator threshold.

Pixel Cell Control Logic.
A complete block diagram of the analogue part with several additional circuit blocks is shown in Fig. 3. Each pixel has several parameter that can be tuned through a 14-bit control register. Those bits are:

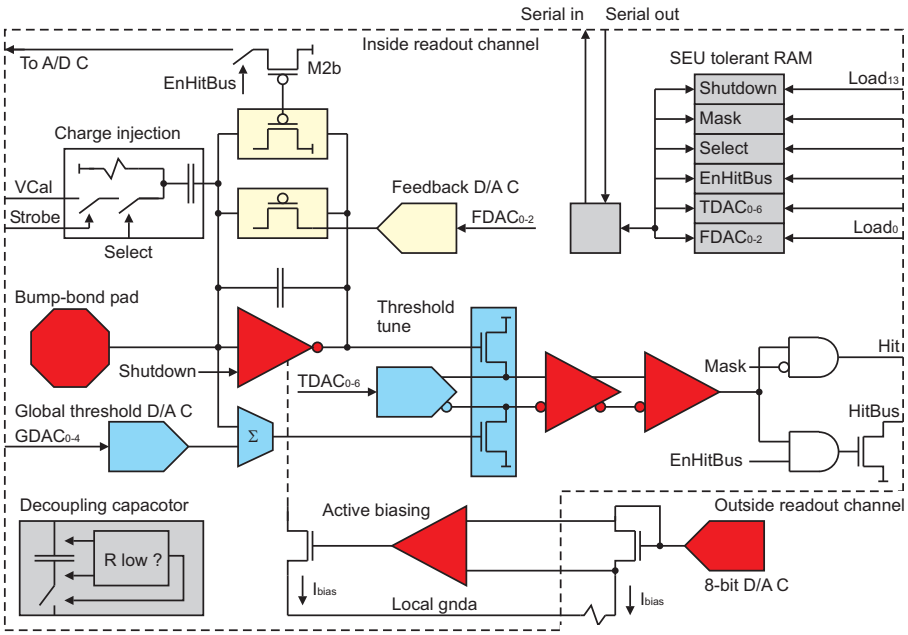

Figure 3: Pixel cell block diagram.

- *FDAC 0-2:* 3-bits to trim the feedback I_f current for tuning the ToT response.
- *TDAC 0-6:* 7-bits to trim the threshold in each pixel.
- *MASK:* the digital output of the analogue part can be switched off locally by setting this bit.
- *EnHitBus:* the digital outputs of all readout channels can be directly observed using a wired OR which is locally enabled with this bit. This bit bit also controls, through transistor M2b, the summing of a current proportional to the feedback plus leakage current in the preamp, allowing the monitoring of the feedback current and of the leakage current from the sensor.
- *Select:* enables the pixel for test charge injection. Amplitude is generated from *VCal* whereas timing comes from an external *Strobe* signal.
- Shutdown: disables the charge amplifier therefore no output is generated from the pixel.

Pixel Cell Readout Logic.
A block diagram of the column-pair readout is shown in Fig. 4. The digital circuitry in the readout cells

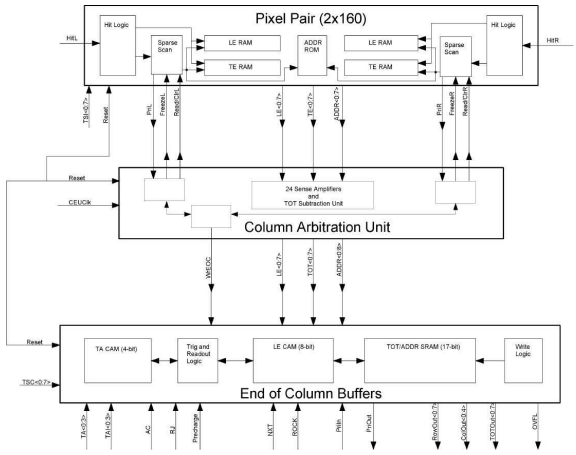

Figure 4: Block diagram of the column-pair readout (picture must be redrawn, simplified and span one column).

generates hit information: time of leading edge (LE), time of trailing edge (TE) for ToT calculation, row address. All of this information is temporarily stored in local memories before being transferred to the hit buffers at the chip periphery. A digital circuitry generates two short (1*ns*) strobes at the LE and TE discriminator signals, respectively. These signals are used to store the 8-bit Gray-coded time stamp into two memories. The time stamps, generated at the chip periphery, running at 40 MHz are distributed differentially, in order to decrease the digital crosstalk, to analogue circuits and sensor electrodes. The complete hit information is available after the TE of the comparator signal and data transfer can start. Time stamp of the LE (8-bits) of the TE (8-bits) and the row number (8-bits) are transferred to the end-of-column (EoC) buffers. Transfer happens by a priority mechanism that selects cells with data starting from the top row. The top most cell with a hit puts the data on the bus and all the cell below it are inhibit. When the cell is readout, it releases the priority encoder bus and the next coming hit is selected and put on the readout bus. The readout speed is limited by the time the priority logic needs to ripple down. Hits can ripple through at programmable speed that is obtained from the 40 MHz clock division. In the actual chip, the maximum speed to transfer a single hit to the EoC is 20 MHz.

Column Readout Controller.
Readout is column based, and two columns are readout from the same controller. The first task of the controller is the generation of the readout sequence to transfer hit information: LE and TE timestamp, plus pixel row address into an EoC buffer. This operation begins when data is complete, which is after discriminator TE. The transfer of hits from a column pair is synchronized by the Controller end-of-columnn Unit (CEU), which operates at a speed of 5, 10, or 20 MHz. A total of 64-hit buffers are available for each double-column.
The second task is some digital processing of the hit data. Hit information is formatted by the CEU. Formatting includes ToT calculation: subtraction of TE time stamp from LE timestamp. Optionally, a digital threshold may be applied to ToT, a timewalk correction may be applied (write hit twice if below correction threshold, once with LE and once with LE-1), or both. These operation are pipelined to minimize deadtime, but EoC writes cannot occur faster than 20MHz Hit information is written to the EoC buffer, and waits there for a corresponding L1 trigger. If a trigger arrives at the correct time, checked using LE timestamp of hit, the data is flagged as belonging to a particular 4-bit trigger number. Otherwise it is reset and the buffer is freed. Once the chip has received L1 triggers, the trigger FIFO will no longer be empty. This initiates a readout sequence in which the EoC buffers are scanned for the presence of hits

belonging to a particular trigger number. If hits are found, they are transmitted to the serializer. After all hits for a given trigger number have been sent, an End-of-Event (EoE) word is appended to the data stream. All of these operations occur concurrently and without deadtime, with all column pairs operating independently and in parallel.
Event readout from the EoC buffers happen concurrently to the column readout. When the chip-level readout controller starts processing of a particular L1 event, it first broadcasts the correspond-ing L1 readout address to all buffers. All cells with hits waiting for readout compare their stored L1 address with the request value. The readout of the selected L1 hits is controlled by a priority network.

Chip Level Readout Controller.
The chip-level readout controller collects hit data from the EoC buffers and sends them out of the chip serially. All the hits belonging to the same L1 are grouped together into a single event and events are transmitted out of the chip into consecutive trigger order. When a L1 trigger arrives, the current bunch crossing time and a buffer overflow bit are stored in a 16 locations deep FIFO memory. This allows the chip to keep track of 16 pending L1 signals. The write pointer of the FIFO is used as the L1 identification sent to the hit buffers. The readout sequence is started as soon as the FIFO is not empty. If the L1 priority scan in the hit buffers flags cells with matching trigger numbers, the data of the first cell in the hierarchy is sent to a global data bus from where the information is copied to a shift register. The content of the shift register is then transmitted serially. This is repeated until the priority scan shows no more hits. An End-of-Event (EoE) data word, which includes error flags, is then added to the event.

Chip Configuration.
FE-I3 has 231 global configuration bits plus 14 local bits for each of the 2880 readout channels. The global bits are the settings for eleven 8-bit bias current DACs and for one 10-bit calibration voltage DAC, global threshold bits, the L1 latency, ToT filter thresholds, column enable bits, and others. Loading of configuration in the chips happen by a very simple serial protocol running at 5 MHz. The protocol to shift-in configuration data uses three chip pins: data input, clock and load. The 16 chips in the module are selected using their geographical address (four wire-bonded pins to VDD/GND of each chip) that is sent serially at the beginning of each read or write operation.

4.1.4 Requirements and Measured Performance

Design requirements comes from operation of the pixel detector at high radiation dose, from the time resolution of 25 ns to separate two contiguous bunch crossings, from noise, from minimum operation threshold and dispersion and from the overall power budget. Measurements give a typical threshold dispersion across a module of 60 $e \div 70$ e with an operation value of 4000 e, a noise of 160 e and an in-time threshold of 1500 e above the discriminator threshold [11]. Measurements made on few modules irradiated to the full LHC-life dose (60 MRad) show negligible threshold variation (after re-tunind) and a 20% increase in the noise. During irradiation modules were continuously readout and, from measurement of Single Event Upset (SEU), we can predict a very stable operation at LHC without a significant lost of configuration data due to bit-flip in the memory elements. For a configured chip the typical digital current is 45 mA at 2 V and the analogue current is 75 mA at 1.6 V for a total power of 220 mW. Chip production was made in batches of 48 wafers. There are 288 chips on each 12-inch wafer. 6 production batches have been bought that with the 6 wafers from the engineering production run sum up 294 wafers. Average yield was about 80%[7)]. 27904 front-end chips are inside the ATLAS pixel detector.

[7)] editor note: value from Bonn, check with LBL

4.2 Module Control Chip

expand

Ref. [12] Article describing MCC architecture for the AMS version. SimPix. Performance of the chip obtained from SimPix for the AMS and DSM version.

4.2.1 Prototype History

4.2.2 Current Design

4.2.3 Performance

4.2.4 Production

4.3 Optical Communication

4.3.1 Optolink Architecture

The communication between the detector modules and the off-detector electronics is established via optical links. This is to implement electrical decoupling and minimize material. The architecture was inherited from the ATLAS SCT, modifications where needed to adapt for data-rates, modularities and radiation hardness.
The two main components of the optical link are the opto-board as on-detector, and the Back of Crate Card (BoC) as the off-detector end.
For fibre-routing reasons, it was decided not to install individual on-detector components on each detector module, but to install one so-called opto-board per half-stave at $z \approx 1\,\mathrm{m}$ on the patch-panel zero, at the inner wall of the pixel support tube. It was needed to implement pixel-specific versions of the VCSEL Driver IC (VDC) and the Digital Optical Receiver IC (DORIC), as the ondector components have to withstand pixel radiation level, because of this position.

For all communication to the detector-modules, individual links are foreseen. The configuration, the clocking, the trigger signaling and some synchronization information is sent via one channel per module. The control-infromation and the clock signal are encoded as biphase mark signals on the BoC. This encoding is introducing a transition (on to off or off to on) on every rising edge of the clock. Additional transitions at the falling edge of the clock are introduced if the data to be transferred is one. This scheme allows for individual timing of each module, as the phase of the signal sent can be adjusted with respect to the LHC-clock, received by the BoC.

WHO IS TAKING CARE OF TIM?

To transfer the hit informations back to the readout system, data rates (including safty margins [**?**]) of 40MBaud per L2 module, 80MBaud per L1 or Disk module, and 160MBaud per B-Layer module are needed. These data-links are realised with non-return-to-zero signals without special encoding. Taking into account the throughput of data the ROD is able to handle, three configurations of the optical link are used.

These are established using two flavours of the opto-board, both equipped with seven clock/control channels driving six or seven modules of a half-stave or a disk-sector. The so-called D-Board is equipped and with seven data channels. This is used for Layer2, Layer1 and Disk modules. Layer2 modules are configured to drive 40MBaud data streams, while Layer1 and Disk modules are configured to drive 80MBaud stream in a double data rate coding. The second opto-board flavour, the B-Board, is equipped with 14 data-channels, providing two data-links per module attached. These are configured to drive 2×80MBaud streams.

For the off-detector electronics, there is always one BoC per ROD. One BoC is taking care of a Layer2 bi-stave, a Layer1 stave, two Disk sectors or one B-Layer half-stave. These three BoC flavours

a equipped with different numbers of opto-components, which are realised as plug-ins. After opto-electrical conversion, the BoC is taking care of synchronizing the data with the ROD clock, and devides the double data rate streams and equally distributes the modules data to the ROD input stages.

4.3.2 Optopacks

Expand In this section goes the description of DORIC/VDC, VCSEL/Pin Diode, Optocard and BOC.

VCSELs VCSEL arrays are used to transmit the data optically. The main advantages of VCSELs are that they provide large optical signals at very low currents and have fast rise and fall times. The VCSELs[8)] used for SCT and Pixel have an oxide implant to achieve the current confinement, which is becoming the standard VCSEL technology as it produces lower thresholds and higher bandwidth. The VCSELs are built in arrays of 8 channels each. The typical fibre coupled power per channel is greater than 1 mW at a drive current of 10 mA. This optical power at 10 mA is sufficient to give a noise immunity of 6.2 dB and an additional safety factor of about 1.8 dB can be obtained by running at slightly higher current. A larger amplitude optical signal also reduces the Single Event Upset (SEU) rate in the TTC system and an amplitude of 1 mW for the optical signal ensures that the resulting BER is always less than 10^{-9}.

PiN arrays Arrays of silicon PiN diodes are used to receive the data sent by the VCSELs. Epitaxial silicon PiN diodes[9)] are used because the intrinsic layer provides a thin active layer allowing for fast operation at low PiN bias voltage. The active area of each individual PiN diode is circular with a diameter of 130 μm and the depth of the intrinsic region is 35 μm [13].

4.3.3 The Optoboard

The optoboard is the opto-electrical interface in the detector area. It is a 2×6.5 cm^2 beryllium-oxide (BeO) printed circuit board. Six or seven modules are connected electrically to an optoboard. In the pixel detector there will be two flavours of optoboards, the B-boards and the Disk-boards. The Disk-boards are foreseen to connect the modules on the Disks, Layer 1, and Layer 2 to the readout electronics, while the B-boards are designed especially for the B-Layer modules. The Disk-boards are equipped with one PiN diode array and one VCSELc-array, while the B-boards have one additional VCSEL-array each. To decode the BPM-signals received by the PiN diode two four-channel Digital Optical Receiver ICs (DORIC) are assembled on each Optoboard. The VCSELs are driven by the VCSEL Driver Chip (VDC). The VDC is a channel chip, therefore two (Disk-board) or four (B-board) VDCs are assembled per Optoboard. In total, 272 optoboards 44 B-boards and 228 Disk-boards are built into the detector.

The DORIC The DORIC decodes BPM encoded clock and data signals received by a PiN diode. It is made as a four channel chip handling four BPM-signals in parallel. The amplitude of the current from the PIN diode is expected to be in the range of 401000 μA. The 40 MHz clock recovered by the DORIC is required to have a duty cycle of $(50 \pm 4)\%$ with a total timing error (jitter) of less than 1 ns. The bit error rate of the DORIC is required to be less than 10^{-11} at end of life. The typical PIN current thresholds for the DORIC to decode the BPM signal with no bit errors are low, < 20 *mA*. In order to keep the PIN bias voltage off the DORIC, there is a single-ended preamp circuit to amplify the current produced by the PIN diode. The DORIC has to withstand a severe radiation level over the 10 years of ATLAS operation. It therefore is implemented in the standard deep submicron $(0.25\ \mu m)$ CMOS technology.

[8)] 6TSA-8B12-00 Truelight, Taiwan.

[9)] Designed by Truelight, Taiwan, manufactured by Episil, Taiwan.

The VDC The VDC is used to convert an LVDS input signal into a single-ended signal appropriate to drive a VCSEL in a common cathode array. It is made as a four channel chip also, serving four VCSEL channels. The output current of the VDC should be variable between 0 and 20 mA through an external control current, with a standing (dim) current of $\sim 1\ mA$ to improve the switching speed of the VCSEL. The nominal operating current for a VCSEL is 10 mA. The electrical output should have rise and fall times (2080%) between 0.5 and 2.0 ns; nominally 1.0 ns. In order to minimize the power supply noise on the opto-board, the VDC should also have constant current consumption independent of whether the VCSEL is in the bright (on) or dim (off) state. An externally controlled voltage ($V_{I_{set}}$) determines the current I_{set} that sets the amplitude of the VCSEL current (bright minus dim current), while the dim current is controlled by another externally controlled voltage.

4.3.4 Back of Crate Card

The Back of Crate (BOC) card is the opto-electrical interface in the counting room. It is responsible for the timing of the on-detector and off-detector components. The BOC card receives the system clock and distributes it to the modules and the Readout Driver (ROD). In addition, there are clock copies for the data recovery and phase adoption. Each of these clocks, for the on-detector parts and for the data recovery, can be delayed using a PHOS4 chip. A custom made delay chip providing a delay between 0 and 25 ns on four independend channels. To recover the data received from the on-detector modules, the data streams can also be delayed using PHOS4 chips. For communication with the on-detector hardware, there are plugins to be connected to the Back of Crate card, being the TX-plugin and the RX-plugin. The TX-Plugin is comprised of an 8-channel VCSEL array and a BPM ASIC. Here the TTC-data received from the readout driver (ROD) is encoded into BPM signals and transmitted optically to the optoboard. The RX-plugin is comprised of an 8-channels PiN diode array and a DRX ASIC. The RX-plugin receives the optical signal from the optoboard and converts it into electrical signal, being amplified and fed out as LVDS signals to the BOC data recovering section.

DRX The DRX ASIC is used to discriminate the electrical signals from the PiN arrays to reproduce the data signals received from the Optoboard. It is used for the SCT and the Pixel subdetectors and contains 12 channels of which 8 channels are used for the Pixel case. Each of these channels consists of a comparator with an LVDS output driver. The input comparators are DC coupled to allow for the NRZ data stream. Each channel of the DRX ASIC has an individually adjustable threshold which can be set by an external reference voltage to correspond to an input signal amplitude in the range 0 to 255 mA.

BPM The BPM ASIC is used to combine the 40 MHz system clock and the 40 Mb/s command data stream. It is used for the SCT and the Pixel subdetector and consists of 12 channels of biphase mark encoding and VCSEL drive circuitry, of which 8 channels are used in the Pixel case. Each channel has an input 40 Mb/s data stream and there is also a common input 40 MHz system clock for all channels. The latency between the input and output data must not be too long because of the fixed pipeline depth of the front-end electronics. The measured latency was 60 ns.

Fibres The connection between the BOC card and the optoboard is done via optical fibres. These fibres are ribbonized into 8-way ribbon of which eight form an optical cable. Two different kinds of fibres are used, Stepped Index Multi-Mode fibres (SIMM) and GRaded INdex multi-mode fibres (GRIN). While the SIMM fibre is utilized in the innermost part of the ATLAS detector (the first 12 m) it is spliced to a GRIN-fibre which makes the rest of the distance to the readout electronics in the counting room ($\sim 70\ m$).

4.3.5 Performance

Expand Put here measurements and irradiation results

Two paragraphs:

performance of the opto-board intensive prototyping of the opto-board. one or two plots of irradiation studies

performance of the BoC detailed study in the context of the ATLAS combined test-beam. one plot of optimized timing adjustment

4.3.6 Production

The production of the opto-boards was apportioned $\frac{3}{4}$ to Ohio State University and $\frac{1}{4}$ to Universities of Siegen and Wuppertal. An intensive program of initial measurements of components, post-assembly and pre-aging by thermo cycling was established, followed by a careful characterisation at different temperatures. This revealed that for some of the VCSEL production batches, the amount of light coupled into the fibre is strongly temperature dependant. This is why an active temperature control of the opto-boards (including cooling and heating) was introduced into the detector system.

Aside from this, the production of the opto-boards
give yield and time needed, here
one Plot showing ...

refs to:
(internal) opto-board production procedure document
some phd thesis

4.4 Data Acquisition System

Ref. [14] Describes ROD hardware for both Pixel and SCT. Describes operation modes.

4.4.1 Architecture

Expand Describe briefly DAQ architecture, with focus on ROD.

4.4.2 ROD

4.4.3 Software

Note:

system test goes to a separate section.

4.5 Detector Control System (DCS)

The operation of the pixel detector modules and of the on-detector opto-components requires a complex power supply [18] and control system [15]. The adjustment of the operation conditions of the system requires a large modularity. Robust software packages are used to monitor and control all the options in the hardware of the large system. There is, in addition, an independent interlock system that takes care of the safety of equipment and human operators.

4.5.1 The Hardware of the DCS

The scheme of the powering, control and interlock system is shown in fig. 5. The main components of

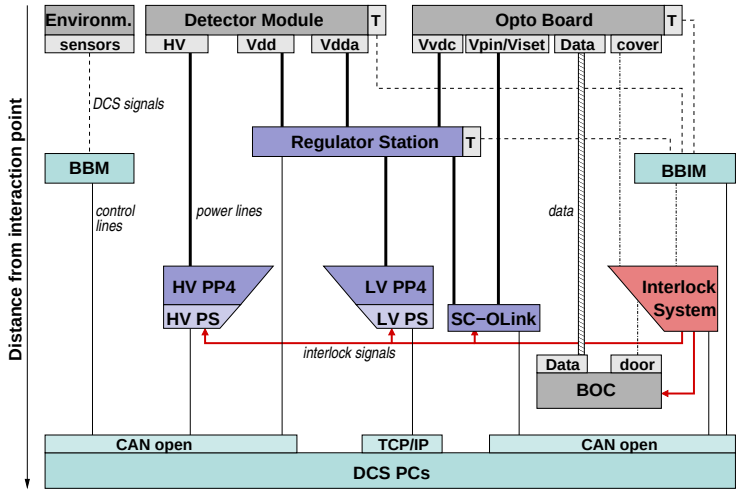

Figure 5: Overview on the hardware of the pixel detector control system.

the Pixel DCS are:

- The power supplies to operate the sensors, the front end chips and the opto boards;
- The Regulator Stations;
- Temperature and humidity sensors plus monitoring devices for their readout;
- Multi channel current measurement units;
- The Interlock System;
- The DCS computers to control the hardware.

To comply with the ATLAS grounding scheme all power supplies and monitoring systems must be floating. Radiation damage during lifetime operation of sensor and on-detector electronics requires that all power supply have adjustable voltage outputs. For operation safety also over-current protection and interlock input signals are available in all the power supplies. The pixel power supply system has four main components: low voltage power supply (LV-PS), high voltage power supply (HV-PS), Regulator Station, Supply and Control for the Opto Link (SC-OLink). Two low voltages supply the analog (Vdda) and digital part (Vdd) of the front end read out electronics. are delivered by the LV-PS, which is a commercial component: the PL512M from WIENER [10)]. To protect the sensitive front end electronics against transients, remotely-programmable Regulator Stations are installed as close as possible to the detector. These Regulator Stations protect the high sensitive front end from over-voltage transients and allow an individual tuning of the power lines through digital trimmers.
The pixel sensors are depleted by the high voltage Vdet (up to 700 V) form the HV-PS. The HV-PS is assembled with EHQ-F607n_405-F modules provided by Iseg [11)]. The LV-PS and HV-PS are respectively

[10)] WIENER, Plein & Baus GmbH, Burscheid, Germany
[11)] iseg Spezialelektronik GmbH, Rossendorf, Germany

connected to the low voltage patch-panel-4 (LV-PP4) and to the high voltage patch-panel-4 (HV-PP4) that are used to distribute the power and monitor the currents of the individual lines.
The SC-OLink, a complex channel consisting of three voltage sources and a control signal, delivers the adequate levels for the operation of the on detector part of the optical link. Monitoring of temperatures and of humidity is performed by the Building Block Monitoring (BBM) and the Building Block Interlock and Monitoring (BBIM) crates. While the first just provides a reading of values, the second additionally creates logical signals, which are fed into the Interlock System. All components of the LV-PS, HV-PS, SC-OLink in addition to the BOC boards are connected to the hardware based Interlock System, that acts as a completely independent system. It consists of several units that guarantee safety for human operators as well as for sensible detector parts. The Interlock System has high modularity; more than a thousand of individual interlock signals are distributed. This high modularity has been chosen to keep low the number of detector modules out-of-service in case of some component failure. The DCS software has only the function of monitor and test and not of safety for the detector. The Regulator System and many sensors, installed inside the ATLAS detector, used by the Interlock System had to pass requirements of radiation tolerance; this required extensive qualification of many components.
Besides the LV-PS and HV-PS all other components in the system are custom designs, adapted to the pixel specific needs and using the Embedded Local Monitoring Board (ELMB) for the monitoring through the DCS. ELMB is the ATLAS standard front end I/O unit for the slow control signal. The Control Area Network (CAN) interface of the ELMB and its CAN-open protocol ensure a reliable and robust communication. Different Openness, Productivity, Collaboration (OPC) servers are used to integrate the hardware into the higher level of the software. All together 630 CAN nodes on 43 CAN busses and 48 TCP/IP nodes for the LV power supplies are building the pixel control network. In total more than 44000 variables need to be monitored.

4.5.2 The Software of the DCS

The DCS software has to establish the communication to the hardware, to support the operator with all required monitoring and control tools, and to provide automatic procedures for safety and for easier operation of the detector for non DCS experts. A permanent operation and reliable data taking must be ensured. Additionally the operation of the detector requires a good coordination of DAQ and DCS actions and for the offline analysis relevant data must be recorded and stored into the conditions database. The core of the DCS software are the Prozess- Visualisierungs- und SteuerungsSoftware (PVSS), [12)] projects, which run as a distributed system on eight control stations. As each part of a distributed system has its own control and data managers (processes inside PVSS) an independent development and operation of the different projects is possible. The core of the control software are the Front-end Integration Tools (FIT) which establish the communication with the hardware components. For each hardware component, like the HV-PS, the LV-PS and the different device using the ELMBs, dedicated FIT exist. Each FIT consists of an integration and a control part. The integration part initialises each given hardware component and creates the data structures required to control it. The control part of the FIT instead supervise the operation of the same component. The hardware is mapped into the software in a device oriented way. The FITs are mainly foreseen for the DCS expert who needs to check the correct behaviour of the hardware. For persons that will run shift in ATLAS a detector oriented view of the hardware is provided by the System Integration Tool (SIT). The mapping of the read-out channels to the detector devices is done by the SIT. The SIT creates a virtual image of the detector inside the DCS; It combines all information which is relevant for the operation of a detector unit like a half stave, a disk or the full detector. Furthermore the SIT is responsible for the storing of the data into the conditions database.
The software used to operate on the detector is the Finite State Machine (FSM), provided by the CERN

[12)] PVSS is made by ETM, Eisenstadt, Austria

JCOP group. FSM uses the geographical organised data structures, created by the SIT, and provides the user with a set of commands, to act on smaller or larger fraction of the detector simultaneously. The actual status of the detector is returned by the FSM. Further, the proper settings and special power on sequences are performed automatically by the FSM. In addition the FSM builds the link into the ATLAS wide control system. As part of the overall ATLAS control system, the pixel FSM will receive commands from the ATLAS FSM during normal data taking. The communication between DAQ and DCS is provided by DAQ-DCS Communication (DDC), which provides command transfer from the DAQ system to DCS, publishes DCS values to DAQ and vice versa. Especially for the tuning of the optical link DDC is of major importance.
The DCS hardware and software system has been fully exercised in different occasions during the prototyping and construction phase of the Pixel Detector: in the test beams, with cosmic tests and during the integration of the Pixel Detector at CERN [16, 17].

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