# 1 Modules

## 1.1 Overview

The sensitive area of 1.73 $m^2$ of the ATLAS pixel detector is covered with 1744 identical modules, independent of their spatial position, with a small exception (see below). Each module has an active surface of $6.04 \times 1.64 cm^2$. A module is assembled from the following assembly parts

- the sensor tile containing 47532 pixels in an area of $6.34 \times 2.44\,cm^2$
- sixteen front end electronics chips (FE) each consisting of 2880 pixel cells with amplifying circuitry, connected to the sensor by means of fine-pitch bump bonding (see section 1.2)
- a xx $\mu$m thin, fine-pitch double-sided flex-kapton foil on which routings for signal and service traces are done
- a module control chip (MCC) situated on the flex-kapton foil
- for the barrel modules another flex-kapton foil, called pigtail, provides the electrical connection to the outside through a connector to which the micro cable is attached; for the disk modules the micro cables are attached without the pigtail connection.

The concept of the ATLAS hybrid pixel module is illustrated in Fig. 1. Sixteen front-end chips are connected to the sensor by means of the bumping and flip-chip technology. Each chip covers an area of $0.74 \times 1.09\,cm^2$ and has been thinned before the flip-chip process to $\approx$190 $\mu$m thickness by back-side grinding. A sizeable ($\approx$25%) fraction of the front-end chip is dedicated to the End of Column (EoC) logic. Once bonded, most of the EoC logic extends out of the sensor area. Wire bonding pads at the output of the EoC logic are thus accessible to connect each front-end chip to the flex-hybrid kapton foil by means of Al wire wedge bonding. On the flex-kapton foil copper traces route the signals to the Module Control Chip (MCC). The MCC receives and transmits digital data out of the modules via the pigtail to micro-cable connection. The flex-kapton circuitry is also used to distribute properly decoupled low voltage to all chips. These lines are dimensioned such that the voltage drop dispersion on the flex be limited to $\approx$50 mV in order to keep all chips in the same operating conditions. The substrate material must have a low pin-hole probability, as it also houses high voltage ($\approx$600 V) traces for the sensor bias. The kapton material must not degrade after LHC (500 kGy) irradiation doses. Passive components are added to the flex-hybrid kapton for decoupling and filtering of the front-end chips.

The module temperature is remotely monitored via a Negative Temperature Coefficient (NTC) resistor placed on the kapton circuit and a fast interlock will power off a module when overheating occurs. This is necessary as the large power density and the low mass of the support and cooling structure imply temperature rises of up to 10 degrees per second in case of a cooling fault.

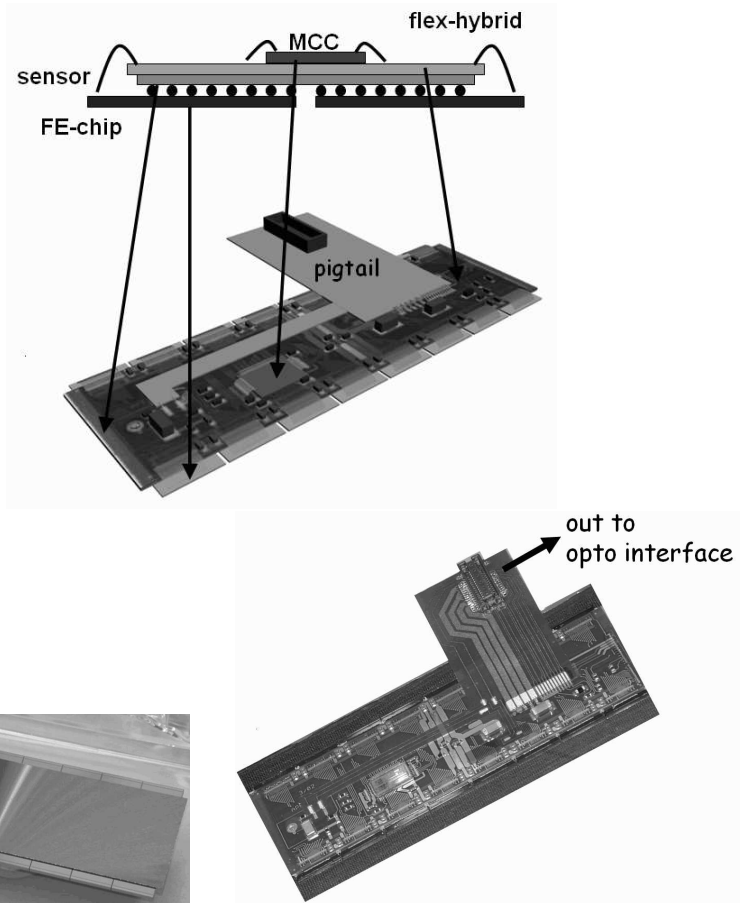


Abbildung 1: The pixel module. (top) overview, showing the components of the module assembly: sensor, FE-chips, Flex-kapton-hybrid, module controcl chip (MCC), pigtail. (b) photograph of a BARE module, (c) photograph of a fully assembled module.

A complete module draws 1.15 A at 1.6 V on the analog supply and 0.8 A at 2 V on the digital supply, i.e about 3.5 W per module. This value is expected to increase to about 5 W after an accumulated dose of 500 kGy.

The bump and flip-chip operation results in a so-called BARE module. The sixteen chips of an assembled module are first tested on a probe station to detect the defective ones and possibly rework the module which can only be done at this point of the assembly chain.

### Region in between Chips

### Here is some text that may belong elsewhere

The sensor pixels have dimensions of $50\,\mu\text{m}\times400\,\mu\text{m}$, except for 2% which have a size of $50\,\mu\text{m}\times600\,\mu\text{m}$, to allow for a contiguous sensitive area between chip boundaries in the long pixel direction. In the other direction, two times four pixels under each of the two adjacent chips cannot be covered by active pixel circuitry. These off-side sensor pixels are connected through metal lines on the sensor to 4 + 4 neighboring electronics pixels at the top of the columns in addition to the cells which lie directly underneath as is illustrated in Fig. 2. The resulting hit ambiguity is resolved by the off-line pattern recognition software.

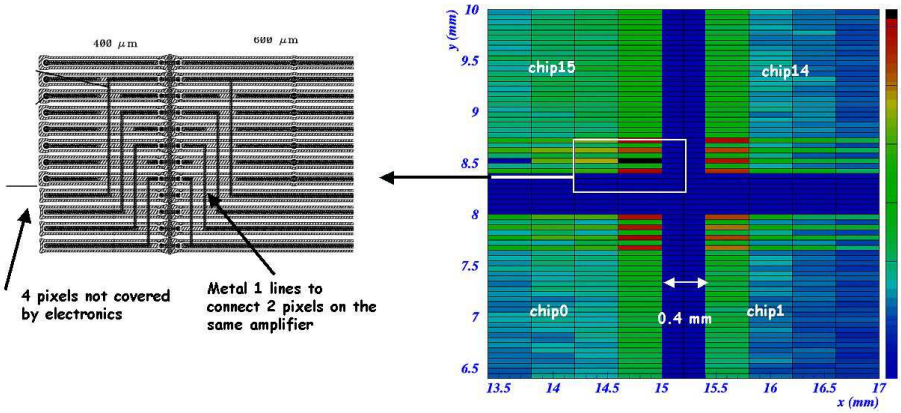


Abbildung 2: End region of the pixel detector at the edge of four FE-chips. The area of the sensor covered by the chip edges is marked in grey. The pixels in between the chips (white rectangles) are connected through metal lines to another pixel underneath the chips.

## 1.2 Bump Bonding

Bump bonding is extensively used in the electronics industry for the attachment of integrated circuit dies to printed circuit boards or other substrates. Two different bump bonding techniques have been used for ATLAS: electroplated solder (PbSn) bumping [1, 3] and evaporative indium bumping [4]. Both bump deposition processes are done at the wafer level. The principle of a bumped sensor – electronics pixel element is sketched in fig. 3. The fairly substantial demands on

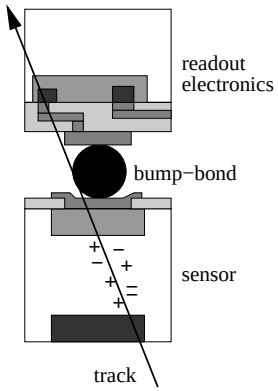


Abbildung 3: Blow-up sketch (not to scale) of the cross section of a hybrid pixel detector, showing one connection between a sensor and an electronics pixel cell. A a particle track releases ionization in the sensor volume

the handling require that the wafers get bumped with their original thickness ($\sim 700\mu m$ for the 20 cm IC wafers). Wafer thinning is done after bump deposition by covering the bumps by a photo resist layer and a UV releasing tape for bump protection and for handling. The wafers are then thinned by backside grinding to 180 $\mu$m–190 $\mu$m. They are diced and singularized immediately afterwards and then they are tested again on a probe station to assure that they are still functional and ready for the flip-chip process.

### 1.2.1 The Solder Bumping and Bonding Process

In eutectic PbSn solder bumping [1, 3] the solder is deposited through electroplating. On an "under bump metallization" (UBM), which is a set of several metal layers sputtered on the contact pad for reasons of adhesion, diffusion barriers and wettability, a $PbSn$ cylinder is galvanically grown and melted to a sphere on the chip wafer, while the sensor wafer receives only the UBM [2, 5]. The parts are mated by flip-chipping with reflow which provides self-alignment. The process flow is displayed in [8]. The distance between chip and sensor is about 20 – 25 $\mu$m, thus minimizing the cross-talk between electronics and sensor. The connection resistance is smaller than 1$\Omega$ and the ultimate shear stress

is ≈50 MPa. Pictures of a small dimension $PbSn$ bump after reflow and of a sequence of bumps on an ATLAS FE-chip are shown in Fig. 4.

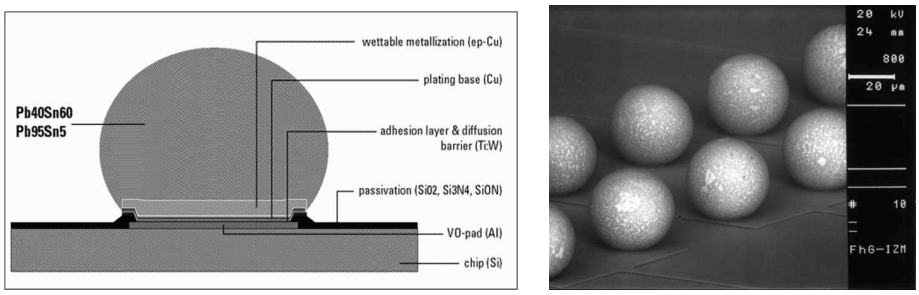


Abbildung 4: left) Built-up of a eutectic PbSn solder bump [1, 3], (right) rows of a PbSn bumps (curtesy IZM-Berlin).

### 1.2.2 The Indium Bump Bonding Process

In the case of indium bonding, the bumps are grown by evaporation [**?**]. Bump pitches can be as low as 30 $\mu$m, but the bump height is limited to 10 $\mu$m due to the use of a lift-off process for the removal of the polyimide evaporation mask. Bumps are deposited both on the sensor and on the electronics. Mating is obtained by $In$-$In$ thermocompression. The process flow is shown in [8]. Figure 5 shows a micrograph of 50 $\mu$m pitch Indium bumps deposited on two glass samples and then flip chipped together [4] at a temperature of ∼100°C applying a pressure of about 20 $N/\mathrm{cm}^2$ per chip. The distance between chip and sensor after bonding is ≈10 $\mu$m.

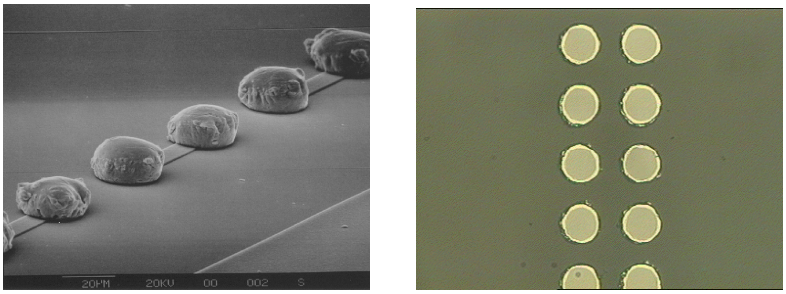


Abbildung 5: Micrograph of a Indium bump deposition on Silicon at 50 $\mu$m pitch (left) and of a flip-chip assembly of two 50 $\mu$m pitch bump arrays (right) on glass substrates (courtesy SELEX Sistemi Integrati, Rome)[4]

### 1.3 Quality Control of Bump Bonded Assemblies

Inspections before and after flip-chip assembly are crucial to obtain the highest yield for functional pixel modules. Automated inspection of bumped wafers with the combined use of a television camera and laser interferometry allows to find missing bumps, merged bumps, deformed bumps or other defects as well as to measure bump height on wafers. Inspection with high resolution (2 $\mu$m) X-ray machines allows to detect misalignment or merged/bridged bumps previously not detected or caused by the flip-chip process. Both solder and indium bump bonding have been used to produce more than 2000 pixel modules by two different firms with bump defect rates of $\approx 10^{-4}$–$10^{-5}$ at wafer level and $\approx 10^{-3}$–$10^{-4}$ after flip-chip.

### 1.4 Reworking of Bump Bonded Assemblies

A module is built with Known Good Dies (KGD), i.e. all dies are tested prior to flip-chip and only the good ones are used. This is a crucial requirement as the module yield goes with the $n^{th}$ power of the electronics chip yield, n being the number of chips per module. Both solder and indium bump bonded modules have been successfully reworked [7, 5] with a success probability of more than 95%. In both cases the operation requires heating and application of a force pulling off the die to remove it, while leaving some metal on the bond pads. A new die is flipped to the sensor with high likelihood to properly connect all pixels.

## Literatur


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