Fermi National Accelerator Laboratory

BTEV Co

Pixel Detector Module for the BTeV Experiment at Fermilab

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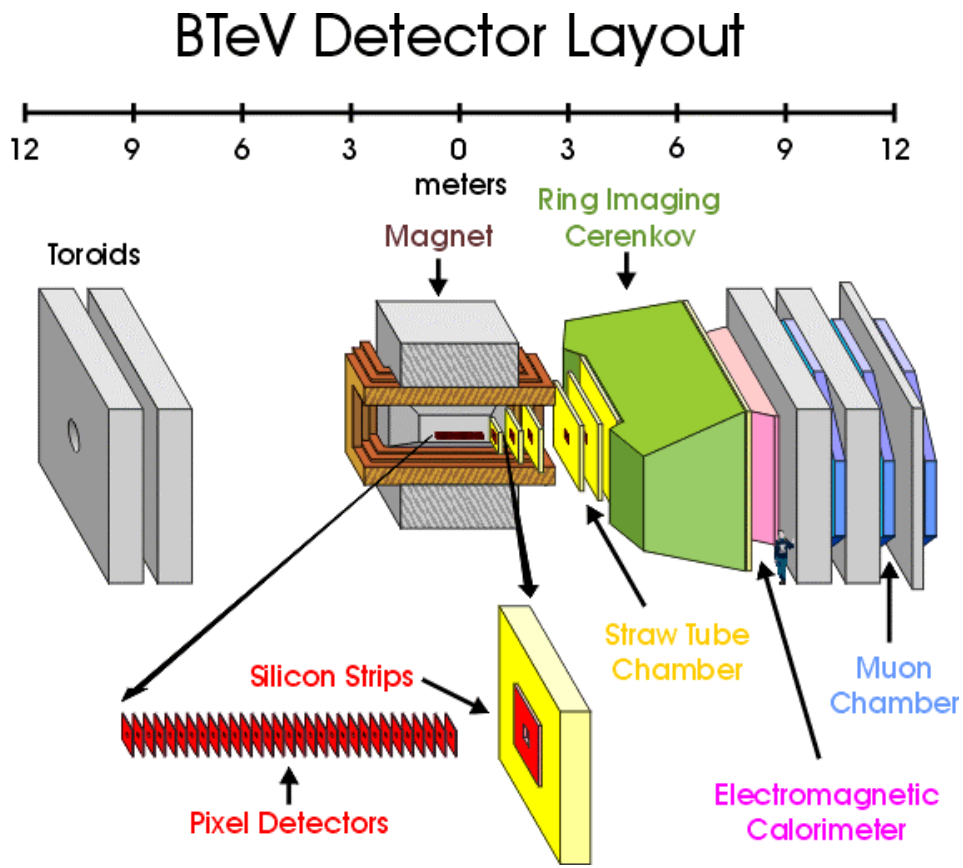
Outline

- BTeV Pixel detector
- Some design constraints
- Cabling
- Pixel half detector
- Pixel module readout scheme
- Pixel module prototypes
- Conclusions

BTeV Pixel Detector

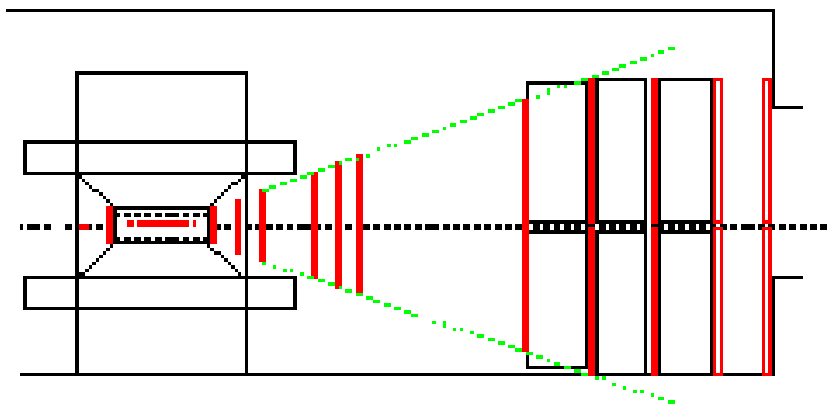


- ~22 million pixel channels.
- 30 pixel detector stations.
- Each pixel station consists of 48 pixel modules.
- Each pixel module consists of either 4, 5, 6, or 8 FPIX readout chips and silicon sensors.

Some Design Constraints

- High readout efficiency required – *Data is used in lowest level BTeV trigger to reconstruct tracks.*
- Cabling
- High radiation environment – *Must use rad-hard components ⇒ ASICs.*
- Inaccessible – *Motivation for designing a reliable/robust readout.*
- HDI and flex cable features –
  - *a) Constrained by feature size of flex technology.*
  - *b) Limited width to avoid interference with adjacent modules ⇒ need to minimize number of lines.*
  - *c) Small production quantities (by industry standards)*
- Cable Bandwidth – *Limits data readout speed.*
- Cost

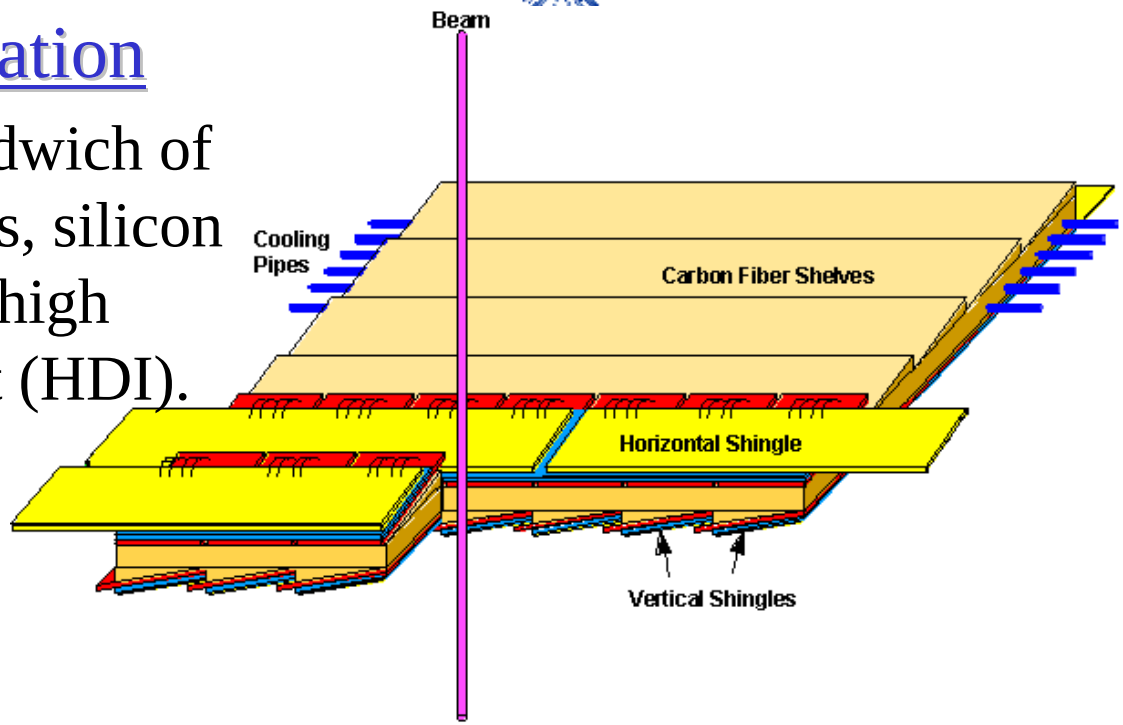
Cabling



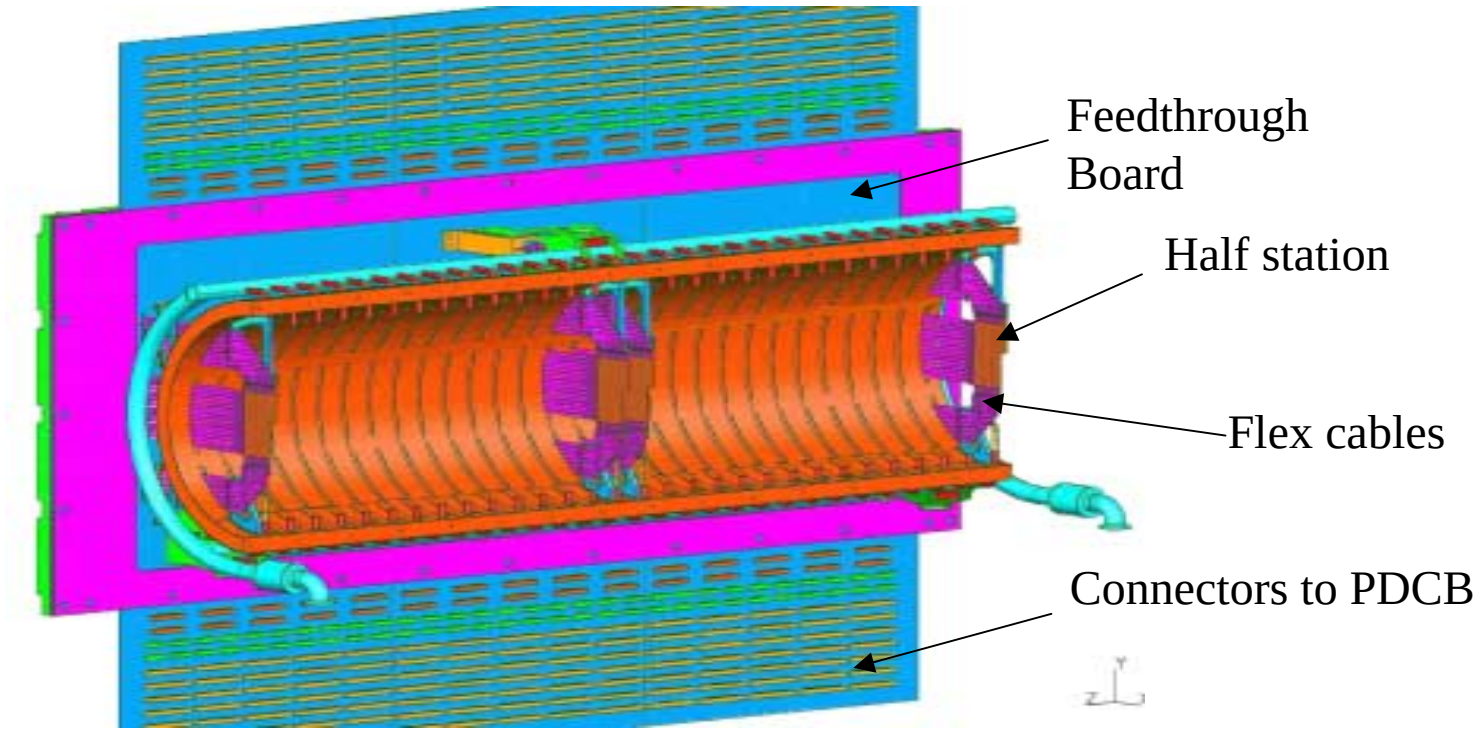
- Several detectors cover forward direction between 10-300 mrad
- The volume outside this region is not instrumented.
- We can add mass to region not instrumented
- Proposal: use copper cables to control and readout the Pixel modules.

Pixel Half Station

- Modules are a sandwich of FPIX readout chips, silicon pixel sensors, and high density flex circuit (HDI).
- High density flex circuit brings power, control and data signals to/from FPIX chips.



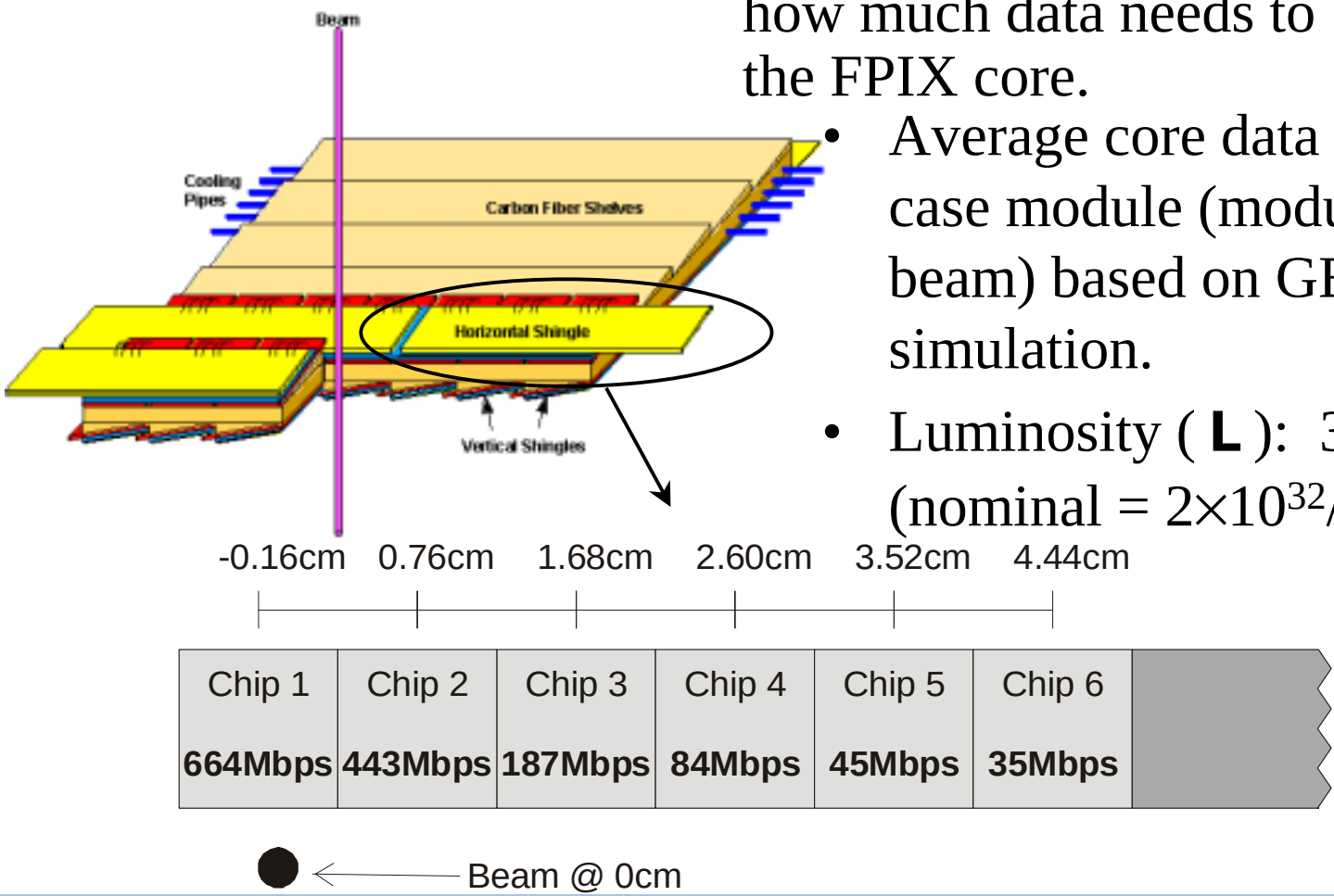
Pixel Half Detector: Point-to-point readout



- FPIX2 → HDI → Flex cables → Feedthrough Board → 10 m twisted pair → Pixel Data Combiner Board (PDCB)

Readout: Simulations

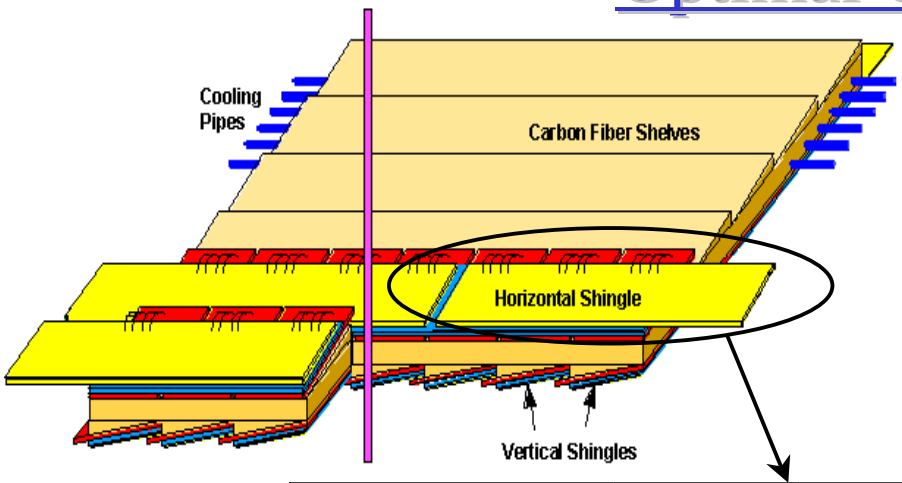
- 1st step in design process is to understand how much data needs to be moved out of the FPIX core.
  - Average core data rates for worst case module (module closest to beam) based on GEANT simulation.
  - Luminosity (**L**): 3× nominal (nominal = $2\times10^{32}/cm^2sec$)



Readout: Design Solution – Key Features

- All signaling is low voltage differential (LVDS) – *Immune to common mode noise, easy to drive 10m, and can be driven and received by today's FPGAs.*
- Data paths are point to point for reliablity.
- Data is serialized – *Core data word is formatted then serialized to save data lines.*
- Configurable number of serializers (6, 4, 2 or 1) – *High data rate chips with 6 serializers while lower data rate chips use a few as 1 serializer.*
- Match core bandwidth to total bandwidth of serializers – *Core operating frequency depends on configuration.*
- Simple word alignment scheme for receiver.

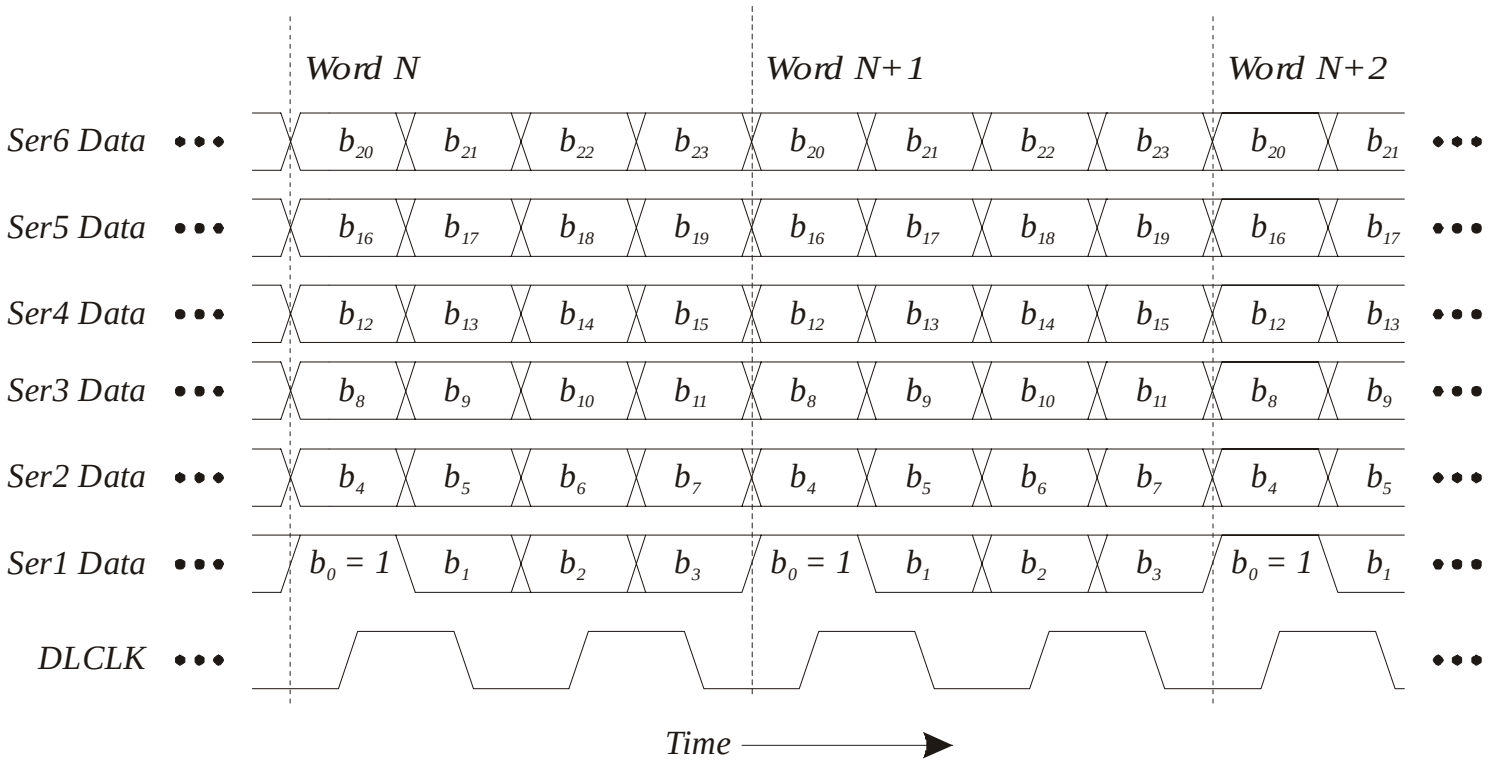
Readout: Verilog Simulations Determine Optimal Configuration



- Simulations (~3000 crossings, ~6500 hits) were run on Verilog model of FPIX core to determine minimum number of serializers while still maintaining high readout efficiency.

	Chip 1	Chip 2	Chip 3	Chip 4	Chip 5	Chip 6
Hits (approx.)	6400	4250	1700	800	450	350
# Serializers	6	6	4	2	1	1
Efficiency @ nominal L	99.7%	100%	100%	100%	100%	100%
Efficienct @ 3× nominal L	98.0%	99.6%	99.6%	99.9%	100%	99.7%

Readout: Data Latch Clock and Example Waveform

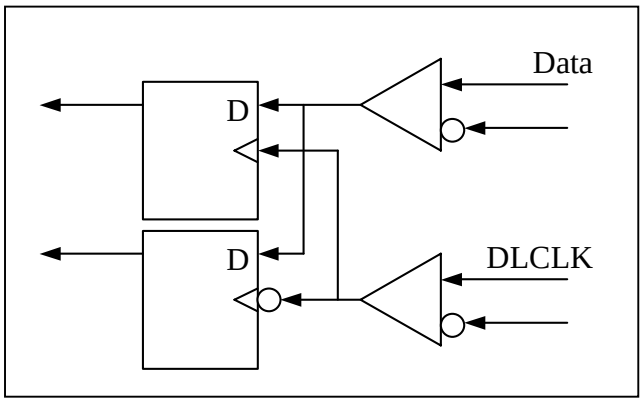


- Both edges of DLCLK used by receiving FPGA to latch data.

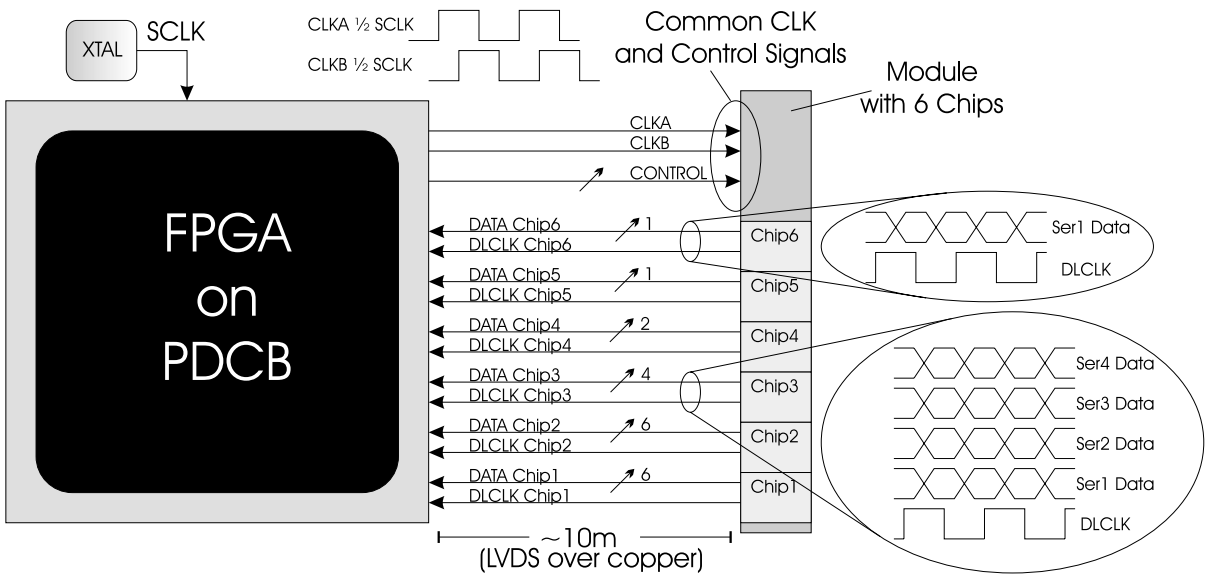
Readout: Pre-FPIX2 LVDS Drivers

- Good quality of the 140Mbit/s eye-pattern of Pre-FPIX2 LVDS drivers.
- 50 foot flat-twisted cable.

Readout: Data Combiner Board and Pixel Module



- Xilinx Virtex II FPGA input blocks configured for LVDS input and double edge data sampling.



Pixel Module Prototypes

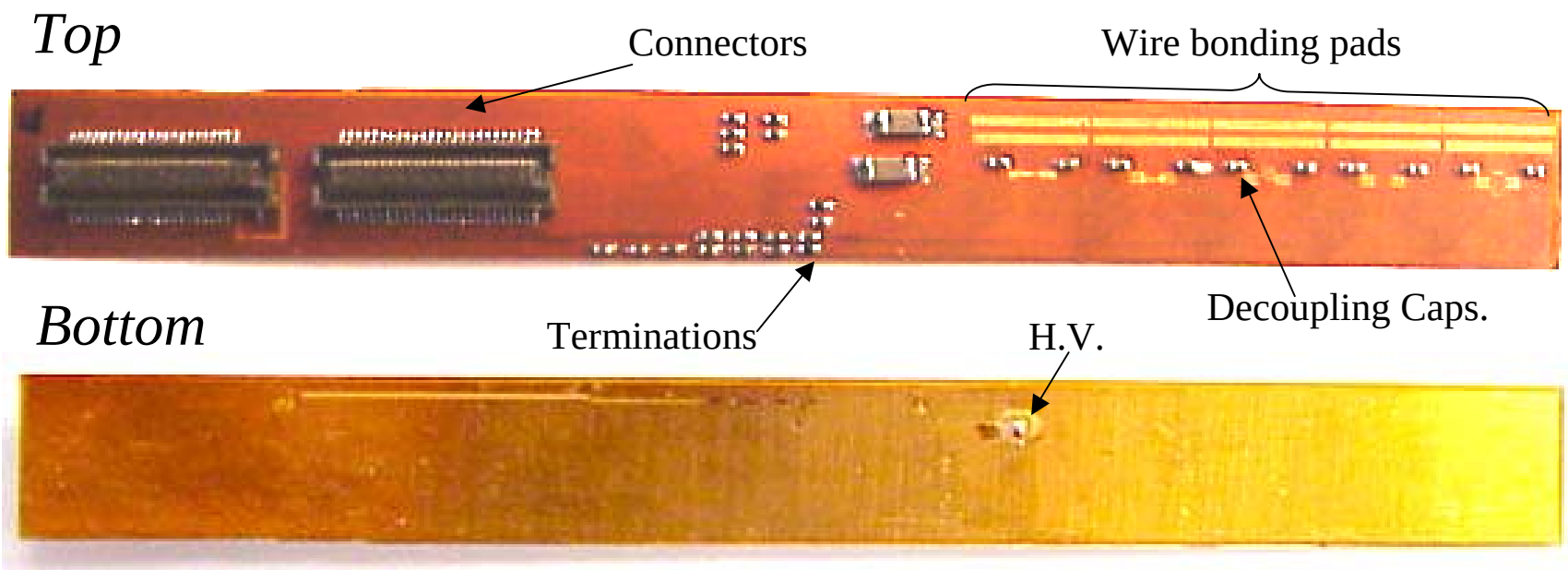
- Uses FPIX1
- HDI with four metal layers
- Two modules characterized:

a) Single readout chip bump bonded to single SINTEF sensor (Indium bumps)

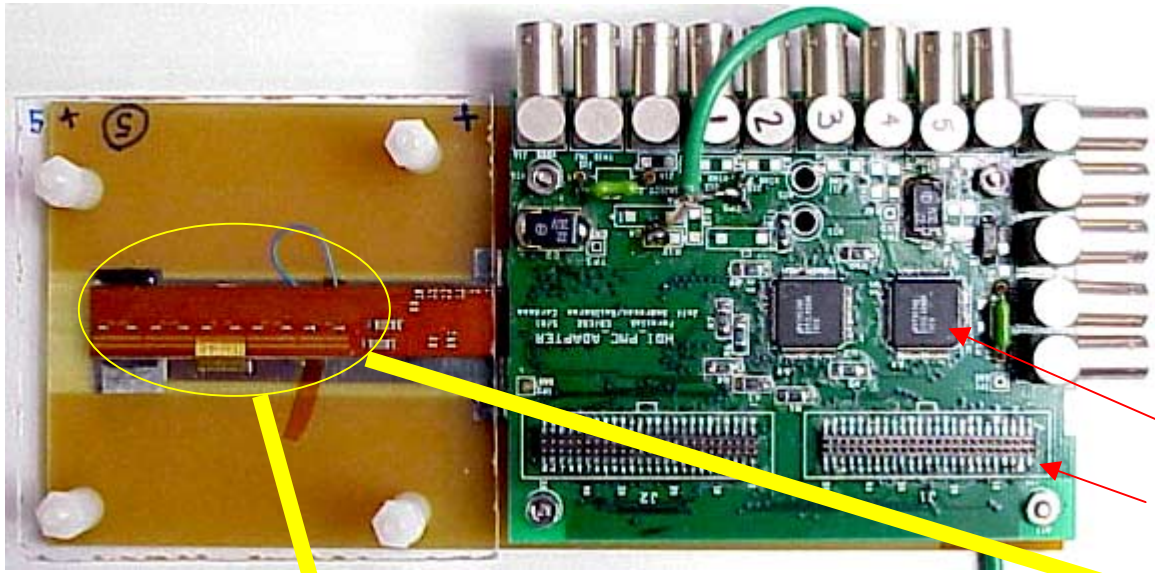
b) Five readout chips with dummy sensor

Prototype: Flex Circuit

- **Dimensions:** 98.5mm x 10.25mm
- **Line width:** 35µm
- **Line to line clearance:** 35µm
- **Metal layer thickness:** 10µm
- **Number of layers:** 4
- **Via pad:** 108µm
- **Lamination:** 5µm epoxy
- **Film thickness (Apical):** 25µm

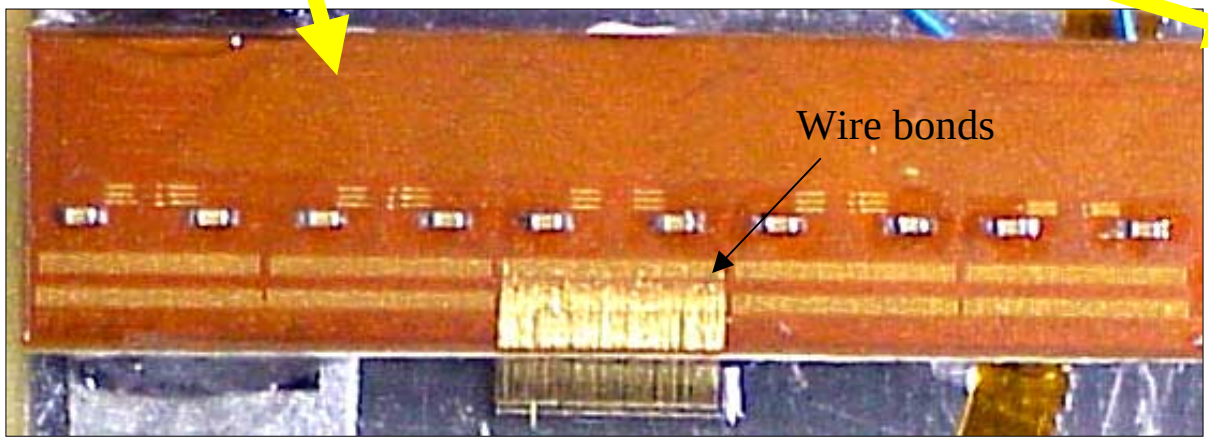


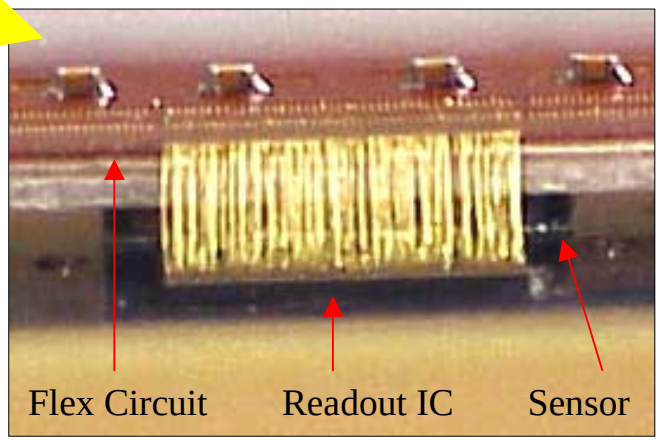
Prototype: Single chip (FPIX1) bonded to SINTEF sensor



LVDS drivers

Connectors to DAQ

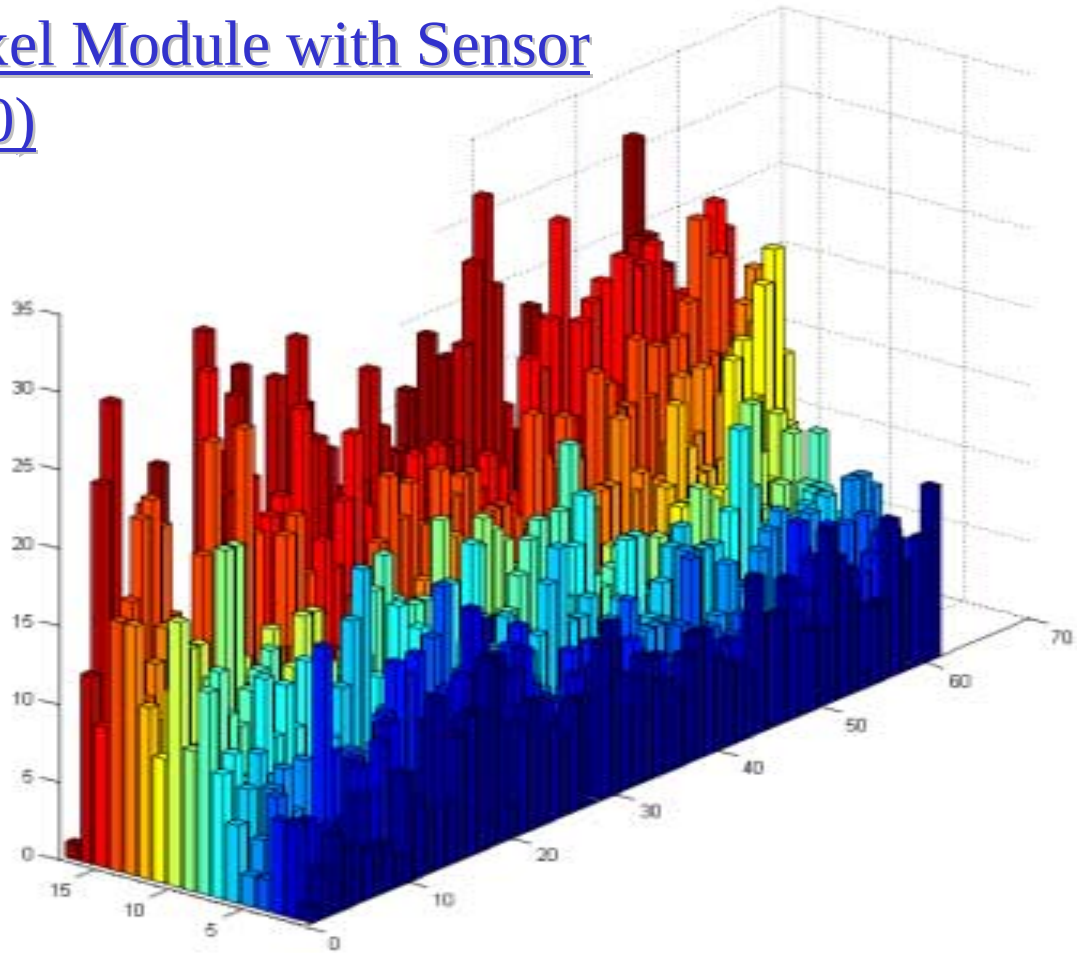


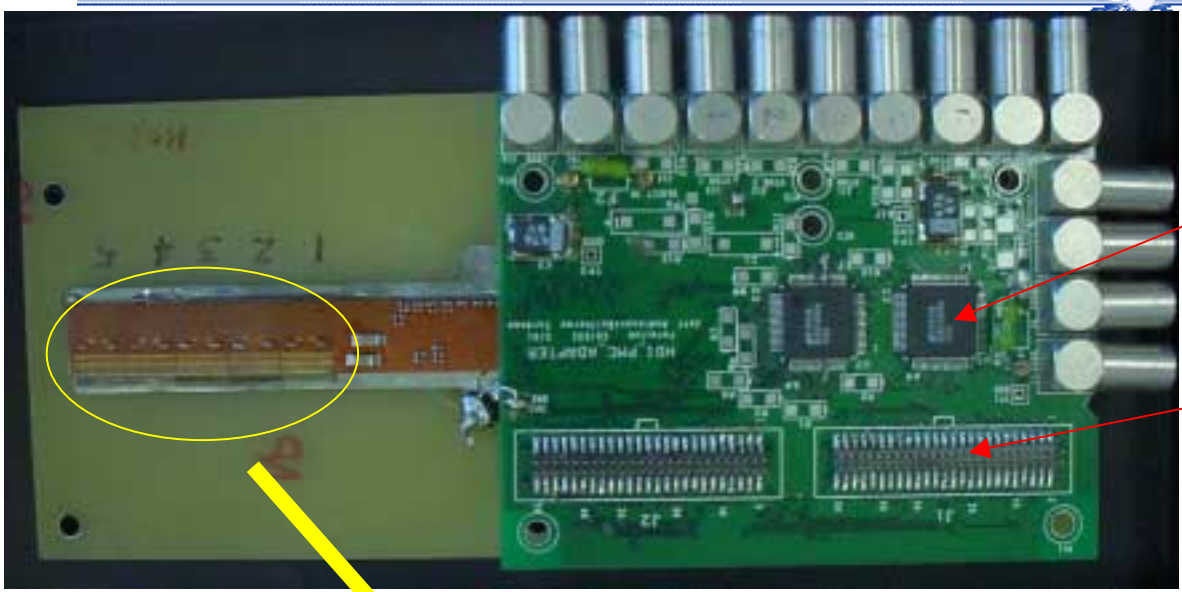


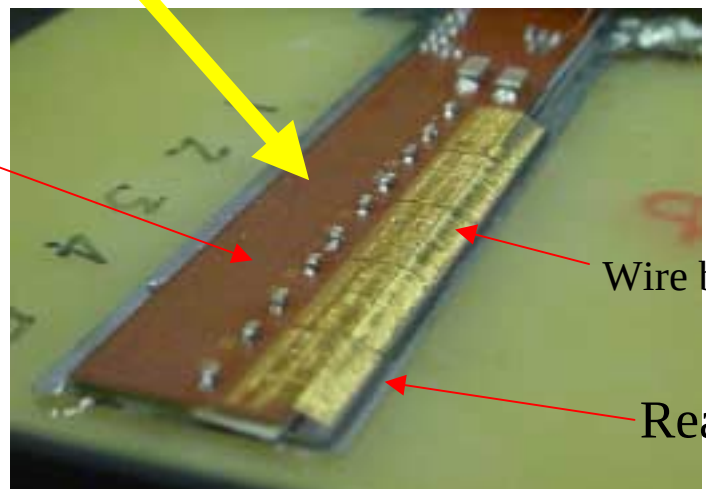
Prototype: Single chip with various threshold settings [e^-]

μ_{Th}	σ_{Th}	μ_{Noise}	σ_{Noise}
7820	408	94	7.5
6529	386	111	11
5500	377	113	13
4410	380	107	15
3338	390	116	20
2289	391	117	21

Prototype: Pixel Module with Sensor Hit Map (Sr90)





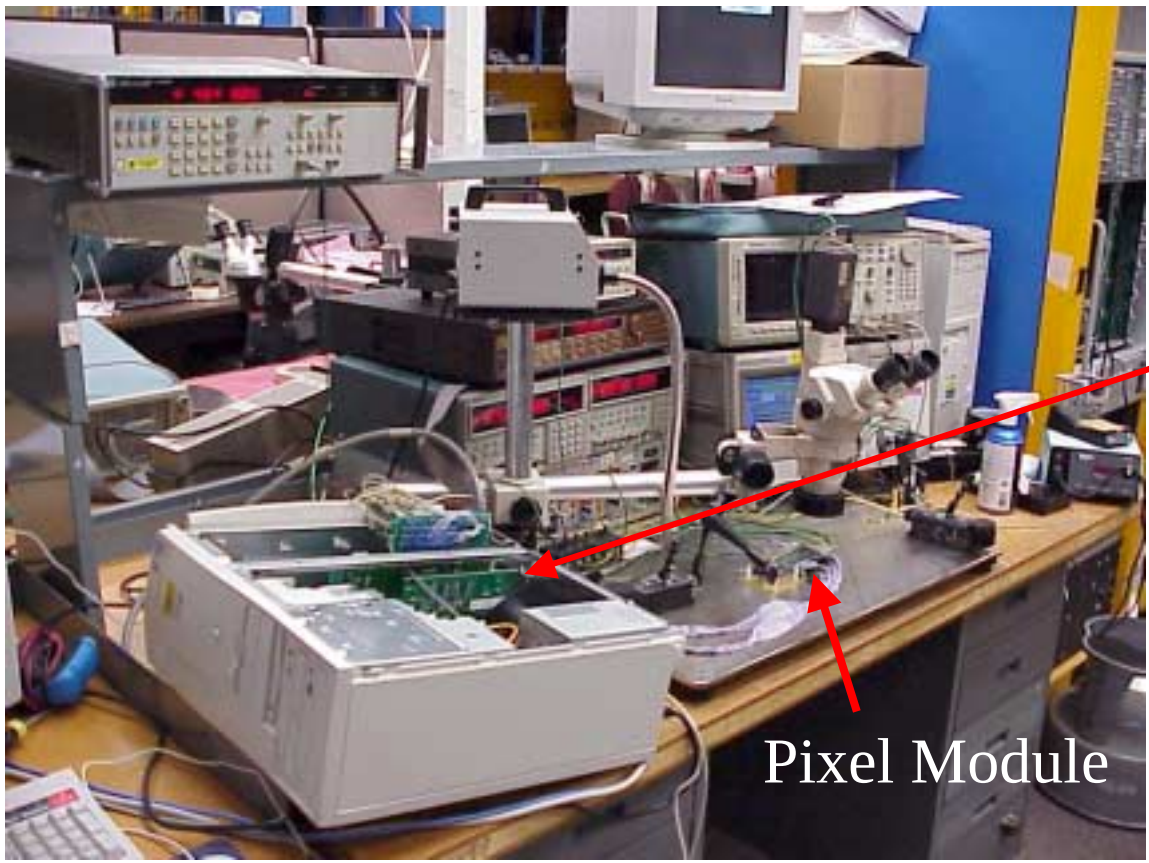


Prototype:
Five chips (FPIX1)
with dummy sensor

Prototype: Five readout chips with dummy sensor [e^-]

	Chip # 5				Chip # 3			
V_{Th}[V]	μ_{Th}	σ_{Th}	μ_N	σ_N	μ_{Th}	σ_{Th}	μ_N	σ_N
1.95	11110	375	92	12	8843	335	88	10
2	10327	345	94	13	7800	300	88	8
2.05	9170	345	90	16	6790	316	87	9
2.1	8196	371	96	15	5715	330	96	10
2.15	7225	367	91	16	4683	329	95	10

Prototype: PCI Based Test Stand



- FPGA controlling all functions
- PCI interface
- 4MB of RAM
- Daughter card interface (IEEE1386)
- JTAG
- USB
- RS232

Conclusions

- Only one rad-hard component necessary (FPIX itself) – digitizes, serializes, each output drives 140 Mbps over 10m.
- Pixel control/readout system using copper cables.
- Configurable readout bandwidth to optimize data path width.
- Readout efficiency adequate for BTeV trigger system for track reconstruction.
- Prototype
  a) No significant increase in noise and threshold dispersion when compared with previous single chip prototypes
  b) No crosstalk problems between the digital and analog sections of the readout chip and flex circuit.
- Readout design offers 2 Tbps bandwidth for BTeV pixel detector.