
Flip Chip Hybridization of Pixel Detectors for the ALICE and LHCb Experiments

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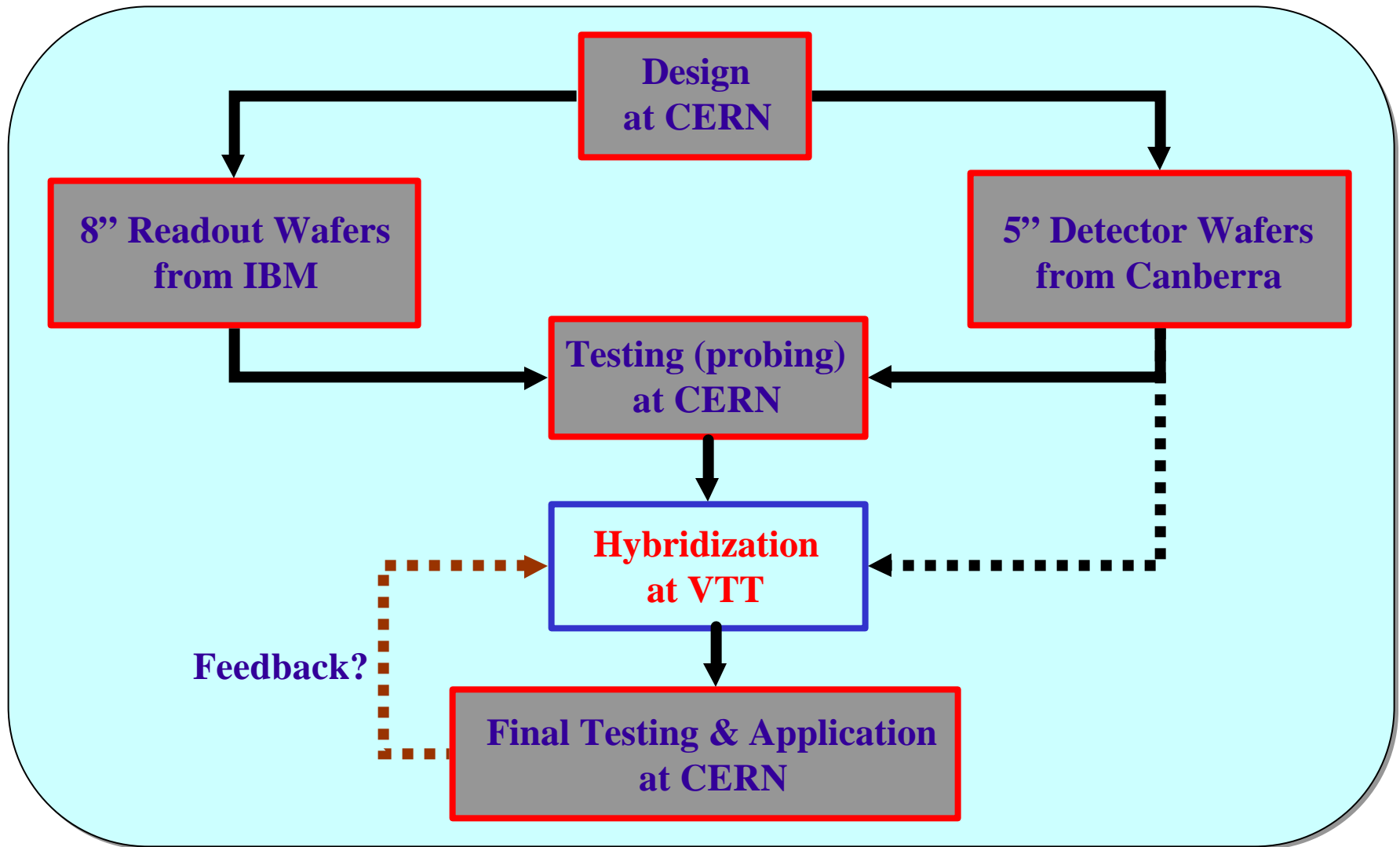
Thursday, September 12, 2002, 9:20am - 9:40am



Outline

- Logistics
- Bumping Process
- Facilities/Equipment
- Thinning of Wafers
- Flip Chip Assembly
- CERN ALICE & LHCb Chips
- Test Results on Assemblies
- Yield Factors
- Shortlist of Things
- Summary

Logistics



Process Steps for Hybridization at VTT

- Solder Bumping of Readout Wafers
- Solderable Pads on Detector Wafers

← Done in Class-10
clean room

- Optional Thinning of (Readout) Wafers

- Dicing

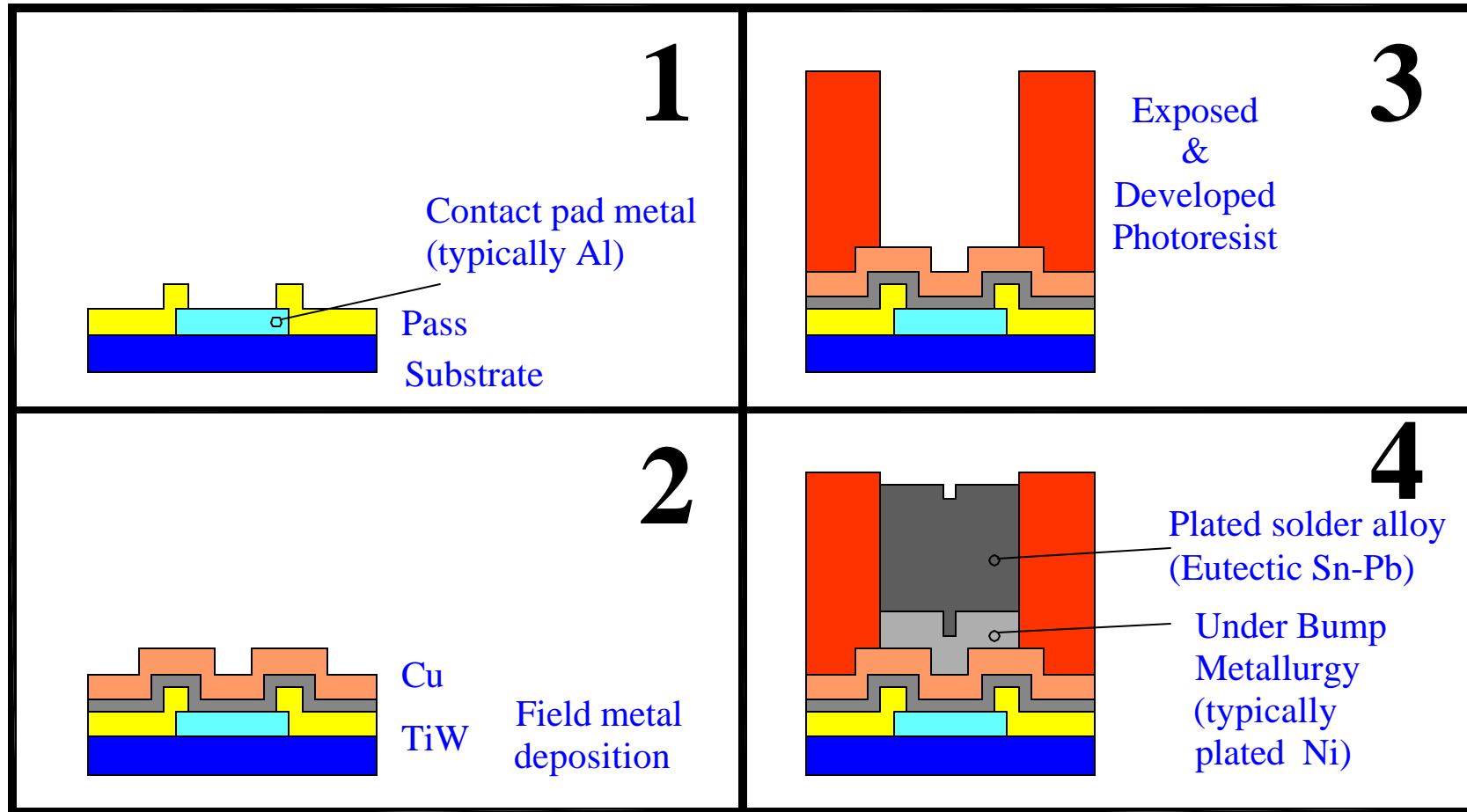
- Flip Chip Bonding

← Done in Class-10
clean room

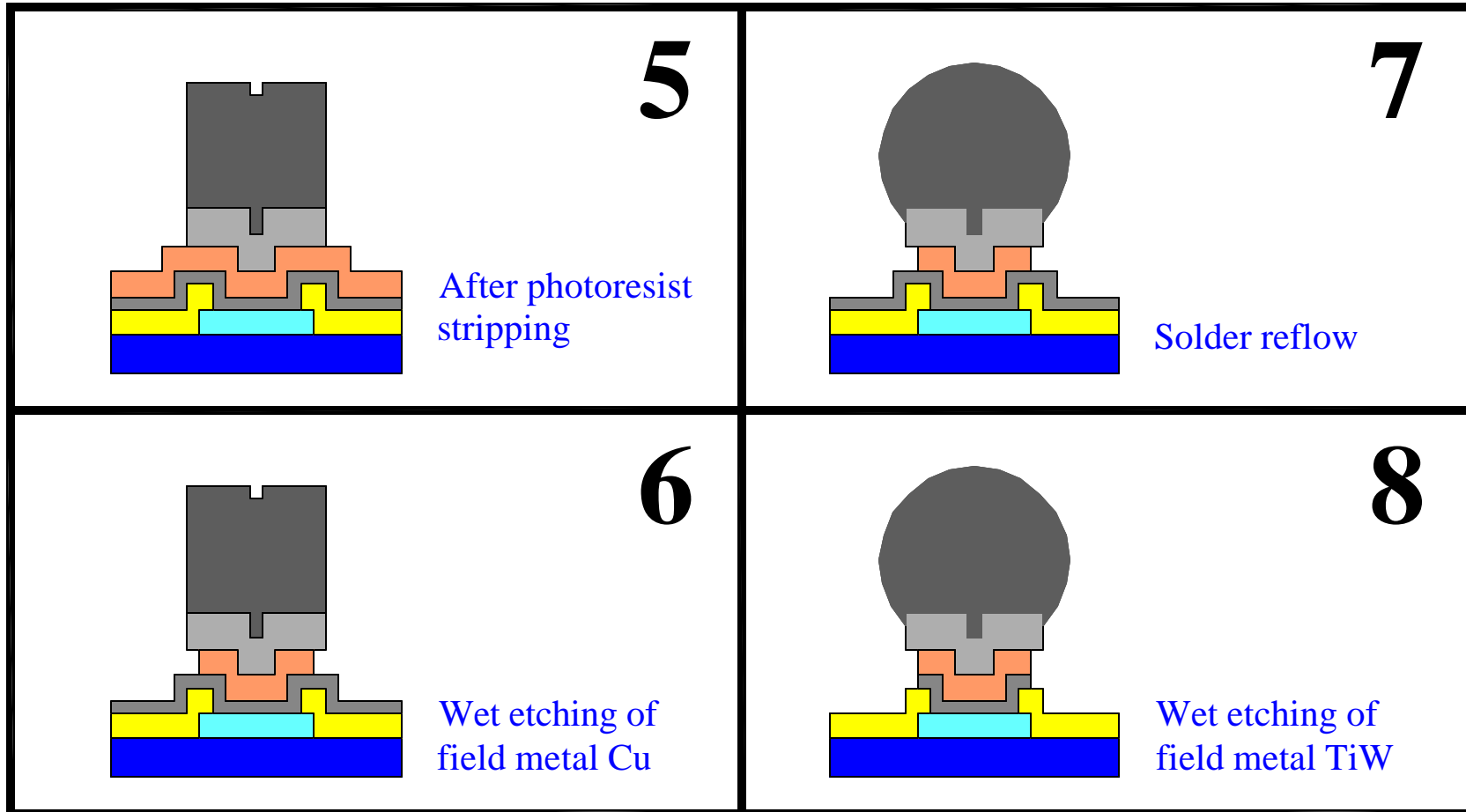
Flip Chip Process: Key Features

- **200-mm (8") wafer capability.**
- **Eutectic tin-lead solder bumps are used for mechanical strength of bonded assemblies.**
- **Bump deposition by electroplating.**
- **Process is compatible with wire bonding pads and unpassivated backside metallization.**
- **Thinning (back grinding) of bumped readout wafers.**
- **'Clean' dicing with front side protection using either photoresist or tape.**
- **Fluxless flip chip bonding.**

Bumping Process



Bumping Process [cont'd]



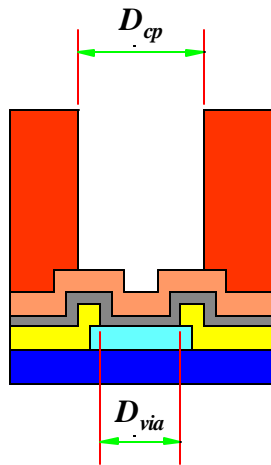
Processes/Equipment at VTT

PROCESS	EQUIPMENT
Photoresist coating	Suss MicroTec ACS200
Mask Aligners	Suss MicroTec MA6 & MA200CC
Thin film sputtering	Von Ardenne CS730S, MRC 903
Electroplating (Ni, Sn-Pb)	Proprietary System
Bump Reflow	ATV SRO-704-R formic acid oven
Wafer Thinning	Strasbaugh 7AF Intelligent Grinder
Dicing Saw	Disco DFD651
Flip Chip Bonder	Suss MicroTec FC150

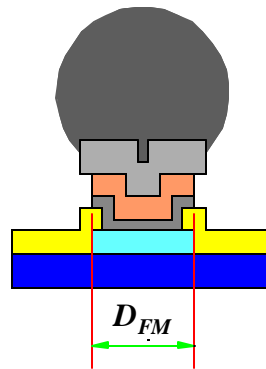


Photolithography Step for Bumping

Bump opening on mask overlaps passivation via. Overlap is determined by field metal underetching & alignment accuracy.



passivation via

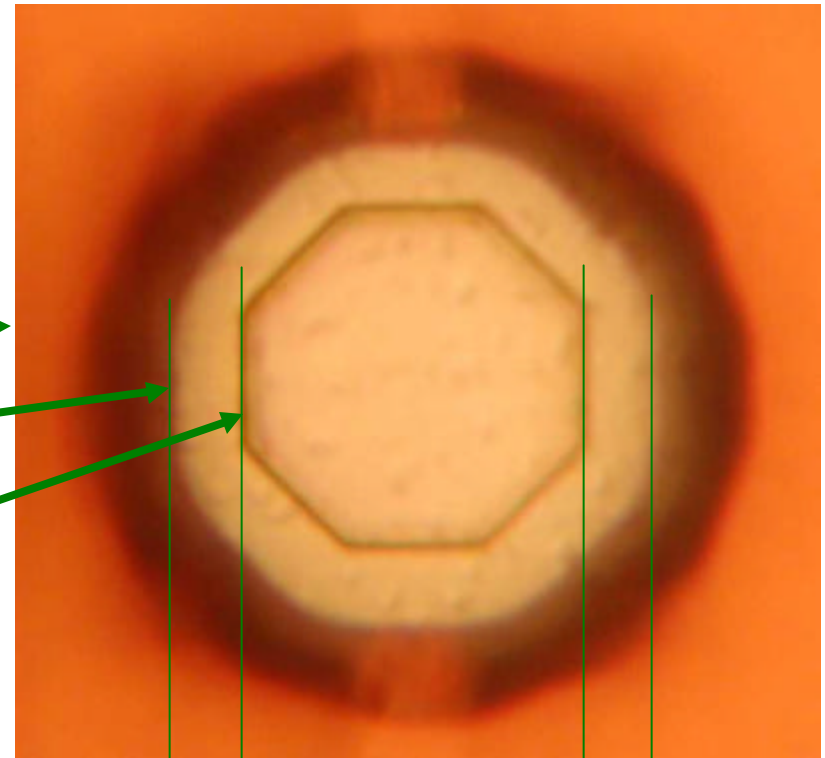


final bump foot

Thick photoresist

Opening in resist

Passivation via



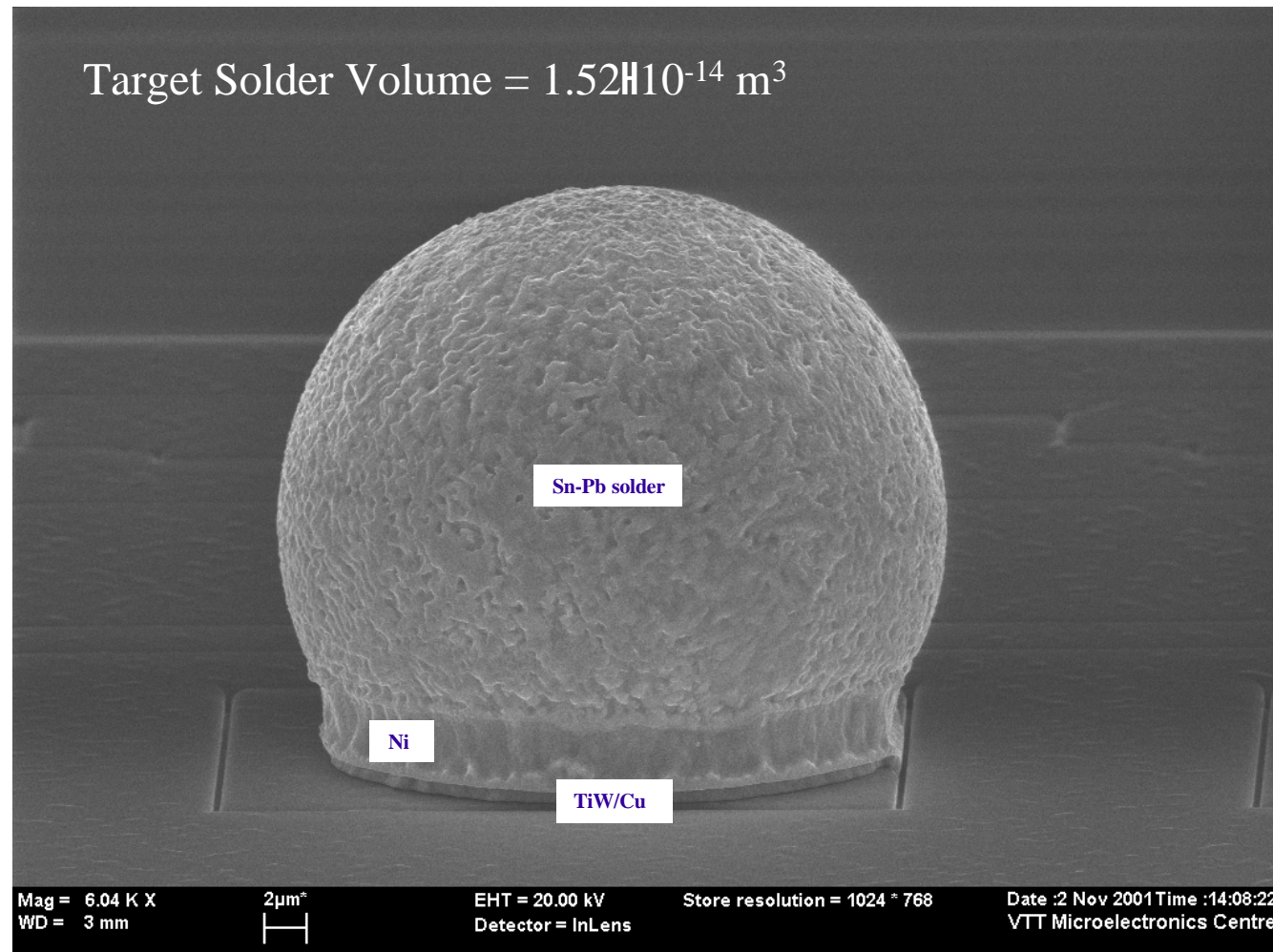
24 mm

29 mm

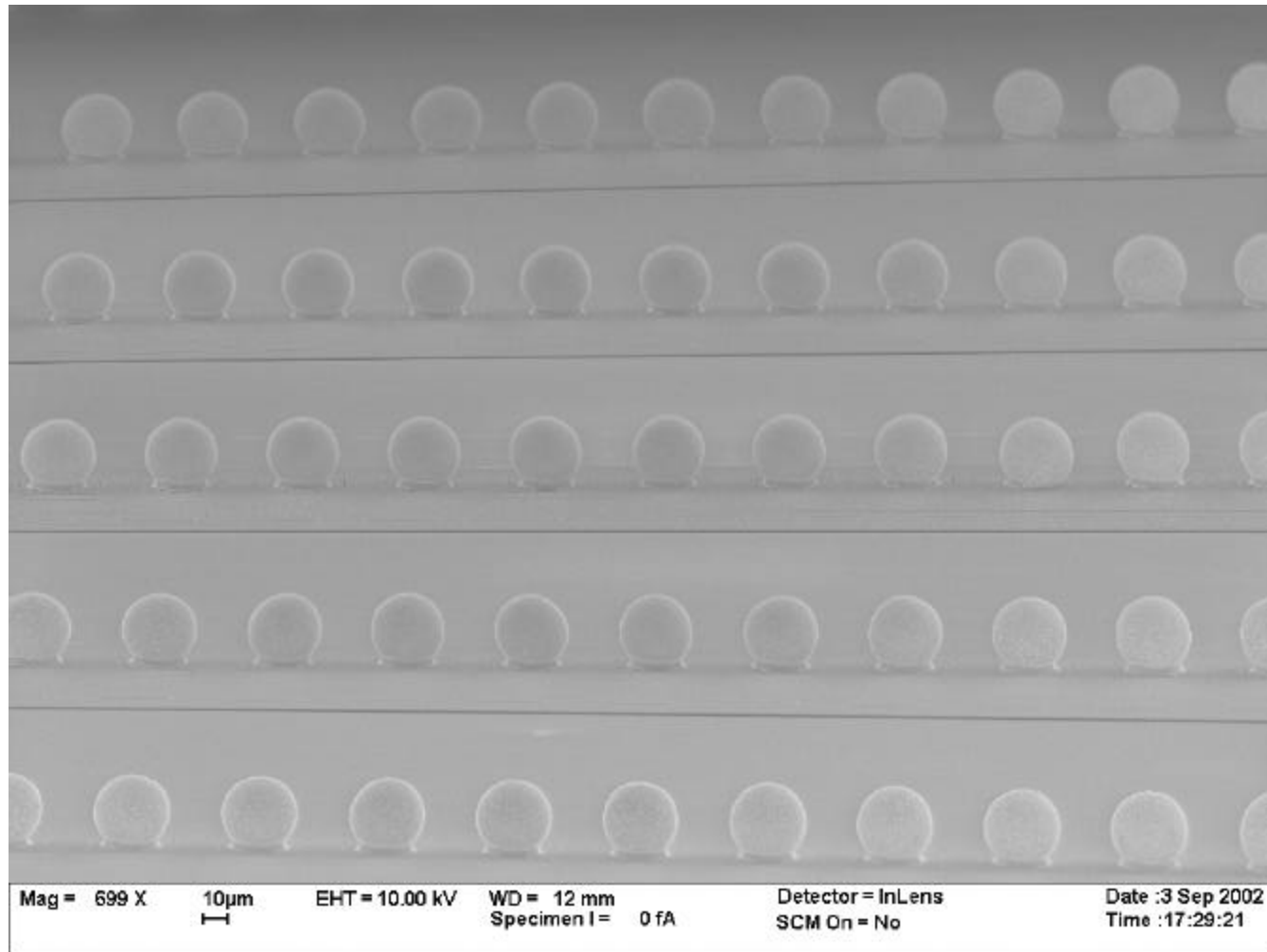
Example: CERN ALICE1LHCb readout.



Solder Bump on ALICE1LHCb Readout Chip After Reflow



5 Rows of Bumps on ALICE1LHCb Readout Chip After Reflow



Wafer Thinning

Thinning is preferably done after bumping!



**Strasbaugh 7AF
Intelligent Grinder**

PROCESS STEPS

- Front side protection/planarization: UV-curable tape laminated on wafer.
- Back grinding using diamond wheels with two different grit sizes (coarse + fine).
- Defect layer left by mechanical grinding is removed by wet chemical etching.
- Protective tape is UV-exposed and delaminated.

NOTES

- Thickness down to 150 μm (200-mm/8" wafers).
- Total thickness variation (TTV) with protective tape < 5 μm .
- Post-grinding defect layer wet chemical etching improves die strength.



Flip Chip Bonding

Flip chip assembly is done in a Class-10 clean room.



Suss MicroTec FC150 Flip Chip Bonder with both Universal and Solder Reflow Bonding Arms.

PROCESS STEPS

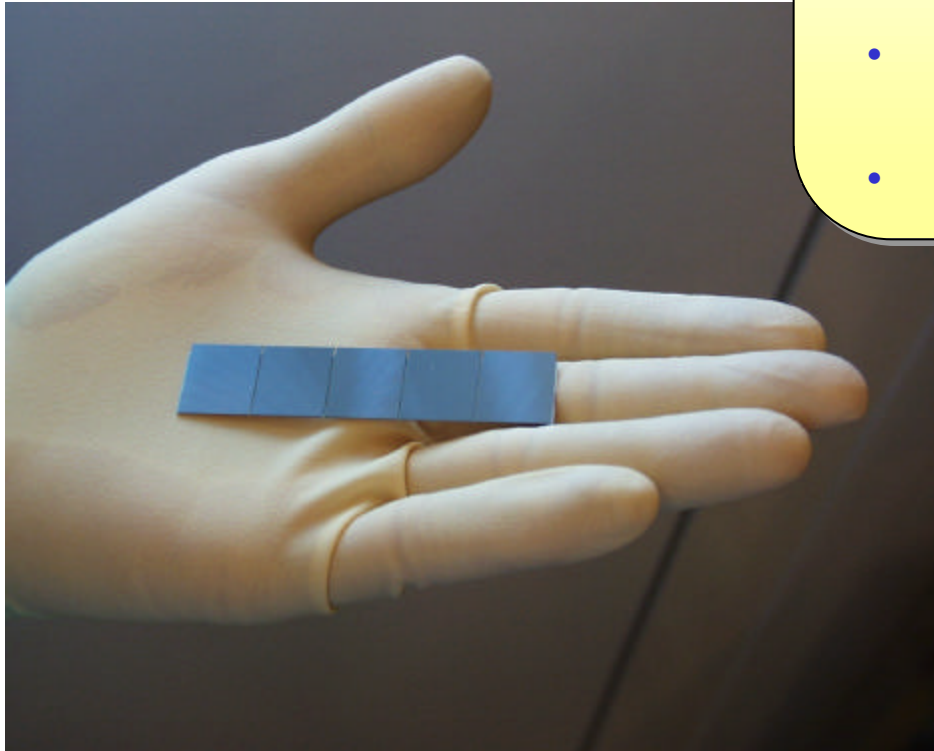
- Preliminary alignment.
- Detector and readout chips are adjusted exactly parallel using a laser autocollimator.
- Lateral alignment (x,y, q).
- Pre-bonding compression of softened bumps.
- Reflow bonding.
- Cooling.

NOTES

- Chips are heated through custom SiC vacuum tools using infrared halogen lamps.
- Alignment accuracy: < 3 mm.
- Throughput: 3-4 bondings/hour.

ALICE1 'Ladder' Assembly

Five ALICE1LHCb readout chips bonded on ALICE1 detector ladder

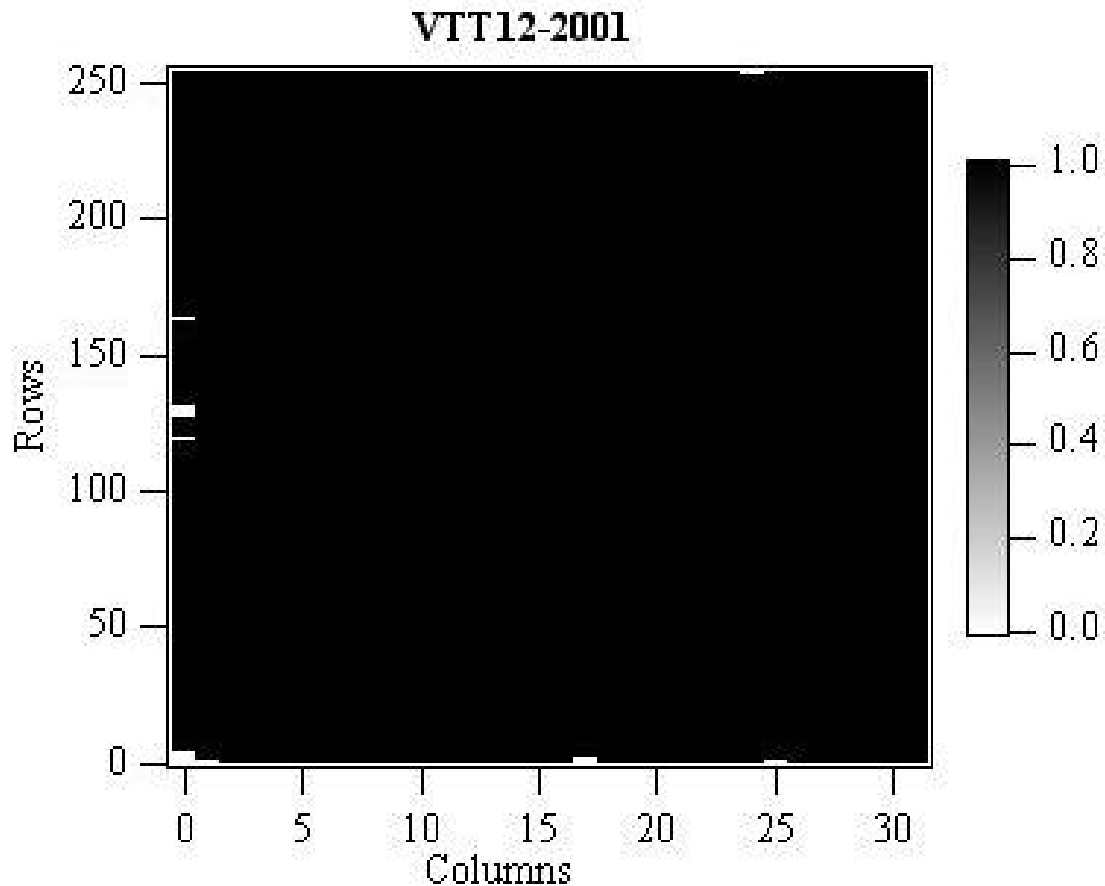


DIMENSIONS

- Detector chip size: 70.7 mm x 13.9 mm.
- Readout chip size: 13.7 mm x 15.9 mm.
- Detector thickness: 200 mm or 300 mm.
- Readout thickness: 300 mm or 750 mm.
- Chip-to-substrate distance: 20 mm.

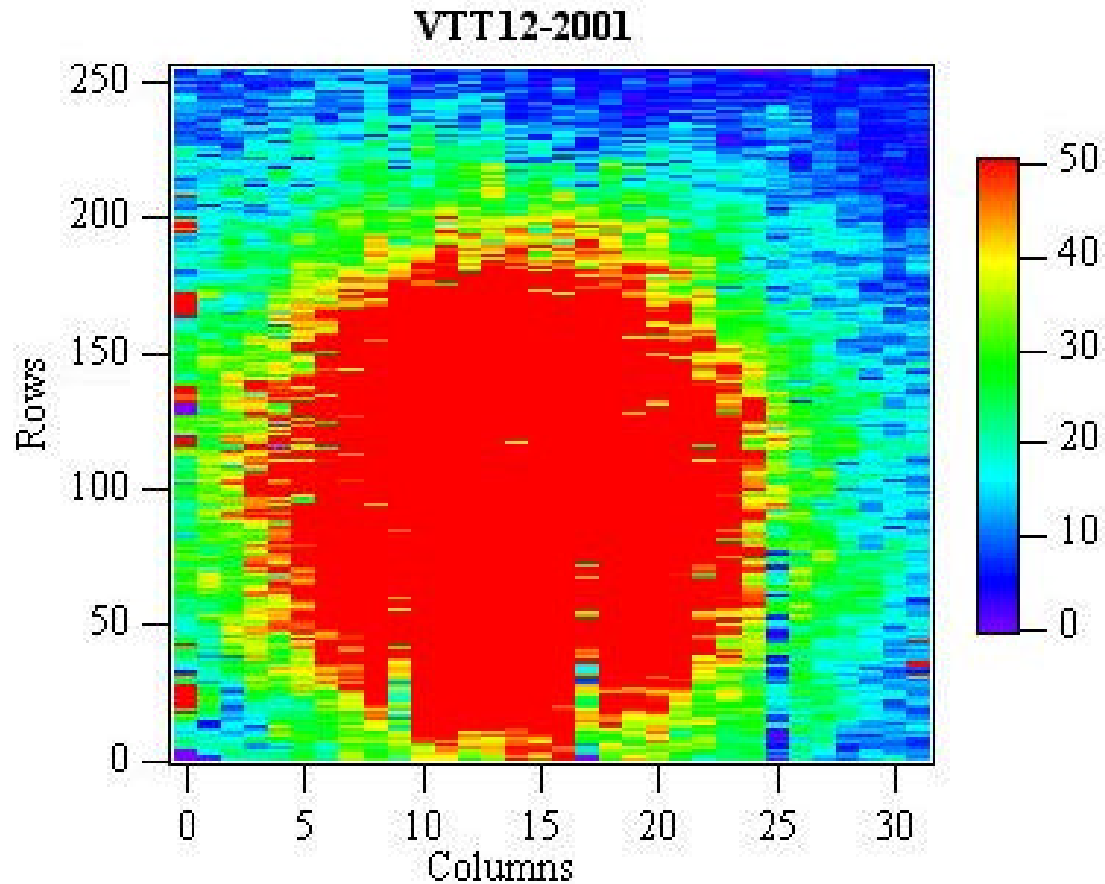
ALICE1 Single: "VTT12"

"VTT12" assembly (an early one, made in 2001) irradiated with a strontium source. Output scaled to "1" to show dead pixels. The number of dead pixels is 14 out of a total of 8,192.



ALICE1 Single: "VTT12"

"VTT12" assembly irradiated with a strontium source. Output scaled to max. "50" to show intensity of beam. The columnar imperfections are due to artefacts of the readout chip.



Yield Factors

- **Pre-bumping/assembly.** Foundry yield, particles generated in probing and handling (and history of wafers in general). Detector side: Defects in polyimide passivation.
- **Bumping/assembly.** Missing bumps, shorted bumps, high contact resistance (influenced by history of wafers), detector dicing, bonding yield.
- **Post-bumping/assembly.** Handling, correct test procedure, interpretation of test results.

Yield [cont'd]

- **VTT's 'generic' flip chip process has been customized to the wafers used by CERN, with consequent improvements in yield.**
 - **Field metal deposition on detector side.**
 - **Field metal etching: both sides**
 - **Reflow on readout side.**
 - **Detector dicing process.**
 - **Flip chip bonding parameters**
- **About 30 ALICE1 single, 5 ALICE1 ladder, and 20 LHCb single assemblies have been delivered to CERN.**
- **The latest assemblies seem to have around 5 to 10 dead pixels per readout chip (0.06 % to 0.12 % of a total of 8,192). ("Class-1" readout chip pixel loss up to 1 %!)**

Shortlist of Things...

- Whole wafers preferred for bumping!
- Alignment targets with known locations are required on wafers (and matching targets on masks).
- Potential stitching problem with stepper-processed wafers (1:1 contact aligners used at VTT).
- Kerf width in dicing is non-zero. Preferably no metal on dicing lanes (on either side of wafer).
- Three smooth areas of at least 50 mm in diameter are needed on both detector and readout chips at the same mutually aligned locations near chip periphery for laser leveling in flip chip bonder.

Summary

- **A brief overview of VTT's bumping and flip chip assembly capabilities was presented.**
- **The hybridization of CERN's ALICE and LHCb detectors was shown as an example.**
- **We wish to thank Michael Campbell, Petra Riedler & Ken Wyllie of CERN for providing test results on bonded assemblies.**