Active Pixel Sensor Architectures in Standard CMOS Technology for Charged-Particle Detection

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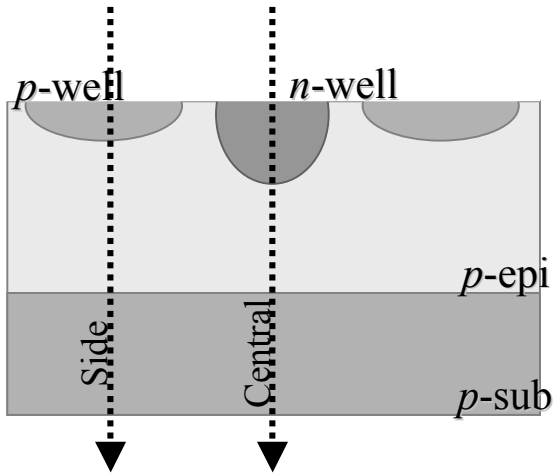
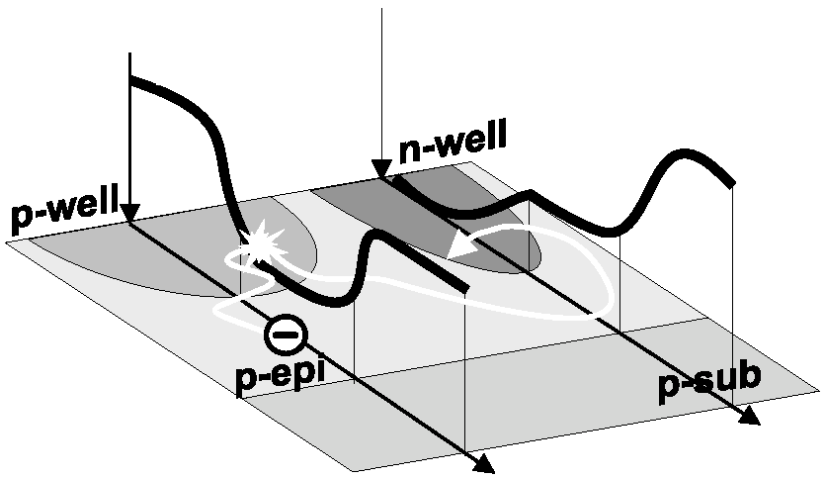
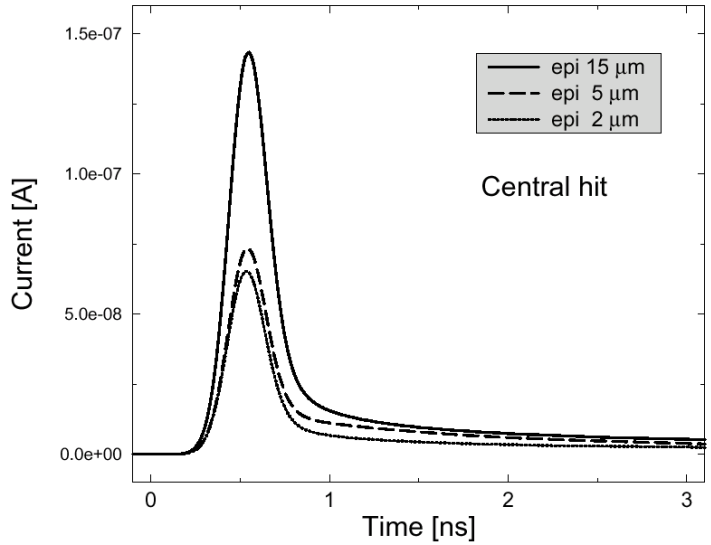
Outline

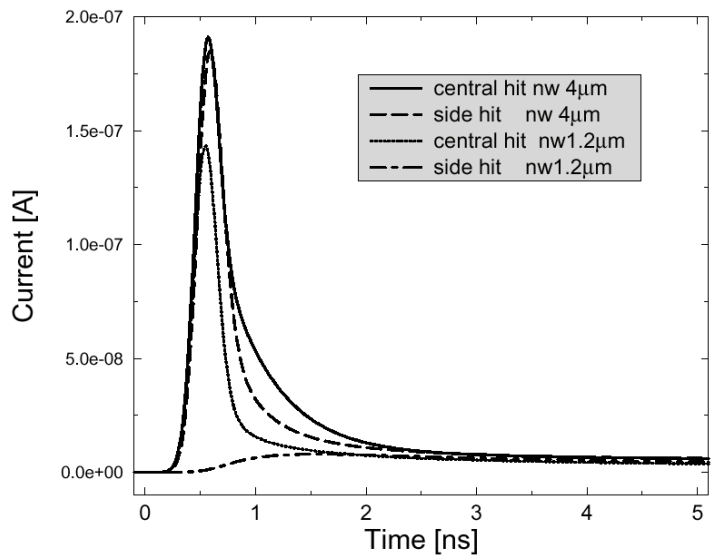
- Introduction.
- Active Pixel Sensor in standard CMOS technology.
- Technology Optimization.
- Design flow.
- Architectures of charged-particle CMOS sensors.
- Results analysis.
- Conclusions.

Technology Analysis









Technology Hints for CMOS APS

- EPI layer importance …
- Substrate generation contribution is important !
- n-well depth impact on charge collection…

⇩

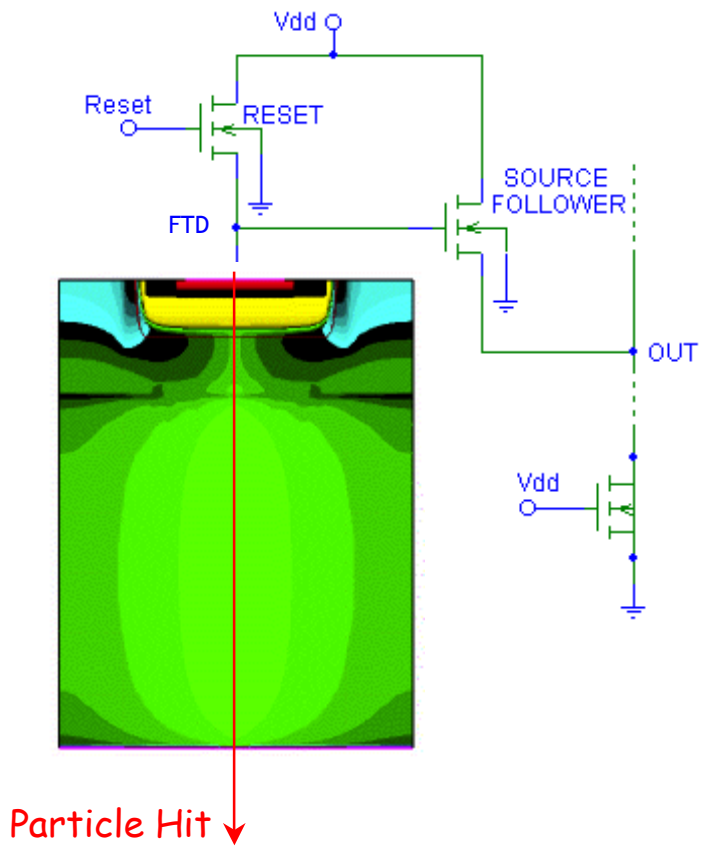
Standard CMOS (deep-submicron) technologies:

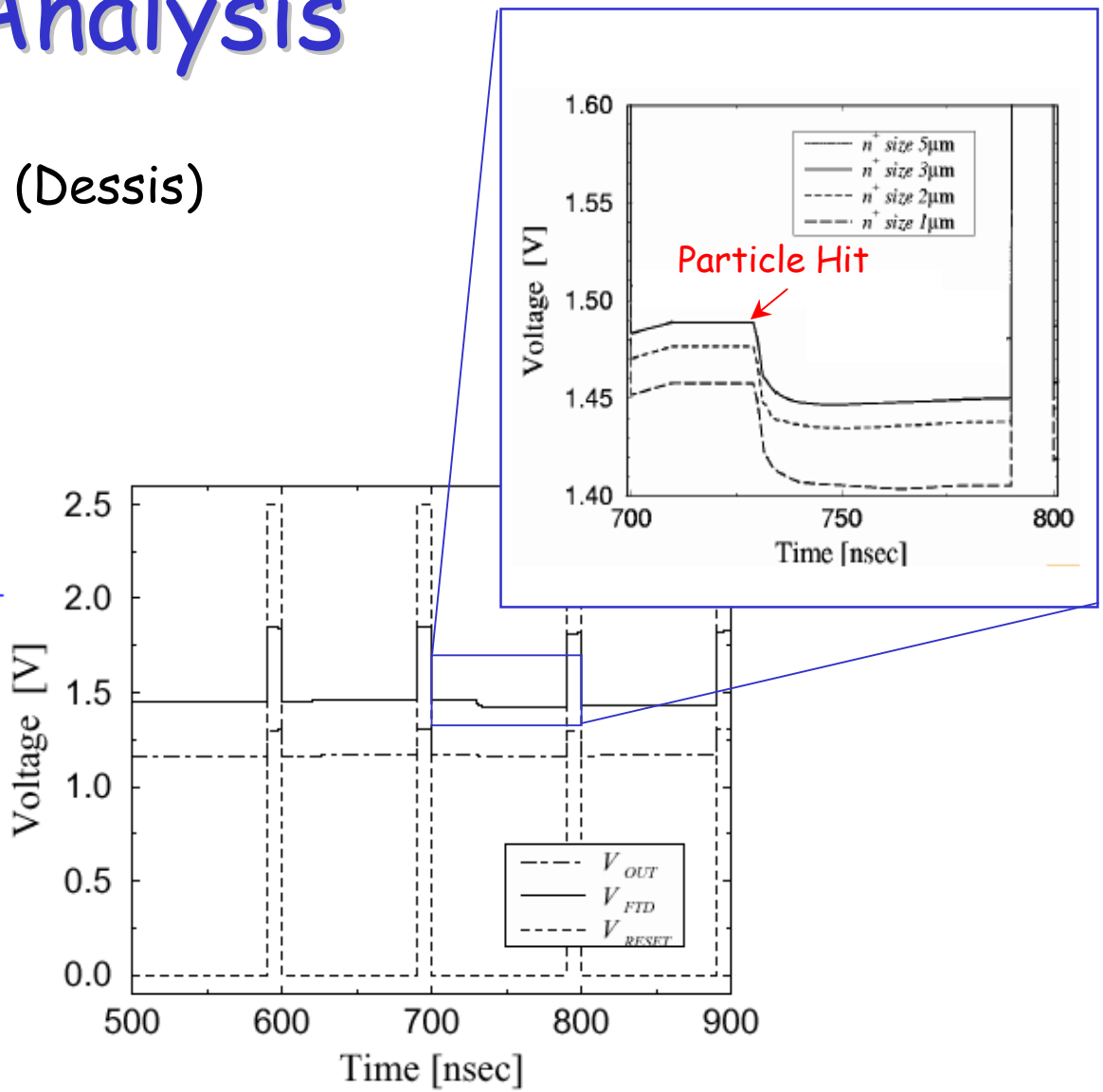
- Smart read-out electronics integration is easier.
- $C_{photodiode}$ is lower, S/N is still acceptable.
- Better control of life-time of the technology node.

↳ Comprehensive technology-node analysis…

Mixed-Mode Analysis

- Device/Circuit Simulations (Dessis)



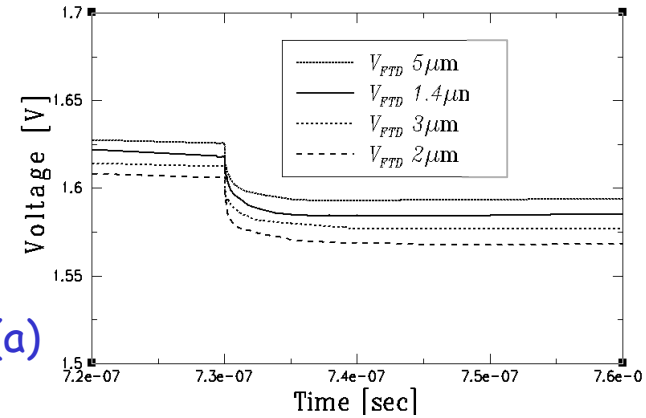


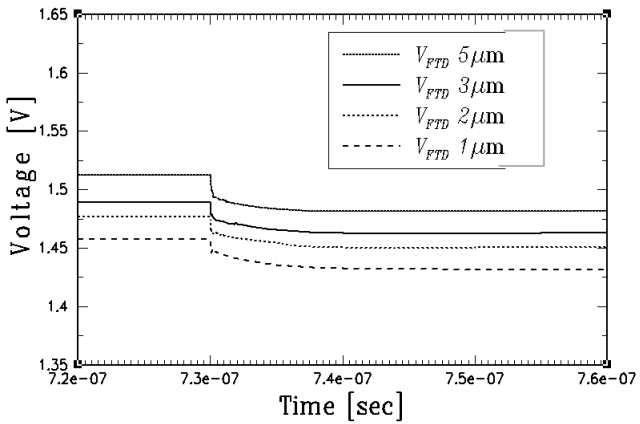
Technology Options

A - No EPI-layer

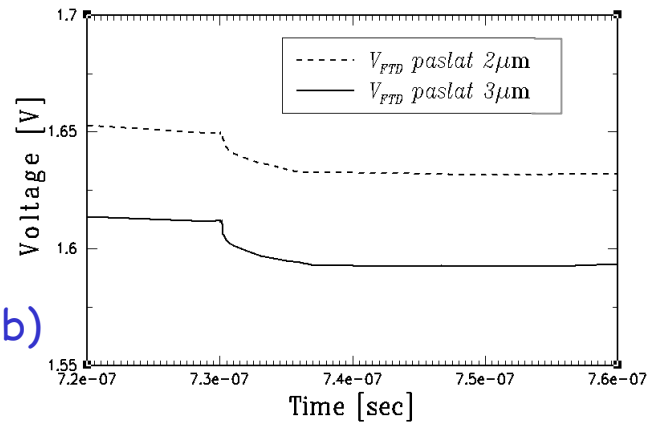
B - EPI-layer

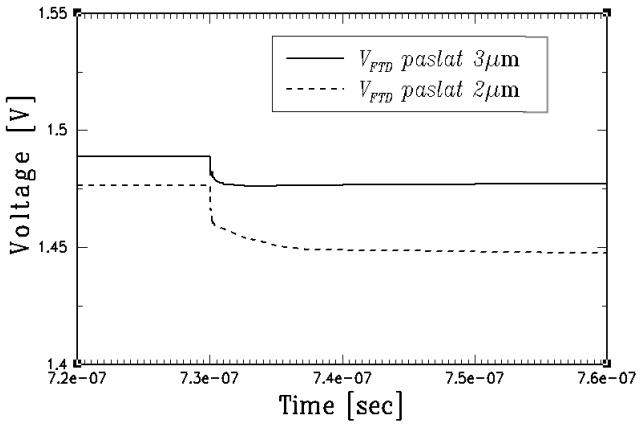
(a)





(b)



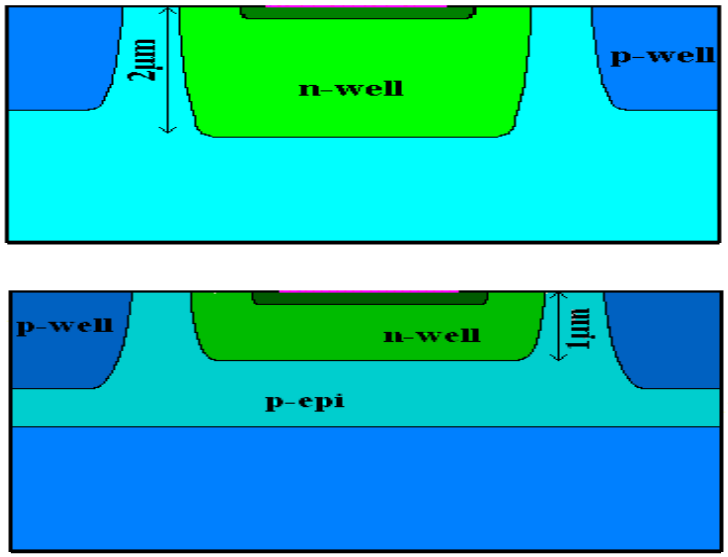


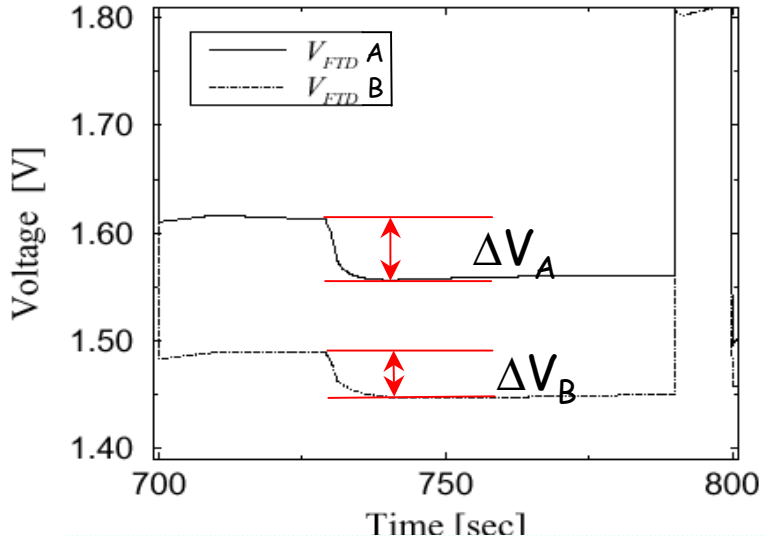
A		B	
Diode Area	ΔV_{FTD}	Diode Area	ΔV_{FTD}
1.4x1.4	34 mV	1.0x1.0	32 mV
2.0x2.0	40 mV	2.0x2.0	25 mV
3.0x3.0	36 mV	3.0x3.0	26 mV
5.0x5.0	32 mV	5.0x5.0	30 mV

A		B	
Diode Area	ΔV_{FTD}	Diode Area	ΔV_{FTD}
2.0x2.0	28 mV	2.0x2.0	30 mV
3.0x3.0	20 mV	3.0x3.0	18 mV

Voltage responses as a function of the sensitive element area for different particle trajectories: (a) central, (b) lateral.

Technology Options (2)

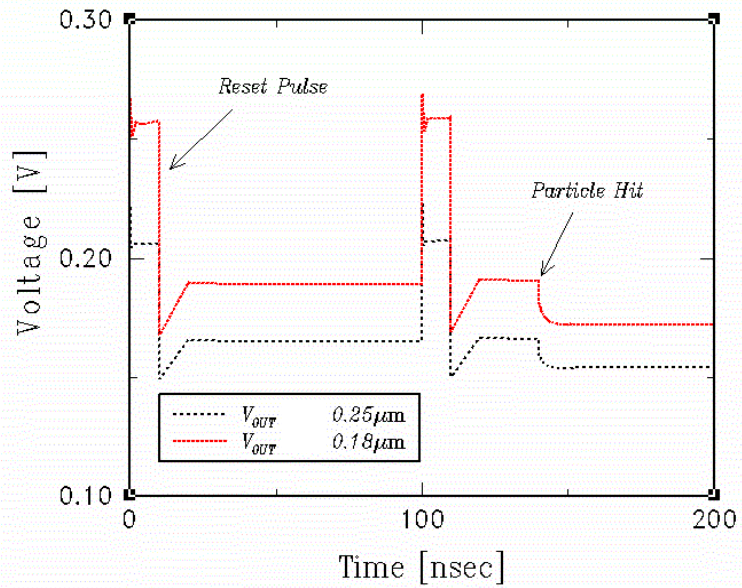




ΔV_A swing greater than ΔV_B !

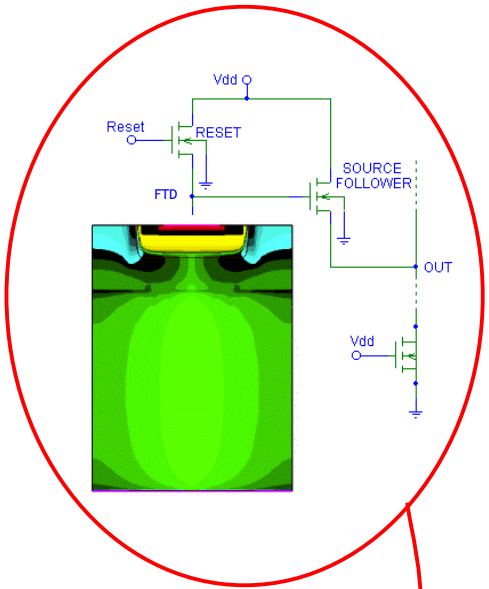
$\Delta V_{A\ 0.18}$ swing greater than $\Delta V_{A\ 0.25}$!

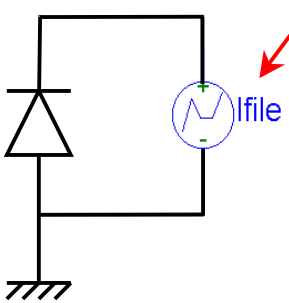
The 0.18 μm technology has been selected !

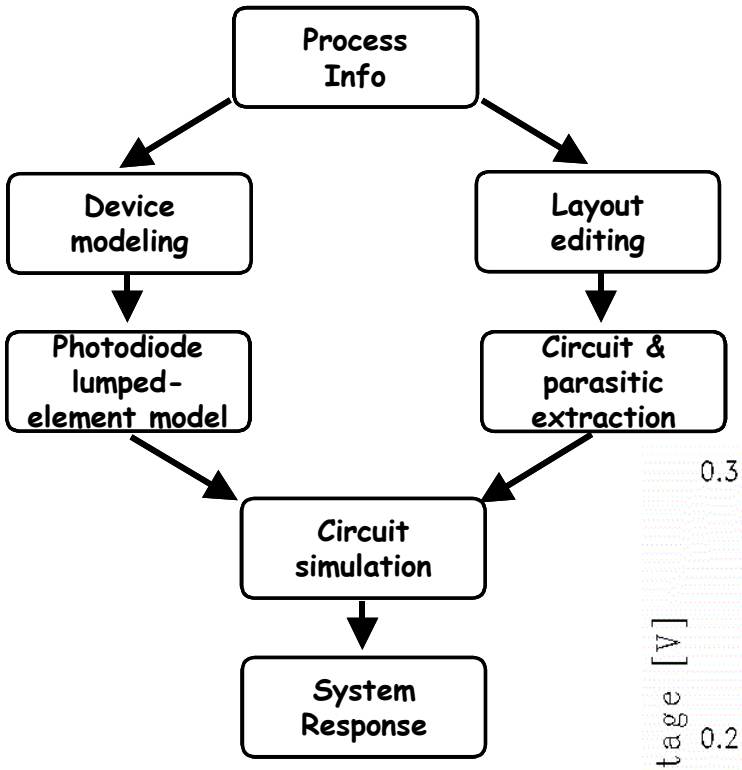


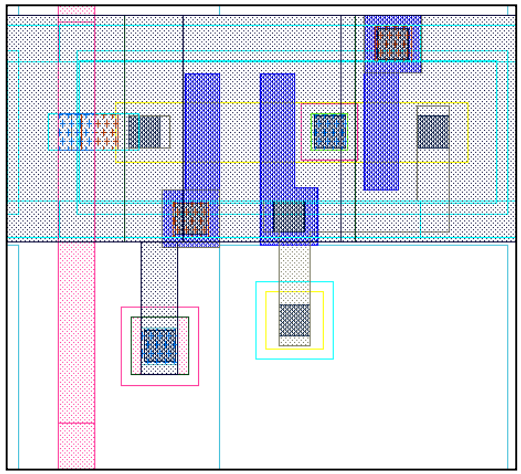
Design flow

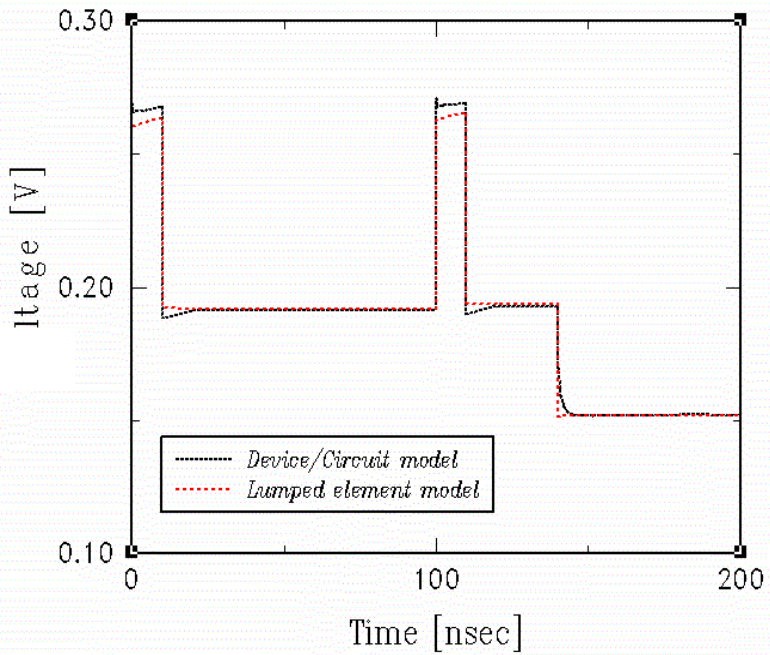
CADENCE IC Design System







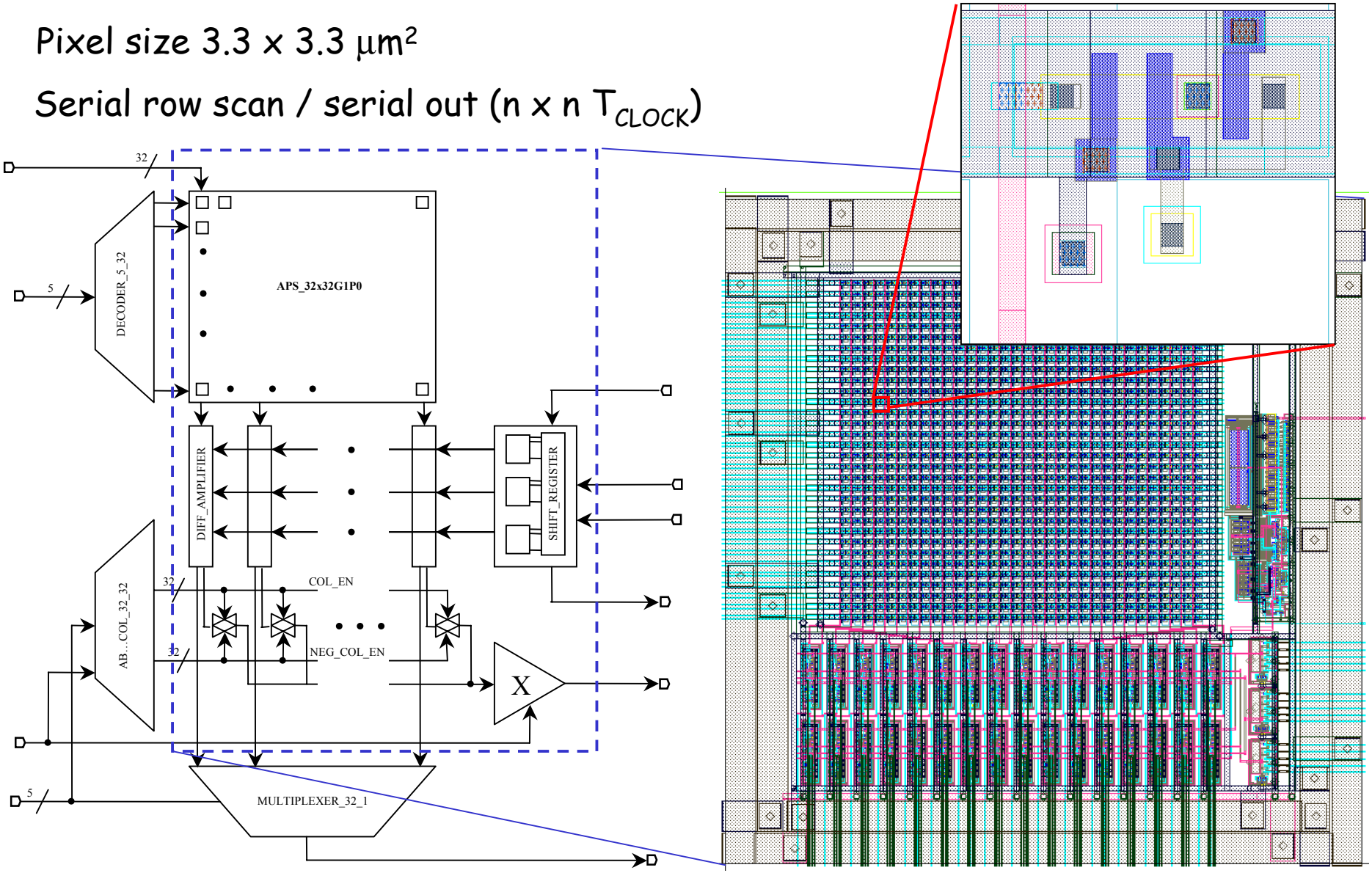




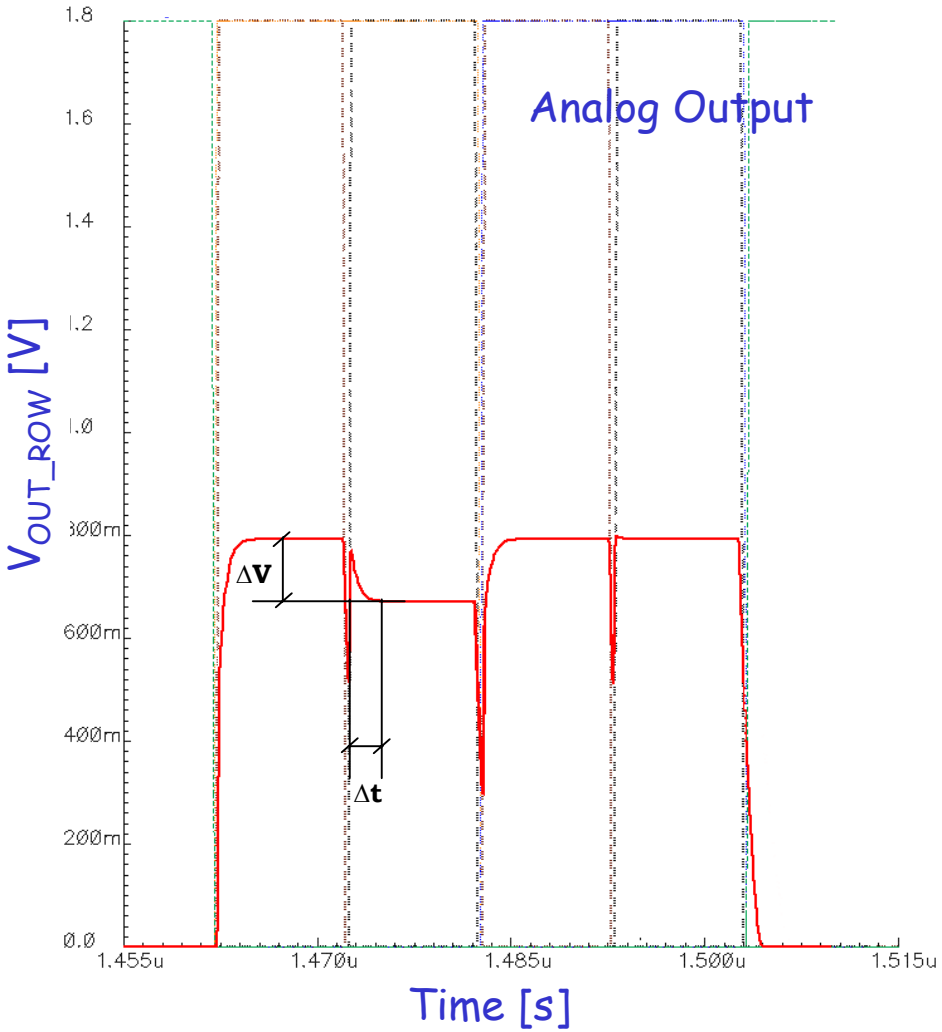
APS matrix architecture

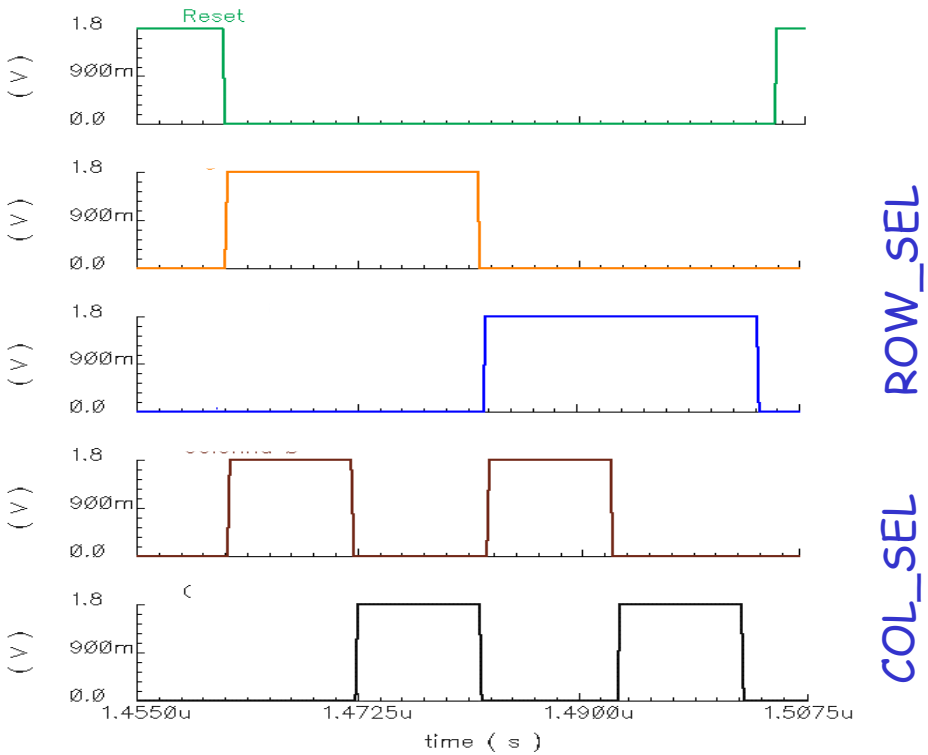
Pixel size 3.3 x 3.3 μm²

Serial row scan / serial out (n x n T_{CLOCK})



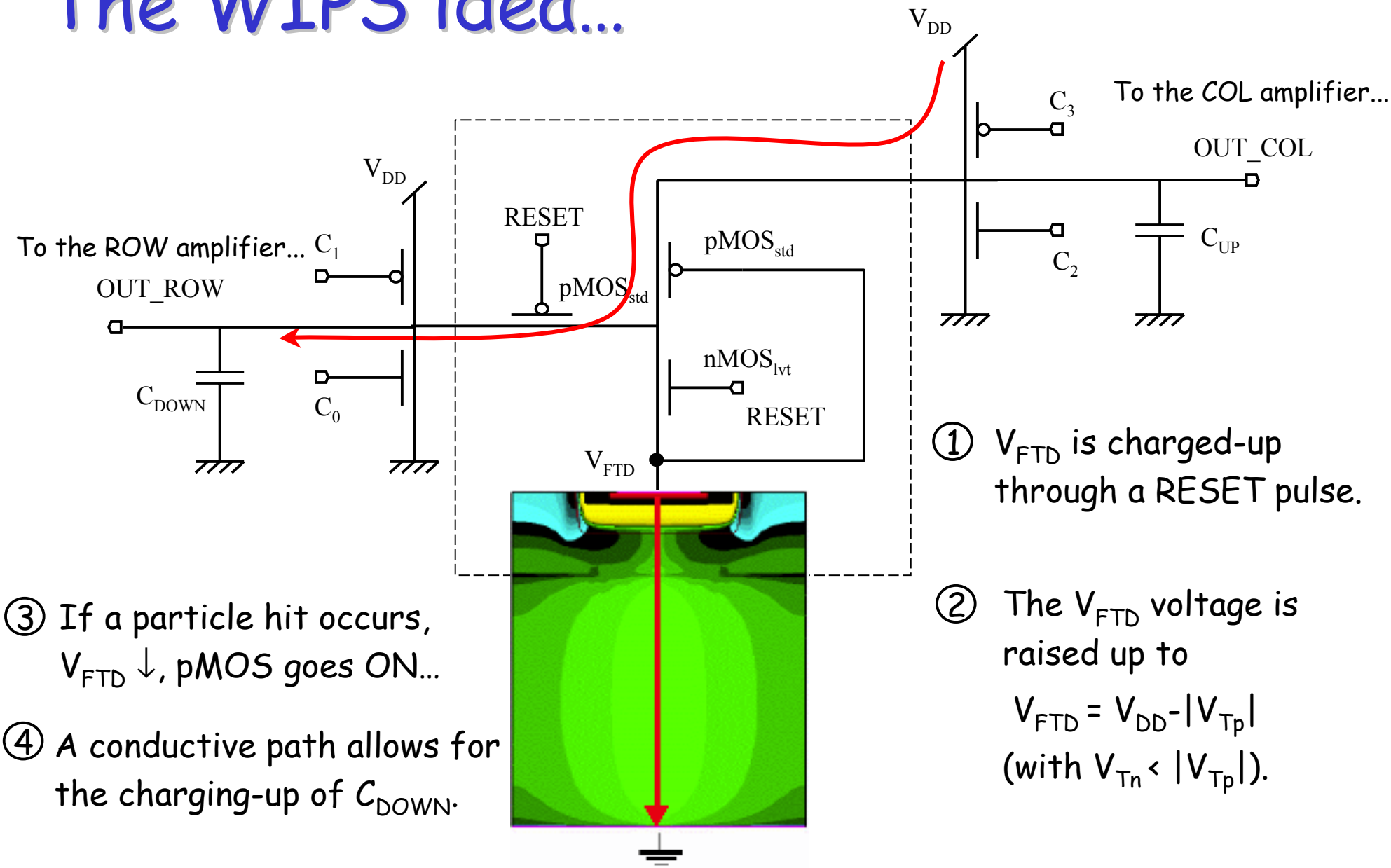
APS simulation results





Parasitic Extraction	V_{dark} [mV]	V_{light} [mV]	ΔV [mV]	Δt_{max} [ns]
WORST	993	883	110	7
TYPICAL	906	795	111	5
BEST	720	600	120	4

The WIPS idea…



① V_{FTD} is charged-up through a RESET pulse.

② The V_{FTD} voltage is raised up to

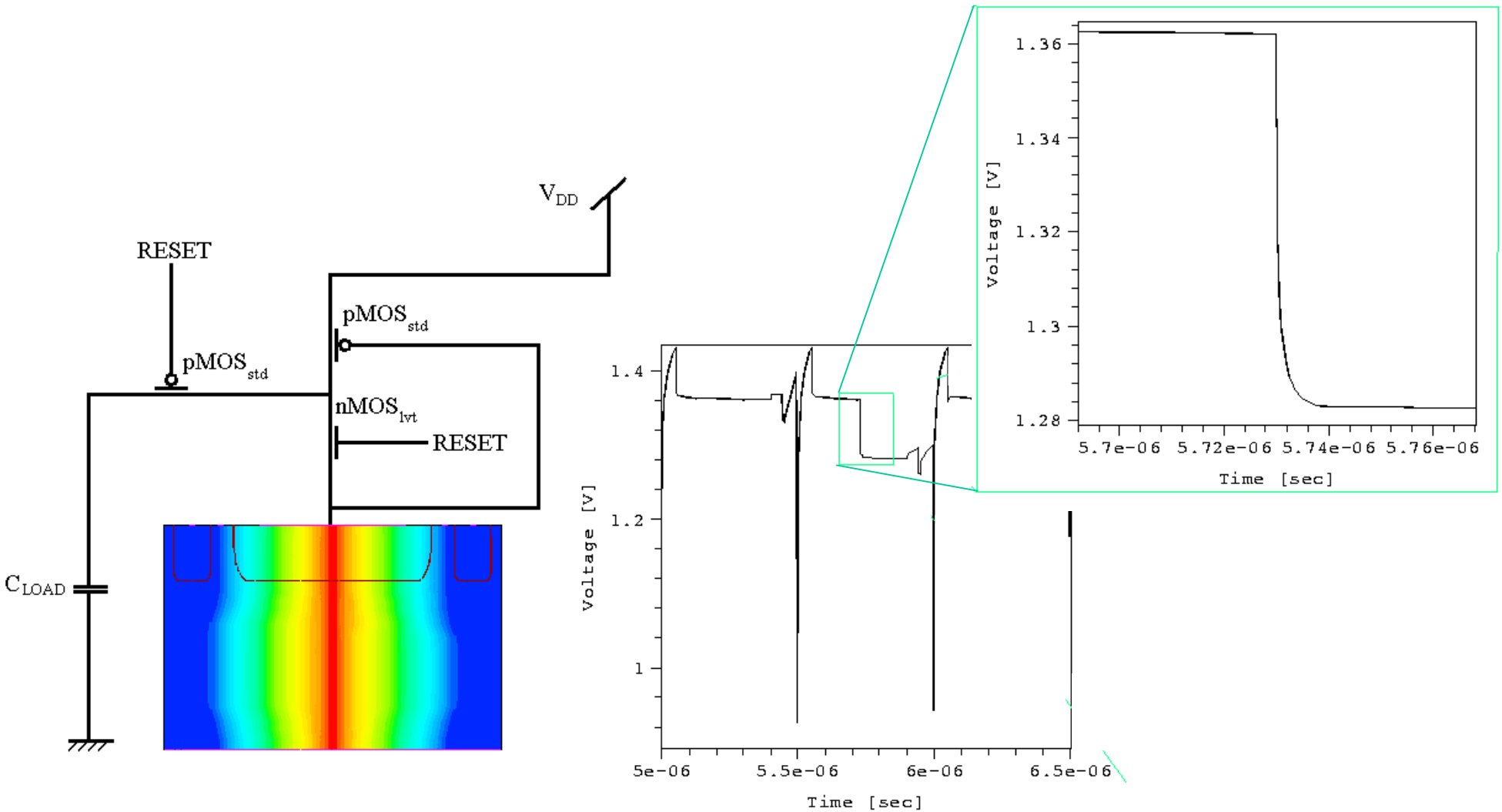
$V_{FTD} = V_{DD} - |V_{Tp}|$

(with $V_{Tn} < |V_{Tp}|$).

③ If a particle hit occurs, V_{FTD} ↓, pMOS goes ON…

④ A conductive path allows for the charging-up of C_{DOWN}.

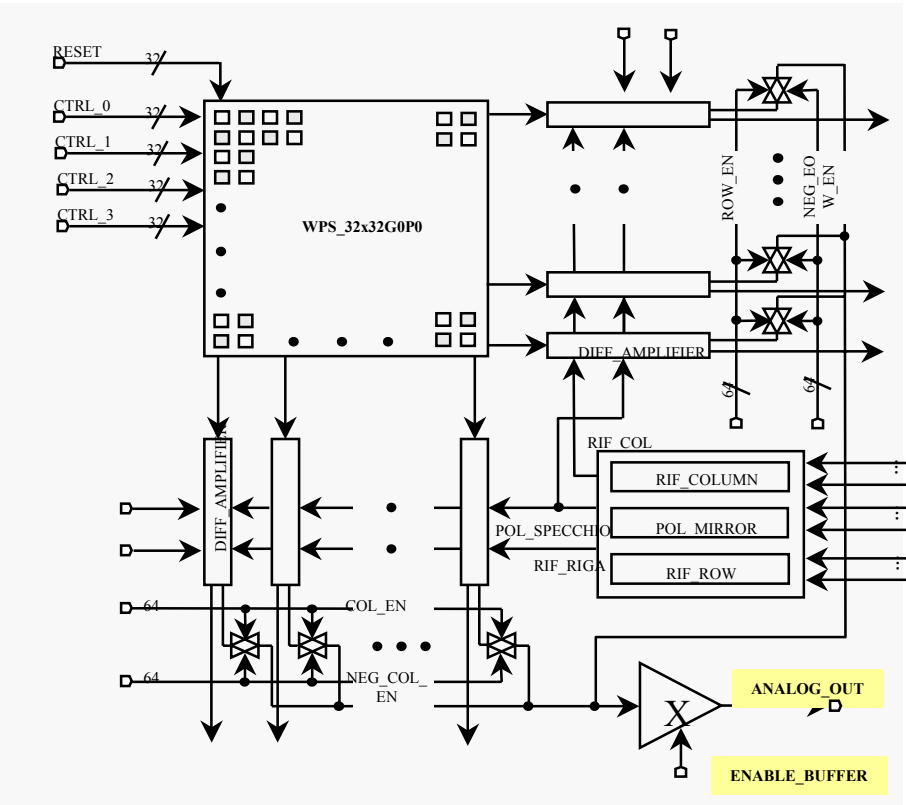
WIPS Mixed-Mode Analysis

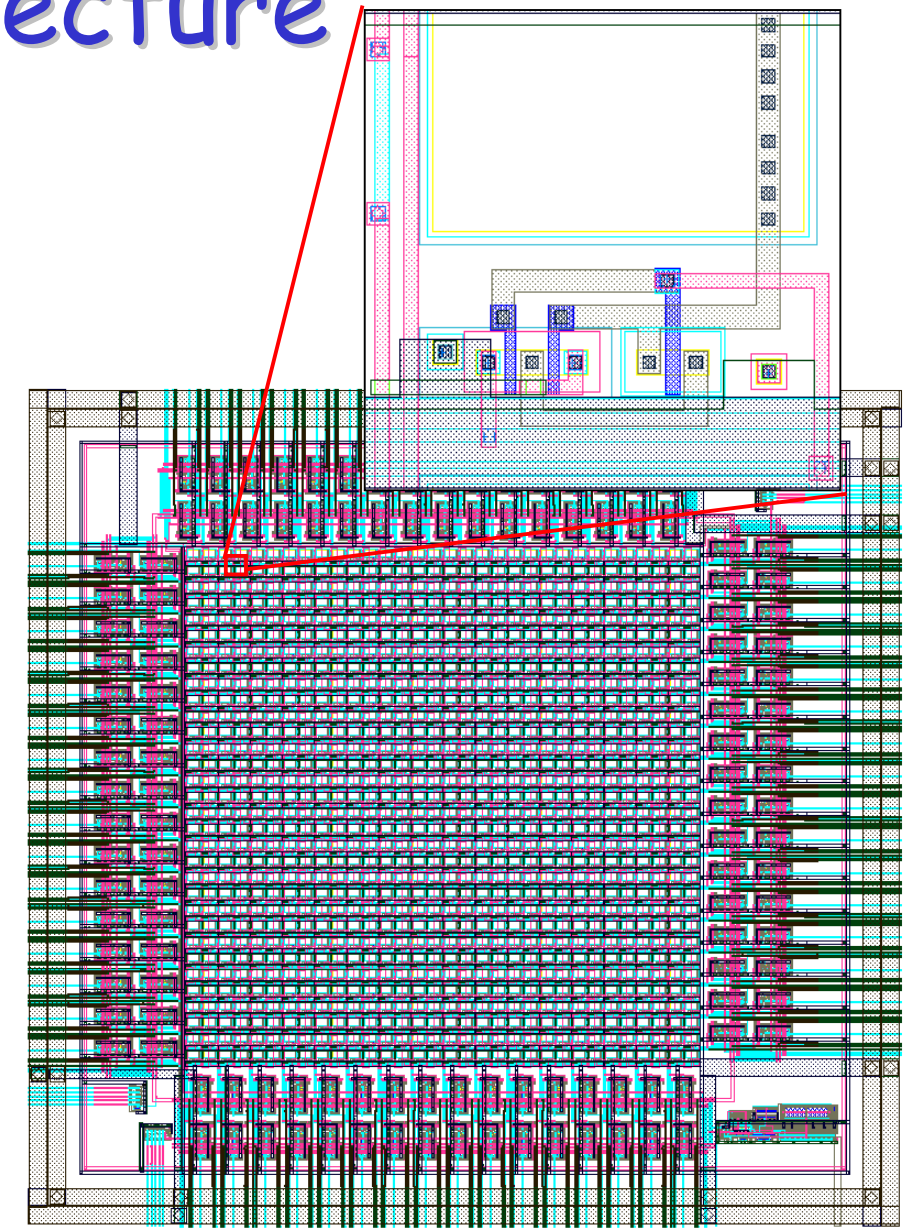


WIPS matrix architecture

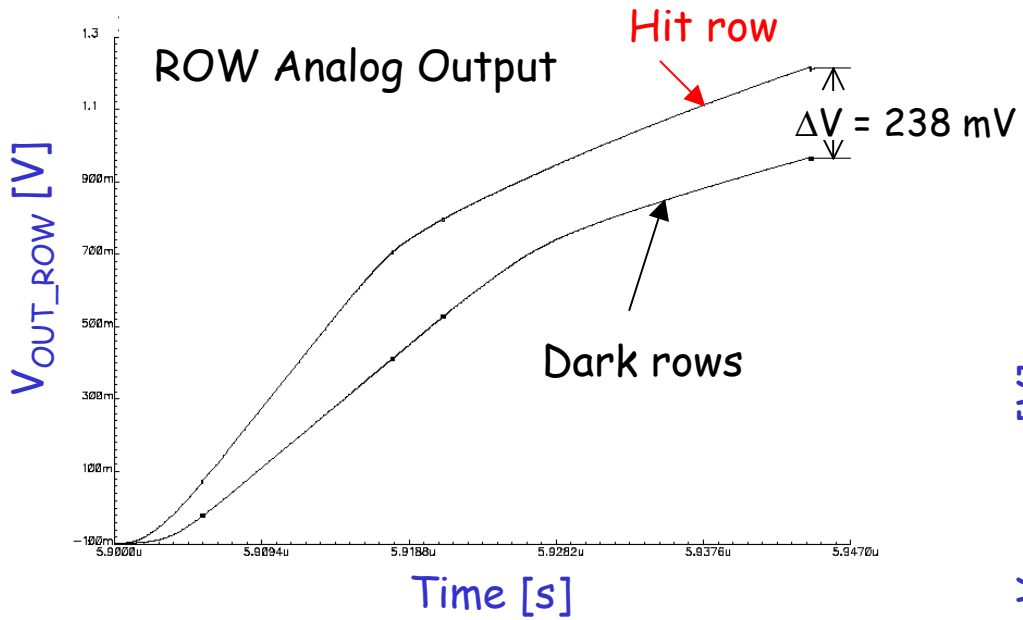
Pixel size 10 x 10 μm^2

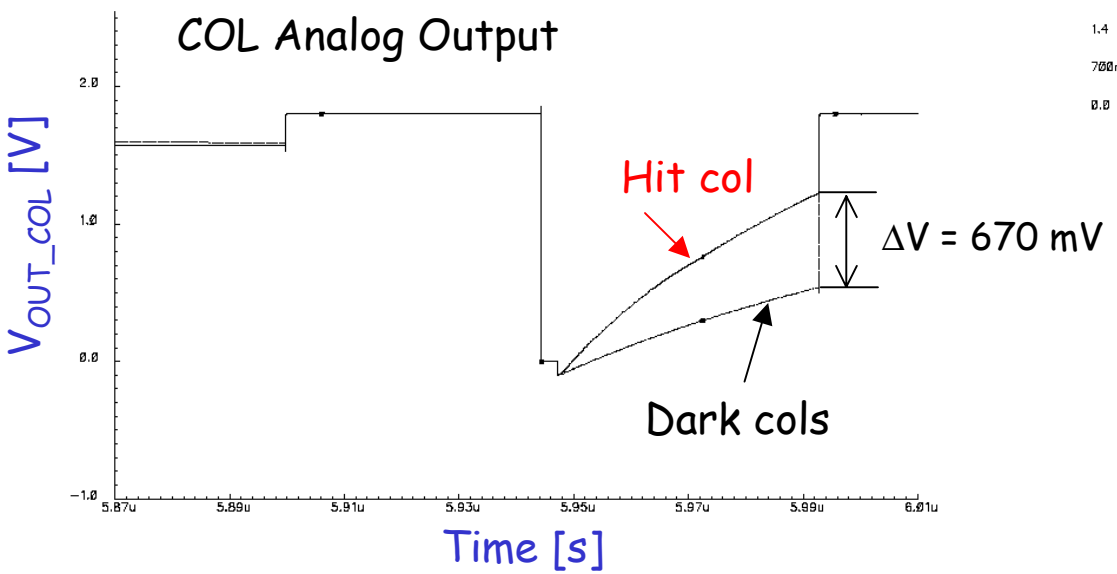
Single row scan / serial out ($n + n\ T_{CLOCK}$)

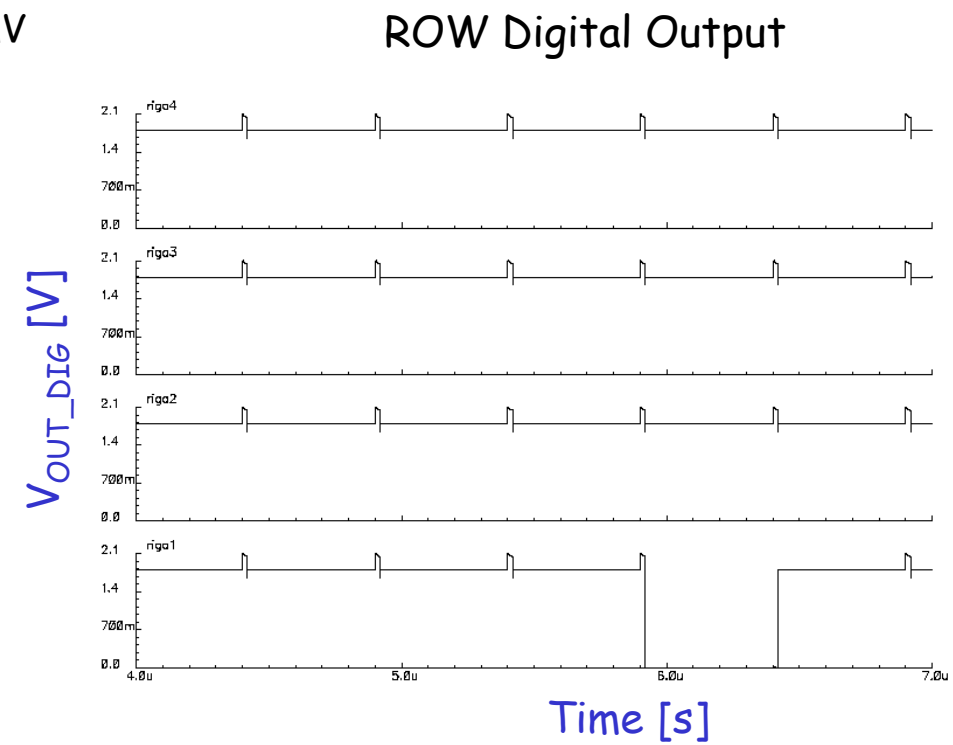




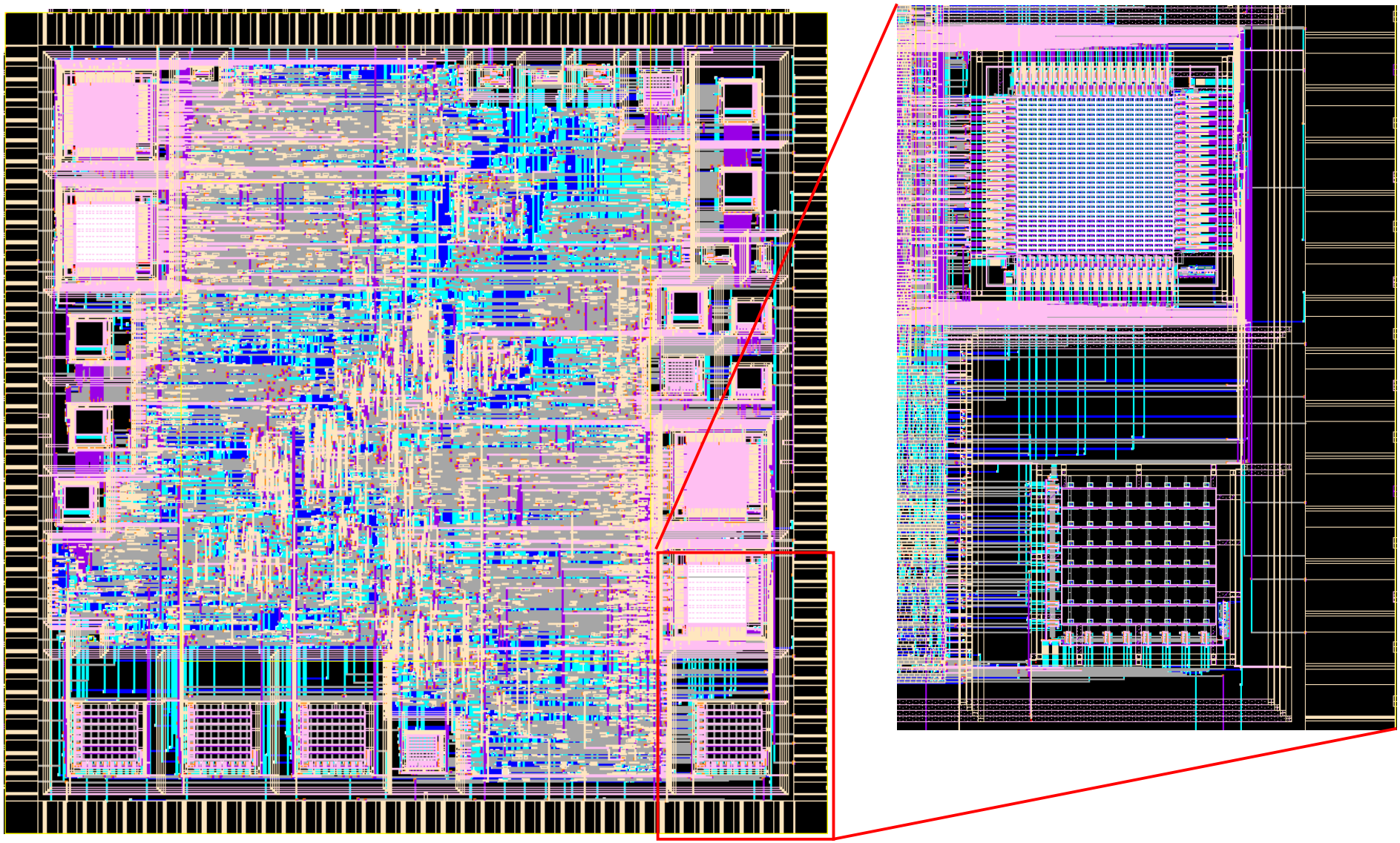
WIPS simulation results







RAPS01 chip layout



Conclusions

Standard VLSI CMOS technologies have been evaluated for the implementation of charged-particle detectors.

Deep submicron technologies appear suitable for such a purpose, allowing for increased spatial resolution and for the integration of smart read-out electronics.

Different pixel architectures have been proposed, especially tailored for the detection of single hits, thus allowing for a simplification and a potential speed-up of the read-out system.

The design of a set of prototypes has been completed, and their fabrication in 0.18 μm technology is under way.

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