Eutectic Sn/Pb Fine-Pitch Solder Bumping and Assembly for Rad-Hard Pixel Detectors

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MCNC

Advanced Packaging and Interconnect

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Outline

- MCNC Overview
- Solder Bumping Overview
- Fermilab Pixel Detector Bumping (BTeV)
- NWU Pixel Detector Bumping (US-CMS)

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MCNC - Who We Are

- A non-profit technology development and service company.
- Customer base includes
  - Government agencies
  - Academic institutions
  - Commercial companies
- For-profit spinoff companies
  - Unitive Electronics – high volume commercial bumping
  - Cronos Integrated Microsystems – commercial MEMS provider, acquired by JDSU, now part of MEMSCAP
- Technology Groups
  - Materials and Electronic Technology Division (METD)
  - Signal Electronics Division
  - Network Research Division
  - High Performance Computing and Communications

NEWS FLASH!

- In October, the technology development groups will spinoff and retain the MCNC name.
- No services, staff, or assets will change.

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METD Research Focus Areas

- 3D and Heterogeneous Integration
- Advanced Packaging and Interconnect
- Organic Electronics and Optoelectronics
- Novel Sensors and Actuators
- Prototype Development and Foundry Services

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MCNC Flip-Chip Bumping Services

- **Full-service prototype and low volume bumping and flip-chip assembly supplier.**
- **Bump fabrication facilities for 3”- 8” wafer sizes.**
- **Current production bump size: 25-micron bumps on 50-micron pitch (40,000 I/O per cm^2); smaller available on developmental basis.**
- **Thermal and mechanical reliability services**
- **Analytical services through MCNC Analytical Labs**
  - **Cross sectioning**
  - **SEM, XRF, EDS**
  - **X-ray photomicroscopy for bump integrity verification on assemblies**

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Bump Design Rules

- **I/O pad pitch**
  - **Rule of thumb - bump base diameter is 1/2 the smallest I/O pad pitch.**
- **Wafer final passivation opening size**
  - **Affects size of via openings in repassivation layer.**
- **Final passivation material on wafer**
  - **Inorganics (i.e. SiN, SiO2) are preferred, organics (i.e. polyimides) can be used depending on material and processing conditions.**
- **Desired bump height**
  - **Maximum bump height is limited by bump base diameter (a function of I/O pad pitch).**

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Bumping Process Overview – ROC wafer

- **Five Main Process Steps**
  - **Repassivation – Dow Chemical Cyclotene™**
    - **Low dielectric constant – 2.6**
    - **Photopatterned vias connect bumps with I/O pads**
  - **UBM Deposition**
    - **Cu-based blanket metallurgy engineered for long-term reliability and mechanical bump strength**
  - **Eutectic Sn/Pb Solder Electroplating**
    - **Plated into openings defined in a thick photoresist**
  - **UBM Etching**
    - **Removal of field UBM from wafer, UBM under bumps remains intact**
  - **Wirebond Pad Opening**
    - **Dry etching of BCB reopens access to wirebond pads**

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Bumping Process Overview – Sensor Wafer

- **Four Main Process Steps**
  - **Repassivation**
  - **UBM Deposition**
  - **Ni/Au Solder Bondpad Electroplating**
    - **Au provides a solderable surface, Ni forms intermetallic with Sn to provide mechanically strong bond**
  - **UBM Etching**

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Flip-Chip Assembly of Pixel Detectors

- Multiple chip placements on a single substrate are required
- Two flip-chip aligner/bonders from Research Devices
  - Placement accuracy of 3 microns or better
  - Reflowed device alignment ~ 1 micron
- Nitrogen-inerted reflow system provides accurate control of reflow operation
- Accuracy of dicing operation is critical to ensure that chips can be placed next to each other.
  - In-house dicing facilities allow tight control over dicing procedure
- Fluxless assembly is used due to the difficulty of removing flux residues

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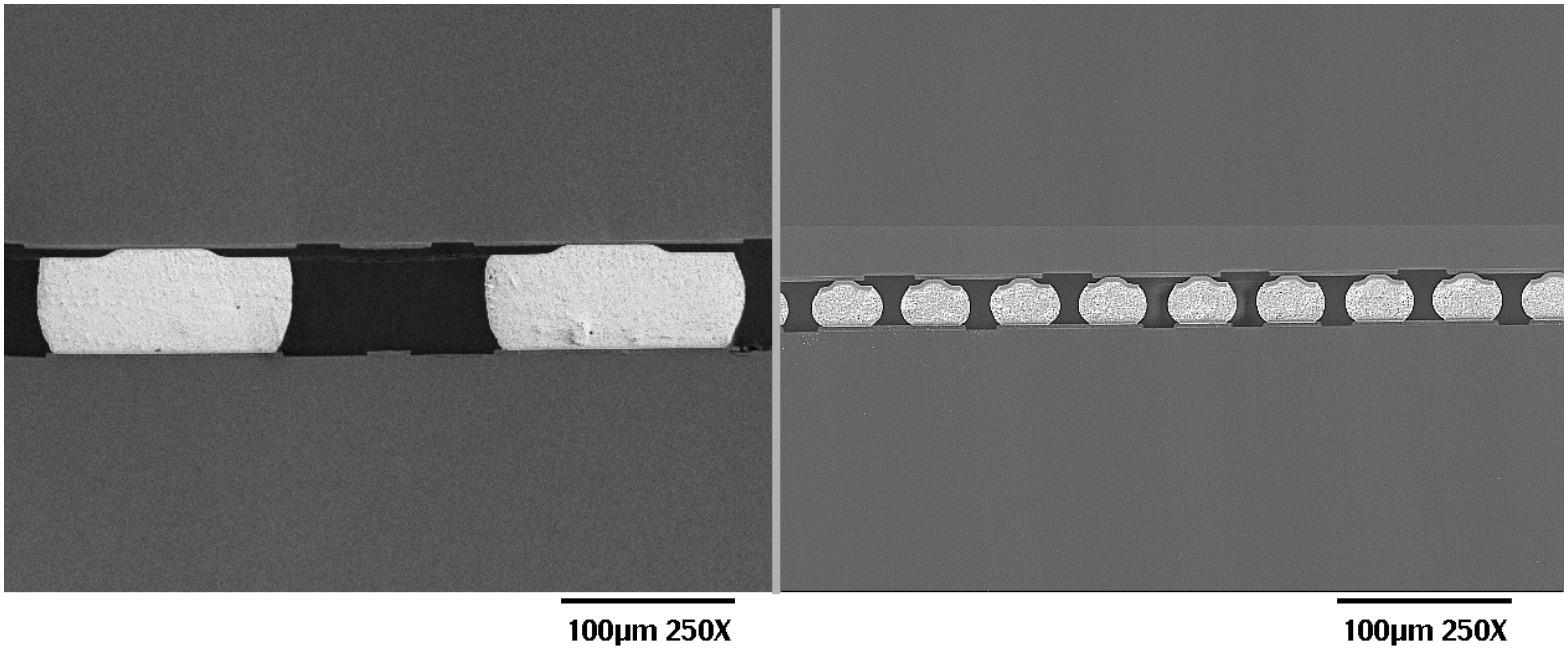
Standard Vs. Fine Pitch Assembly



- SEM cross sections of commercially available 250-micron pitch and 50-micron pitch assemblies
- Chip-to-substrate gap reduces from 65 microns to 22 microns for the 50-micron pitch design

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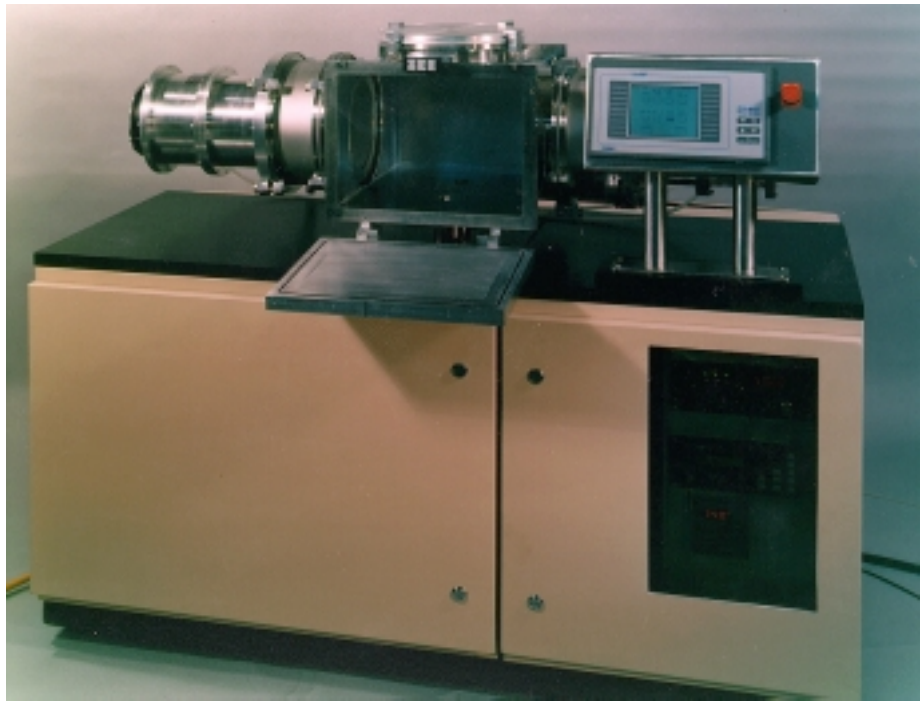
PADS (Plasma Assisted Dry Soldering)



- **Patented plasma process breaks up Sn oxide surface during reflow, allowing wetting without flux.**
- **PADS leaves no residues on chip or substrate**
- **R&D Magazine Technology 100 Award, 1996**

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BTeV Pixel Detector Bumping

- Two test phases completed using internally generated 50-micron pitch daisy chain test design.
- Two device build phases completed using 4-inch SINTEF and Atlas prototype sensor wafers and 6- and 8-inch FPIX readout chip (ROC) wafers.
- Bump dimensions
  - Base diameter - 25 micron
  - Typical bump height - 30 micron
- ROC wafers will require thinning after bumping to 200 microns by external vendor before assembly.

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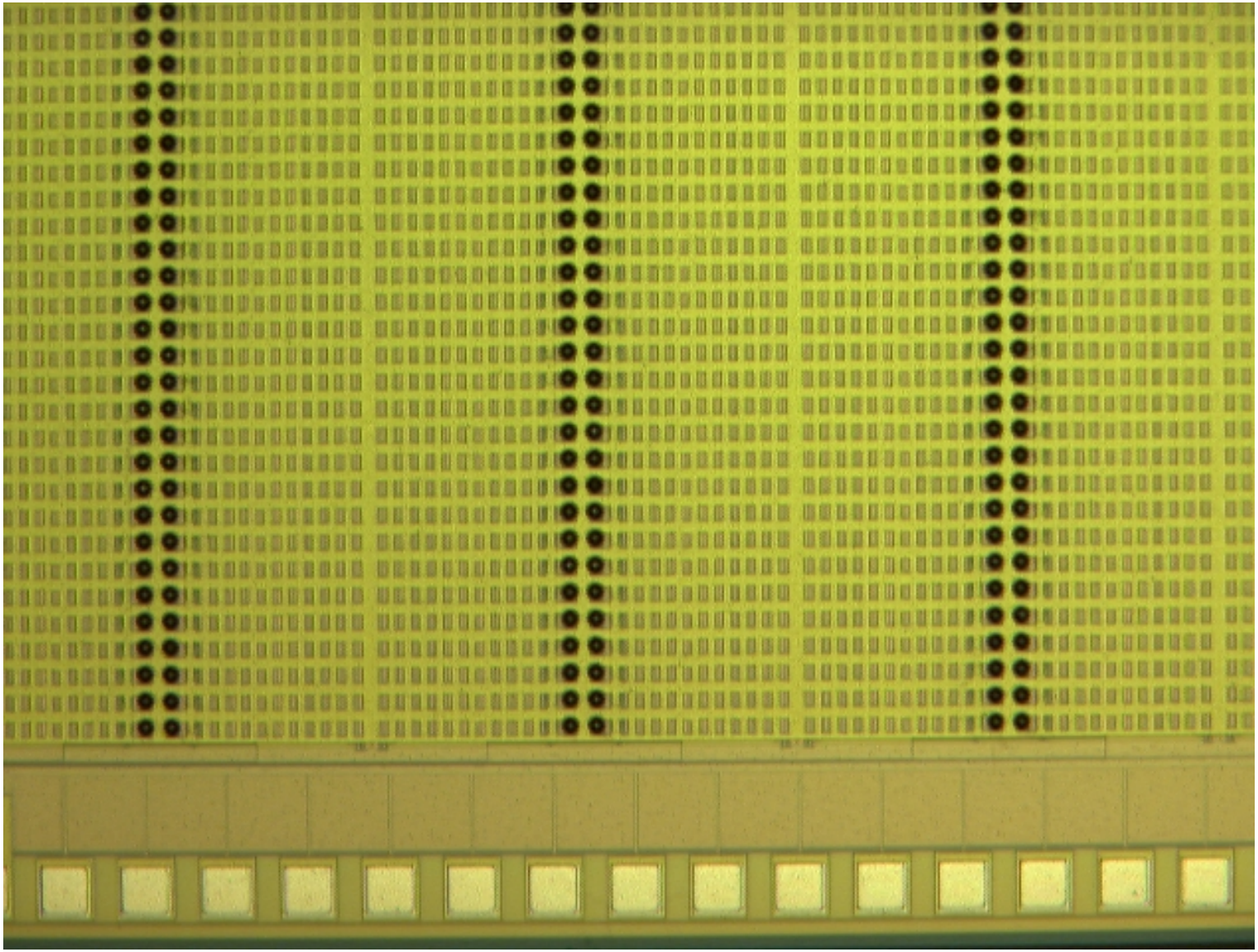
Bumped FPIX ROC



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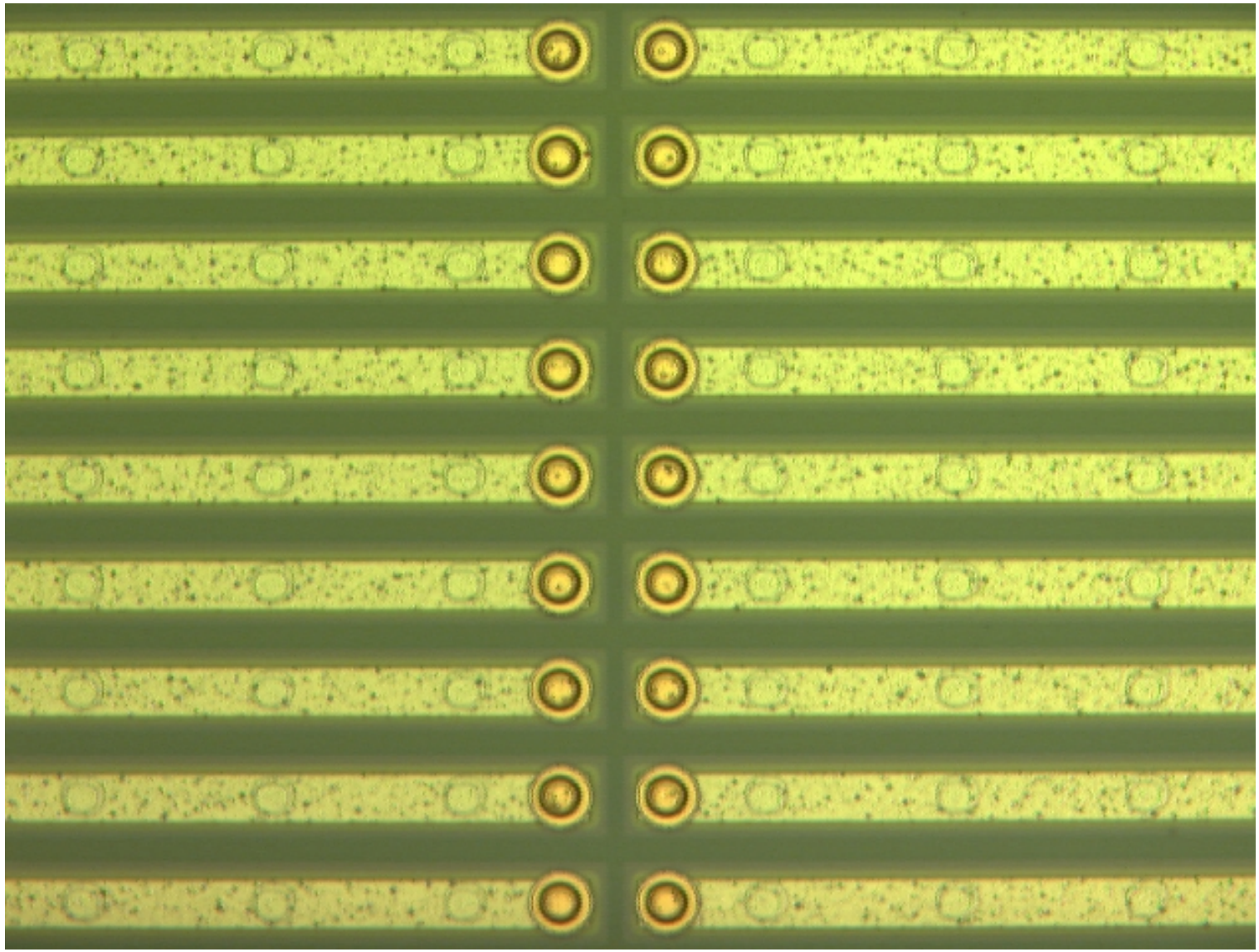
Atlas Prototype Sensor With Solder Bond Pads



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BTeV - Bump Yield Results*

- **Yield numbers from tests performed on daisy chain test design**
  - **Assembly yield of 91.5%**
  - **Channel yield of 99.32% or 6.8×10^{-3} failed-channel/channel**
  - **Bump yield of 99.95% or 4.5×10^{-4} failure/bump**
    - **Assumes one failed bump per channel**
    - **Internal studies of separated assemblies show this is largely valid**

*** S. Cihangir and S. Kwan; talk presented at 3rd International Conference on Radiation Effects on Semiconductor Materials, Detectors and Devices, Florence, Italy (June. 28-30, 2000).**

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BTeV - Thermal Cycling Results*

- Test conditions, performed on daisy chain test design
  - -10°C for 144 hours
  - 100°C in vacuum for 48 hours
- Measurement after cooling
  - 4.6×10^{-5} failures / bump on Known Good Modules
- Measurement after heating
  - 3.3×10^{-4} failures / bump on Known Good Modules
- Measurements may be affected by trace and/or probe pad damage due to repeated probing

* Cihangir, et. al.; talk presented at 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden (Sept. 10-14, 2001).

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BTeV - Radiation Exposure Results *

- **Test conditions, performed on daisy chain test design**
  - **13 MRad dose from Cs-137 source**
- **Failure rate: 1.8×10^{-4} failure / bump**
  - **Failure rate may be affected by radiation damage on Al lines or probe pads**
  - **Test design chips are NOT rad-hard**

*** Cihangir, et. al.; talk presented at 7th Workshop on Electronics for LHC Experiments, Stockholm, Sweden (Sept. 10-14, 2001).**

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BTeV - Future Plans

- **Prototype phase expected to continue with new sensor and ROC designs.**

- **Preproduction phase assembly requirements**
  - **10% build of full production module quantities, approximately 140 modules with >800 total chip placements on 4-, 5-, 6-, and 8-chip modules**

- **Production phase assembly requirements**
  - **Approximately 1800 modules**
  - **>10,500 total chip placements**

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US-CMS Pixel Detector Bumping

- Two concept test phases completed using internally generated 100-micron pitch daisy chain test design.
- Bump dimensions
  - Base diameter – 50 microns
  - Typical bump height – 45 microns
- Future phases are moving to 25-micron bumps.
- Assembly of MCMs up to 5x2 arrays.
- Device ROC wafers will require thinning before assembly to sensors

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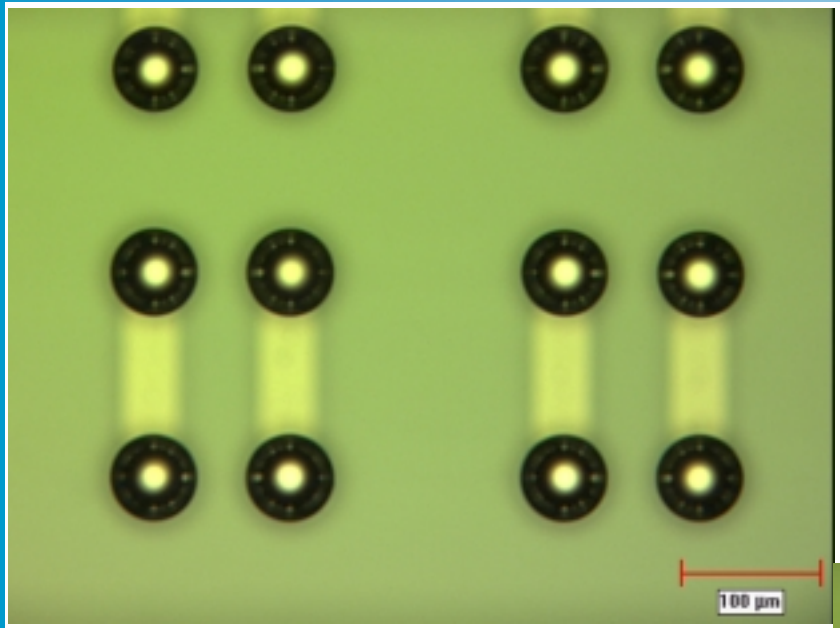
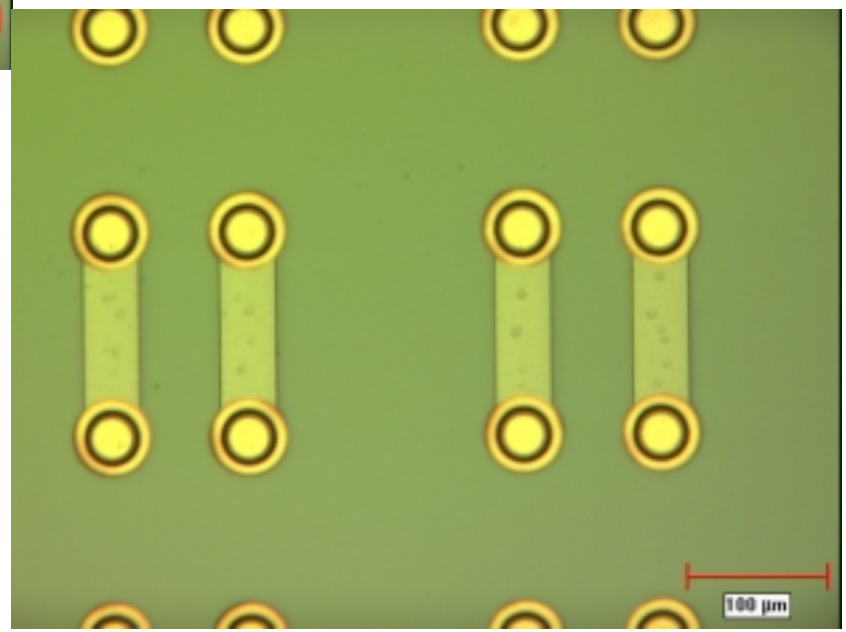
US-CMS - Daisy Chain Test Design



Test Design - Sn/Pb solder bumps, 100um min. pitch

Test Substrate - Ni/Au bond pads



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US-CMS - Bump Yield Results*

- **Bump yield of .9997 ± .0001, measured at UCD by D. Lander**
- **Assumes only one failed bump bond on a failed trace**
- **Reasonable based on internal studies of failed traces**

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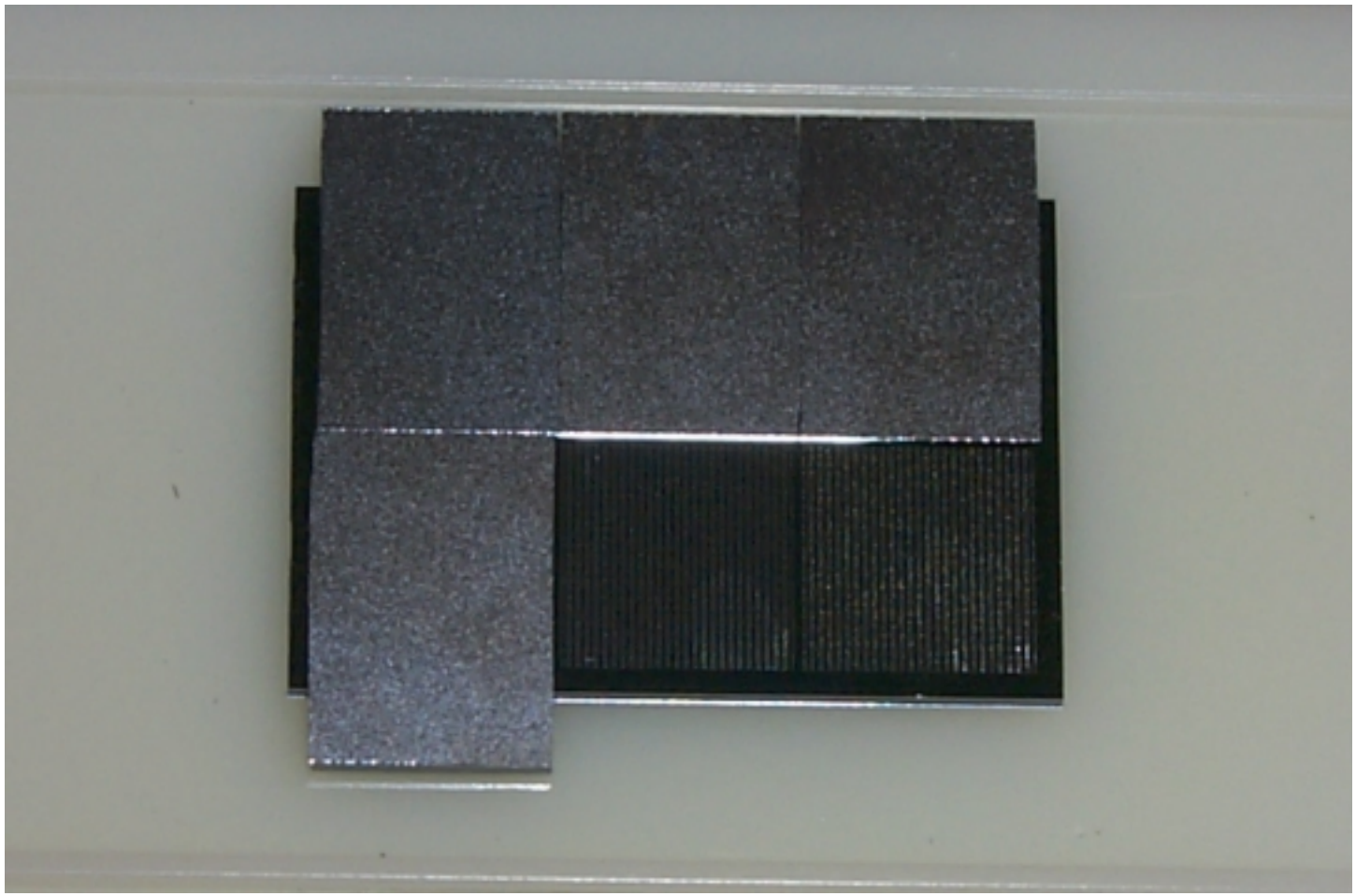
US-CMS - Module Assembly



NWU 3x2 MCM, partial build to show detail

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Summary

- **MCNC has demonstrated robust flip-chip bumping and assembly processes that meet the pitch and bump size requirements of pixel applications.**
- **Bump yields have been demonstrated to be acceptable for pixel detector applications by Fermilab (BTeV) and NWU (US-CMS).**
- **Thermal cycling tests indicate that the solder bump-bonded detector modules are robust and will survive construction and subsequent heat-up / cool-down cycles.**
- **Radiation exposure testing indicates a minimal effect on failure rates.**
- **Future work will concentrate on increasing the number of wafers processed and modules assembled to identify issues involved in moving from prototype phases to production.**

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