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Monolithic CMOS Pixel Detectors in Particle an Nuclear Physics

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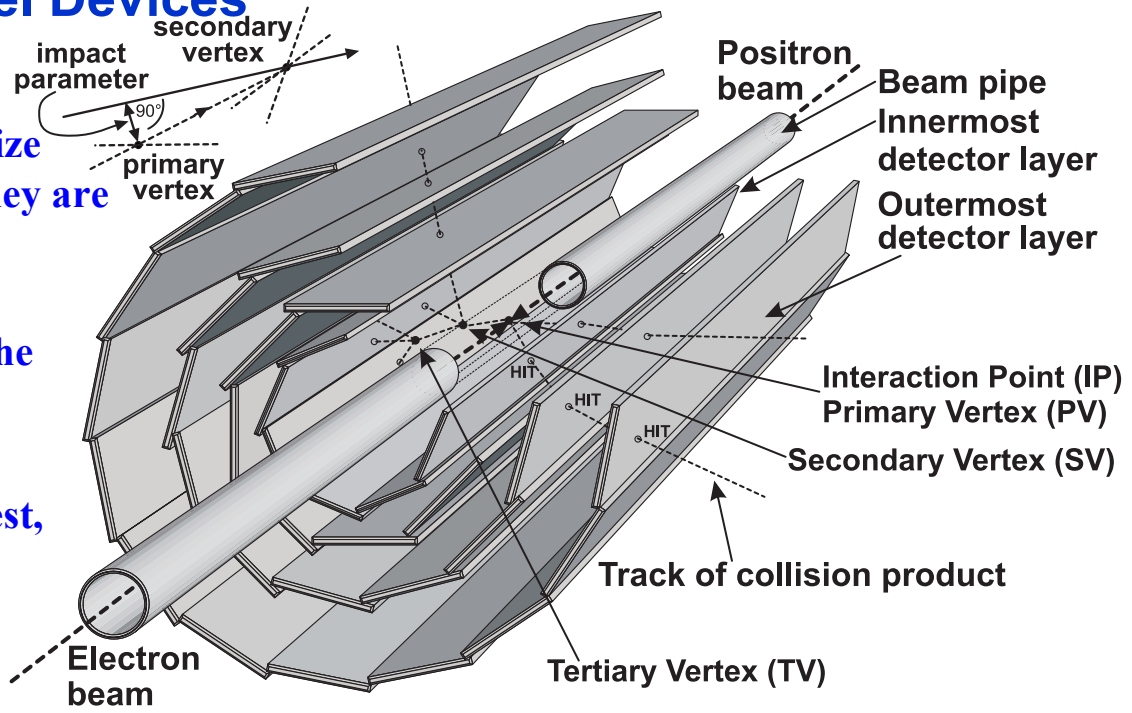
☑ Motivation for Monolithic Pixel Devices

Vertex Detectors (VXD)

- Quarks from primary interaction hadronize within typical distances of a few fermi (they are not seen),
- Hadronization of quarks yields in jets of particles, which retain the direction and the energy of the parent,
- Final states with large number of jets; b, c, τ present in most final states of interest,
- Future Vertex Detectors should :
  - allow assigning each track to its vertex origin ,
  - allow reconstructing Q, M, E and 2^{ry} - 3^{ry} vertices
  - allow reconstructing the flavour of each vertex in a high particle density multi-jets environment,



Untill today the flagship are Charge Cupled Devices...
but VXDs should also ...

- provide constant performances under relatively harsh radiation environment,
- allow fast readout - to cope with background.

$$\sigma_{IP} = \frac{r_1\sigma_1 + r_2\sigma_2}{(r_2 - r_1)^2}$$

Impact parameter precision and Multiple Coulomb Scattering

$$\Theta_0 = \frac{13.6\ \text{MeV}}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right]$$

The solution being sought is very granular, ultra light, radiation hard, poly-layer VXD installed close to the IP.

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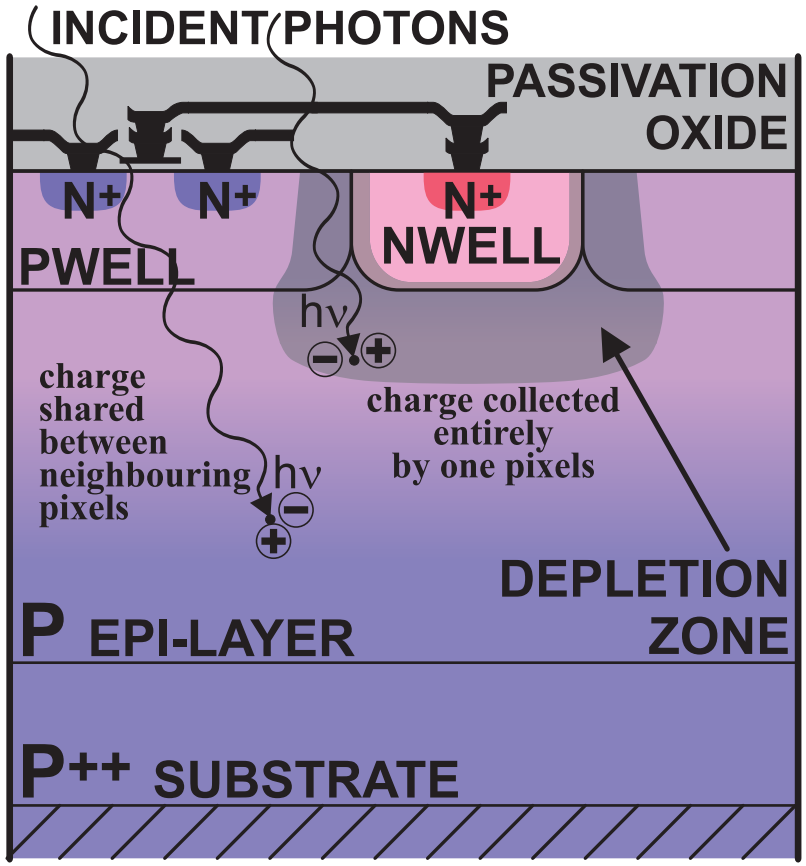
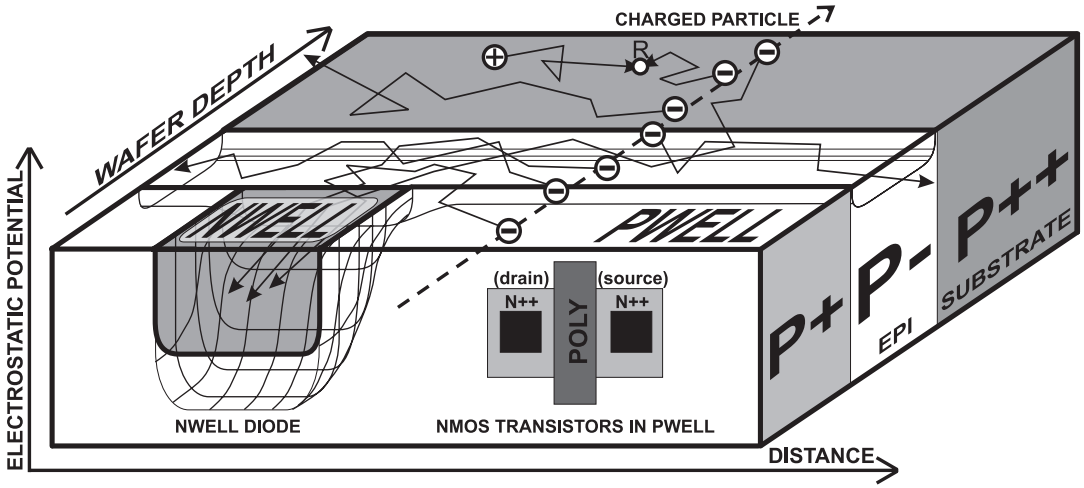
☑ Operation Principle of CMOS Sensors for Particle Detection

- In visible light CMOS cameras, moderately doped epitaxial layer provides long minority carrier lifetime ...



- Charge generated in non-depleted region collected through thermal diffusion (or it recombines…) ...



- Potential barriers at layer interfaces confine the charge - improving collection efficiency ...

- Active volume underneath the readout electronics ⇨ **100% fill factor**; charge collected by deep n-well/p-epi diode.

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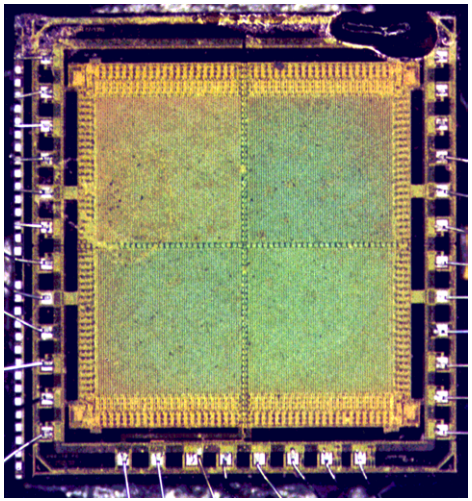
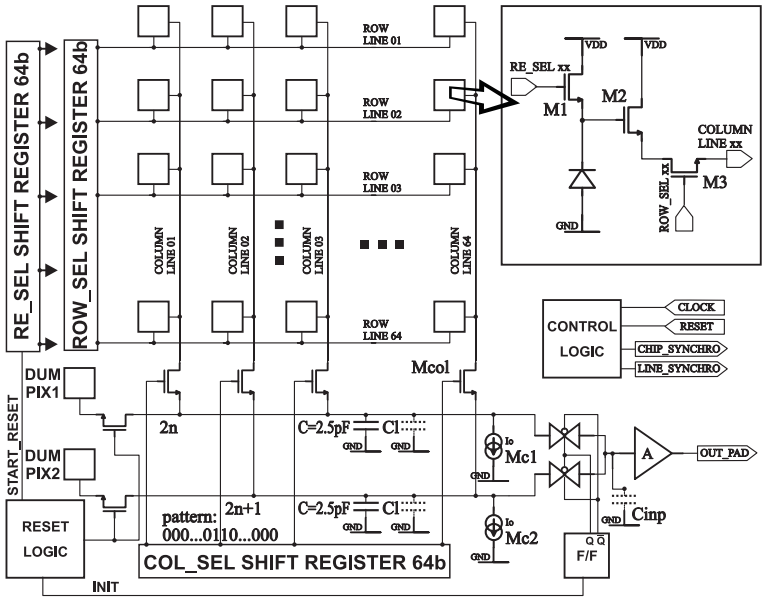
☑ First Prototypes - Summary of Performances

MIMOSA I
die size 3.6 × 4.2 mm²

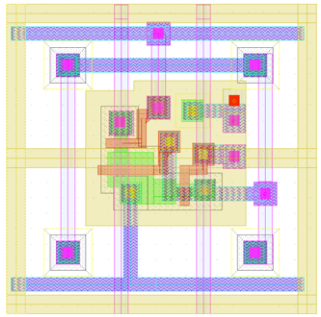


Device internal architecture e.g. MIMOSA II

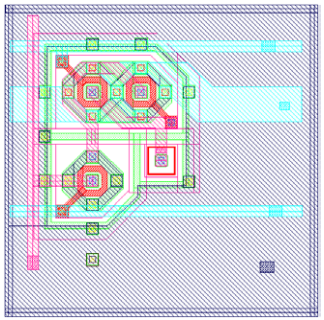


Examples of pixel layouts

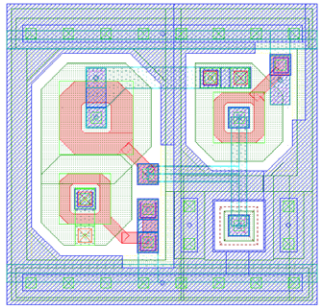
M I: 20× 20 µm²



M II: 20× 20 µm²



M III: 8× 8 µm²



Prototype, Process	Epitaxial layer, Pixel pitch	Chip configuration	Sensitive diode element	Peculiar features
MI /'99, 0.6 µm	~14 µm, 20 µm	4×64×64 pixels square layout	n-well/p-epi 3.1×3.1 µm²	thick epitaxial layer, 1 and 4 diodes / pixel serial analogue readout f_{clk}<5MHz
MII /'00, 0.35 µm	~4 µm, 20 µm	6×64×64 pixels square and staggered layouts	n-well/p-epi 1.7×1.7 µm²	1 and 2 diode / pixel structures for irradiation tests serial analogue readout f_{clk}<25MHz
MIII /'01, 0.25 µm	~2 µm, 8 µm	2×128×128 pixels staggered layout	n-well/p-epi 1.0×1.0 µm²	thin epitaxial layer, 1 diode / pixel varied size of SF transistor structures for irradiation tests serial analogue readout f_{clk}<40MHz
MIV /'01, 0.35 µm	p⁻-type substrate, 20 µm	4×64×64 pixels square layout	n-well/p-sub 2.0×2.0 µm²	no epitaxial layer, 1 and 3 diodes pixels current mode pixel (photoFET) auto-reverse-polarised diodes serial analogue readout f_{clk}<40MHz

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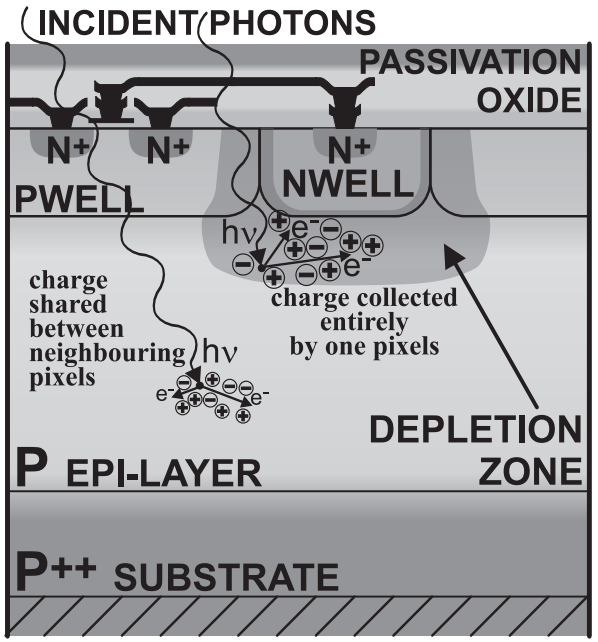
☑ First Prototypes - Summary of Performances

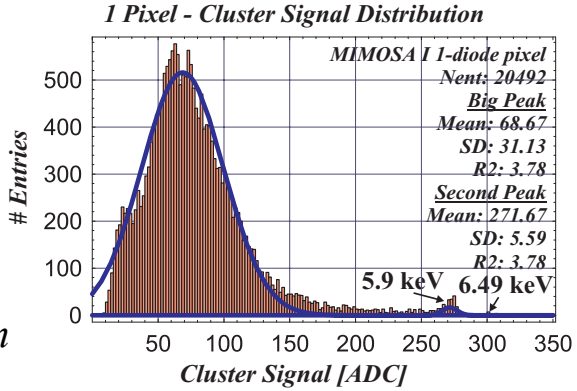
- **Tests with low energy X-rays ...**

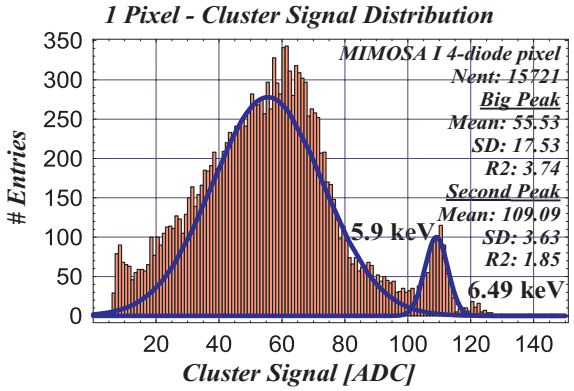
Purpose: Conversion gain calibration

Emission spectra of a low energy X-ray source e.g. iron ^{55}Fe emitting 5.9 keV photons.

very high detection efficiency even for thin detection volumes - μ =140 cm^2/g, constant number of charge carriers about 1640 e/h pairs per one 5.9 keV photon

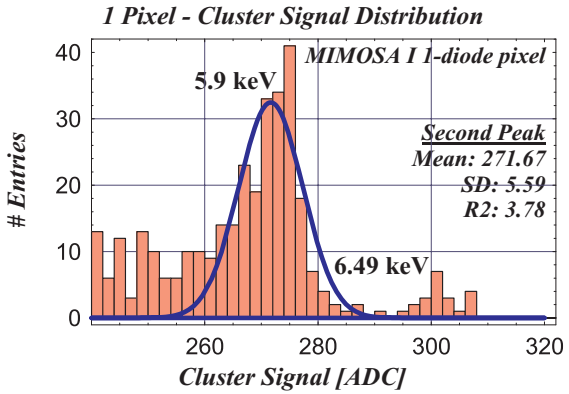


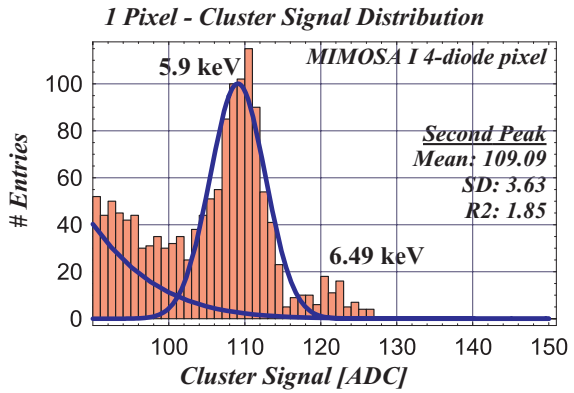




MIMOSA I (14 µm EPI) configuration with single diode in one pixel

MIMOSA I (14 µm EPI) configuration with four diodes in one pixel





MIMOSA I CMOS 0.6 µm	1 diode – 14.6 µV/e$^-$	4 diode – 6.0 µV/e$^-$
	ENC = 14 e$^-$ @1.6 ms f. rate	ENC = 30 e$^-$ @1.6 ms f. rate
MIMOSA II CMOS 0.35 µm	1 diode rad. tol.– 22.9 µV/e$^-$	2 diode rad. tol.– 17.5 µV/e$^-$
	ENC = 12 e$^-$ @0.8 ms f. rate	ENC = 14 e$^-$ @0.8 ms f. rate

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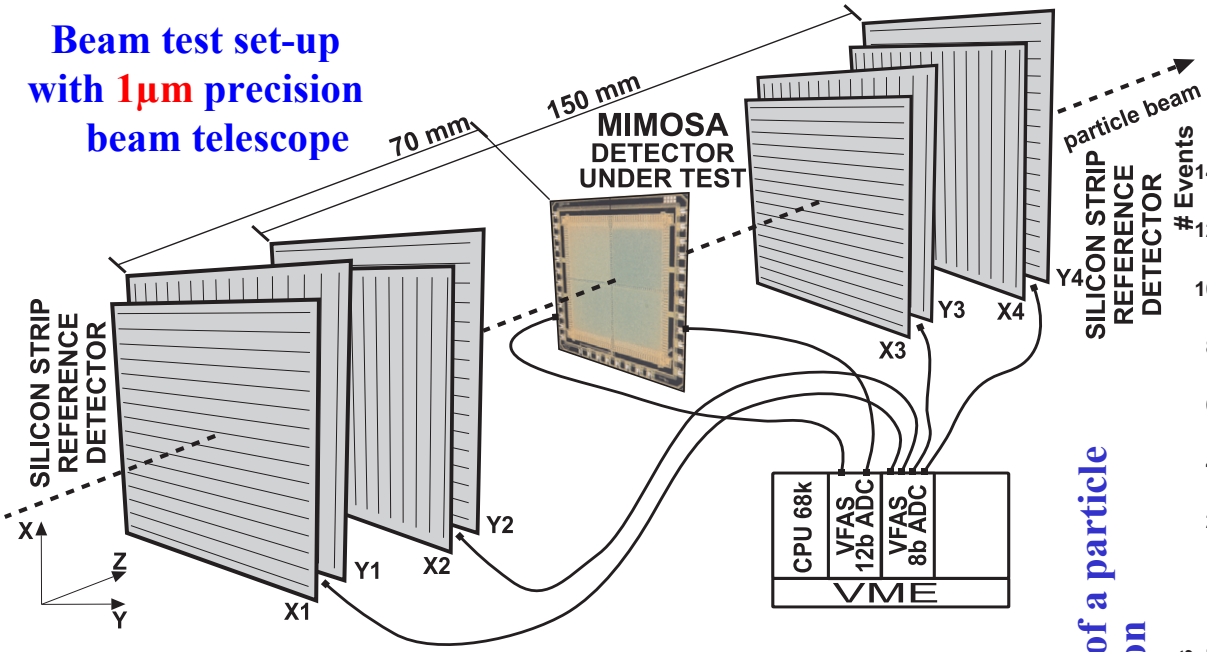
☑ First Prototypes - Summary of Performances

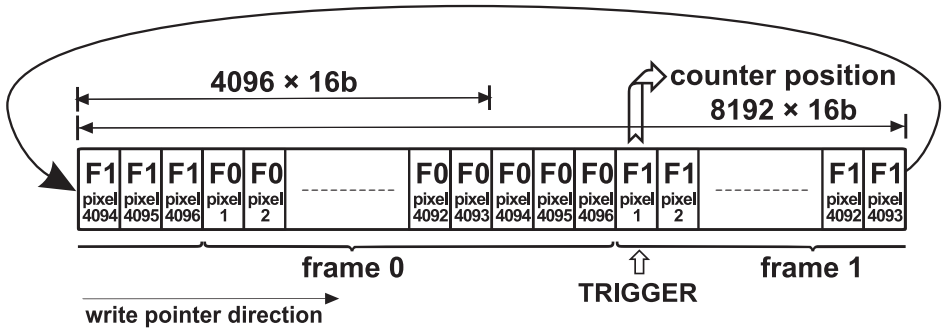
- Tests high energy charged particle beams (CERN SPS: π^- 120 GeV/c)

Charge collection time (90 % of charge) <150 ns verified with an infrared laser

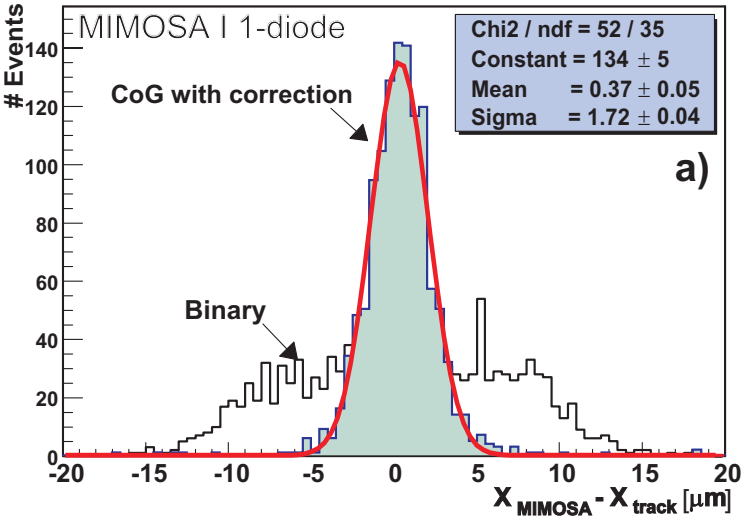
Beam test set-up with 1µm precision beam telescope

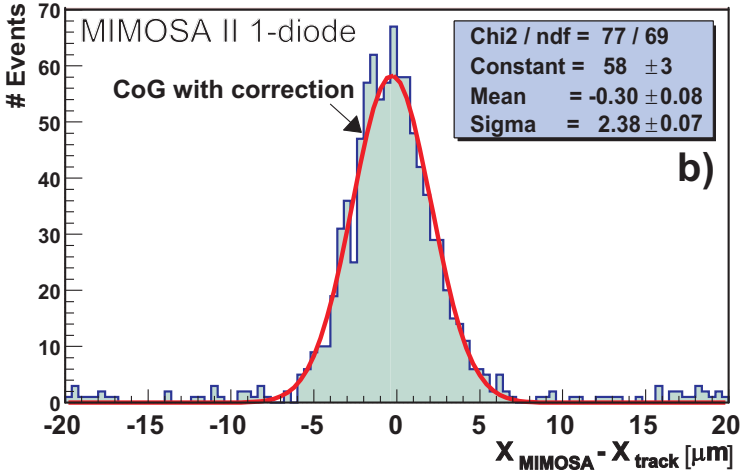


Readout with circular buffer memory architecture allowing Correlated Double Sampling (off-line)



Residual distribution of a particle track position





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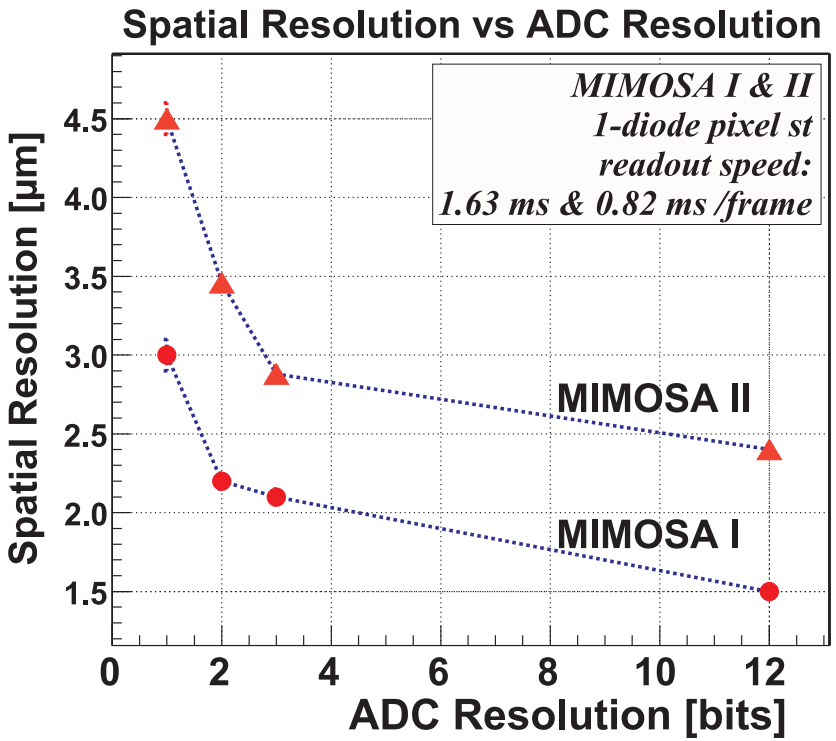
☑ First Prototypes - Summary of Performances

		Noise mean ENC [e⁻]: single pixel	mean S/N: 3x3 cluster
MIMOSA I:	1 diode	12-14	42
	4 diodes	25-30	32
MIMOSA II:	1 diode	9-12	22

		Collected charge [e⁻] seed pixel	'Landau peak': 3x3 cluster
MIMOSA I:	1 diode	302	896
	4 diodes	517	1155
MIMOSA II:	1 diode	110	315
	2 diodes	136	407



Spatial resolution (µm):

MIMOSA I:	1 diode	1.4+/-0.1
	4 diodes	2.1+/-0.1
MIMOSA II:	1 diode	2.2+/-0.1

Efficiency (%)

MIMOSA I:	1 diode	99.5 +/- 0.2
MIMOSA I:	4 diodes	99.2 +/- 0.2
MIMOSA II:	1 diode	98.5 +/- 0.3

MIMOSA = Minimum Ionising MOS Active Pixel Sensors

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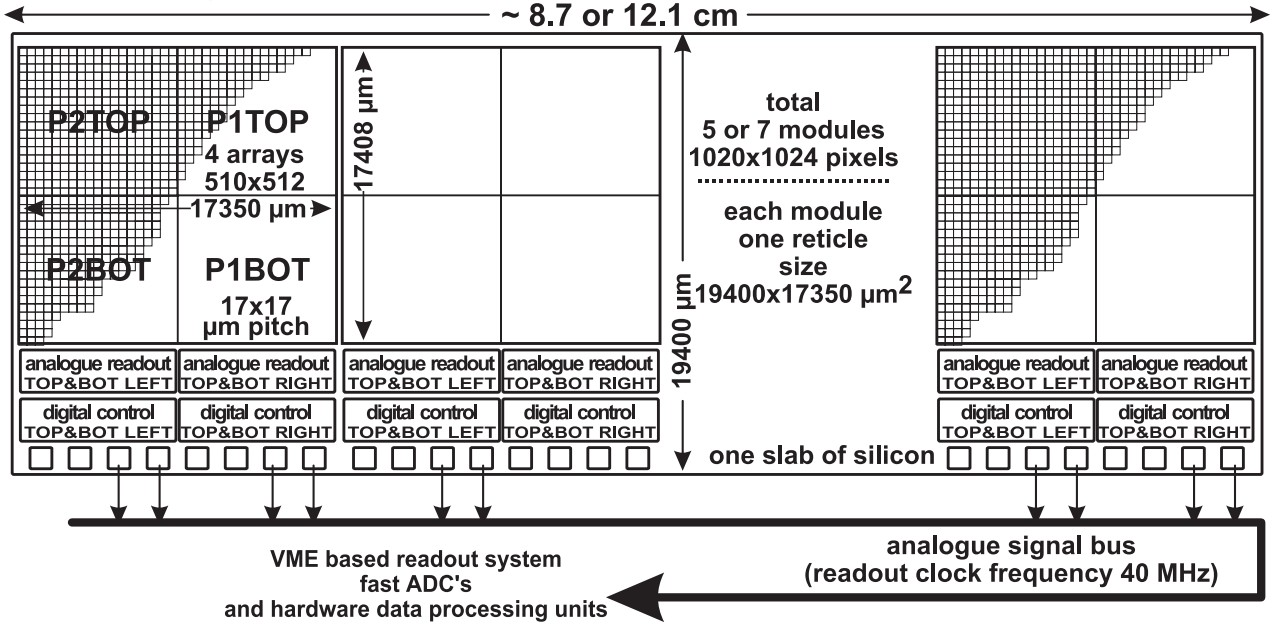
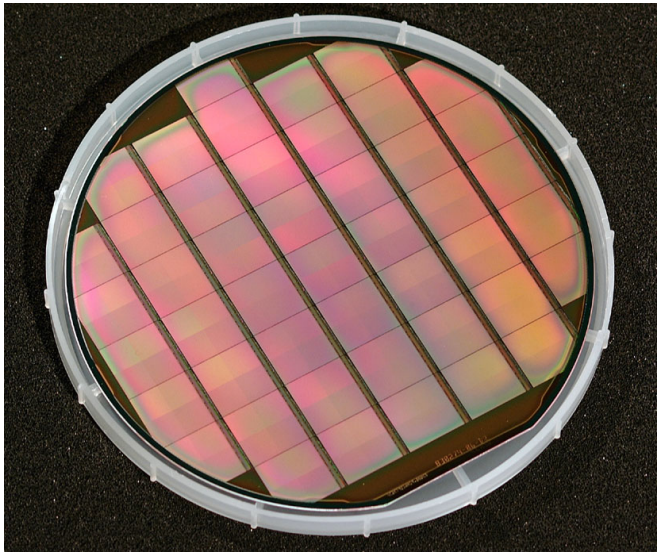
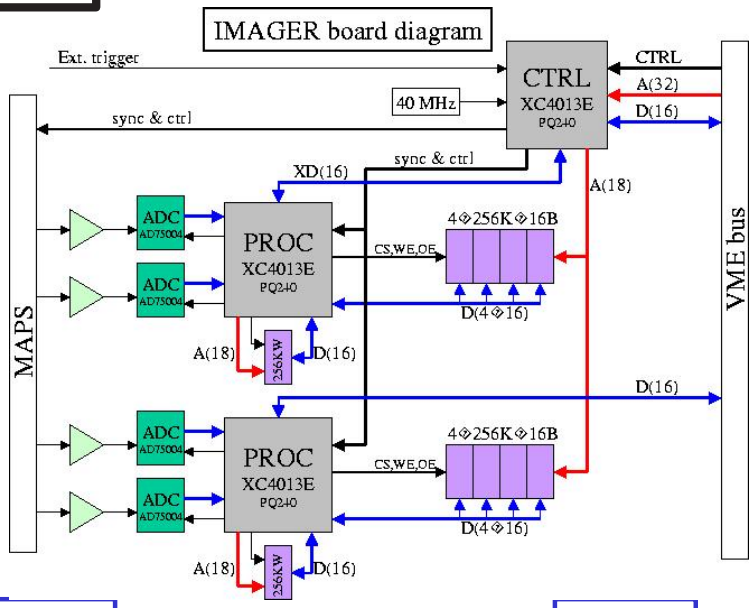
☑ Design and Performances of 3.5 cm², 1M Pixel Device





- 0.6 µm CMOS process with 14 µm epitaxial layer,
- Pixel - 17 × 17 µm², diodes P1 - 9.6 pm², P2 - 24.0 pm²,
- Stitching coarse: 100 µm + scribeline, option precise: 1µm,
- Analogue readout - with hardware processing; CDS, pedestal subtraction, S/N analysis, sparsification on-line,
- Several readout option: summation of signals from 3 pixels in horizontal direction, fast scan every third pixel read-out, rolling reset,
- Cost of a lot of six 6 inch wafers ~44 kEuro.



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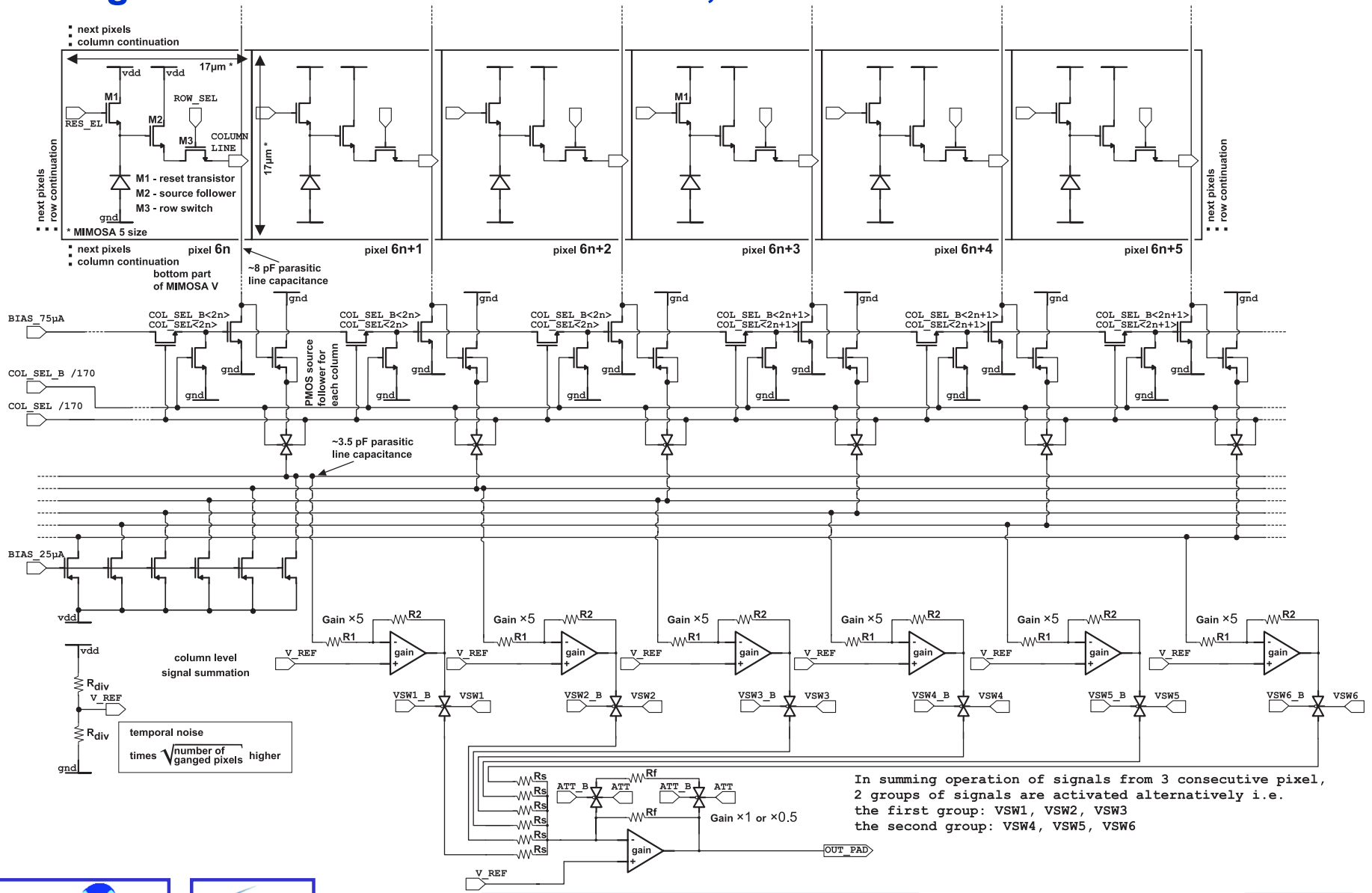
☑ Design and Performances of 3.5 cm², 1M Pixel Device



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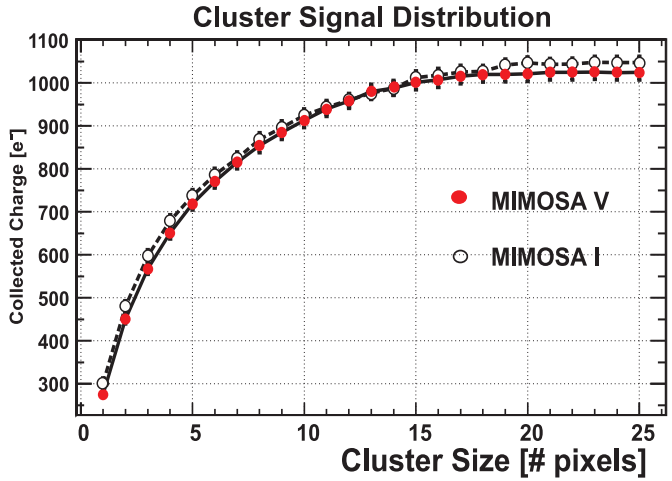
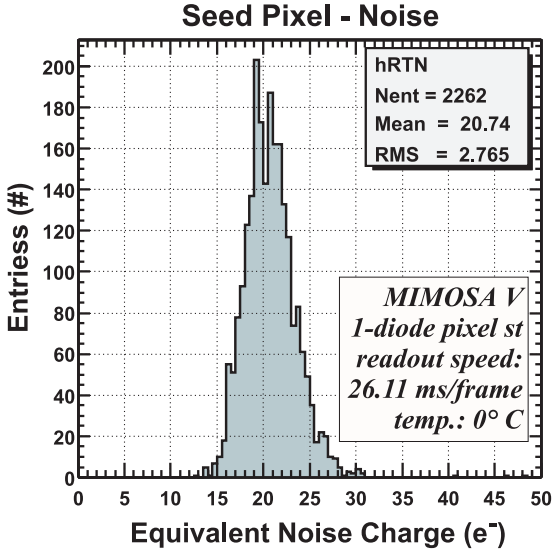
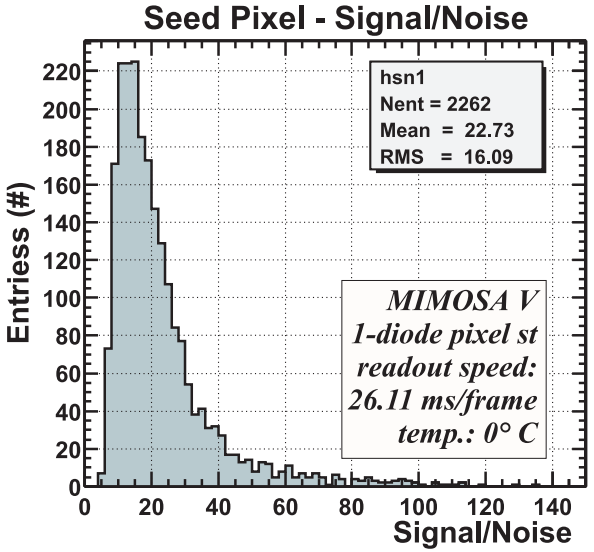
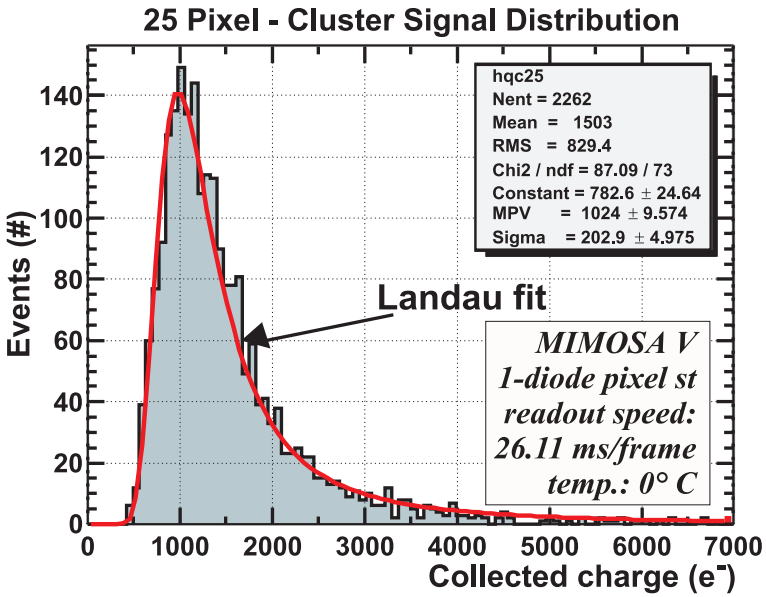
☑ Design and Performances of 3.5 cm², 1M Pixel Device









- **4 matrices of 510 × 512 pixels read-out in parallel etched down to 120 µm:**

Preliminary results:

Noise mean ENC:	20.74 e⁻
Single pixel S/N mean:	22.73
detection efficiency ε:	99.3%
spatial resolution σ:	1.7 µm
macro-scale gain nonuniformity:	0.2%

- **Twice noise MIMOSA I ⇦ wider frequency bandwidth, double source follower stage...,**
- **Problem to be solved - fabrication yield.**

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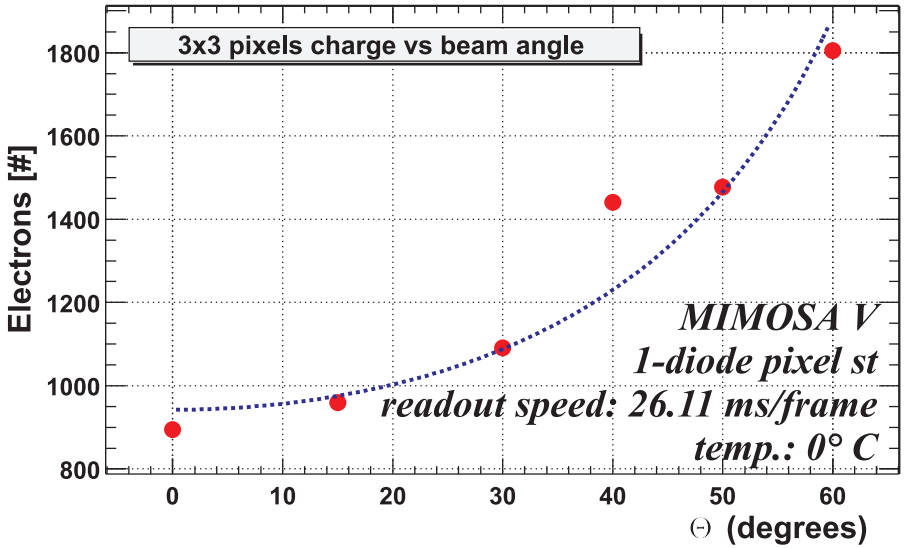
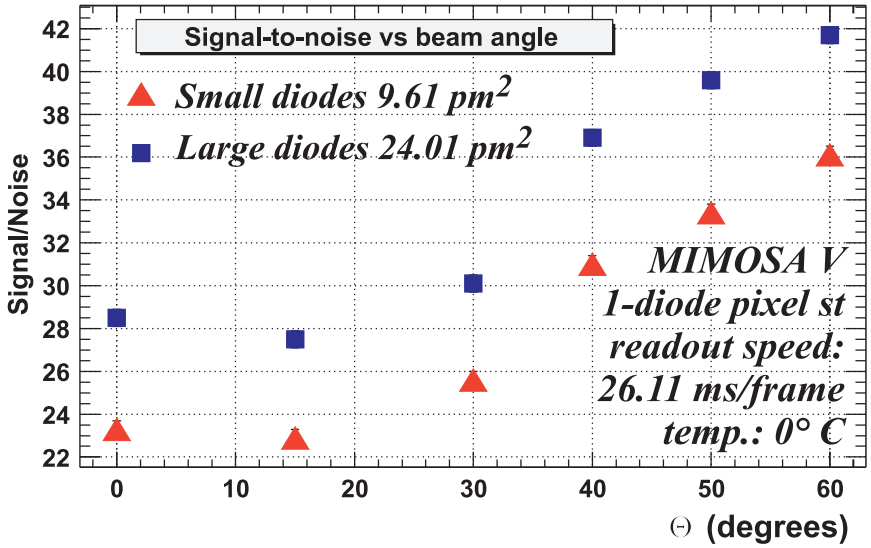
☑ Design and Performances of 3.5 cm², 1M Pixel Device

◎ MIMOSA V rotated with respect to the beam direction





◎ Increase of signal observed ⇨ aproximate cos(θ) dependence,

◎ Saturation observed for central pixel ⇦ geometrical effect.

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☑ Radiation Hardness • Neutron irradiations

The carrier lifetime is related to the concentration of defects by:

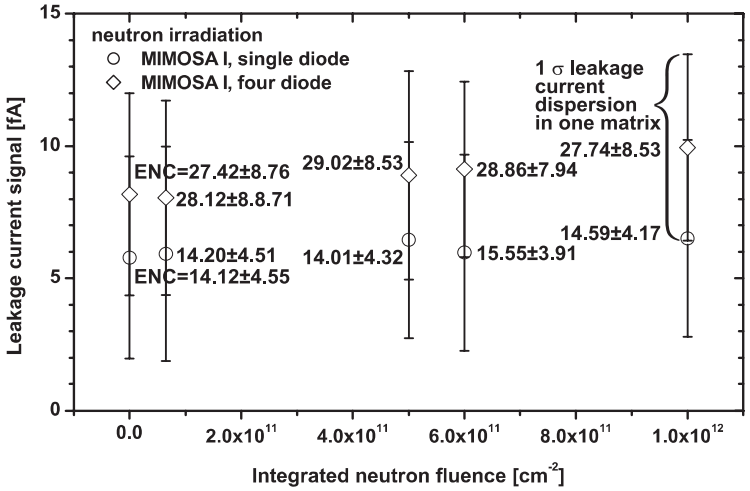
$$\tau_{def} = \frac{1}{v_{th}\sigma_{def}N_{def}}$$

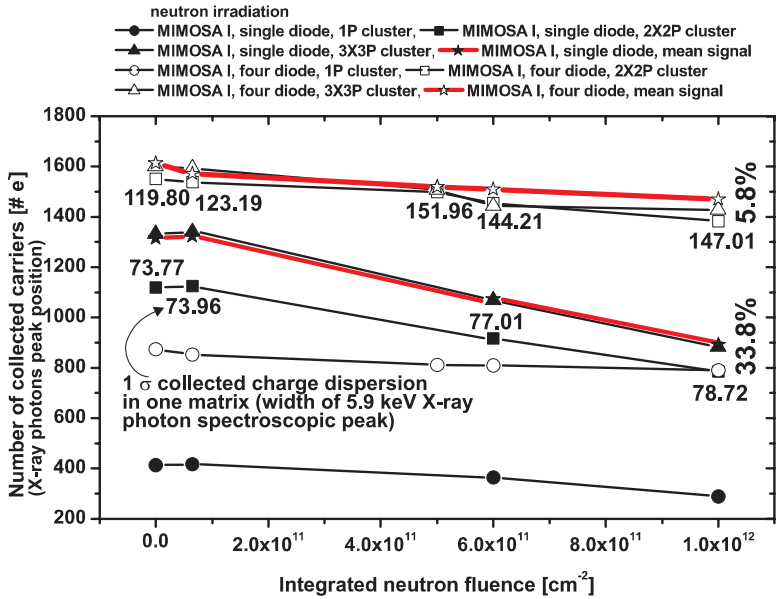
The dependence of the lifetime on the irradiation fluence is given by:

$$\frac{1}{\tau_R} = \frac{1}{\tau_0} + \frac{1}{\tau_{def}} = \frac{1}{\tau_0} + \kappa_\tau \Phi$$

For large fluences second factor starts to dominate and carrier lifetime decreases like $(\kappa_\tau)^{-1}$

MIMOSA I neutron irradiations 10^{12} n/cm^2





MIMOSA II neutron irradiations 10^{13} n/cm^2 *(charge loss for 2 × 2 pixel cluster)*

MIMOSA II configuration	fluence 0 n/cm^2	fluence 1.2×10^{12} n/cm^2	fluence 1.4×10^{12} n/cm^2	fluence 2.8×10^{12} n/cm^2	fluence 1.0×10^{13} n/cm^2
M II, 1 diode	1206 e$^-$ (0%)	952 e$^-$ (21%)	not measured	958 e$^-$ (21%)	442 e$^-$ (63%)
M II, 2 diode	1249 e$^-$ (0%)	1254 e$^-$ (0%)	1089 e$^-$ (13%)	1004 e$^-$ (20%)	667 e$^-$ (46%)

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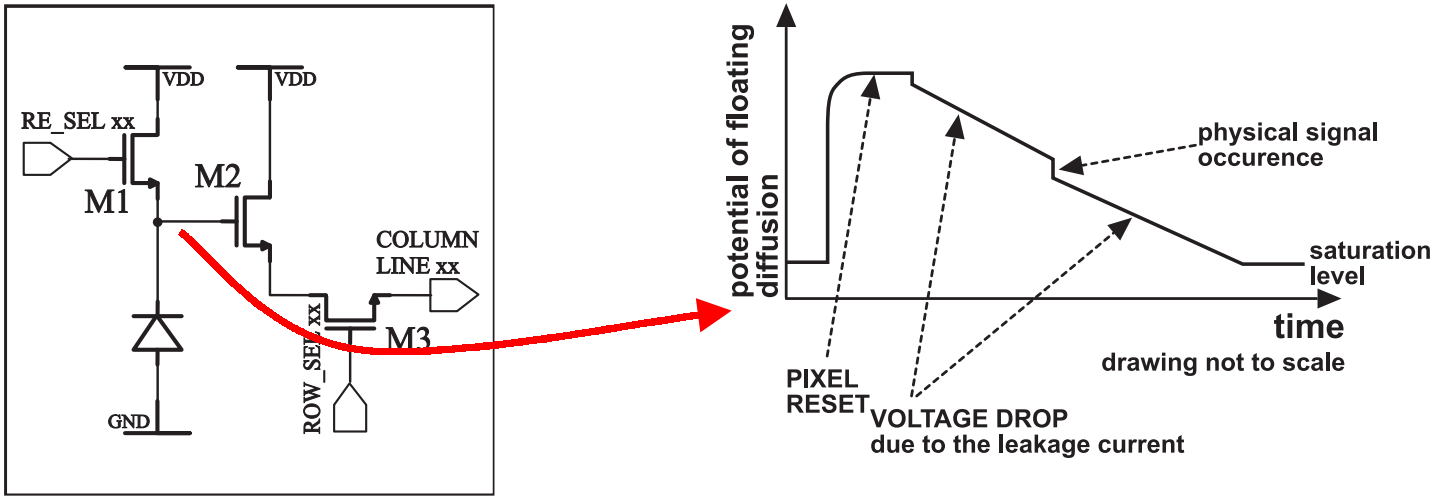
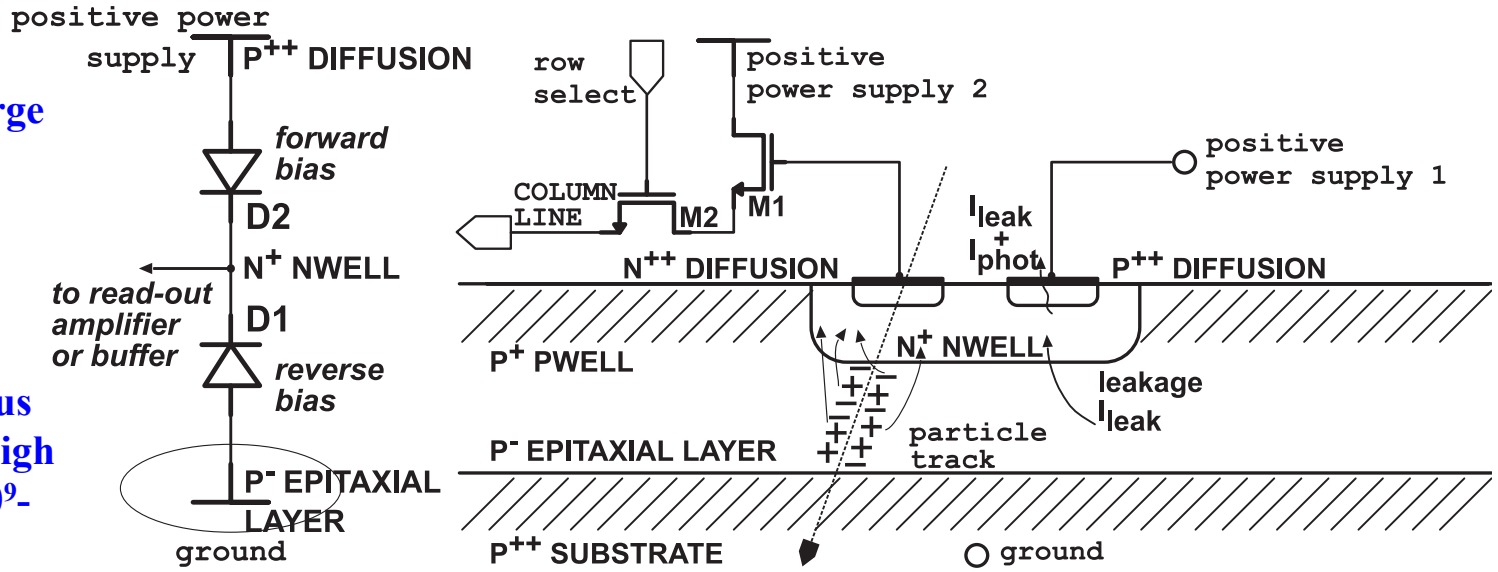
☑ Alternative Architecture of Charge Sensing Element - *example*



- On-pixel amplification requires suppression of the leakage current effect - preserving charge integration,

- Self-reverse polarisation of charge collecting diode,

- In darkness, the diodes D2 conveys only a small value leakage current, thus it represents very high value resistance (10^9-10^{12} Ω).



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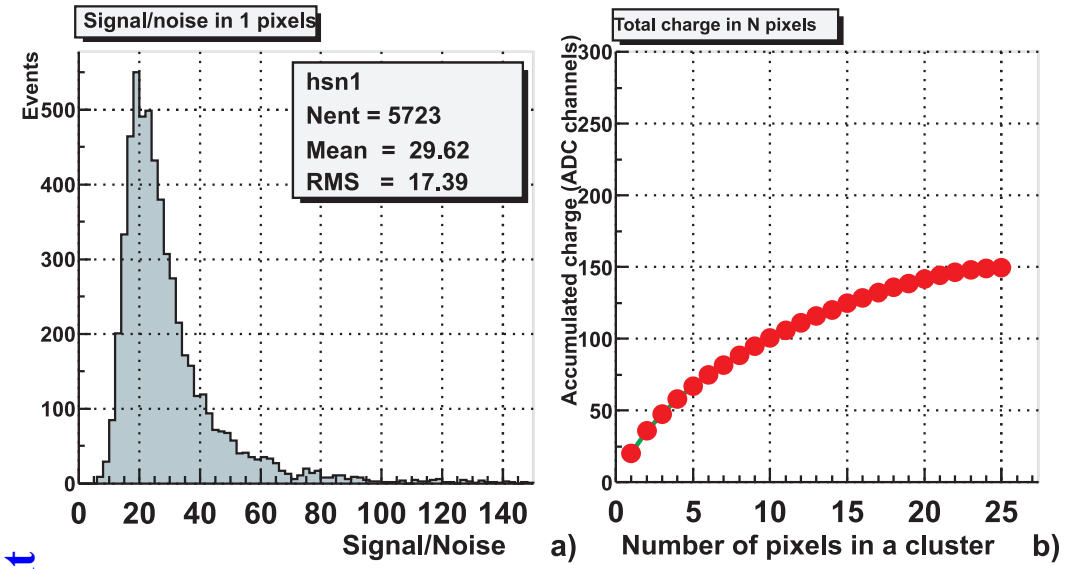
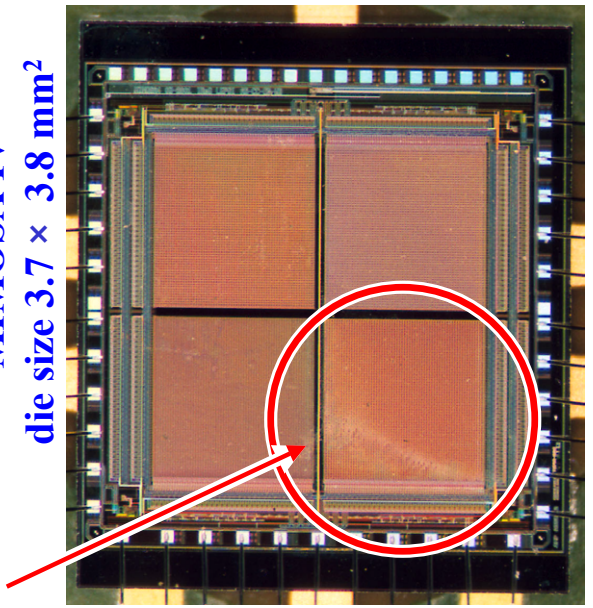
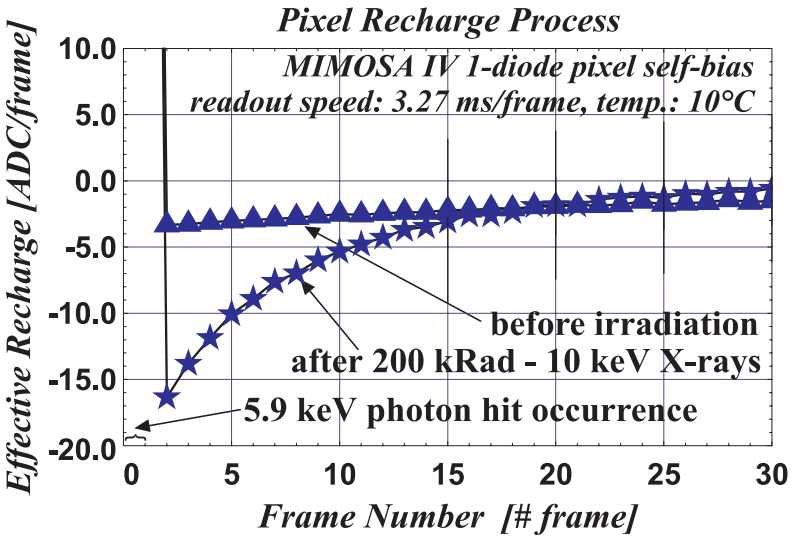
☑ Performances of Self-Bias Test Structure on MIMOSA IV

◎ 120 GeV/c pions beam tests

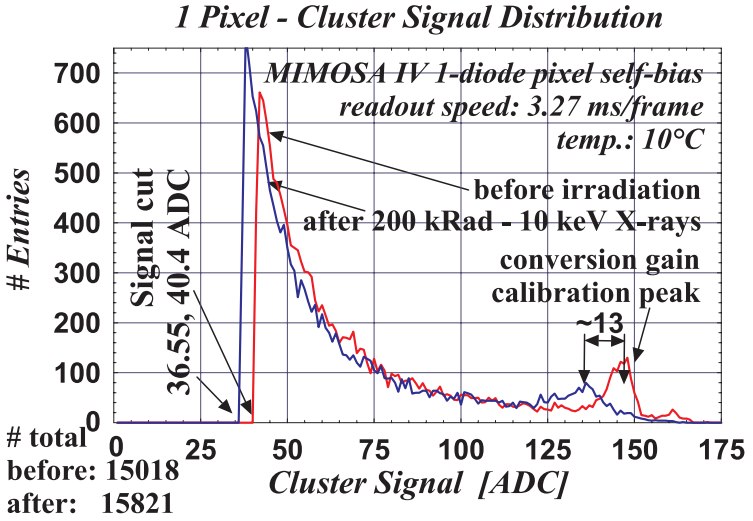




Effective recharge of the node after ^{55}Fephoton hit



Threshold correction in hit finding procedure for ^{55}Fe X-ray source



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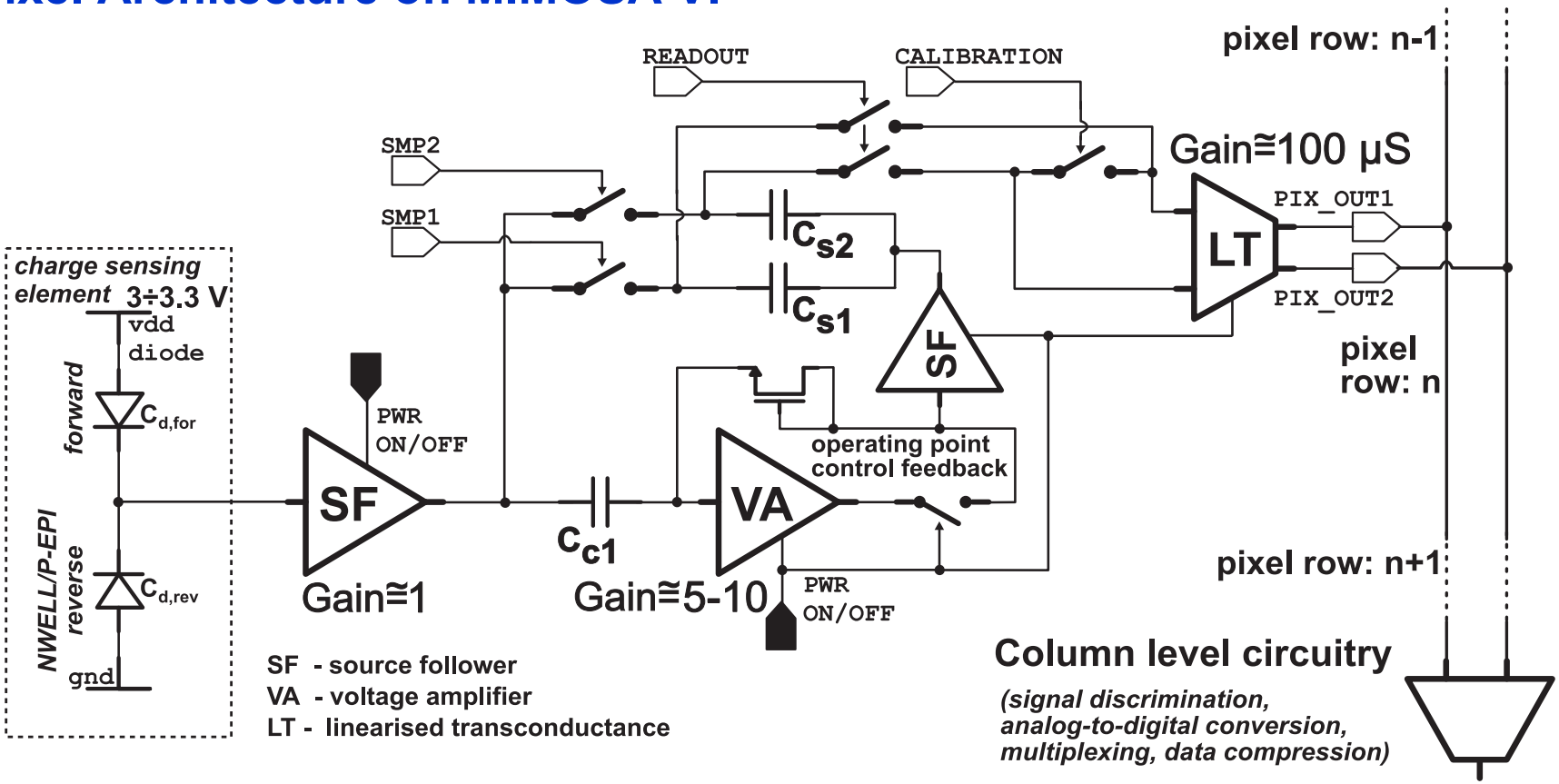
☑ Pixel Architecture on MIMOSA VI



- Charge converted to voltage on diode cathodes; resulting voltage buffered by SF,
- Amplified voltage stored on first capacitor,
- Second capacitor stores amplified voltage from previous cycle,
- The signals are substracted on the transcosnduction stage, and currents sent for discrimination.

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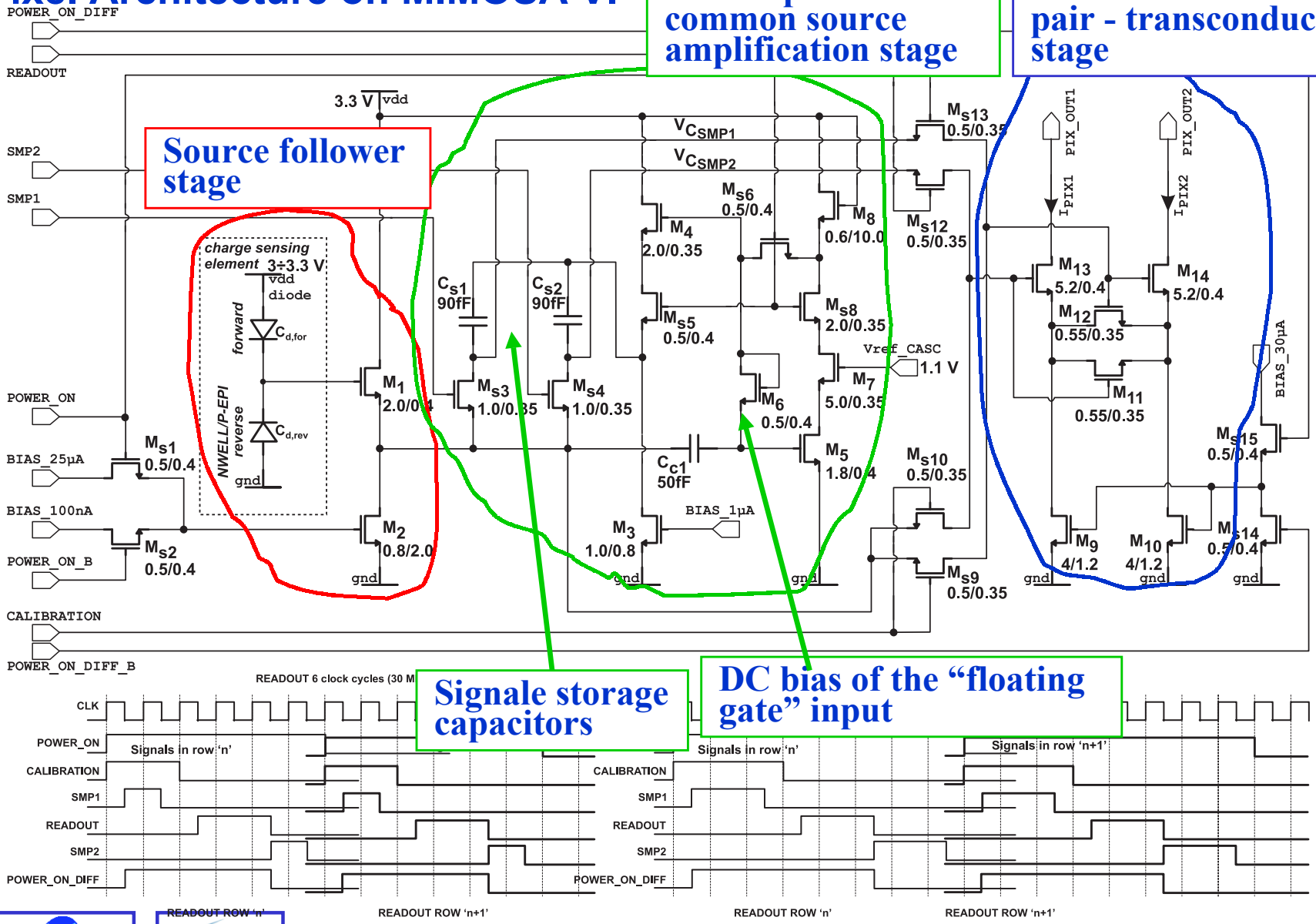
☑ Pixel Architecture on MIMOSA VI

AC-coupled common source amplification stage

Linearised differential pair - transconductance stage

Source follower stage



Signale storage capacitors

DC bias of the "floating gate" input

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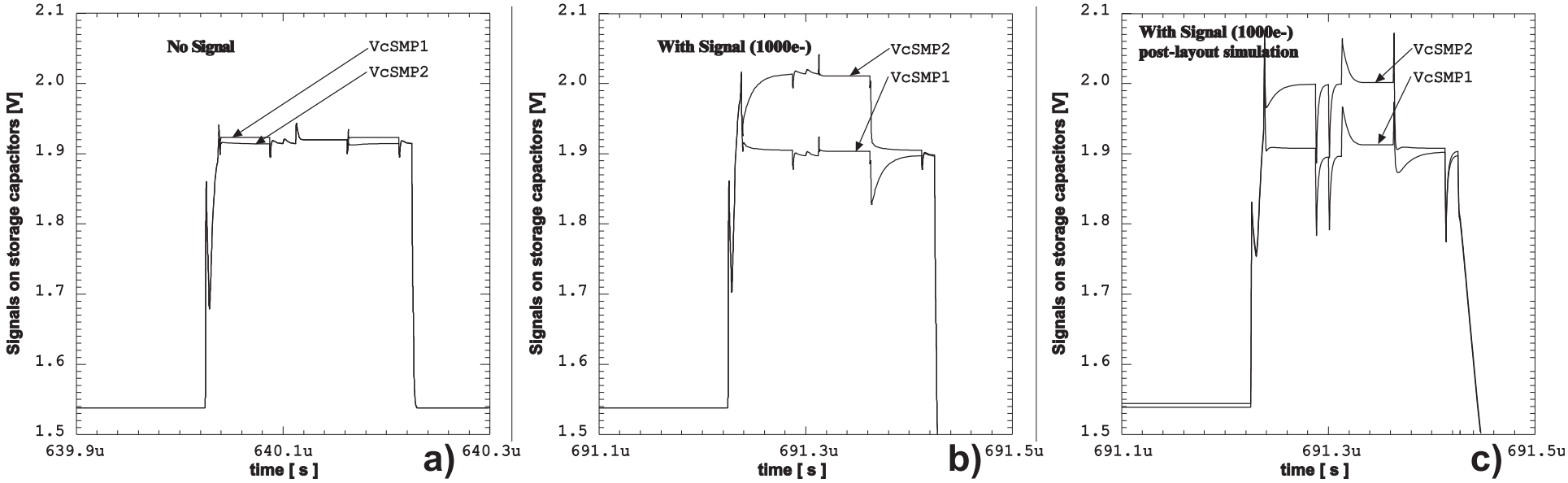
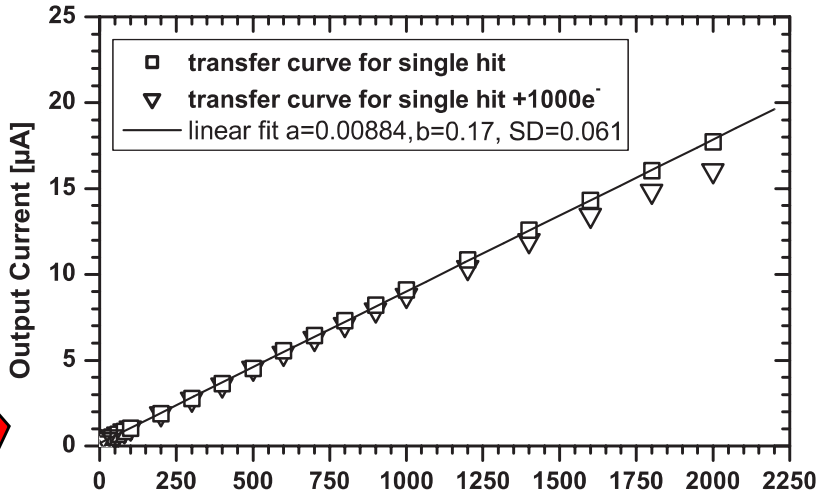
☑ Pixel Architecture on MIMOSA VI

◎ SPICE simulation of pixel response



Response of the pixel amplifier, measured as a voltage on two storage capacitors:
(a) in absence of any charge deposited,
(b) for signal of 1000 e^- (schematic) ~0.10 mV/e^-,
(c) post layout simulation ~0.09 mV/e^-.

Current gain of the pixel as a function of the charge acquired



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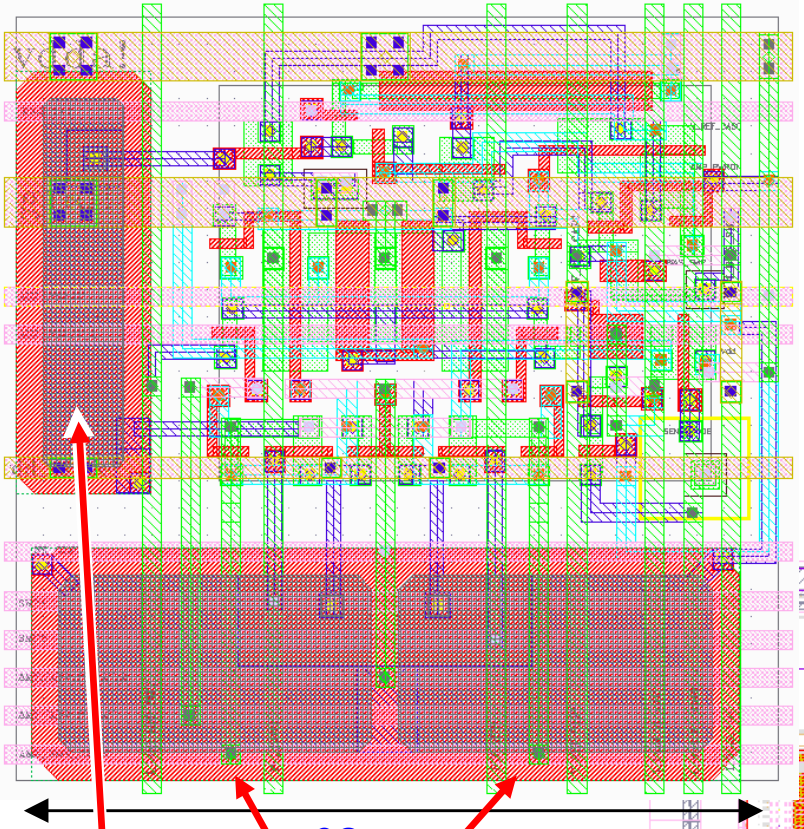
☑ MIMOSA VI

Pixel layout



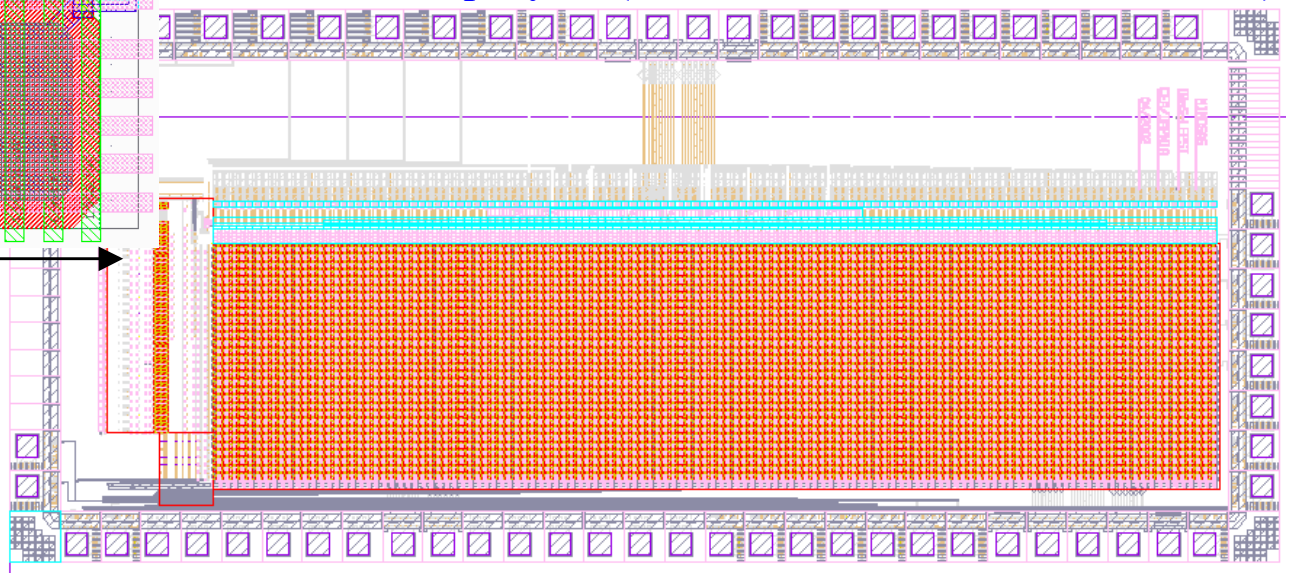
◎ Pixel design features

- only NMOS transistors, nwell/psub and pdiff/nwell diodes and poly1-to-poly2 capacitors.

◎ MIMOSA VI design features

- 0.35 µm CMOS 4.2 µm thick EPI layer,
- 1 array (24+6) × 128 pixels, pitch 28 × 28 µm^2,
- 24 columns read-out in parallel,
- 30MHz f_{clk}, 6 clock cycles per pixel,
- amplification and double sampling operation on-pixel,
- discrimination integrated on chip periphery,
- diode (nwell/p-epi) size 4.0 × 3.7 µm^2 - 3.5 fF,

MIMOSA VI chip layout (IReS-LEPSI/DAPNIA collaboration)



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☑ Summary & Outlook

Achievements

⊙ Monolithique CMOS Pixel Detectors *(pixel architecture used in visible light application)* offer detection efficiency, spatial resolution and radiation hardness requested for the VXD at the FLC (TESLA),

⊙ Preliminary results from MIMOSA V indicate that performances obtained with small size prototypes are reproducible with real size detectors (120 µm thin devices),

⊙ Depending on application, alternative pixel configurations are appealing i.e. use of low doping non epitaxial substrate, auto-reverse polarisation of charge sensitive element, etc.,

⊙ Adequacy of the two-diode *(logarithmic)* pixel configuration for charged particle detection has been assessed with the MIMOSA IV prototype,

⊙ As a result... design combining on-pixel signal amplification with double sampling operation and column level discrimination - coming back soon from fabrication,

⊙ Development of this pixel concept is a first attempt for signal processing functionalities, including e.g. data sparsification, performed on-line on the detector,

⊙ Worth highlighting - room temperature operation.

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☑ Summary & Outlook

Goals

⊙ Whether the thin chips/ladders can be produced? Improving fabrication yield and demonstrate (yield?) thinning technique as a post-processing technology,

⊙ Optimise granularity, readout speed and material budget to fit application requirements,

⊙ Integrate functions leading to the on-line data sparsification (column parallel readout, on-pixel data processing, etc., ⇨ **processes with ≥ 5 metal layers ☺ (in contrast to visible light application no limits from quantum efficiency),**

⊙ For some application e.g. consisiting in low-energy (~10 keV) direct electron imaging, - demonstrate back illumination (correlated with detector thinning),

⊙ System integration - DAQ, mechanical support, coolling, etc,

⊙ Understanding radiation effects (ionising radiation) and improving radiation tolerance.

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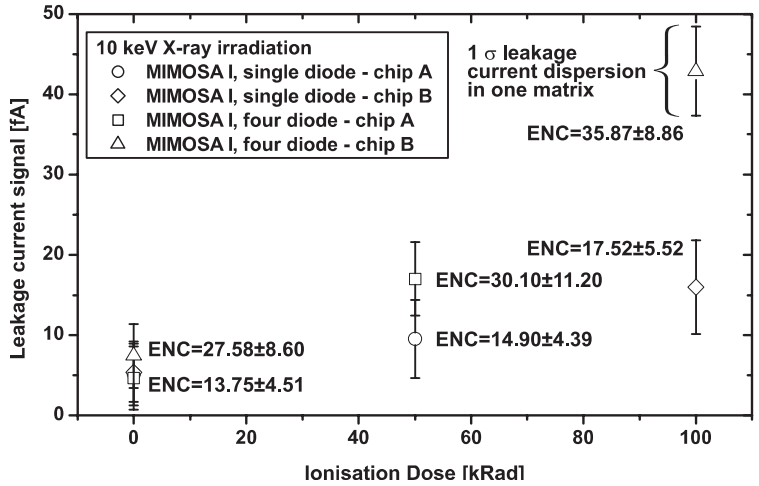
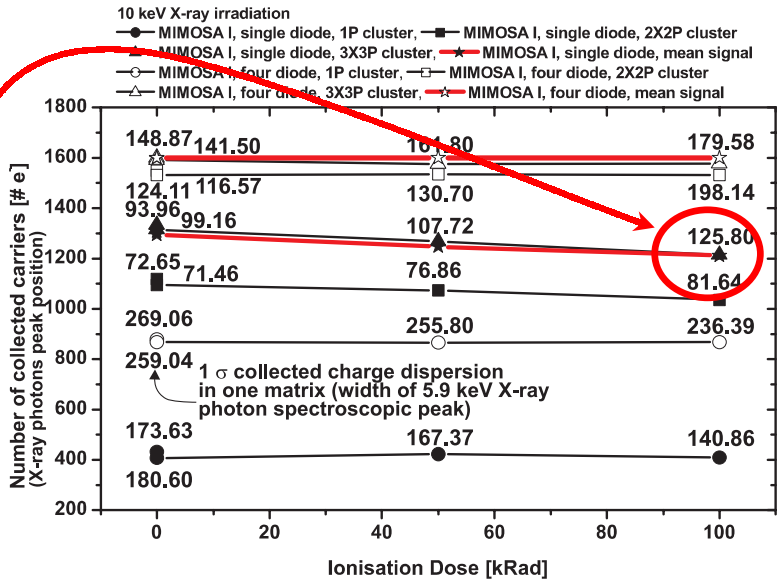
☑ Radiation Hardness • Ionising irradiations

Irradiation damages are manifested by charge built-up in isolation materials - oxide

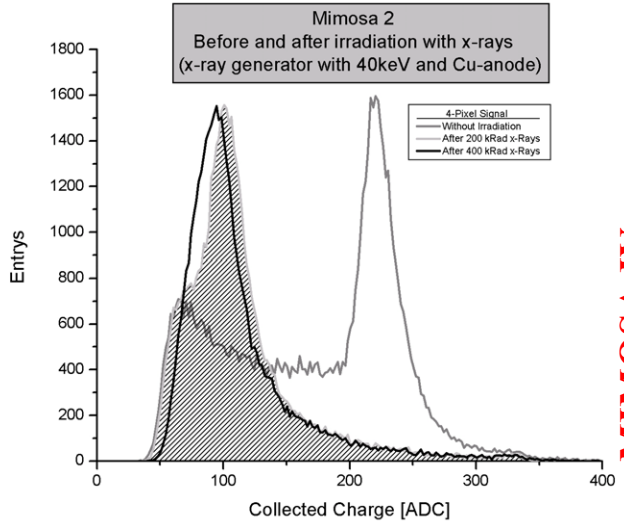
MIMOSA I increase of leakage current



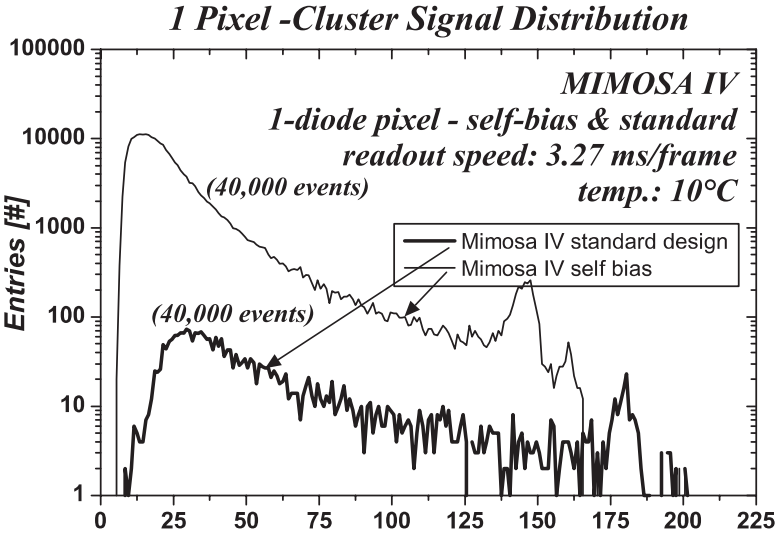
MIMOSA I slight losses in collected charge



MIMOSA II strong charge losses in collected charge



MIMOSA IV - non irradiated shows dependence of charge collection on pixel layout - this has effect like irradiation!



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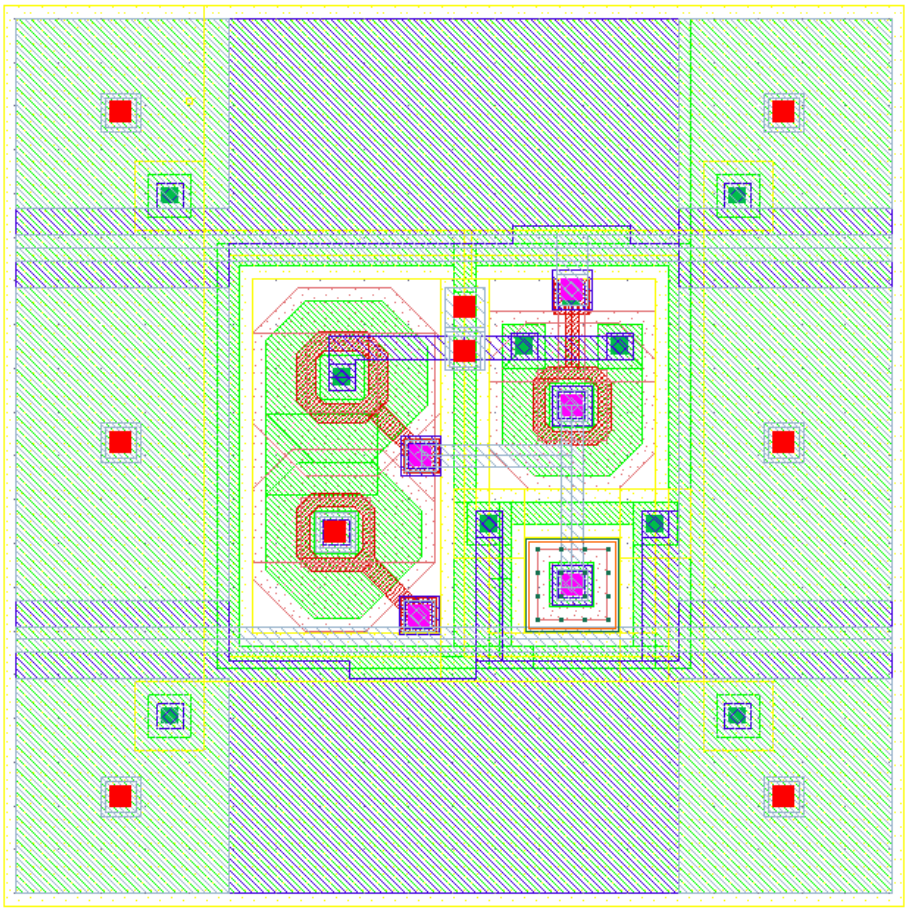
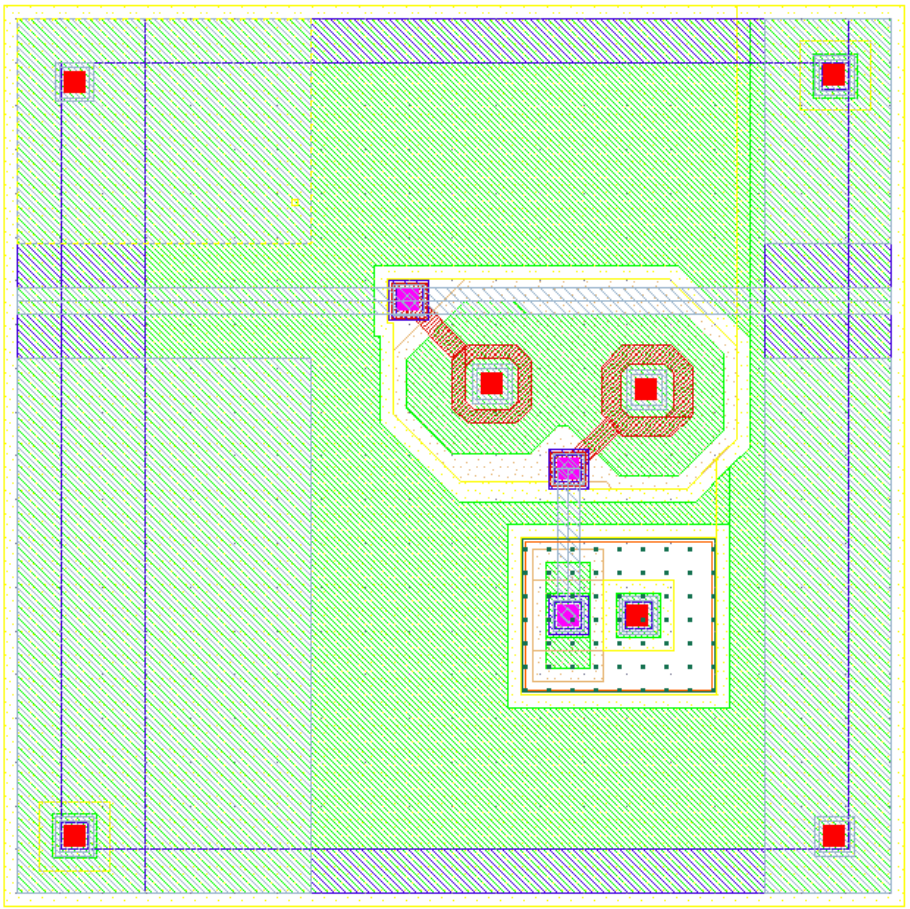
☑ Radiation Hardness

MIMOSA IV
pixel layout suffering from poor charge collection



MIMOSA IV
pixel layout allowing good charge collection



What is the difference?