The Architecture of the BTeV Pixel Readout Chip (FPIX2)

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FPIX2 Chip Designers

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(analog design +
overall responsibility)

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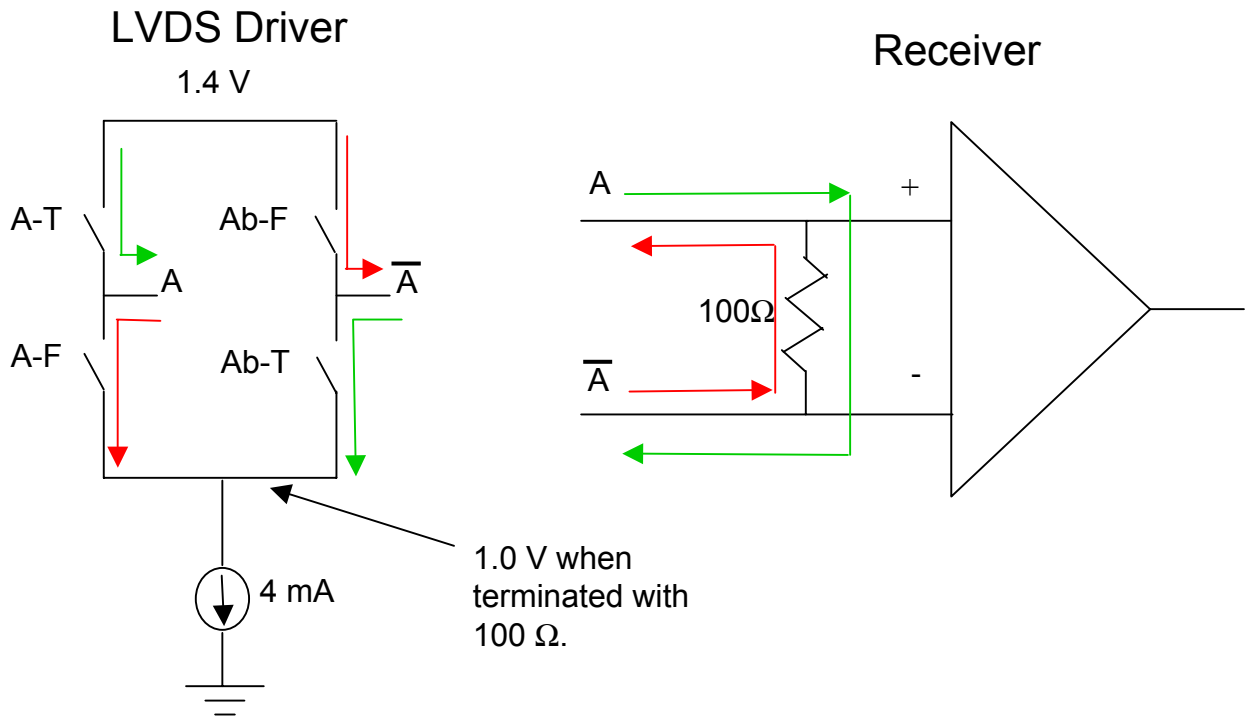
Digital design

FPIX2 Overview

- 0.25μ CMOS (rad hard) – will be submitted to TSMC ~10/1/02.
- 128 rows x 22 columns – 50μ x 400μ pixels.
- The only supply voltages required are 2.5V and ground; all other bias voltages, bias currents, and threshold voltages are generated by programmable DAC's.
- Very high speed, data driven, zero-suppressed readout – no trigger; every hit is read out.
- Readout off chip is point-to-point, using a configurable number of 140 Mbs serial links (1,2,4, or 6).
- All I/O is LVDS (Low Voltage Differential Signaling); a single row of pads is used.

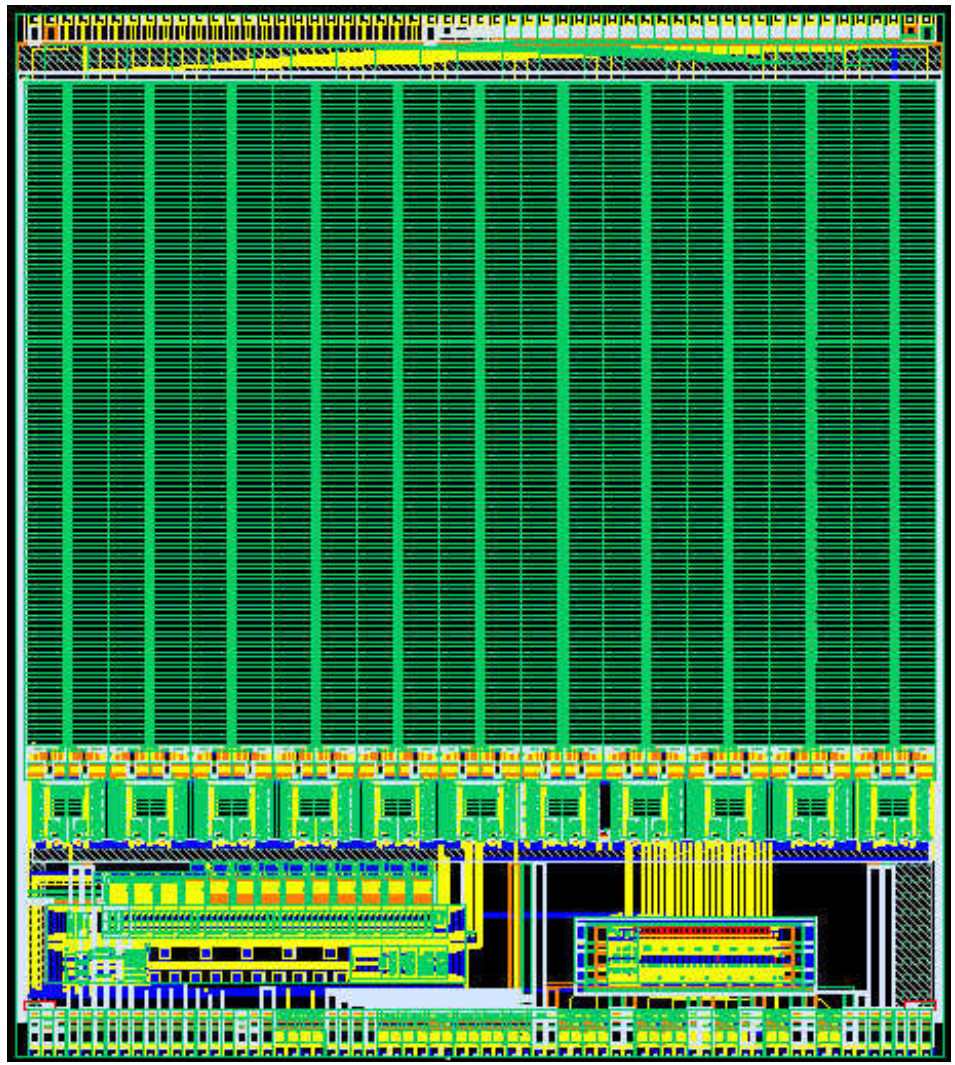
Low Voltage Differential Signaling (schematic)



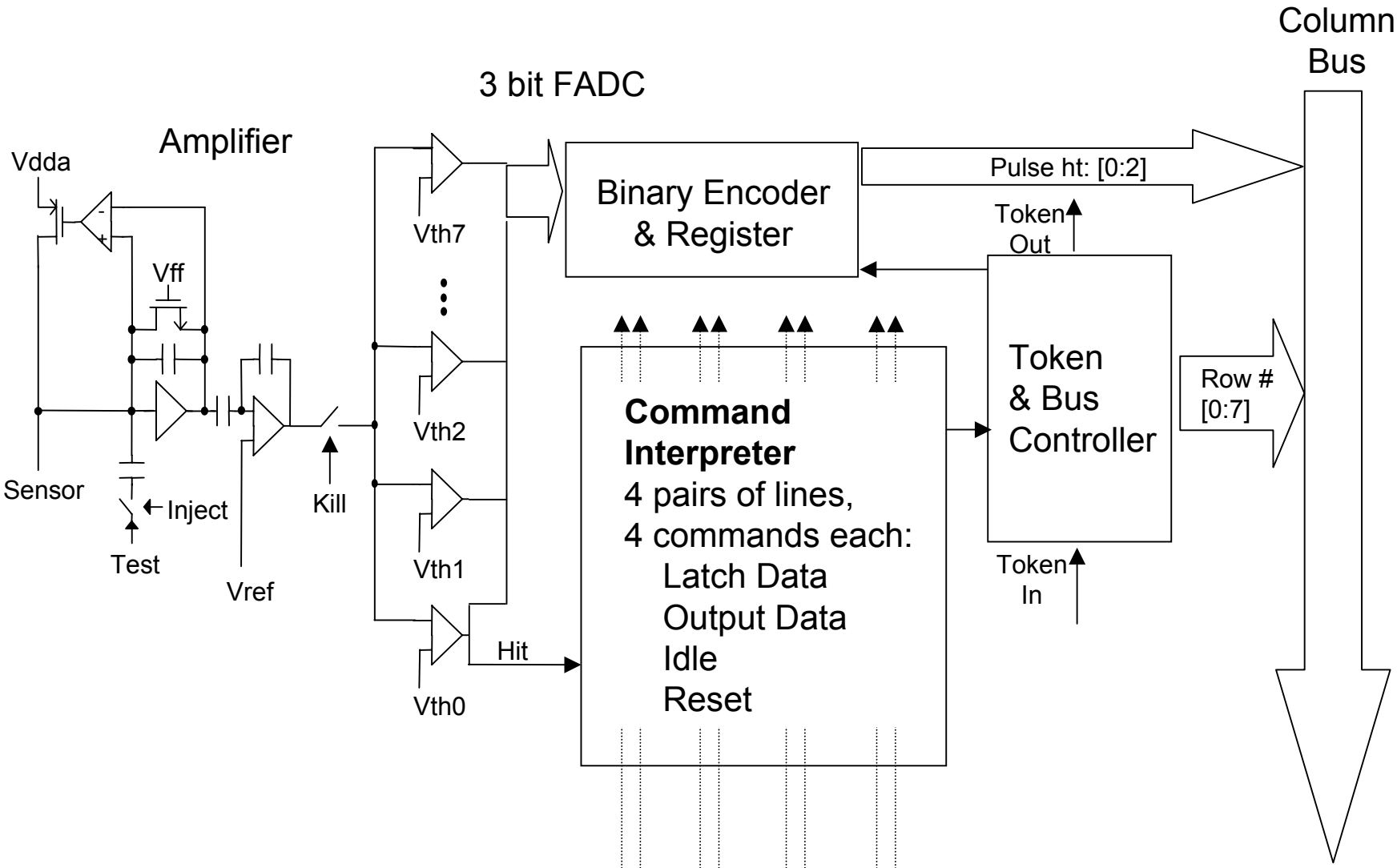
"True" is green current flow; "False" is red current flow.

LVDS is an industry standard & is supported by many FPGA's.

FPIX2 Layout

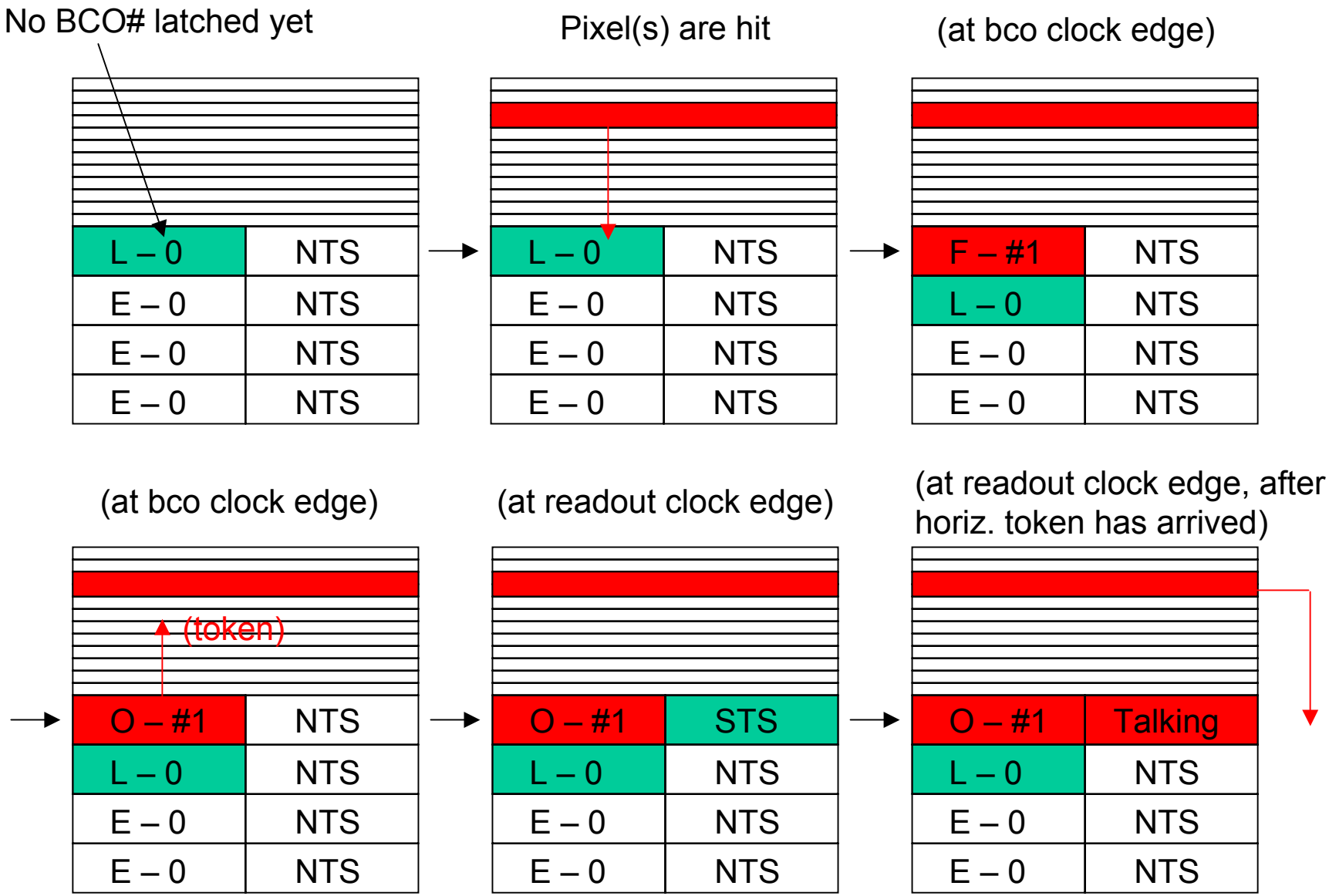


Pixel Unit Cell



Example of chip operation

- I will illustrate FPIX2 operation by focusing first at the base of a column of pixels.
- Each column contains four “command sets” and can hold data associated with four separate beam crossings.
- Command set actions are determined by two state machines, one which changes state on Beam Cross Over clock edges (1/132 ns), and one which changes on Readout clock edges (max frequency = 35 MHz = 1/29 ns).
- EOC logic is constructed so that the BCO clock & Readout clock need not be related to one another, either in frequency or in phase.



States: (Empty/Listen/Full/Output) & (Nothing To Say/Something to Say/Talking/Silent)
Priority logic insures only 1 command set at a time in Listen or Output.

Core Readout

- Readout is controlled by two sets of tokens, horizontal & vertical.
- The vertical tokens are launched (independently) when a command set enters the “Output” state. They move again as data is driven off of a pixel.
- When any EOC command set enters the “Something to Say” state, the core logic launches the horizontal token on the next readout clock edge (if it is not already active).
- When the token arrives at a column with something to say, the command set in STS goes to “Talking” at the next readout clock edge, and data is driven onto the Core output bus on this readout cycle.

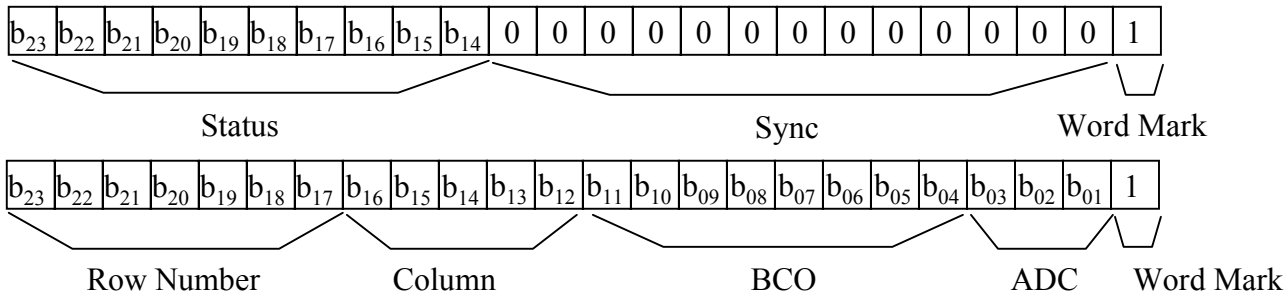
Core Readout (continued)

- When the vertical token arrives at the last hit pixel associated with the command set in the “Output” state, the horizontal token is released and stops at the next column with something to say. This insures that there will not be an empty readout cycle between the last hit in one column and the first hit in the next column.
- When the horizontal token passes the last column, the core goes silent for one readout cycle. Another readout cycle is required to relaunch the horizontal token, so there are always two empty readout cycles every time the horizontal token sweeps past all 22 columns. These are the only “wasted” readout cycles.

Data Output

- Data is driven off of a hit pixel onto the Core output bus, which is 23 bits wide. The data word consists of the information generated in the pixel unit cell (7 bit row number, and 3 bit ADC value), plus a 5 bit column number and an 8 bit BCO number, which are added by the end of column logic.
- The Data Output Interface latches data from the Core output bus on the *falling* edge of the readout clock, serializes the data, and drives it off chip.

Output Data Format



• Five bits are used to encode 22 columns. The column numbering scheme has no column number ending in 00. This ensures that a data word can never have 0's in b_{01} – b_{13}. This feature distinguishes a data word from a sync/status word.

•Synchronization between the FPIX2 and the Pixel Data Combiner Board is established and maintained using the "sync/status" word. Whenever no data is available for output, the FPIX2 transmits the sync/status word. At least two sync/status words are guaranteed to be output every time the column number decreases. In addition, 23 bit hit data is transferred using a 24 bit word. The PDCB uses the word mark bit as a sync check on every word transfer.

RCLK and SCLK

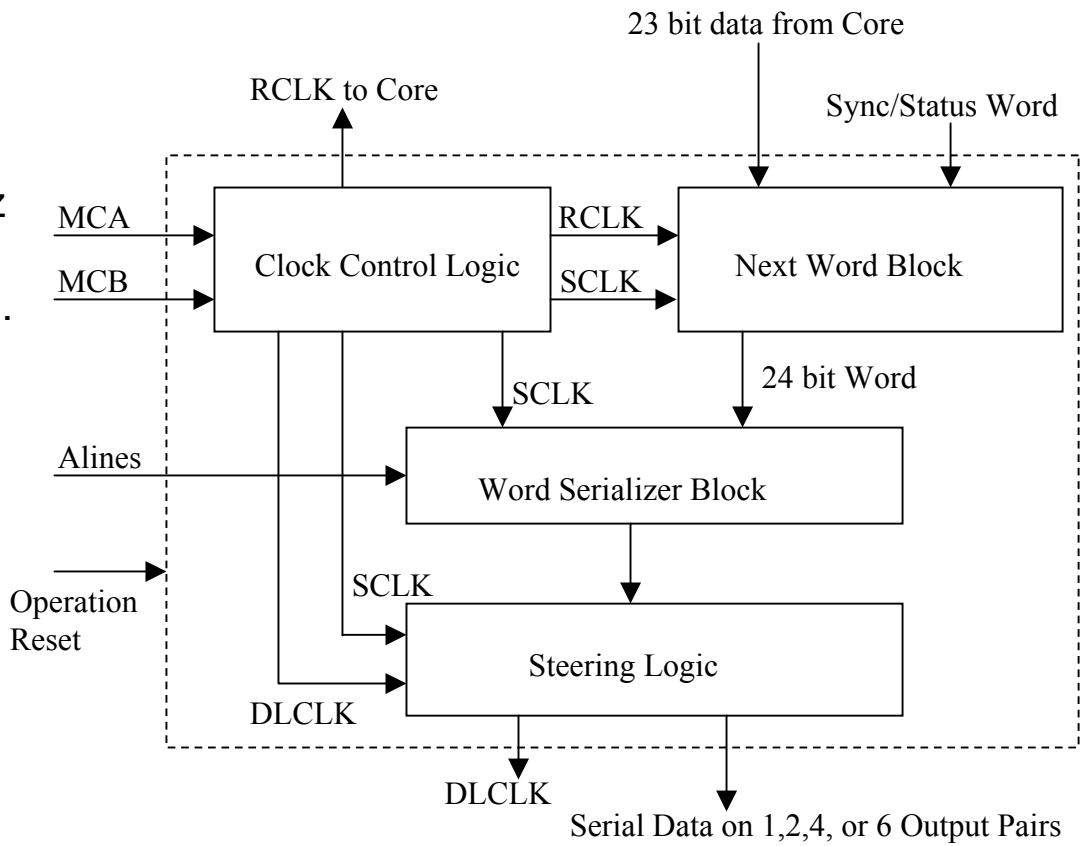
- The core readout clock (RCLK) is derived from the serial clock (SCLK). SCLK is constructed from external clocks and is nominally 140 MHz.
- The frequency of RCLK depends on the number of output pairs being used. This relationship means that no buffer memory is required in the Data Output Interface.

Configuration	SCLK Frequency	RCLK Frequency	
6 output pairs	140 MHz	35 MHz	140(6/24)
4 output pairs	140 MHz	23.3 MHz	140(4/24)
2 output pairs	140 MHz	11.7 MHz	140(2/24)
1 output pair	140 MHz	5.8 MHz	140(1/24)

35 MHz = 4.6/132 ns

Data Output Interface

Two 70 MHz clocks, 90º out of phase.

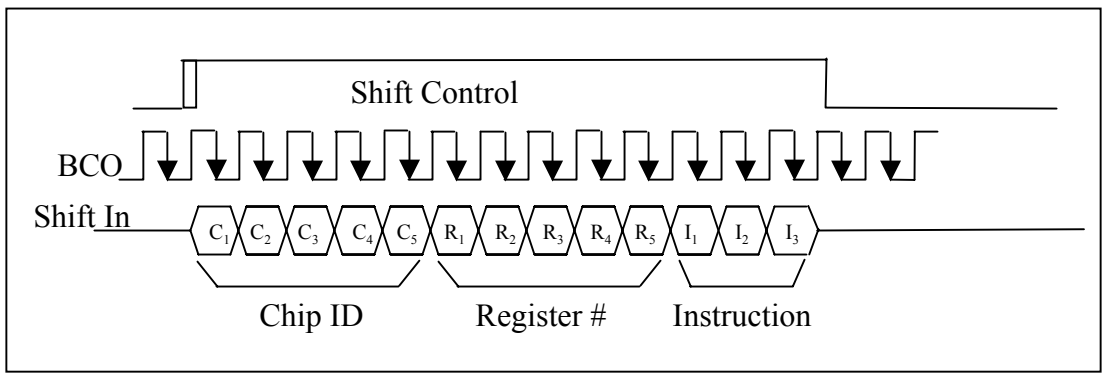


Sergio Zimmermann will talk more about the data transfer from the FPIX2 to the Pixel Data Combiner Board.

Programming Interface

- Each FPIX2 has a chip id, which is set by wire bonds on internal bond pads.
- I/O is bussed on three pairs of lines: shift control, shift in, shift out.
- I/O is synchronous – clocked by the BCO clock.
- Commands can be addressed to a single chip, or broadcast to all chips on the bus.

Command Format



Programming Interface Instructions

- Write (followed by 2, 8, or 2816 bits of data)
- Set (all bits in register = 1)
- Read
- Reset (all bits in register = 0)
- Default (set register to default value)

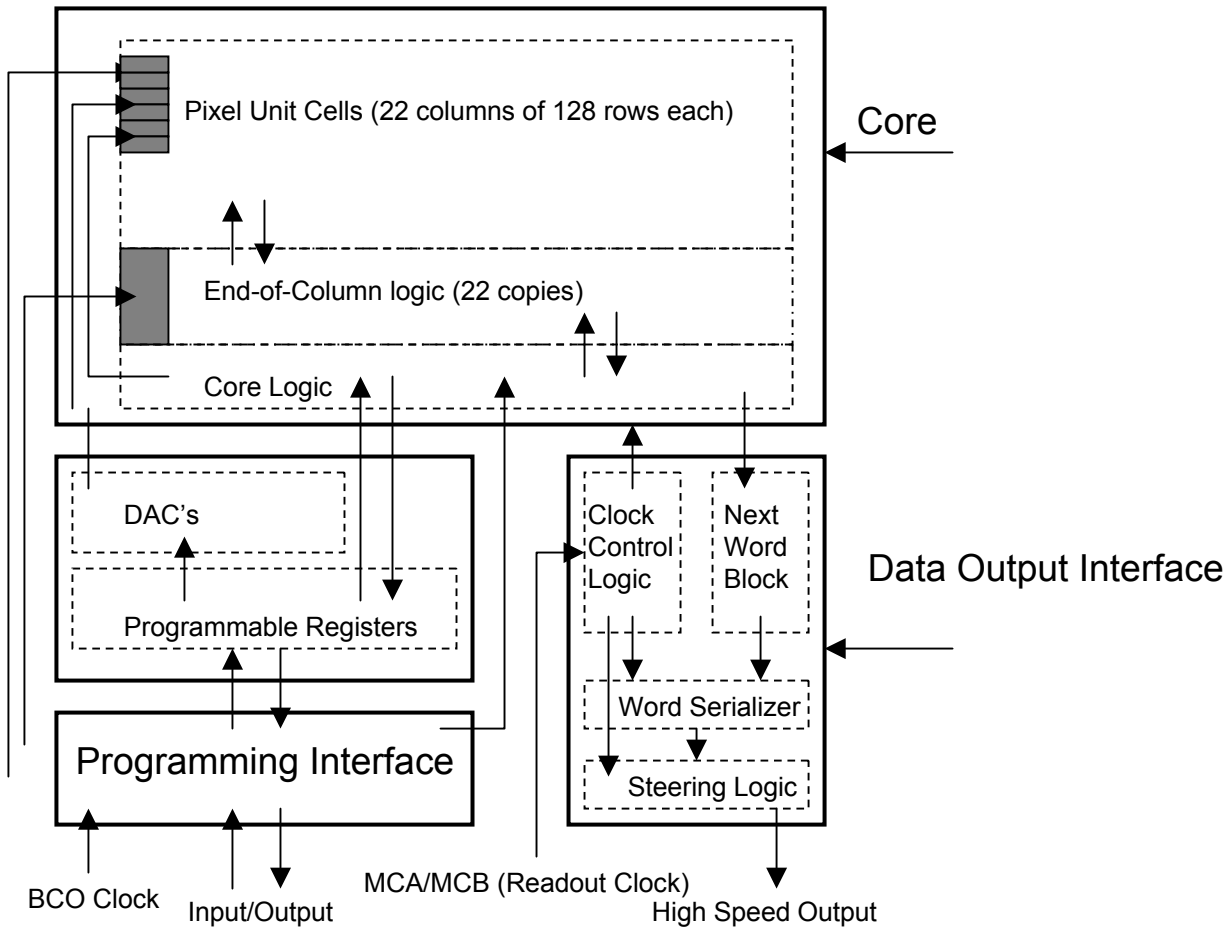
Registers and DAC's

- 23 of 32 possible registers are used.
- 14 are 8 bit registers that control Digital to Analog Converters – used to set bias currents and voltages, and comparator thresholds.
- 2 are serpentine registers (kill and inject) running up and down the pixel columns, with 1 bit in each pixel.
- 6 control facets of chip operation (# of output pairs, BCO sync check, SendData, RejectHits, Core Reset, Programming Reset).

Recap: FPIX2 Block Diagram

All circuit blocks have been tested in a series of small chips.

Our first full sized (128x22) chip with this architecture will be submitted ~10/1/02



More Information

- http://www-btev.fnal.gov/public/hep/detector/pixel/index.shtml
- “Radiation tolerance of prototype BTeV pixel detector readout chips” G. Chiodini, et al. FERMILAB-CONF-02-147-E (7/02).
- “Development of a readout technique for the high data rate BTeV pixel detector at Fermilab” B.K. Hall, et al. FERMILAB-CONF-01-335 (11/01).
- “Radiation tolerant circuits designed in two commercial 0.25μ CMOS processes” A. Mekkaoui, et al. FERMILAB-CONF-01-026-E (3/01).
- “FPIX2: A radiation-hard pixel readout chip for BTeV” D. Christian, et al. NIMA 473:152-156, 2001.
- “PreFPIX2: Core architecture and results” J. Hoff, et al. IEEE Trans.Nucl.Sci. 48:485-292, 2001.