Abstract Listing

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PLENARY 2347: Towards a Detector Control System for the ATLAS Pixel Detector

S. Kersten, K.H. Becks, M. Imhäuser, P. Kind, P. Mättig, J. Schultes, University of Wuppertal, Germany

Topic Selection: *Systems aspects for particle physics experiments - mechanics, cooling, power and control systems (200)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The innermost part of the ATLAS experiment at the LHC, CERN, will be a pixel detector consisting of ca. 1750 individual detector modules. The high power density of the electronics, the harsh radiation environment and the inaccessibility over long terms are the specific constraints to the design of the detector control system (DCS). Selection and development of adequate hardware components as well as efficient software strategies are required to guarantee the safety of the detector and to support a reliable operation during data taking. The various building blocks of the pixel DCS will be described. Following the recommendations for the LHC experiments we have started to implement the Supervisory, Control And Data Acquisition (SCADA) system for the pixel detector using the PVSS commercial software product. We report about the status of the software developments and how the complexity of the various detector components can be mapped onto the SCADA system.

[pb] PLENARY 2359: Design and realization of a Rad-Hard 0.25 micron chip for High Energy Physics data acquisition system

A. Gabrielli, D. Falchieri, E. Gandolfi, University of Bologna, Italy

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The paper explains the design and the realization of a small size digital Rad-Hard chip submitted at a CERN multi-project run on November 2001. The design is a part of the Large Hadron Collider (LHC) A Large Ion Collider Experiment (ALICE) experiment at CERN and, particularly, is a device oriented to a electronic front-end board for the Inner Tracking System (ITS) data acquisition. The chip has been designed in VHDL language and implemented in 0.25 micron CMOS 3-metal Rad-Hard CERN v1.0.2 digital library. It is composed of 10k gates, 84 I/O pads out of the 100 total pads, it is clocked at 40MHz, it is pad-limited and the whole die area is 4x4 mm2. The chip has been implemented using CERN library 0.25 µm CMOS technology employing radiation tolerant layout. CARLOS2 is our prototype tailored to fit in the ALICE ITS readout architecture. Taking into account that the CERN 0.25 µm library contains a small number of standard cells and they are not so well characterized as commercial ones, it has been decided to try and test first the new design flow and the new technology.

The chip has been sent to the foundry in November 2001 and has been tested starting from February 2002. A specific PCB has been designed for the test task; it contains the connectors for probing the ASIC with a pattern generator and a logic state analyzer. The chip is inserted on the PCB using a ZIF socket. This allowed us to test 20 packaged samples out of the total amount of bare chips we have had from the foundry. The test phase has shown that 12 out of 20 chips under test work well. It is planned to redesign a new version of the chip by adding extra features such as a 2-dimensional compression logic.

[pb] PLENARY 2364: The Token Bit Manager for CMS Pixel Readout

E. Bartz for CMS, Rutgers University, USA

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

An intelligent coordinator for the readout of groupings of pixel readout chips, the Token Bit Manager (TBM), has been developed for the CMS experiment at LHC. To guarantee readout synchronization, the TBM needs to be located as close as possible to the readout chips. This forces developing this electronics in a rad-hard process. Test results from the first submission in DMILL will be presented. Also discussed will be the translation into quarter micron technology.

Implied by its name, the Token Bit Manager will coordinate passing of the readout token around a group of from 4 to 16 readout chips. In addition it supplies the optical readout to the DAQ with a header and trailer record to facilitate event recognition by the data acquisition ADC. Details of the architectural design as well as various performance measurements will be presented.

Also present on the same rad-hard chip is a slow-controls network hub, implemented with a modified I2C protocol, which provides command structures and parameter modifications for the TBM itself as well as for all readout chips. Modifications to the standard I2C bus used in the hub will be shown. The procedure and timing constraints for setting and refreshing some 30M pixel trim settings will also be presented.

[pb] PLENARY 2366: Reworking of indium bump bonded pixel detectors

A. Airoldi[1], G. Alimonti[2], M. Amati[1], A. Bulgheroni[1], M. Caccia[1], D. Giugni[2], F. Tomasi[2], [1] Universita' dell'Insubria, Italy, [2] INFN Milano, Italy

Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Yield maximization in multichip hybrid pixel sensors is a crucial issue in large volume productions planned for future High Energy Physics experiments. Bump bonding process optimization can guarantee statistical single bump failure rates at the acceptable level of 10-100 ppm; nevertheless, sytematic effects connected to process repeatibility can affect the functionality of a full chip in a module to a much larger extent. Because of this, the reversibility of the bonding procedure has been

investigated. A feasibility study on single chip assemblies for the ATLAS experiments has been succesfully completed, proving on a test beam the possibility of reworking. As a result of it, a dedicated facility has been conceptually designed, engineered and commissioned. The characteristics of the facility in terms of motion, temperature and tensile strength control are outlined in the talk, together with the main results.

[pb] PLENARY 2368: Localised Feedback in Silicon Avalanche Photodiodes

A. Khodin, V. Zalessky, T. Leonova, V. Kovalevsky, Institute of Electronics, National Academy of Sciences of Belarus, Belarus

Topic Selection: *Photon detection in particle, nuclear and astroparticle physics (195)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Avalanche photodiode structures with wide-bandgap (WBG) barrier based on epitaxial silicon layers of 4 to 20 micrometers thickness with a single p-n-junction, as well as with additional doping to modify electric field profile in the active layer were studied. To optimise avalanche multiplication and current transport processes in silicon avalanche photodiodes (APD) with built-in distributed negative feedback provided by WBG for detector coupled with short-wavelength photons scintillator, the physical model taking into account charge transport mechanisms in WBG layer has been developed. Based on self-consistent solution of current transport equation in the local avalanche multiplication mode, the APD output photoelectric characteristics have been calculated depending on the active layer doping and WBG layer current transport parameters.

The experimental structures been fabricated were designed to reach the regime of slowly fluctuating avalanche process. This process takes place in over-critical non-stationary electric field conditions. To reduce the lateral spreading of current filaments, the nanostructuring of wide-bandgap layer has been proposed. The nanostructured WBG layer includes semiconductor nanoclusters between which electrons may tunnel to reach the field electrode. Thus, additional localisation of every separate avalanche region (filament) is provided.

[pb] PLENARY 2370: The read-out system of the ALICE pixel detector

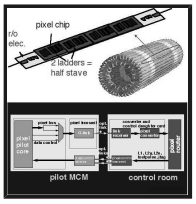
A. Kluge for ALICE SPD Project, CERN, Switzerland

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The on-detector electronics of the ALICE silicon pixel detector includes 1200 front-end ASICs, bump-bonded to silicon sensor ladders. 5 pixel chips, mounted on a front-end bus, constitute a half-stave. The complete detector consists of 120 half-staves on two layers (see illustration). The timing, control and readout of each half-stave are done by a PILOT ASIC, mounted on a MCM together with opto-electronic transceivers. The MCM is connected to three optical fibres. The fibres carry, respectively: the incoming 40 MHz clock, the incoming trigger and configuration data, the outgoing status and readout data. The on-detector chips have been designed in a commercial 0.25 micron

CMOS technology using radiation hardening layout techniques. The PILOT ASIC converts the incoming clock, serial trigger and serial JTAG signals into control signals for the pixel chips. The PILOT forwards the configuration data to the pixel chips, to the GOL, and to an auxiliary analog chip containing DACs that generate reference voltage and current levels. The PILOT ASIC initiates the readout of the pixel chips, converts data levels from GTL to CMOS, reformats the data stream and forwards the data to a serialiser ASIC (named GOL) that includes a driver for the laser diode transmitter. Data are sent to the control room on a fibre at 800Mb/s rate using the G-link protocol (see block digram). In the control room VME-based electronics performs zero-suppression and data encoding. This paper describes the pixel read-out system and reports on the status.



[pb] PLENARY 2375: X-ray Detector For Crystallography and Small Animal Imaging

P. delpierre[1], J.F. Berar[2], L. Blanquart[3], N. Boudet[2], P. Breugnon[1], B. Caillot[4], J.C. Clemens[1], I. Koudobine[1], C. Mouget[2], R. Potheau[1], I. Valin[5], [1] Centre de Physique des Particules de Marseille, France, [2] ESRF, France, [3] LBNL, USA, [4] Laboratoire de Cristallographie/CNRS, France, [5] Institut de Recherche Subatomique, France

Topic Selection: *Biomedical applications (194)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Prototypes of photon counting pixel detectors for crystallography have been produced. The aim is to build high dynamic range and fast readout cameras to fully exploit the performances of the high luminosity synchrotron X-ray sources.

A fast photon counting readout chip (XPAD-1) has already been produced and modules of 6.4 cm2 were built. Scattering images were done but some defects (failure of threshold adjusting) were observed. To correct these defects, a new version (XPAD-2) of this chip has been produced and we present test results. New sensors have also been produced to reduce the size of the contact pads and then to optimize the noise and the photon counting rate for the X-ray application. The pixel size is still 330 x 330 µm2 which is close to the size of the X-ray source and avoid a too large number of channels for large surface. Modules of 4 x 1.6 cm2 and 6 x 0.8 cm2 with XPAD-2 are at the final stage of fabrication. We are planning to make tests and scattering images in an X-ray beam (ESRF, Grenoble). Prototypes of readout and memory boards have been developed to store 128 images with a speed of less than 25 µs/image (for 6.4 cm2). These boards can be linked directly to a PC but also via an Ethernet network. So these detector prototypes include the entire environment necessary for an X-ray experiment from the photon input to the PC. The main effort was the production of full modules working, rather than the best performances for a restricted number of pixels. The long modules are designed to build 36 cm2 plates for crystallography but also to test the feasibility of a CT-scanner to be associated with a micro-PET for small animal imaging.

[pb] PLENARY 2378: Pixel readout electronics developement for an hybrid silicon pixel array gamma camera with on-chip energy discrimination system

V. Cencelli[1], F. De Notaristefani[1], G. Masini[2], L. Colace[2], C. D'Ambrosio[3], [1] INFN, Italy, [2] Universita' degli Studi di Roma Tre, [3] CERN, Switzerland

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

In recent years, we have demonstrated an Imaging Silicon Pixel Array camera, based on the Omega 3 chip developed at CERN. The system could take advantage of the features of Omega 3, but was limited by the nature of the readout electronics, specifically developed for High Energy Physics (HEP). In fact, the particle flow in gamma cameras for medical applications is very different from the one found in HEP experiments. The nature of particle flow is asynchronous being generated by the natural decay of the radio-pharmaceutical tracer and a large background is present due to natural radioactivity, cosmic rays and Compton emission from other organs. This takes the overall count rates in the hundreds of kHz range, while the signal rate of emission from the radio-pharmaceutical in the examined organ stays well below 1 kHz. Discrimination between total energy events and noise can be made by measurement of photon energy

In this contribution we present a novel IC designed to match the requirements of this specific application: the chip consists of an array of 32 x 96 pixel cells, 150 x 150 um each. Single cells are equipped with a front-end preamplifier, pulse shaper and discriminator with locally programmable threshold. A leakage current compensation scheme and six bits configuration register are also integrated. Generation of trigger for array readout is performed by a dedicated on-chip discriminator which compares the current collected by all the cells with externally programmable thresholds. The chip is designed in the UMC 0.25 um technology available trough Europractice.

[pb] PLENARY 2387: New Results from the ALICE Silicon Pixel Detector

P. Riedler for ALICE SPD Project, CERN, Switzerland

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The ALICE silicon pixel detector (SPD) consists of 1200 ALICE pixel readout chips produced in a commercial 0.25 micron CMOS process. Each chip contains 8192 readout cells, leading to an overall 9.8 million readout channels in the whole SPD. The sensors are matrices of p+n-diodes produced on 200 microns thick silicon. Each detector ladder is bump bonded to 5 readout chips. An assembly of 4 ladders, thus 20 chips, then forms one stave of the SPD. 60 staves are mounted on a carbon fibre support in a two-layer barrel configuration. The readout chip has been extensively characterised. A mean noise of about 120 electrons rms and a threshold variation of about 100 electrons rms were observed before individual threshold adjust. Wafer probing results indicate chip yields in excess of

30-50%. First results from radioactive source measurements (90Sr, 109Cd) on full size bump-bonded ladders are presented. Furthermore results from several beam tests carried out at the CERN SPS are shown. The system performance during the tests is in good agreement with the ALICE detector requirements.

[pb] PLENARY 2392: X-ray scatter-to-primary ratio versus thickness, two analytic models evaluated against monte carlo calculations

J.E. Tkaczyk, General Electric Research, USA

Topic Selection: *Photon detection in particle, nuclear and astroparticle physics (195)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

An exact calculation of scatter can be expressed formally by a transport equation;[1] however, the exact solution is not generally known even for the simplest geometries. Two analytic approaches to scatter modeling, one by Swank [2] and another by Smith and Kruger [3] are tested against the results of Monte Carlo calculations using GEANT4. By treating parameters in the analytic equations as fitting parameters, one obtains a convenient way to parameterize measured data. The comparison to Monte Carlo results allows a match of parameters appearing in the analytic expressions to the physical parameters in the transport theory. Specifically, mono-energetic photons having single absorption and scatter cross-sections are studied. The two analytic approaches, although of very different derivation, yield similar expressions that capture the overall magnitude, the thickness dependence and photon energy dependence of the scatter-to-primary ratio.

[1] A. Ishimaru, Wave Propagation and Scattering in Random Media, Academic Press, Inc. N.Y. 1978; S. Chandrasekhar, Radiative Transfer, Dover Pub. N.Y. 1960. [2] R.K. Swank, Appl. Optics, 12, 1865 (1973). [3] S.W. Smith and R.A. Kruger, Med. Phys. 13, 831 (1986).

[pb] PLENARY 2394: Studies on ATLAS pixel modules

F. Hügging for ATLAS Pixel, Universtity of Bonn, Germany

Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The basic building unit of the ATLAS pixel detector is a module consisting of 2x6 cm^2 n+-n silicon pixel sensor with 46080 pixel cells bump bonded to 16 readout chips. These FE-Chips are connected to a module control chip (MCC) through wire-bonds to a 4-layer flex hybrid circuit glued to thebackside of the sensor. Further connection to the off-module electronics, optical data transmission and power supplies is done via a pigtail using twisted pair microcables and low mass power cables. The operation as innermost tracking detector near the primary vertex inside ATLAS Innerdetector requires long term reliability, mechanical stability and thermal compliance together with a low material budget, radiation tolerance and high production yield. Full size prototype modules has been assembled during the last years using different types of sensors, readout chips, flex hybrid circuits and interconnection schemes to the pigtail and to microcables. The so build modules have shown to

fulfil the demanding requirements of the ATLAS experiment. Different aspects like thermal robustness, readout with microcables through the complete opto- link, and different power schemes have studied in detail in laboratory and testbeam measurements. Results of these tests and experiences of the module assembly process will be presented and discussed.

[pb] PLENARY 2395: Active pixel sensor architectures in standard CMOS technology for charged-particle detection

D. Passeri[1], P. Placidi[1], L. Verducci[1], G.U. Pignatel[1], P. Ciampolini[2], G. Matrella[2], G.M. Bilei[3], [1] University of Perugia, Italy, [2] University of Parma, Italy, [3] I.N.F.N, Italy

Topic Selection: *Sensors (196)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The adoption of active pixel sensors (APS) has been recently proposed for charged-particle detection purposes. Very good performances have been obtained, in particular by exploiting some peculiar features of the actual fabrication technology. In this work, we extend such an approach toward advanced VLSI CMOS technologies with the aim of increasing spatial resolution and optimizing the pixel-level response by exploiting state-of-the-art microelectronics devices. To this purpose, extensive CAD-based analyses have been carried out, investigating dependencies on actual technology features. In particular, different technological nodes (0.35, 0.25 and 0.18 μm), coming from different silicon foundries (Alcatel, IBM, UMC) have been taken into account. Device, circuit and mixed-mode simulations have been performed, accounting for the effects of several technology and design options. Steady-state characteristics and transient response to a particle hit have been predicted and correlated to major design parameters and to environmental conditions.

With respect to the standard APS read-out scheme, a few different circuit architectures have been evaluated, more tailored for the detection of single hits, and allowing for a simplification and a potential speed-up of the overall read-out system. In particular, different configurations and bias regimes of the buffering transistors have been evaluated. The obtained results provide useful hints for the selection of optimal read-out electronics architecture and suggest that innovative detectors, featuring high resolution and noise immunity, can actually be fabricated by using strictly standard CMOS technology.

[pb] PLENARY 2396: Sensor developement for the CMS pixel detector

T. Rohe for CMS pixel collaboration, Paul Scherrer Institut, Switzerland

Topic Selection: *Sensors (196)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The CMS pixel detector will be located in a very hostile environment close to the interaction point. In order to keep the largest (and most expensive) layers operational for the complete LHC's runtime of 10 years, all components including the sensors have to withstand a particle fluence of at least $6*10^{14}$ 1MeV neutron equiv./cm^2. As this requires a partially depleted operation of the silicon sensors after irradiation induced type inversion of the substrate an "n in n" approach was chosen.

Further the size of the CMS pixel detector exceeds with an area of about one square meter covered by roughly 800 detector modules the previous pixel projects by an order of magnitude. Therefore special attention has to be paid to yield optimization at all production steps. This requires a fault tolerant design of all components and effective testing possibilities before and during assembly.

In order to perform IV-tests which are very sensitive most kinds of damage already prior to bump bonding a highly resistive connection between the pixels was implemented. Depending on the n-side isolation technique either openings in the p-stop isolation rings or in case of p-spray isolation by a punch through bias grid was used.

In April 2002 sensor prototypes containing numerous design options of both isolation types have been received and carefully tested using typical IV and CV-methods. Some of the sensors were irradiated and afterwards bump boned to readout chips of the type PSI30. This chip delivers an analog signal without zero suppression and is therefore suitable for noise studies. Laboratory and test beam measurements with these ensembles are presented and the different design options are compared.

[pb] **PLENARY 2397: Studies on MCM-D connection structures**

P. Gerlach for ATLAS, K.-.H. Becks for ATLAS, C. Grah for ATLAS, P. Mättig for ATLAS, Univ. of Wuppertal, Germany

Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

In the upcoming ATLAS experiment at LHC at CERN a large pixel detector with about 10^8 channels will be the innermost part of the tracking system. During the development of this detector a new technology for building the necessary interconnections in such a hybrid detector concept has been investigated: the Multi Chip Module Deposited technology. This technology is based on a dielectic (Benzocyclobutene) and copper, which are deposited alternately. The sensor is used as the substrate for the 4+4 layer structure with an overall thickness of 40µm.

The recent investigations focussed on yield expectation studies, the high voltage isolation properties of the dielectric and integration of passive components in the multilayer system.

Besides this, MCM-D offers also the possibility of connecting not adjacent sensor and electronic pixel cells. This leads to the option of building so called "equal sized" or even "equal sized bricked" pixel detector devices, where the uniformity of sensor cell size is 100% in both cases, even in the interchip regions of a detector module. Pushing the technology to its actual limits, bricking of pixel cells becomes possible, increasing the double hit resolution of such a device by a factor of two.

We will give a progress report about the recent investigations and present measurements of these new "equal sized (bricked)" single chip hybrids.

[pb] PLENARY 2398: Pixel Detector Module for the BTeV Experiment at Fermilab

S. Zimmermann, J. Andresen, J.A. Appel, G. Cardoso, G. Chiodini, D.C. Christian, B.K. Hall, J. Hoff, S.W. Kwan, A. Mekkaoui, M.A. Turqueti, R. Yarema, Fermi National Accelerator Laboratory, USA

Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

At Fermilab, a pixel detector multichip module is being developed for the BTeV experiment. The module is composed of three layers. The lowest layer is formed by the readout ICs. The back of the ICs are in thermal contact with the supporting structure while the other side is bump-bonded to the pixel sensor. A low mass flex-circuit interconnect is glued on the top of this assembly, and the readout IC wire-bounded to the flex circuit. All the communication with the DAQ system is done using differential signals over copper cables. This paper will present recent results of the development of the module prototype.

[pb] PLENARY 2399: CVD Diamond Pixel Detector Development

R. Stone, J. Doroshenko, T. Koeth, L. Perera, S. Schentzer, S. Worm, Rutgers University, USA

Topic Selection: *Sensors (196)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Pixel detectors using synthetic diamond are an attractive alternative to silicon for use in radiation harsh environments such as at the LHC. Recent beamtest results using CMS pixel readout electronics are presented which demonstrate a hit efficiency of 94% and position resolution of 31 microns for a diamond pixel sensor with 125 micron X 125 micron pitch.

In order for diamond pixel detectors to be used at the LHC, it is necessary that close to 100% hit efficiency be demonstrated using radiation hard electronics developed for LHC pixel detectors. In addition, the spatial resolution of diamond pixel detectors due to charge sharing from both inclined tracks and from Lorentz drift in a magnetic field should be comparable to that for silicon pixels. We have initiated a series of studies to measure the hit efficiency and spatial resolution of diamond pixel detectors. We present here recent measurements made at beamtests at CERN using diamond pixel detectors with rad-hard CMS pixel electronics.

We have recently received new diamond material which shows an increase in the amount of signal charge on bench tests. We can anticipate an improvement in hit efficiency and perhaps spatial resolution in the next series of beamtests starting in late 2002. With side-by-side tests with equivalent silicon pixel detectors, we hope to demonstrate diamond pixel detectors close to or meeting LHC vertex detector requirements by early 2003.

[pb] PLENARY 2401: The Readout architecture of the ATLAS Pixel System

R. Beccherle, P. Morettini, INFN - Genova, Italy

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The Readout architecture of the ATLAS Pixel Detector is split into three levels: Front-end chip (FE), Module Controller Chip (MCC) and off-detector electronics. The talk will describe the overall architecture and dataflow with emphasis on role and performance of the MCC.

[pb] PLENARY 2402: Test beam results of ATLAS Pixel Sensors

A. Andreazza, T. Lari, C. Meroni, F. Ragusa, C. Troncon, INFN and University of Milano, Italy

Topic Selection: *Sensors (196)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Full prototypes of the ATLAS Pixel Detector and test structures constisting of oxygenated silicon sensors equipped with rad-hard electronics have been tested in a hadron beam at the CERN H8 line. Their performances have been evaluated before and after irradiation, with fluences up to 10^{15} 1 MeV neq/cm^2. In this report the results on charge collection, efficiency and resolution and their impact on the detector operation are discussed.

[pb] PLENARY 2403: Front-end pixel chips for tracking in ALICE and particle identification in LHCb

K. wyllie for ALICE ITS & LHCb RICH, CERN, Switzerland

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

Front-end pixel readout chips have been designed for use in the ALICE inner tracking system and the LHCb ring-imaging Cherenkov detector. The architecture of the chip will be described in detail, together with results on characterisation of the analog and digital circuitry. The first version of the chip meets the ALICE requirements but not those of LHCb, and the necessary improvements incorporated in a second version will be outlined together with discussion of the subsequent measurements.

[pb] PLENARY 2406: Multi-element Si sensor with readout ASICs for EXAFS spectroscopy at NSLS

G. De Geronimo, R. Beuttenmuller, A. Kuczewski, Z. Li, P. O'Connor, P. Siddons, BNL, USA

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

A new detector for EXAFS spectroscopy at NSLS of BNL is being developed. It is based on a multi-element Si sensor and dedicated readout ASICs. The sensor is composed of 384 pixels, each having a 1mm x 1mm area, arranged in four quadrants of 12 x 8 elements and it was produced at the Instrumentation Division of BNL. In this first version each pixel is bonded to an input pad of the front-end electronics. Each ASIC is composed of 32 readout channels, each implementing: low noise preamplification with continuous reset that self-adapts to the pixel leakage current; high order shaper with settable peaking time (0.5μs, 1μs, 2μs, 4μs) and settable gain (750mV/fC, 1500mV/fC); band-gap referenced output baseline with stabilization (BLH) for high rate operation; one threshold comparator and two window comparators, each followed by a 24-bit counter; four 6-bit DACs for fine window adjustment; analog output and pixel leakage current monitors. The ASIC include SPI compatible interface for settings, masking, and counters readout. It was designed at the Instrumentation Division, fabricated in 0.35μm CMOS and is composed of over 180,000 MOSFETs, dissipating about 8mW per channel. First measurements show at room temperature a pixel capacitance of 0.8pF, a pixel leakage current of 60pA, a resolution at 2μs peaking time of 14 rms electrons without the detector and of 40 rms electrons (340eV) with the detector connected and biased. Cooling at –10C a FWHM of 265eV (235eV contributed from the electronics) was measured at the Mn-Kα peak. A resolution below 300eV is expected to apply for rates in excess of 100kcps per channel, with an overall rate capability in excess of 40MHz on a sensitive area of about 400mm².

[pb] PLENARY 2407: The DMILL readout chip for the CMS pixel detector

W. Erdmann for CMS[1], R. Horisberger for CMS[2], R. Schnyder for CMS[2], G. Dietrich for CMS[2], B. Meier for CMS[1], M. Barbero for CMS[3], H.C. Kaestli for CMS[2], [1] ETH Zuerich, Switzerland, [2] PSI, Switzerland, [3] University of Basel

Topic Selection: *Integrated circuit electronics (197)* ***Preferred Presentation Format:*** *Oral Invited*

Abstract

The readout chip for the CMS pixel detector has been implemented in the radiation hard DMILL process.

It is designed to read out the analog pulse height information of 150μm square silicon pixels. An array of 52x53 pixels is implemented on the chip area of 8mm x 10mm. A column drain architecture is used to meet the requirements of data rates and a pipelined trigger in CMS. The chip includes a fast serial interface for configuration and on-chip voltage regulators.

Chips with sensors will be tested in a high rate pion beam at PSI with conditions equivalent to full luminosity LHC running and results will be shown.

[pb] PLENARY 2408: Development of an Active Pixel Sensor Vertex Detector

H.S. Matis[1], F. Bieser[1], G. Rai[1], F. Retiere[1], H.H. Wieman[1], E. Yamamoto[1], S. Kleinfelder[2], H. Bichsel[3], [1] Lawrence Berkeley National Laboratory, USA, [2] University of California, Irvine, USA, [3] University of Washington, USA

Topic Selection: *Sensors (196)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

There is much interest in ultra-relativistic heavy ion physics to measure open charm. With a high-resolution inner vertex detector, charmed particles can be measured.

Active Pixel Sensor (APS) technology, which has been pioneered [1] by the LEPSI group in Strasbourg, has shown that this CMOS process is very promising for a vertex detector. As APS technology is in its infancy, many outstanding issues must be resolved. We have been exploring its suitability for use at the Relativistic Heavy Ion Collider in BNL.

We have fabricated and tested 2 generations of APS chips. The first consists of an array of 128 by 128 pixels with 20 µm pixels divided into four quadrants. Each quadrant uses a different sensor structure and/or readout circuit. The second-generation design has the same geometry but it has 16 different test structures.

The first version was tested in a 1.5 GeV electron beam. To eliminate the noise introduced by resetting the chip, we analyzed the data using the correlated double sampling method. Assuming that all of the energy deposition is in the 8 µm epitaxial layer of the chip, we had good agreement with the calculated [2] energy loss distribution. Measurements with Fe^{55} will be presented as well as radiation hardness tests with a low energy proton beam.

We also have investigated the mechanical properties of an APS detector. We will present results on supports and cooling options for achieving a very thin detector, and we will discuss thermal tests on these structures.

1. R. Turchetta et al., Nucl. Instrum. and Methods A **458**, 8 (2001).

2.H. Bichsel, Rev. Mod. Phys **60**, 663 (1988).

[pb] **PLENARY 2409: The CMS Pixel Detector Project**

R. Horisberger for CMS, PSI, Switzerland

Topic Selection: *Invited Talk (199)* ***Preferred Presentation Format:*** *Oral Invited*

Abstract

The status of the CMS pixel detector is presented. An emphasis will be given to the current develoment of the mechanics, cooling and hybridisation of the detector.

[pb] PLENARY 2422: A Low Mass, Low Profile Interconnect for the ATLAS Pixel Detector Modules

Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Invited*

Abstract

[pb] PLENARY 2423: A Low Mass, Low Profile Interconnect for the ATLAS Pixel Detector Modules

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Topic Selection: *Hybridization (bump bonding, MCM-D, interconnections) (198)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The ATLAS Pixel detector presents many unique challenges for building modules. With over 50k channels, these modules require a more complex interconnection scheme than is typical of Si strip detectors. They are also required to operate in a high radiation environment for up to ten years and must introduce a minimum amount of material. Although the ATLAS Pixel detector modules use sparse readout electronics, there is still a requirement for hundreds of connections between the sixteen front end readout chips and the Module Control Chip (MCC), which provides multiplexing, coding and decoding of control and data signals. Further, the 150 micron pitch of the bond pads for the module electronics presents fabrication challenges for the hybrid. In order to meet these requirements, flexible printed circuit board technology has been chosen. We describe the specification, design, layout and construction of a flexible hybrid that meets the electrical, mechanical, reliability and other constraints of the ATLAS Pixel detector for both prototype and production modules.

[pb] PLENARY 2425: BTeV Silicon Pixel Detector Integration Issues

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Topic Selection: *Systems aspects for particle physics experiments - mechanics, cooling, power and control systems (200)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

The BTeV silicon pixel detector contains thirty planar stations that reside inside the beamline vacuum close to the beam. The detector sits within the analysis magnet. The location of the detector leads to unique designs for the mechanical support, RF shielding, flex-cable feedthrough, and vacuum system.

The design considerations and development status are presented.

[pb] **PLENARY 2485: Pixel hybrid photon detector developments for the RICH counters of LHCb**

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Topic Selection: *Photon detection in particle, nuclear and astroparticle physics (195)* ***Preferred Presentation Format:*** *Oral Contributed*

Abstract

We report on the ongoing work towards a hybrid photon detector with encapsulated silicon pixel detector and readout chip for the ring imaging Cherenkov detectors of the LHCb experiment at the Large Hadron Collider at CERN. The photon detector is based on an electrostatically-focussed image intensifier tube geometry where the image is de-magnified by a factor of ~5. The anode consists of a silicon pixel array, bump-bonded to a binary readout chip with matching pixel electronics. The preparation, tests and performance of full-scale (72:18 mm) prototypes encapsulating the ALICE1LHCB chip are presented. Experimental results are compared with the LHCb baseline specifications for the tube efficiency at detecting single photo-electrons. This efficiency is governed by the combined effects of energy loss and back-scattering of the photo-electrons at the silicon detector surface, charge sharing at the pixel boundaries and the electronics performance of the readout chip, in particular its discriminator threshold. Technological aspects, related to the manufacturing and packaging of bump-bonded chip assemblies and to the tube processing, are summarized.

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