ATLAS Pixel Sensors

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Features of the Experiment	Impact on the Sensor Design
•10-year fluence @ innermost layer >10^{15} cm^{-2} ⟨1-MeV n⟩	Guarantee stable operation @ high voltage; operate below full depletion after inversion.
•1.4 x 10^8 channels (2228 sensors) plus spares; want to test these under bias before investing chips on each	Implement integrated bias circuit.
•All of the other subsystems located outside the pixels	Minimize multiple scattering; minimize mass.

Many of the sensors' detailed features follow from extensive study of radiation damage effects. Summarize those:

- 2 types of damage:
  - non-ionizing energy loss in the silicon bulk
  - ionization in the passivation layers
- Principal effects + impact on design:
  - change in dopant concentration leads to type inversion + increase in $V_{depletion}$
    - segment n-side to operate inverted sensor partially depleted
    - design for high operation voltage
  - increase in leakage current
    - cool sensor to avoid increase in noise, power consumption
  - decrease in charge collection efficiency
    - maintain good S/N; minimize capacitance

Total fluence predicted for each component's lifetime

Component	Lifetime (years)*	Maximum Fluence (x 10^{14} 1-MeV n/cm^2)
B-layer	5	10.44
Layer 1	10	6.64
Layer 2	10	4.00
Disk 1	10	3.92
Disk 2	10	3.76
Disk 3	10	3.76
Disk 4	10	3.68
Disk 5	10	3.60

*This assumes luminosity ramp-up from 10^{33}cm^{-2} to 10^{34}cm^{-2} during Years 1-3

Parameterize the effective dopant concentration N_{eff} to predict the depletion voltage as a function of temperature and time:

$$V_{dep} \propto |N_{eff}| = |N_a + N_c + N_Y|, \text{ where}$$

$$N_a = g_a \Phi \cdot \exp(-k_a t), \text{ “beneficial annealing”},$$

$$N_c = N_{eff,0} \cdot [1-\exp(-c\Phi)] + g_c \Phi, \text{ “stable damage”},$$

$$N_Y = g_Y \cdot \Phi \cdot [1-(1+k_{Y1} t)^{-1}], \text{ “reverse annealing”},$$

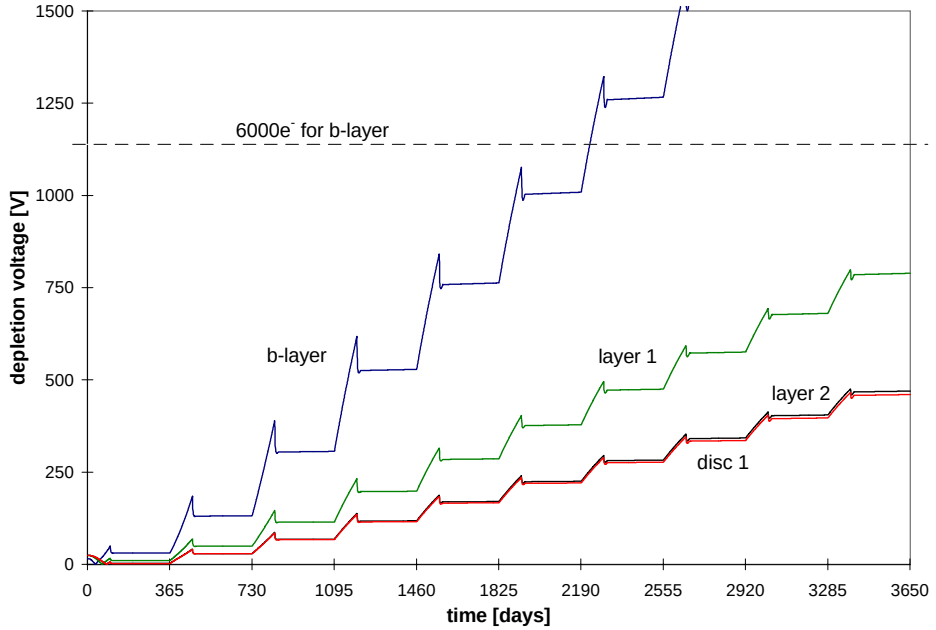
$$k_a = k_{0a} \cdot \exp(-E_{aa}/k_B T),$$

$$k_{Y1} = k_{0Y1} \cdot \exp(-E_{aY}/k_B T),$$

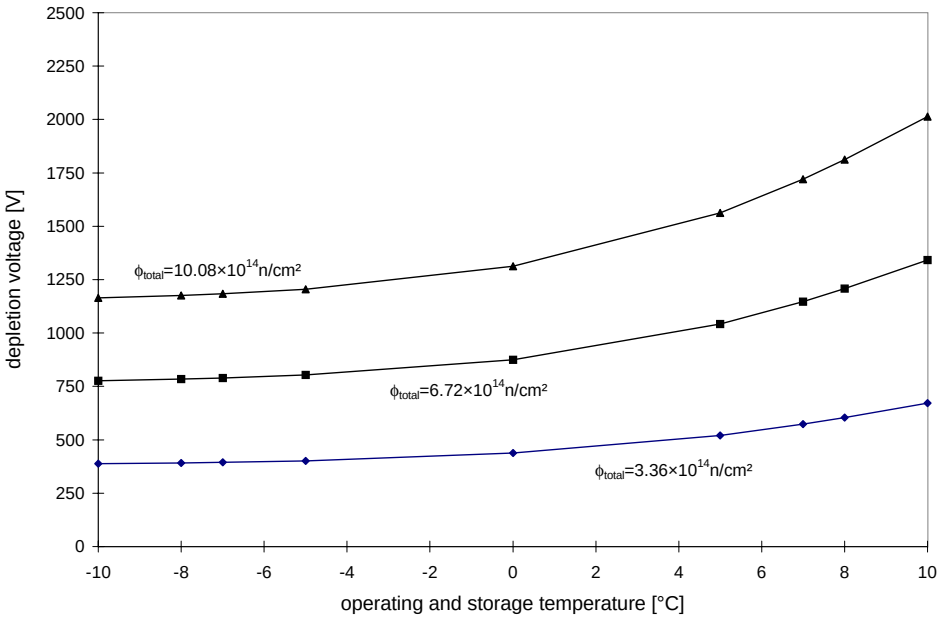
Φ is fluence, t is time, T is temperature, and

g_a, k_{0a}, E_{aa}, c, g_c, g_Y, k_{0Y1}, and E_{aY} are known parameters.

Use this to predict $V_{depletion}$ versus calendar time:



and to select operating and storage temperatures:



•Assuming Standard Access Procedure: 2 days @ 20°C + 14 days @ 17ºC

General Features of the Production Sensor Design

- Rectangular sensors:
  2 chips wide x 8 chips long -
  - Each chip: 24 columns x 160 rows
  - Each pixel cell: 50 x 300 μm^2
  - Active area: 16.4 x 60.4 mm^2
  - Overall dimensions depend on module design but will lie between (18.4 x 62.4 mm^2) and (21.4 x 67.8 mm^2).
- n^+ implants (dose $>10^{14}/cm^2$) in n-bulk to allow underdepleted operation after inversion
- Thickness:
  - 200 μm inner barrel
  - 250 μm outer 2 barrels + disks

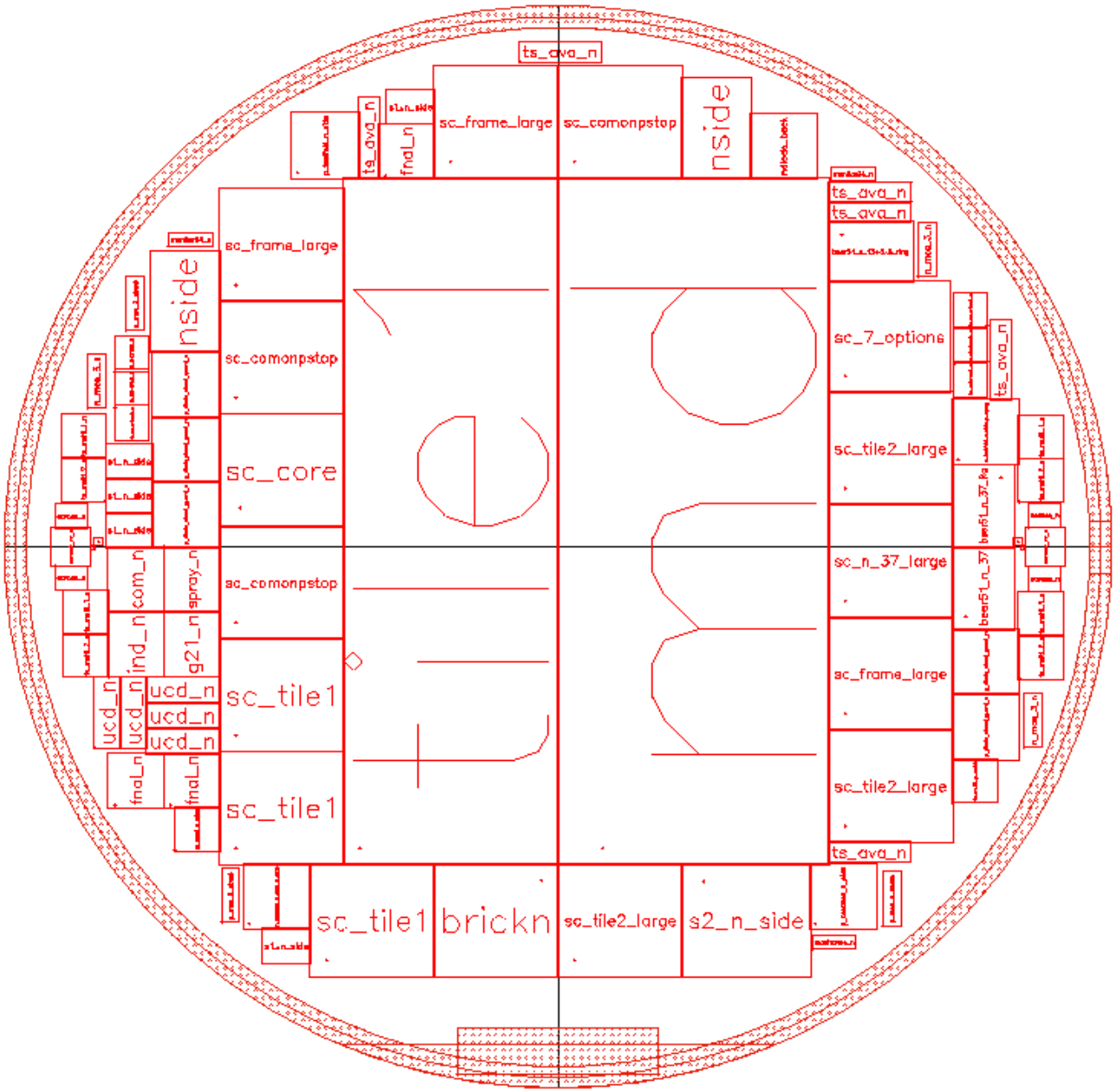
Route to a Detailed Design

- First Prototypes -
  - Designed in ‘97, fabricated by 2 vendors (CiS + Seiko), now under study
  - Each wafer contains
    - 2 designs for full-size sensors (“Tiles”) that can be assembled into (16-chip) modules
    - 17 “single-chip sized” sensors that examine variations
  - Response to rad damage is studied but not used as a rejection criterion against a vendor.
- Second Prototypes -
  - Now in design; to be ordered in April ‘99
- Pre-production Sensors -
  - To be designed and ordered in the first half of 2000.
- Production Sensors -
  - Must be ready to begin assembly in 2000.

The First Prototypes

4-inch wafers, 280 μm thick, with:

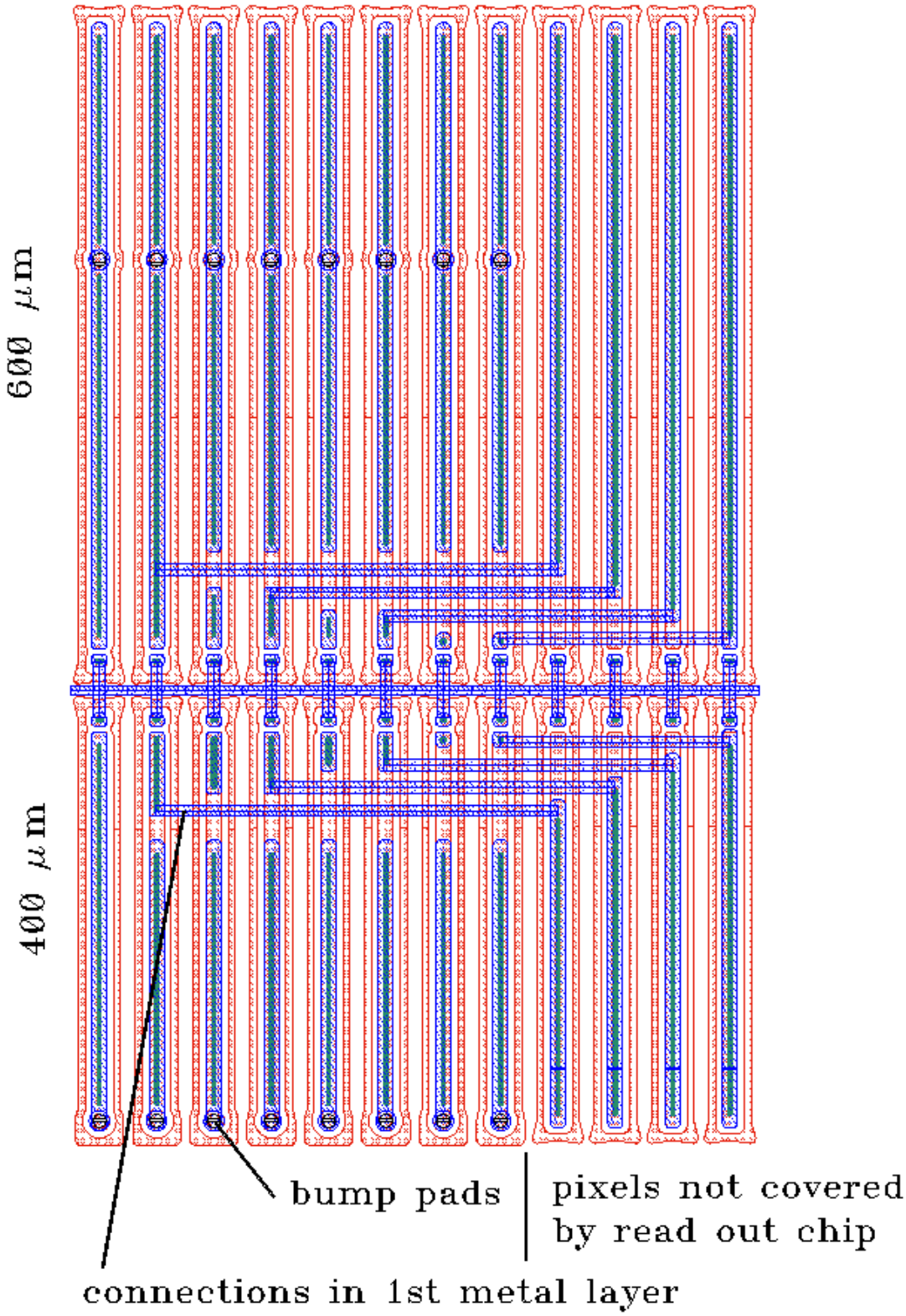
- 2 full-size Tiles
- 17 single-chip sensors
- various process test structures



Features of the Full-size Sensors ("Tiles")

- Pitch 50 x 400 μm^2 to match prototype (18 column x 160 row) electronics
- 47232 cells per sensor
- cells in regions between chips are either
  - elongated to 600 μm to reach the nearest chip, or
  - ganged by single metal to a nearby pixel that has direct R/O

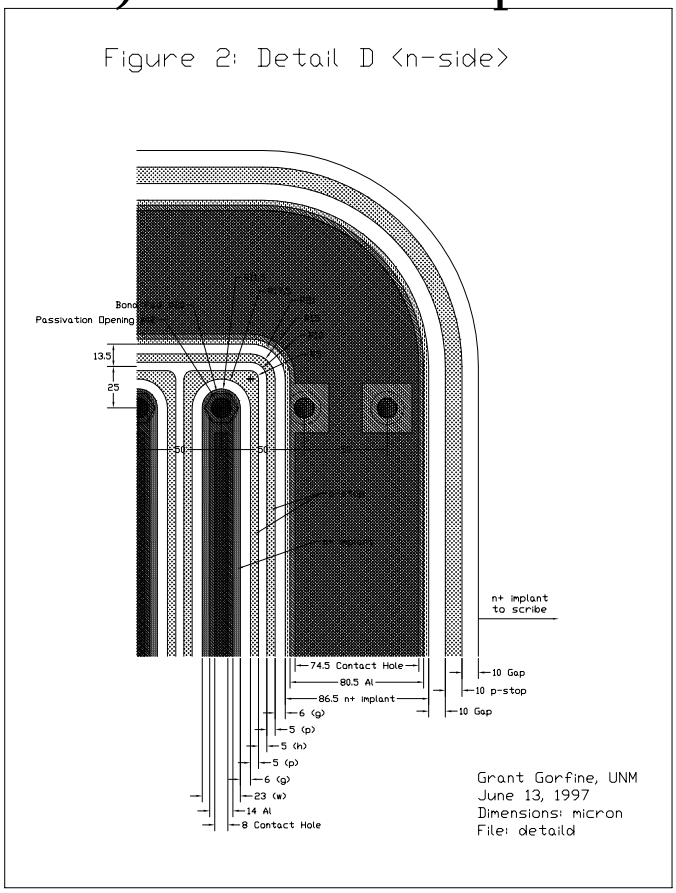
Elongation and Ganging of Implants in the Inter-chip Region



- n-side isolation

This is the principal difference between the 2 Tiles.

- Tile 1: “atoll” p-stops (implant dose $\geq 10^{13}/cm^2$) for low inter-pixel capacitance.



- Dimensions:
  - n^+ implant width - 23 μm
  - p-stop implant width - 5 μm
  - gap between n^+ and p^+ - 6 μm
  - gap between p-stops - 5 μm

– Tile 2: p-spray

A medium [(3.0 ± 0.5) x $10^{12}/cm^2$] dose implant is applied to the full n-side without masks, then overcompensated by the high dose pixel implants themselves.

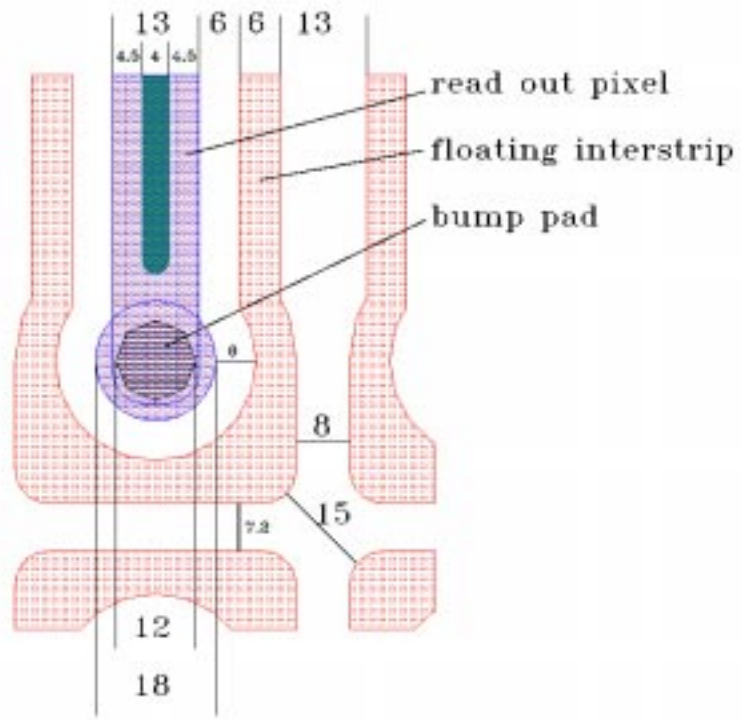
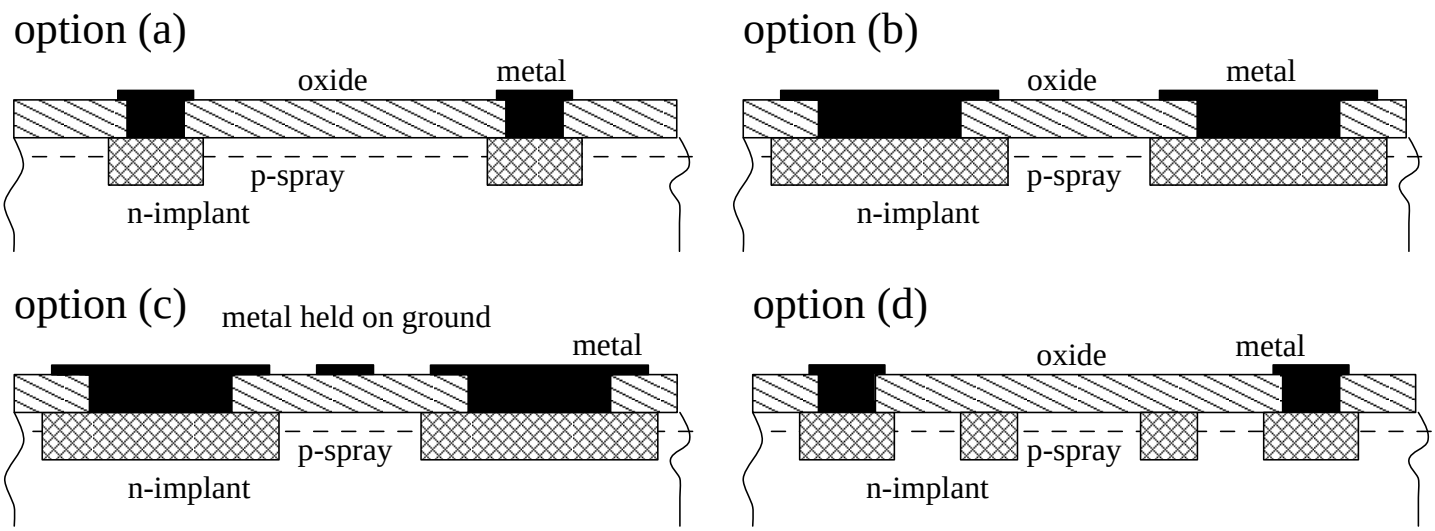


Figure 5, detail B

- Dimensions of structures:
  - n^+ implant width - 13 μm
  - floating n^+ ring width - 6 μm
- Purpose of the floating ring: to keep the distance between implants small (for low **E**) but maintain low capacitance between neighboring channels.

Simulations were undertaken to minimize capacitance and lateral **E**

4 design variations:



Option	Predicted Total Capacitance (fF)
a	162
b	261
c	363
d	128

Option (d) was utilized in the Tile 2 design.

The p-stops are a well-established technique among sensor manufacturers.

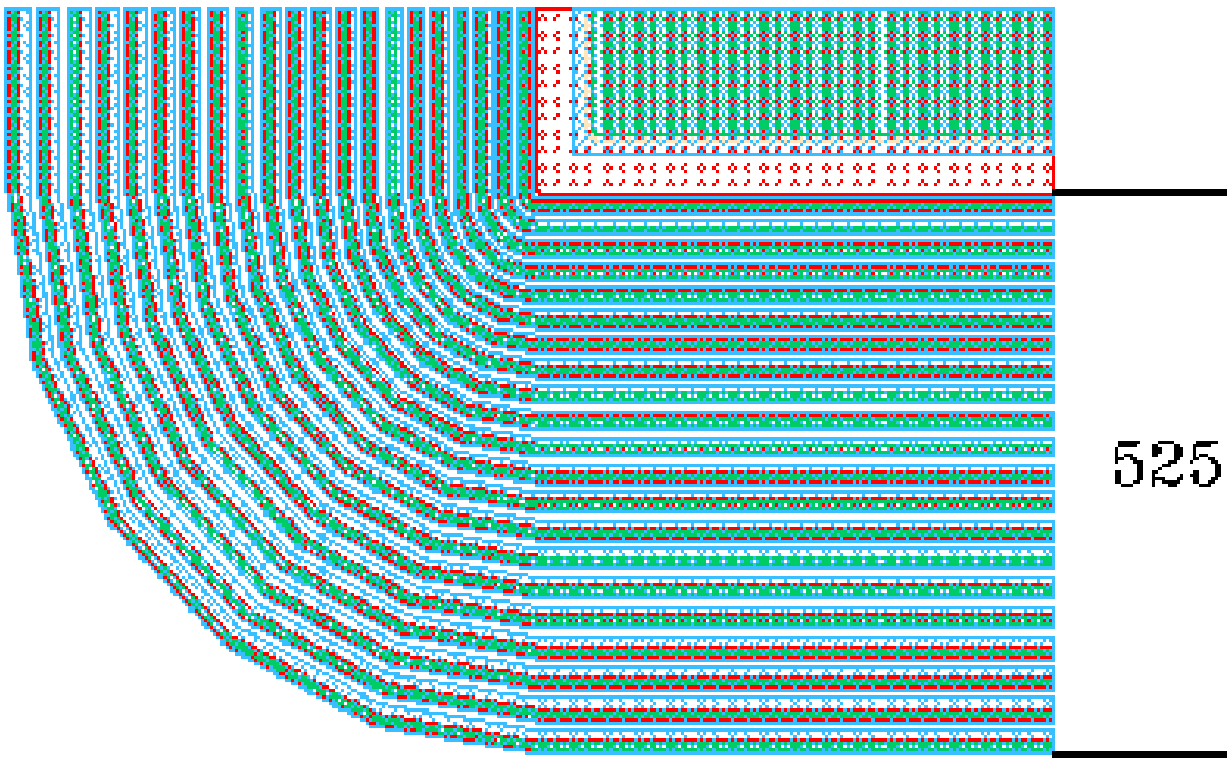
Benefits of p-spray:

•Reduces cost by eliminating a photolithographic step.

•Eliminates possibility of overlap of high dose n and high dose p in case of photolithographic failure or mask misalignment; permits smaller gaps between structures.

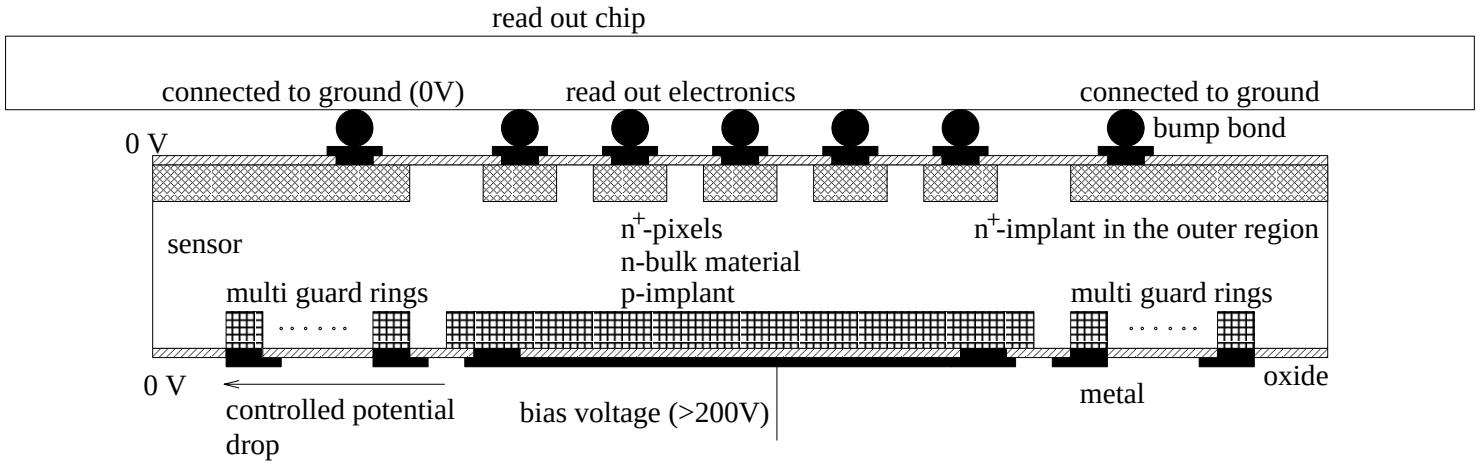
•p-spray is adjusted to the oxide charge saturation value so that as ionizing irradiation occurs, increasing oxide charge compensates the p-spray acceptors, reducing lateral **E** and so reducing microdischarge and increasing $V_{breakdown}$ throughout the sensor's lifetime.

- Guard ring / treatment of the edge
  - on the p-side: a 22-ring structure of 10 μm wide p^+ implants. Pitch increases with radius from 20 μm to 50 μm. Metal overlaps implant by 1/2 gap width on side facing active area. Total width = 525 μm. (See Bischoff, et al., NIM A 326 (1993) 27-37.)



– on the n-side: no conventional guard ring. Inner guard ring of ~90 μm width surrounded by a few micron gap. Region outside gap is implanted n^+ and grounded externally. On Tile 1, center 10 μm of gap is implanted p^+ for isolation.

Recall that the chip is only a bump's diameter away. This design guarantees no HV arc from n-side to chip.



- Double-metal
  - 30% of prototypes use double metal to
    - route ganged pixels in inter-chip region
    - prototype busses (on Tile 2 only) for module interconnect studies
  - Dimensions:
    - ≥10 μm wide
    - thicknesses:
      - Metal 2: 1.5-2.0 μm
      - Metal 1: 1.2-1.5 μm
    - minimum spacing - 20 μm
    - contact holes: 3 x 10 μm^2 in masks
    - SiO_2 or polyimide insulator
- As-cut dimensions

  To accommodate the busses, Tile 2 is wider than Tile 1:

  - Tile 1: 18.6 x 62.6 mm^2
  - Tile 2: 24.4 x 62.6 mm^2

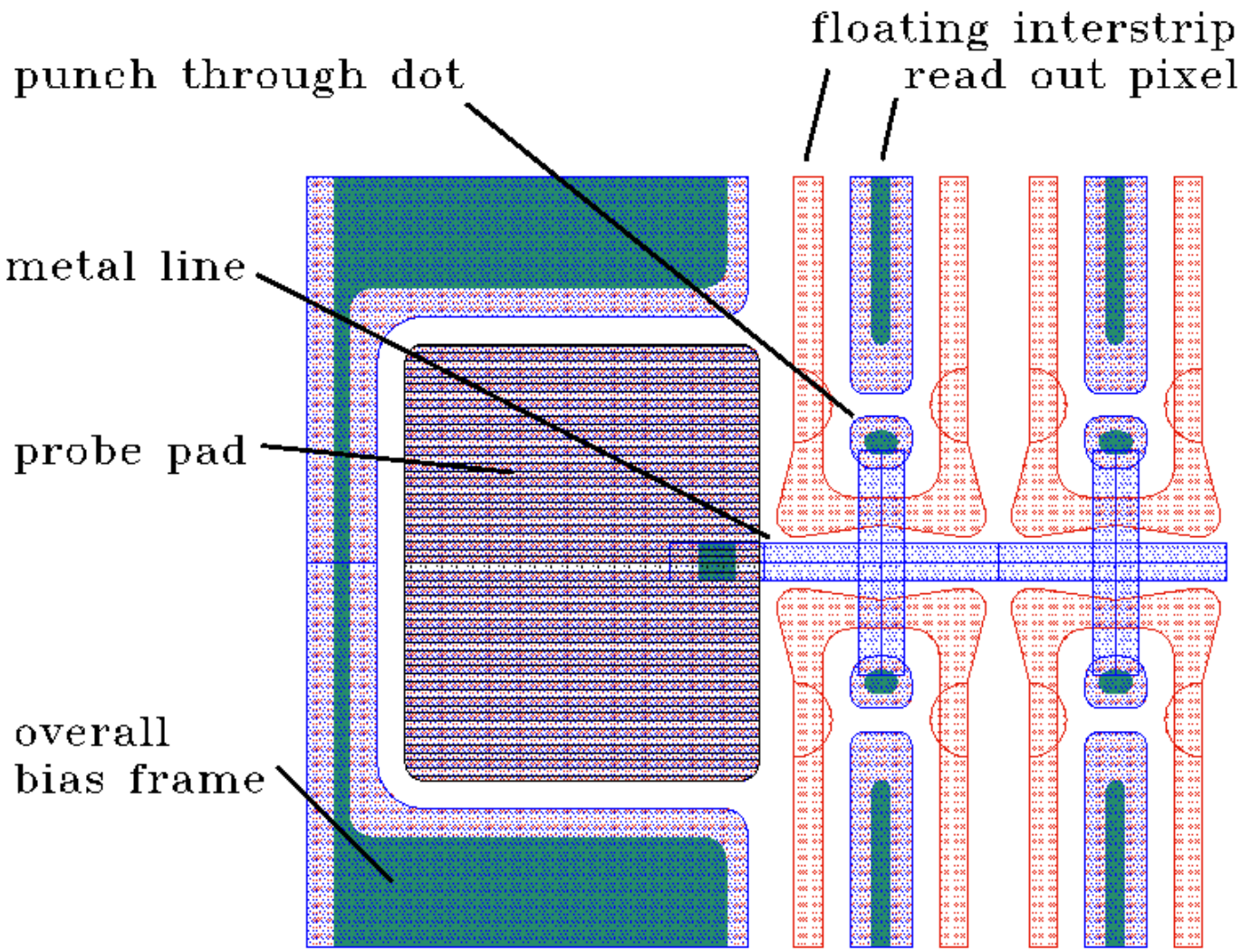
- Pads
  - 18 μm diameter circular bump pads with 12 μm diameter passivation openings
- Passivation
  - 1 μm thick silicon nitride
- Back side
  - p^+ implant (dose $>10^{14}/cm^2$)
  - 30 x 100 μm^2 apertures in metal below each pixel for stimulation by laser
- Metallization
  - 2 - 6 μm narrower than implant to avoid microdischarge

- Bias grid

For high yield on assembled modules, we want to test sensors prior to attaching chips - so we want to bias every channel on a test stand without a chip and without contacting implants directly. A bias grid is included on Tile 2:

- Bus between every pair of columns connects to small n^+ implant "dot" near each pixel
- When bias is applied (through a probe needle) to the grid, every pixel is biased by punchthrough from its dot.
- p-spray eliminates need for photolithographic registration, permits distance between n-implants to be small → low punchthrough voltage
- Bias grid unused after chips are attached but maintains any unconnected pixels (i.e., bad bumps) near ground
- Dot expected to sacrifice 0.8% of active area.

Bias Grid


floating interstrip
read out pixel
punch through dot
metal line
probe pad
overall
bias frame

- First Prototype electrical and mechanical requirements

  – thickness - 300 μm
  – thickness tolerance - ±10 μm
  – mask alignment tolerance - ±2 μm
  – initial depletion voltage - 50-150V
  – initial breakdown voltage - ≥ 200V
  – initial leakage current - < 100 nA/cm^2
  – initial oxide breakdown voltage - ≥ 100V
  – implant depth after processing - ≥ 1 μm

- Radiation hardness

Not required of the prototypes, but they are tested for it. Required of production sensors after 10^{15} p/cm^2

  - Breakdown voltage > 600V
  - Depletion voltage (normalized to 300 μm thickness) < 800V
  - Leakage current (@ -5 ºC and 600 V, after 1 month of annealing at 20 ºC) <25 nA per cell

Variations Studied on Single-chip Sensors

- Bricking - offset cells in neighboring rows by 1/2 length to
  - improve z-resolution on double hits
  - dilute cross talk coupling over 4 cells instead of 2
  - 3 geometries:
    - conventional bricking with single metal routing to preamps
    - conventional bricking with double metal routing to preamps
    - “partial bricking”
- Common p-stop
- p-stop + p-spray
- Geometrical variations on implants + metals

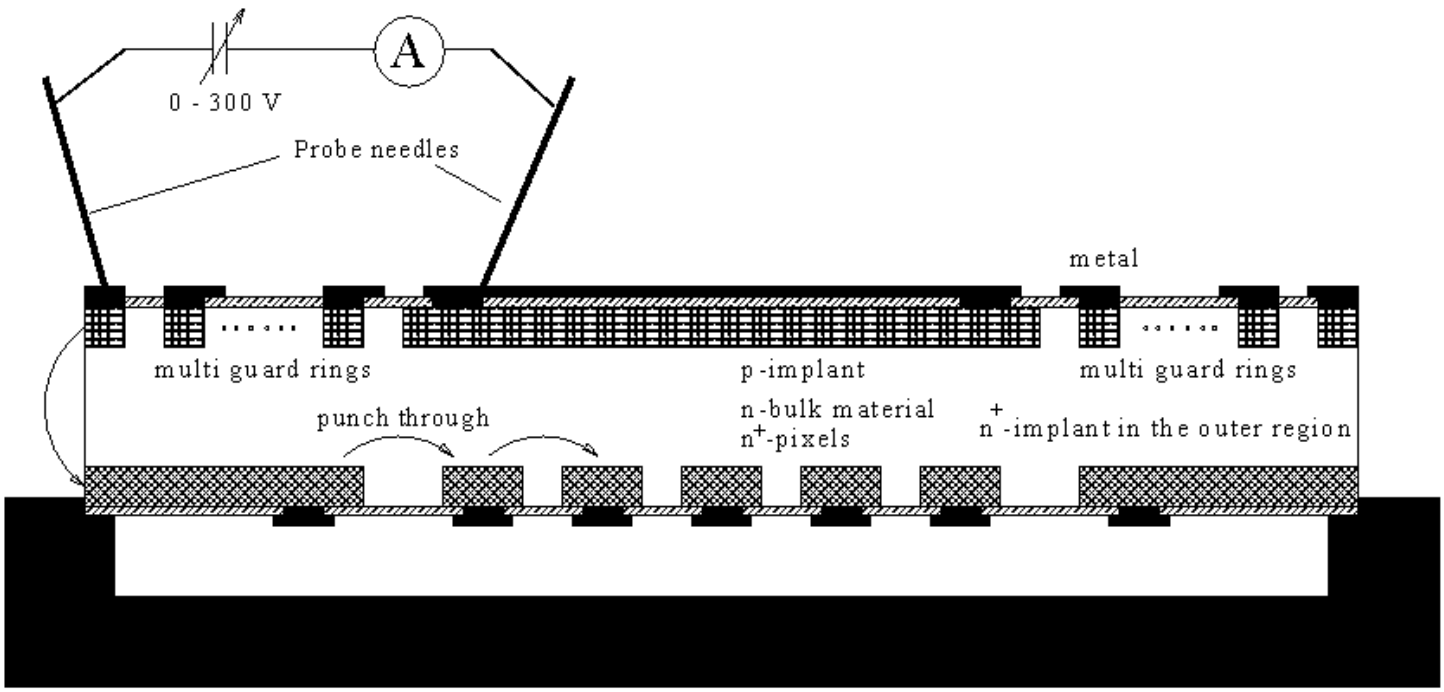
Organization of Pixel Sensor Design and Testing

- Design + testing of prototypes + test structures done entirely by ATLAS; GDS-2 files provided to vendors.
- 30 wafers were received in November 1997:
  - From CiS: 10 single-metal, 6 double-metal, 4 200-μm thick low-ρ mechanical
  - From Seiko: 7 single-metal, 3 double-metal
- Testing involves
  - static studies of irradiated + unirradiated, bumped + unbumped devices, and
  - test beam studies of sensors with amplifiers.

Testing Methods and Results

I-V characteristics are used to identify fabrication defects.

Set-up for unassembled sensors:



•n-side guard ring is contacted via the scribe line.

•Above full depletion, pixels are pinched off from guard ring; their current reaches the guard thermionically.

•The potential of each pixel depends on its distance either from the bias grid or from the guard ring.

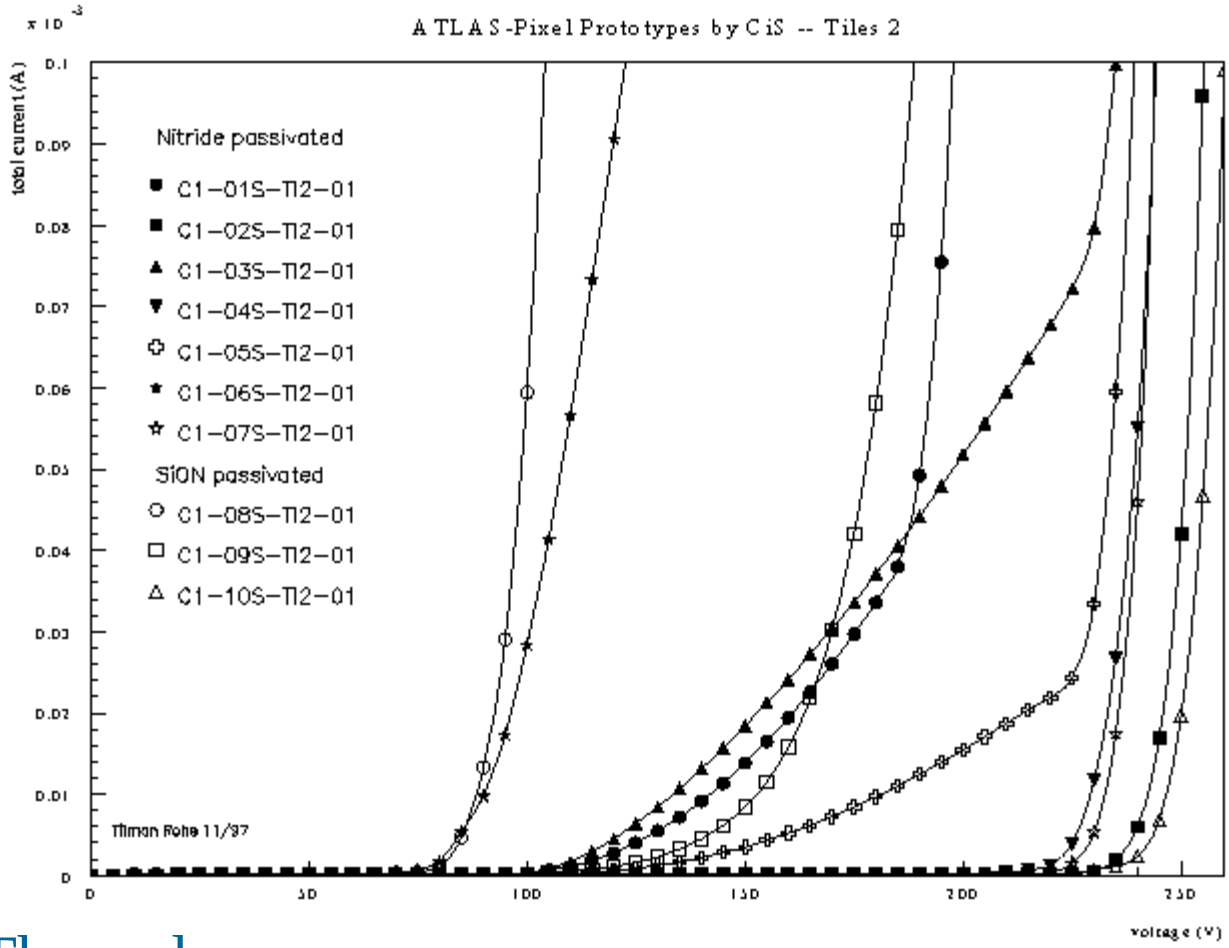
Measurements were made on devices from both vendors, for single-metal and double-metal:

- On new, unirradiated wafers
- After dicing
- After bumping
- After flipping
- After irradiation

...

Sample Results:

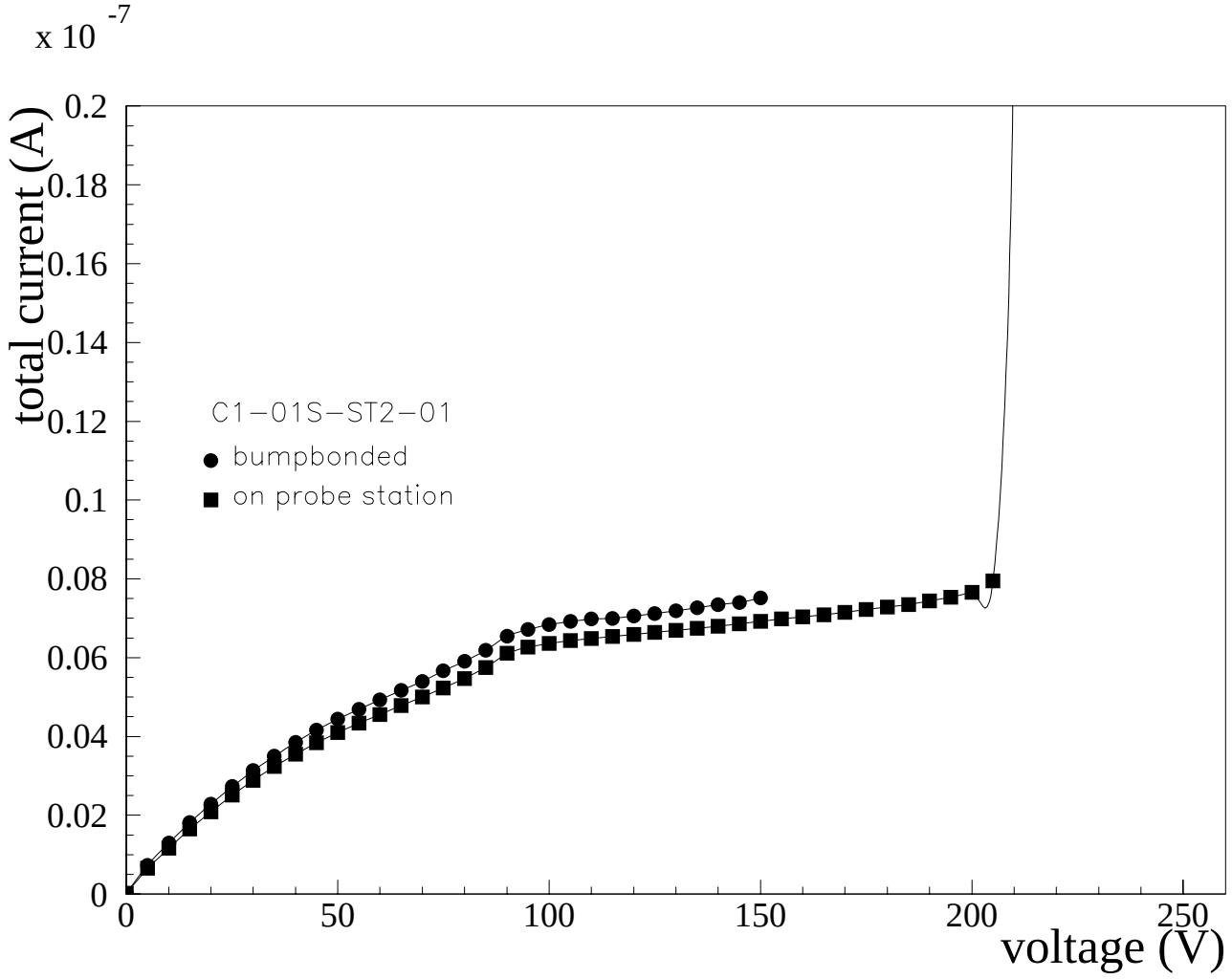
•I-V curves of Tile 2 sensors, before assembly:



Three classes:

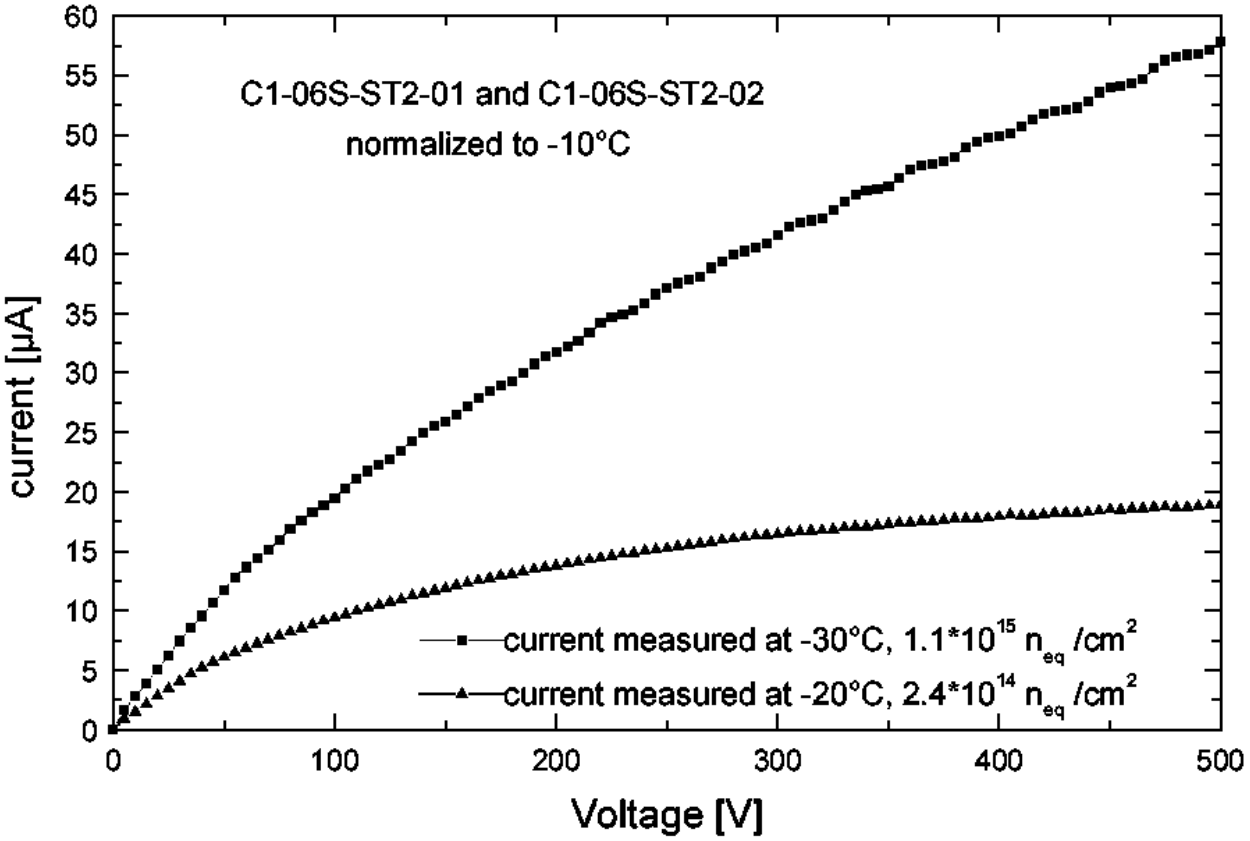
- •Sensors with no significant current rise above full depletion
- •Sensors with small but acceptable current rise above full depletion
- •Sensors which break down below full depletion

•I-V curves of Tile 2-like single-chip sensors, before and after bumping and flipping

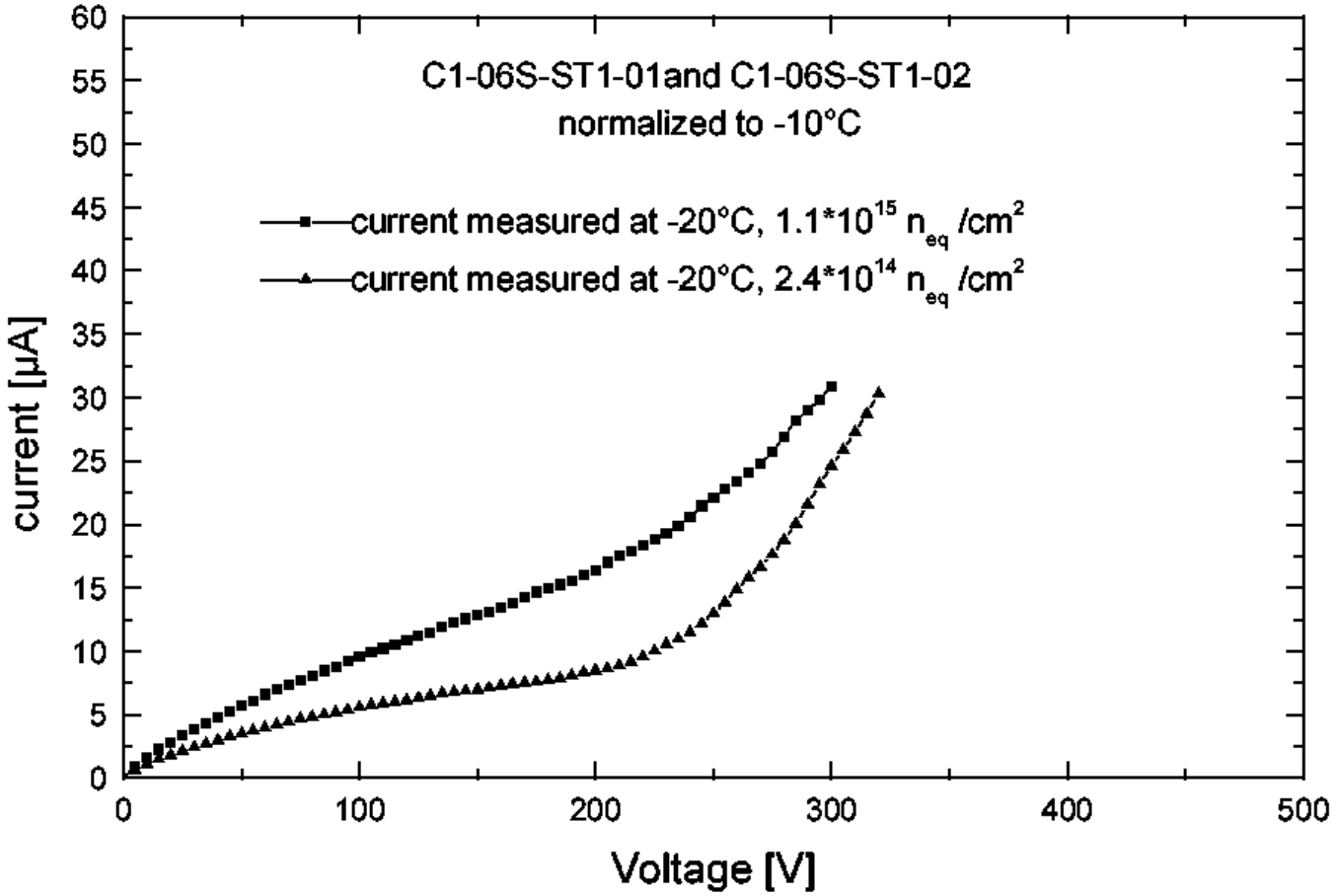


- I-V characteristics before and after irradiation
  - consistent results with protons at LBNL and pions at PSI
  - results obtained at different temperatures are normalized to -10°C

  Sample results for Tile 2-like single-chip sensors -

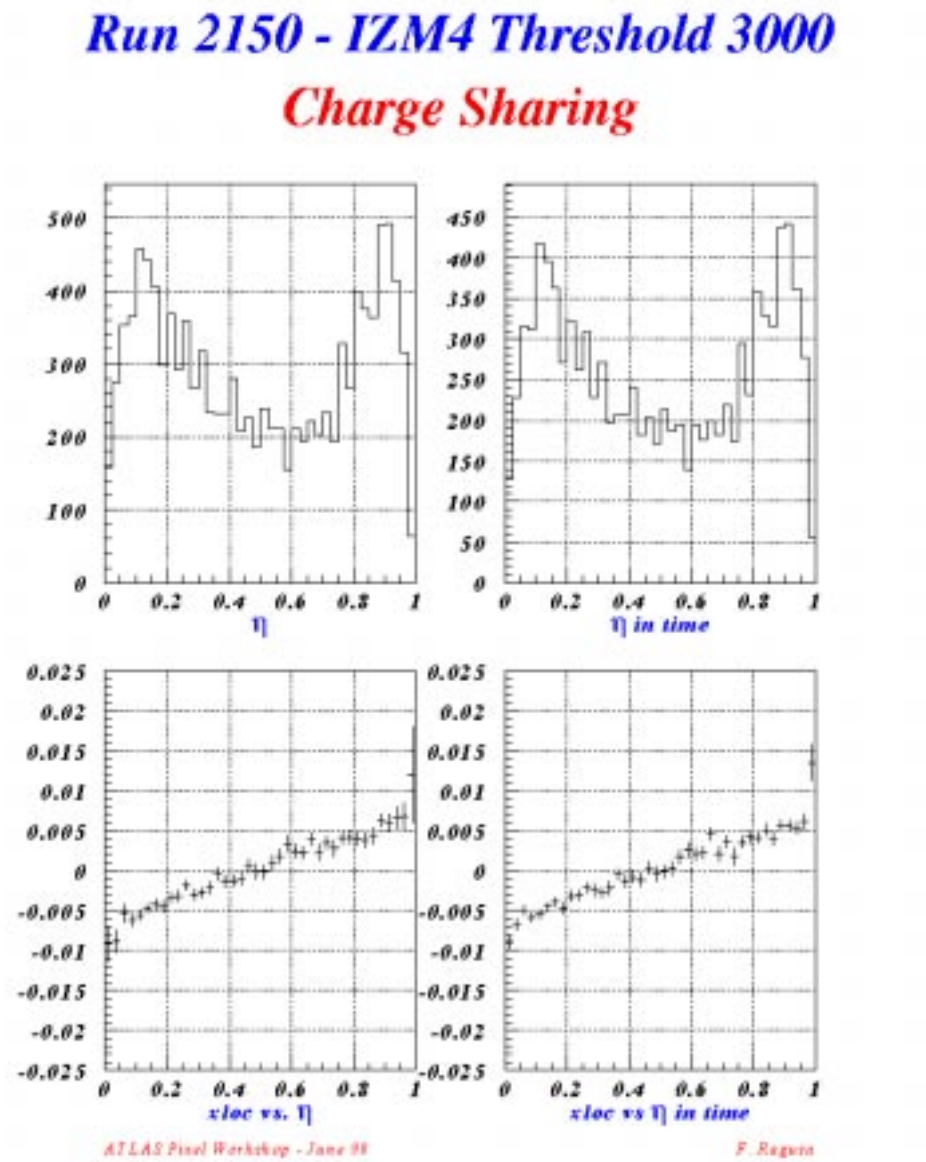


Sample results for Tile 1-like single chip sensors:



Sample Results from Testbeam Studies of Unirradiated Detectors

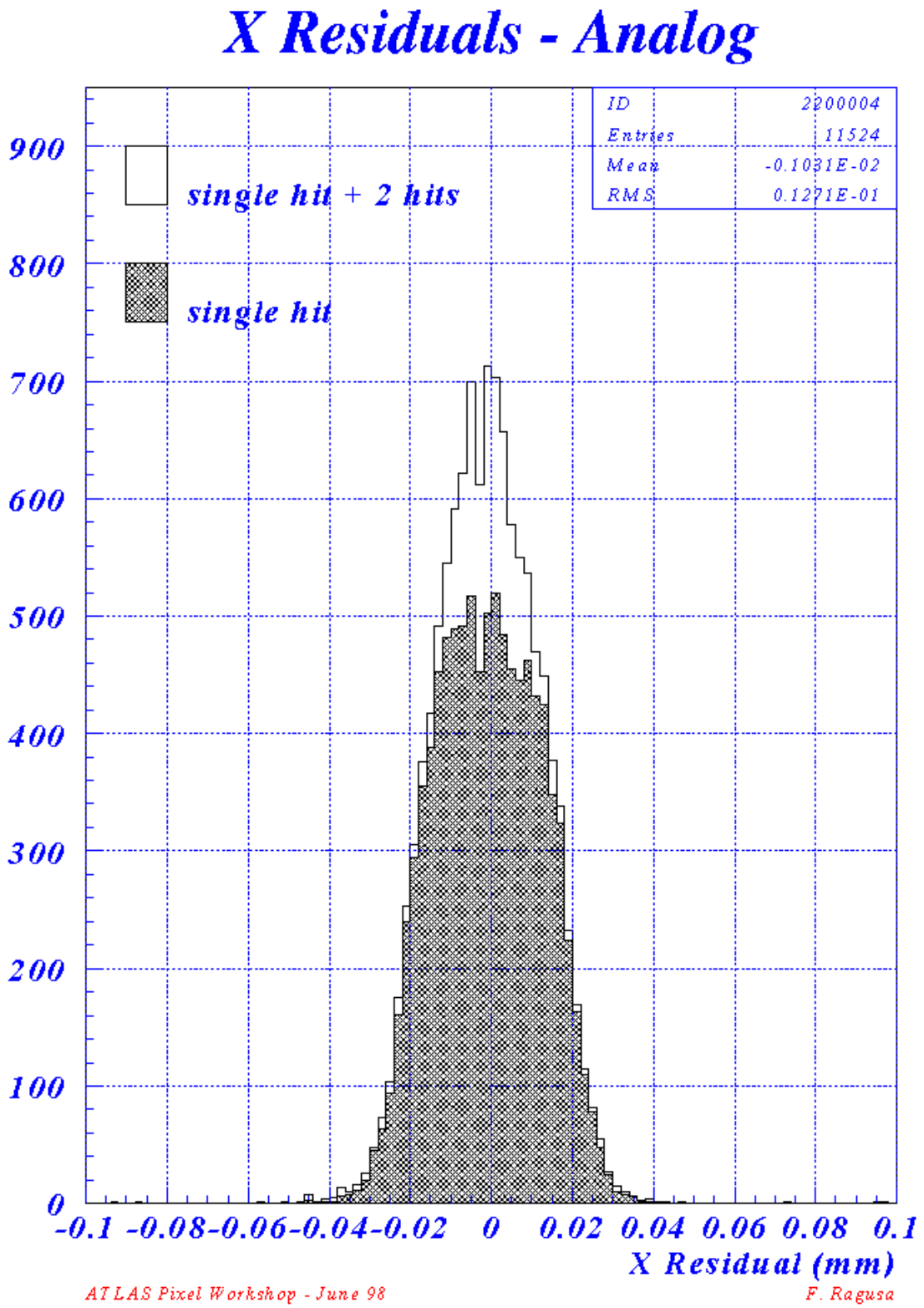
Charge Sharing occurs within ±7μm of the pixel edge:



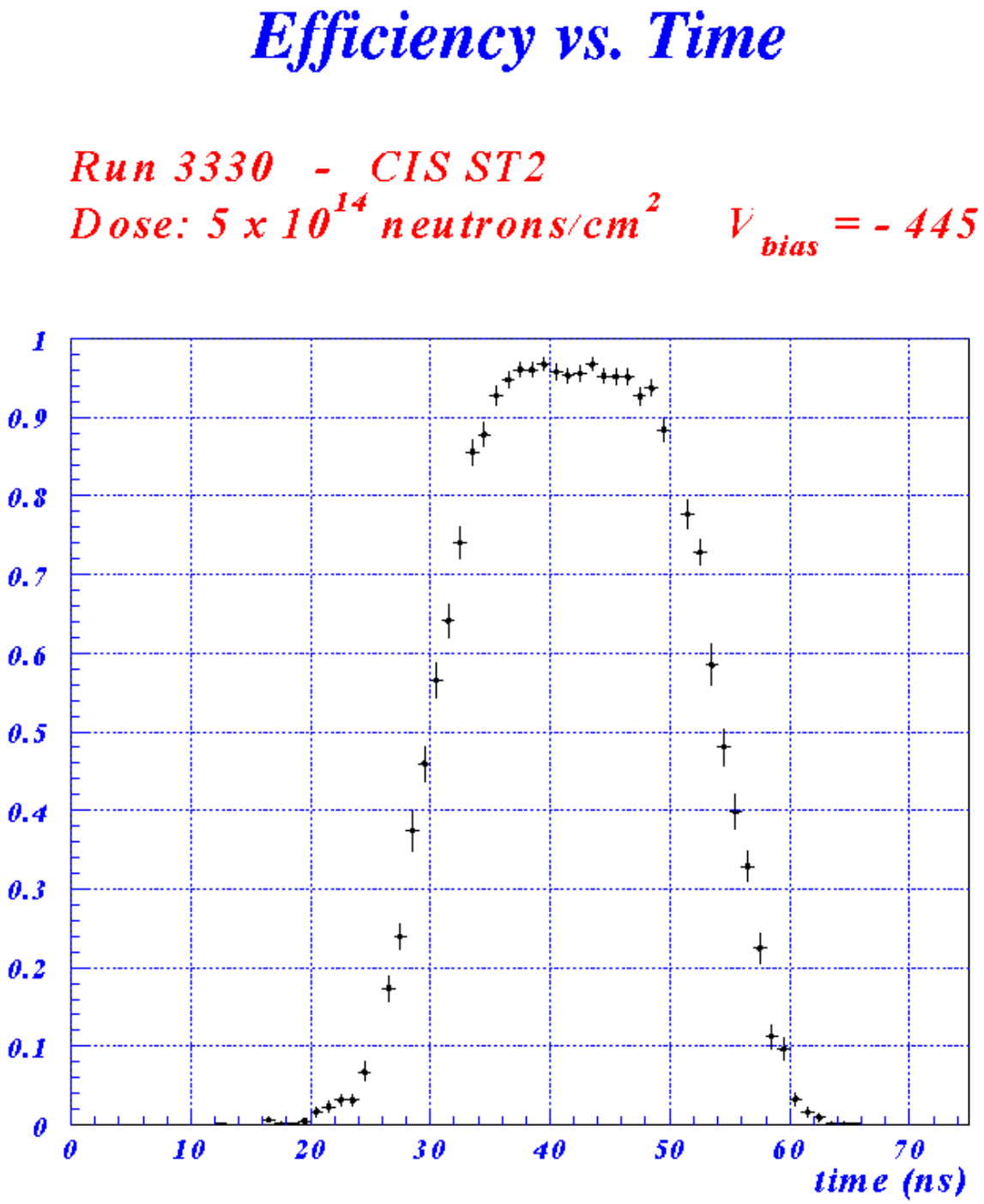
•XLOC is position relative to the interface between 2 pixels

•η = (ToT of the rightmost pixel in a pair) / (ToT of the pair) for 2-pixel clusters

Spatial Resolution Using Time over Threshold Information: 12.8 µm, including extrapolation error; 11.2 µm, deconvoluted.



Sample Results from Testbeam Studies of Irradiated Detectors:



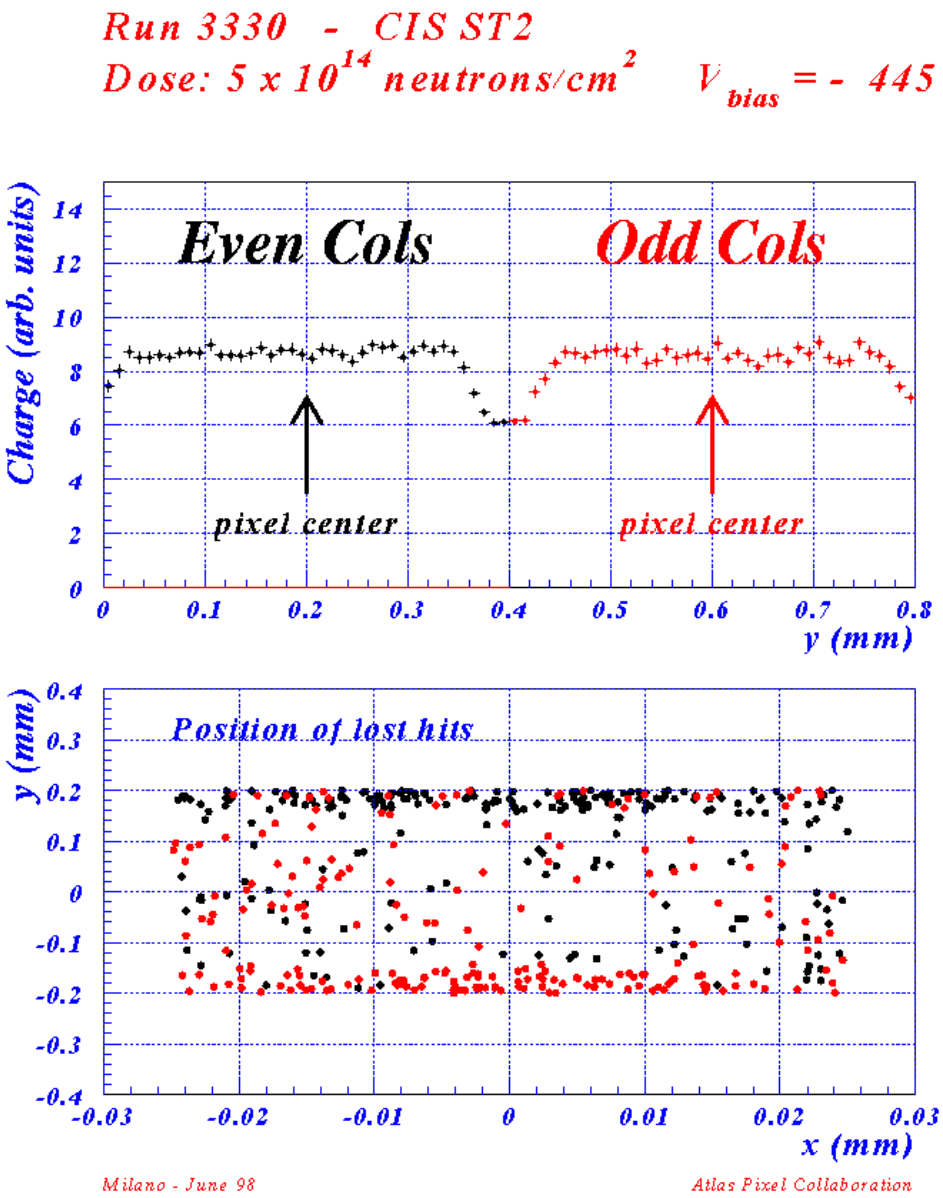
- Tile 2 type sensor
- Efficiency = 95.8% for high bias

Efficiency versus bias voltage, for an irradiated sensor, compared to results for unirradiated sensors.

Efficiency Summary (%)

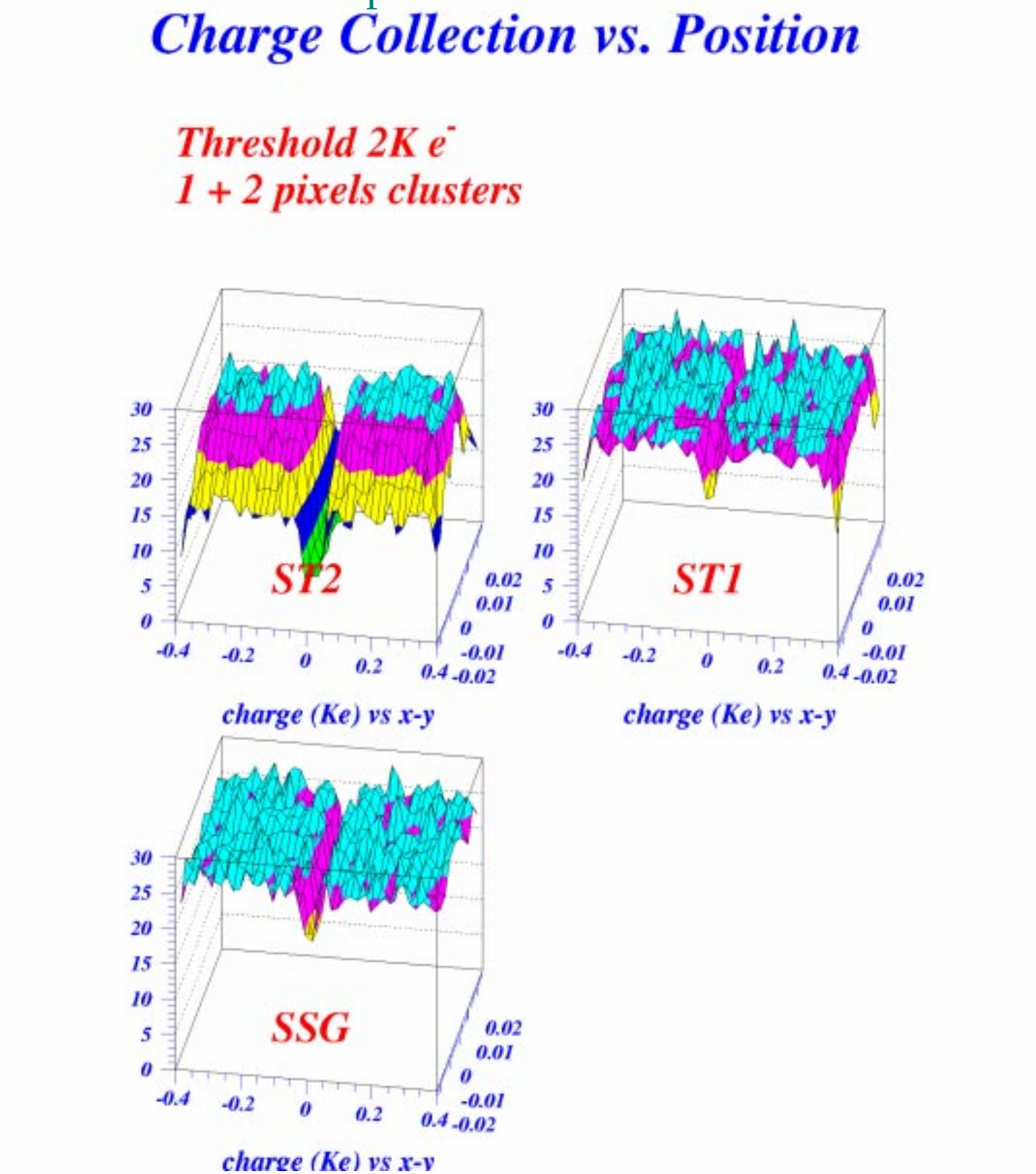
	Dose: 5 x 10^{14} neutrons/cm^2					No Dose
	3342 CIS T2 −65 V	3341 CIS T2 −125 V	3336 CIS T2 −250 V	3343 CIS T2 −399 V	3330 CIS T2 −445	3286 T2 −150 V
1 hit	43.0	62.8	88.0	88.1	89.8	86.7
2 hits	0.5	0.8	3.0	6.5	6.0	12.1
eff.	43.5	63.6	91.0	94.6	95.8	98.8
0 hits	54.7	34.6	7.2	4.7	3.4	0.6
1/BX+1	0.4	0.6	1.1	0.5	0.5	0.4
1/BX−1	0.7	0.7	0.5	0.1	0.1	0.1
1/any	0.5	0.3	0.1	0.1	0.1	0.1
2/BX+1	0.0	0.0	0.0	0.0	0.0	0.0
2/any	0.1	0.2	0.1	0.0	0.1	0.0
losses	56.4	36.4	9.0	6.5	4.2	1.2
Charge	6.55(3)	7.12(3)	8.00(3)	9.03(3)	8.70(3)	20.09(5)

Lost Hits and Charge Collection Efficiency



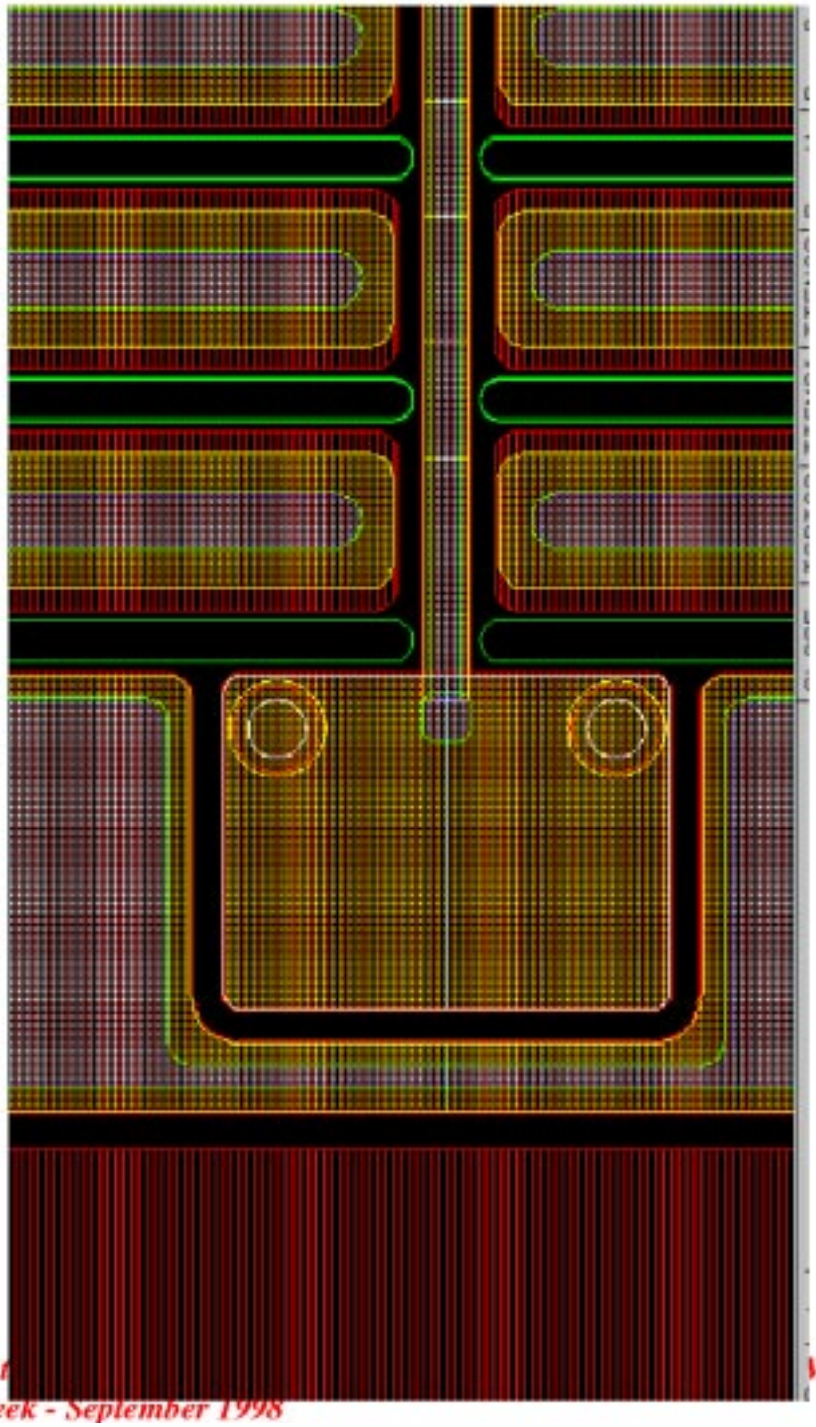
•Some lost hits concentrated in the region of the bias grid on Tile 2 design...

…but SSG, another test structure with a simplified bias grid in the same submission, showed considerably better charge collection behavior and all other characteristics comparable :



The SSG

Small Gap (p-spray)



Conclusions from Prototype 1:

•Prototypes have been fabricated by 2 vendors and successfully tested.

•Within present statistics, sensor characteristics are not degraded by any part of the assembly procedure.

•p-spray selected as baseline isolation technology.

•Design SSG looks good for charge collection, efficiency, high voltage stability.

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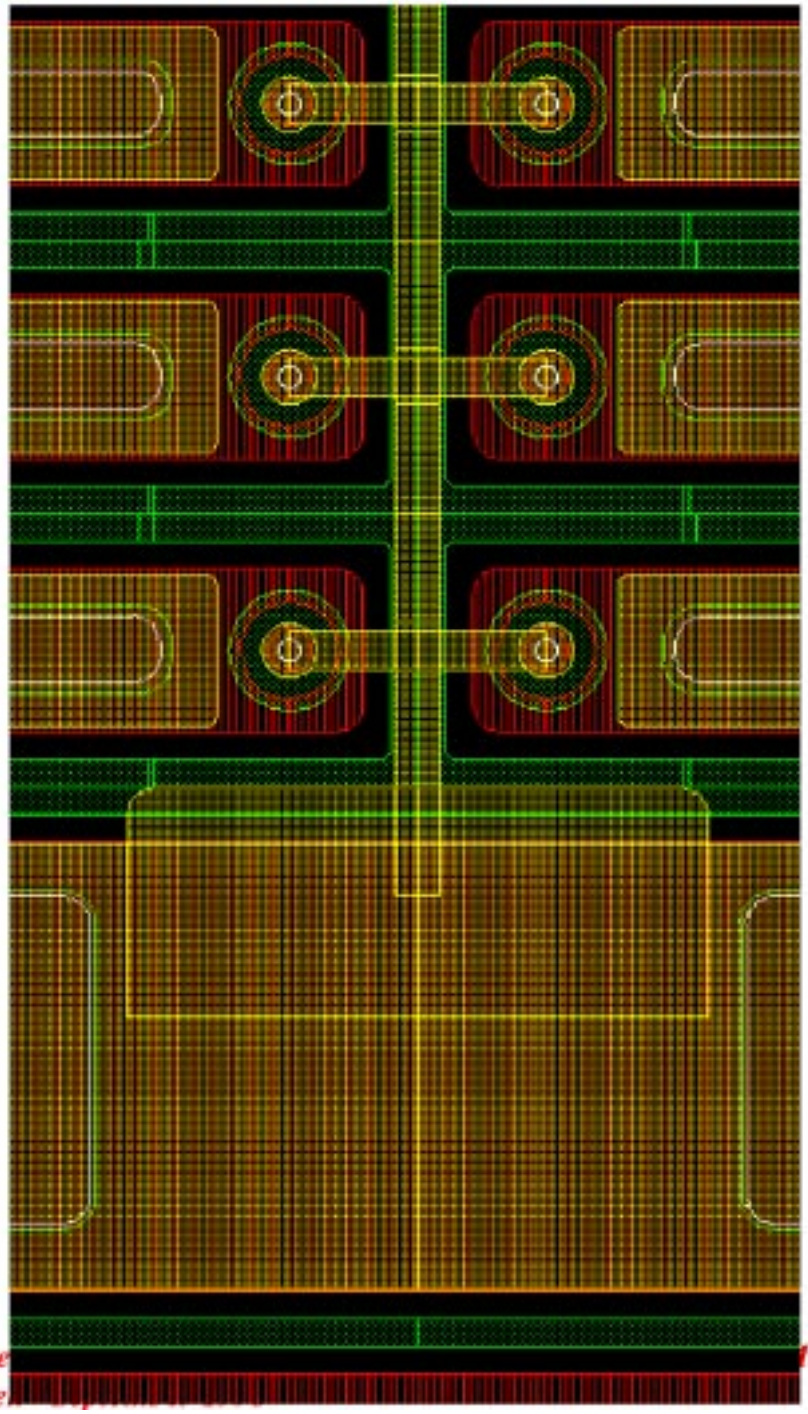
•Simulations were conducted to further optimize the SSG against charge loss + capacitance. The revised design was submitted to the manufacturers as Prototype 1.5, to be ready this month.

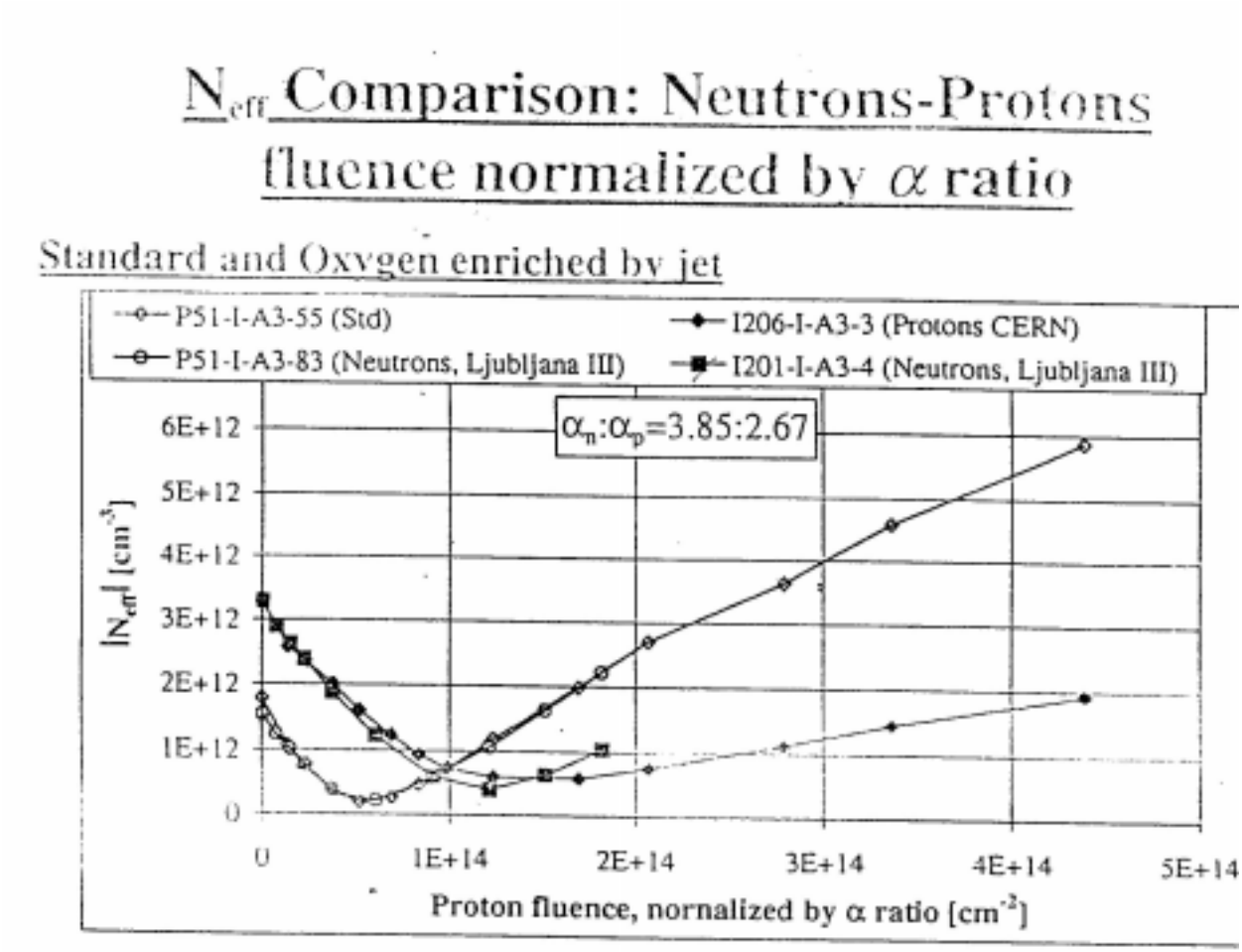
The "New SSG":

New Small Gap (p-spray)

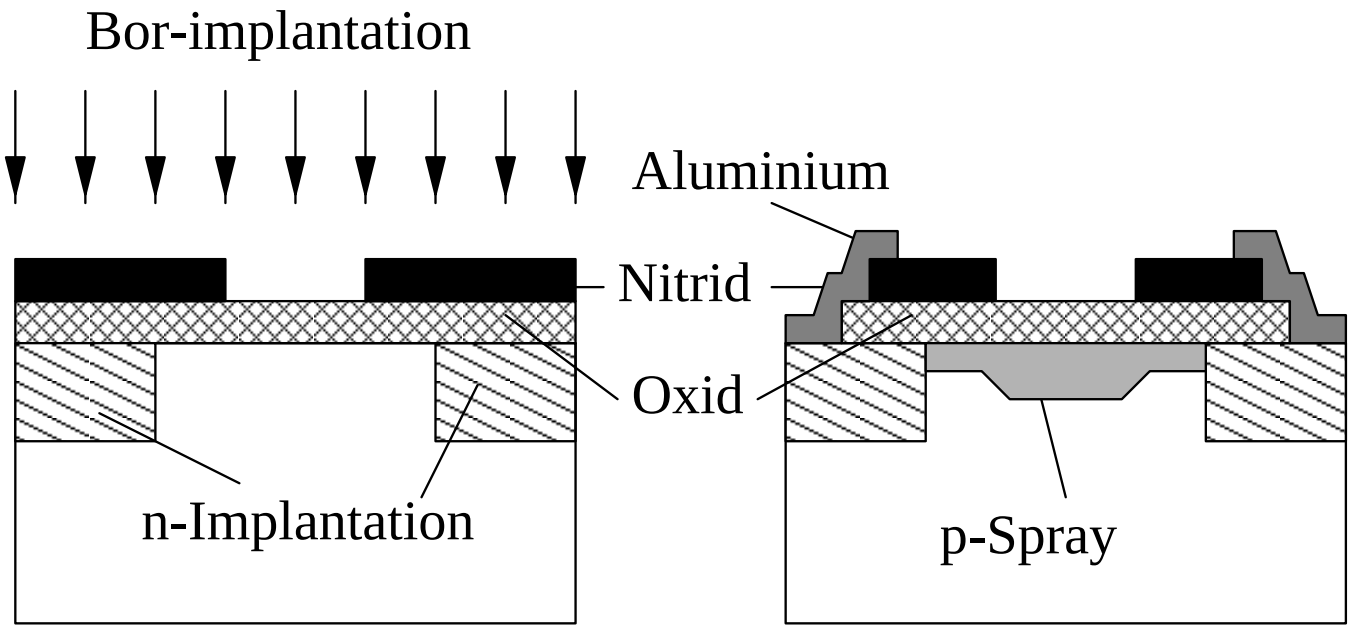


Other new results to input to the design:

1) From the ROSE Collaboration: Oxygen-enriched silicon is significantly more radiation hard than standard silicon as tested with protons or pions.



2) Modified p-spray: attains a lower boron dose near the lateral p-n junction, thereby reducing the electric field. The surface charge at the junction is optimized at the saturation value (1.5×10^{12} cm^{-2}) and is slightly higher in the center (3.0×10^{12} cm^{-2}) for safe overcompensation. The higher dose in the center also reduces the capacitance.



(a) (b)

Prototype 2 wafers now in design:

3 Tiles per wafer; all New SSG style:

- variations on bias grid to optimize yield
- To be ordered in April from at least 2 firms.
- Order split to examine extra rad tolerance of modified p-spray and oxygen-diffused silicon.

The Production Program

- 234 thin B-layer sensors + 1994 250μm sensors for the remainder.
- About 1000 wafers required if yield is 75%.
- 3 Tiles + test structures on each 4” wafer.
- Expect first 50 wafers require 8 weeks for a medium foundry; 1 additional week for each subsequent 25-wafer batch→ we require one foundry-year.
- Expect to distribute production to 2 vendors over 2 years.

Anticipated Production Sensor Testing Program

On all wafers:

- visual inspection by microscope
- probing of thickness
- I-V of every tile

On a representative sample of control structures:

- I-V and C-V
- $V_{flatband}$, layer thickness, implant resistivity, Al sheet resistance, etching uniformity, and alignment

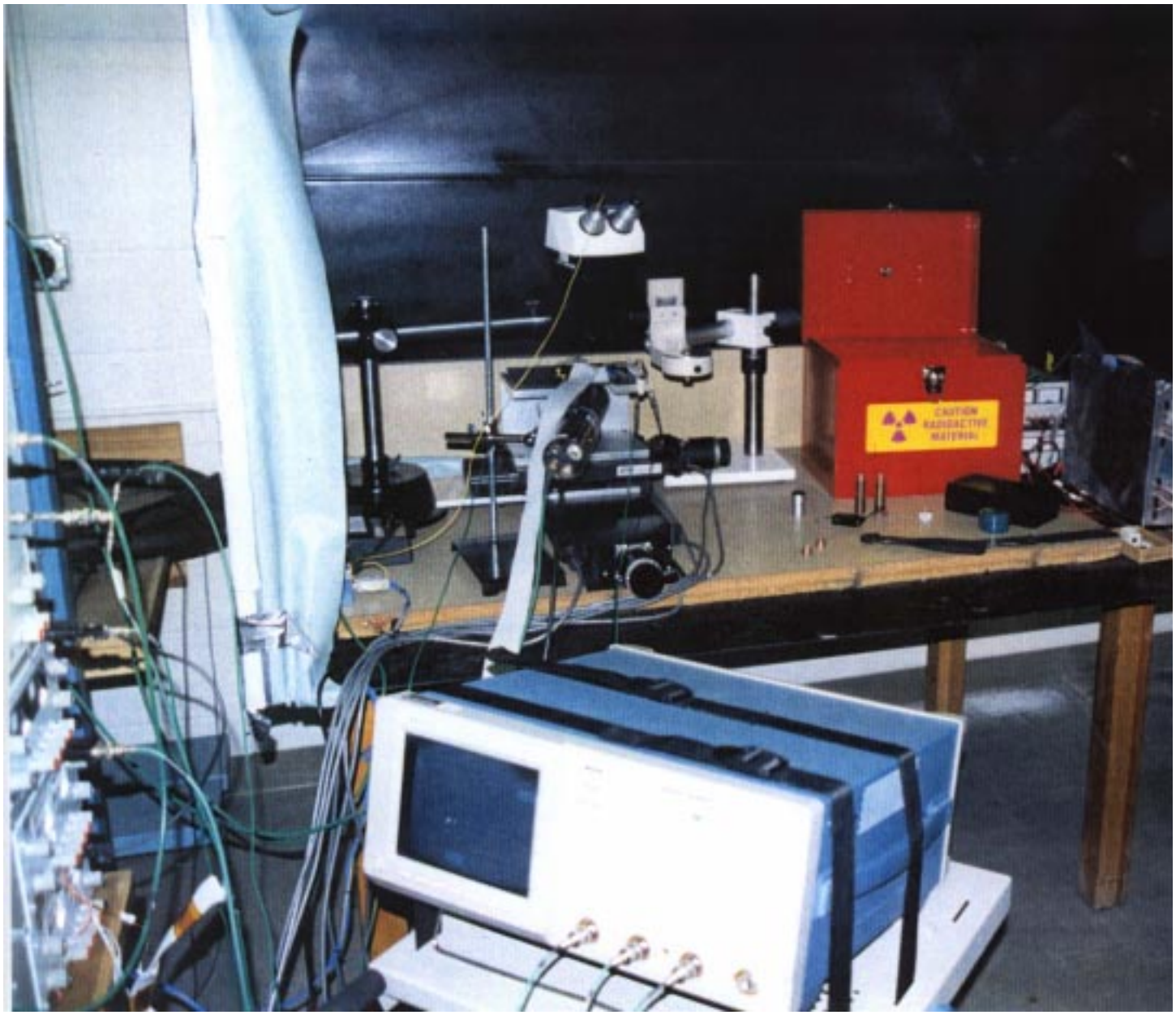
Testing and instrumentation capabilities at UNM:

- For silicon sensor characterization:
  - Alessi manual and semi-automatic probe stations with Mitutoyo Finescope microscope
  - Panasonic CCD camera with Sony monitor
  - Keithley 706 scanner
  - Custom low capacitance probe tips and etching apparatus
  - Dark box with Faraday cage
  - Keithley 617 programmable electrometer with GPIB
  - Keithley 237 high voltage Source/Measure Unit with GPIB
  - HP 4284A precision LCR meter with GPIB
  - Kulicke & Soffa 4123 wirebonder
  - Class 10K clean room
  - Chest & upright freezers and thermoelectrically cooled insulated box instrumented for cold measurements of irradiated sensors
  - 350 MHz Pentium computer and customized LabVIEW

- Software Tools for Silicon Device Characterization and Simulation:
  - Silvaco Atlas 2-D and 3-D device simulator
  - HSPICE with 2-D electrostatic solver
  - IES 2-D and 3-D electrostatic solvers
- Data Acquisition:
  - ATLAS PixelDAQ Test Stand with NI VME interface, crate, & computer
  - 1064 nm laser and focussing optics in dark box with Faraday cage
  - SR-90 Source and custom collimators
  - Computer controlled positioning tables
- Standard internal electronics and machine shop resources

The UNM wafer probing lab

The UNM Source/Laser Test Stand



The Schedule:

Baseline	*Current*	*Item*
11/2/98	12/1/98	Market Survey for Second Proto's initiated
12/1/98	12/1/98	Second Prototype Preliminary Design Review completed
3/5/99	2/12/99	Market Survey for Second Proto's concluded; 4 firms qualified; Price Enquiry initiated
3/29/99	3/29/99	Second Prototype Final Design Review
4/13/99	4/13/99	Complete testing of First Proto's
4/27/99	4/27/99	Complete Second Proto design; select Second Proto vendors
9/21/99	8/30/99	Receive Second Proto's
1/20/00	1/20/99	Complete testing of Second Proto's
1/20/00	1/20/00	Select production sensor type
1/20/00	1/20/00	Production Sensor Final Design Review
1/20/00	1/20/00	Select production vendors
2/24/00	2/24/00	Start pre-production procurement
6/22/00	6/22/00	Complete pre-production procurement
7/19/00	7/19/00	Complete pre-production design
12/13/00	12/13/00	Complete pre-production fabrication
5/29/01	5/29/01	Complete pre-production testing