Recent FE-B Module Experience at LBL and UOK

K. Einsweiler, LBNL

Results from first two FE-B “bare” modules

Results from first FE-B Flex modules

Results of Indium and Solder bumped assemblies

Results from first FE-B solder-bumped module

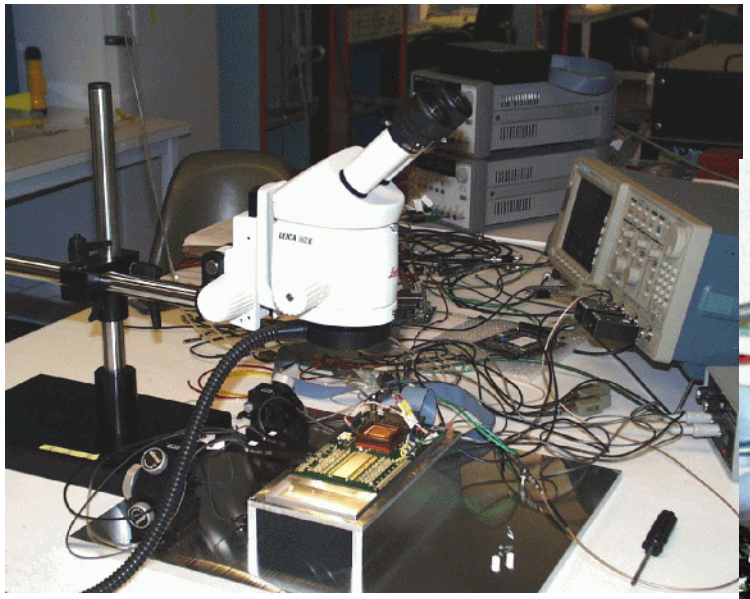
Module Prototypes

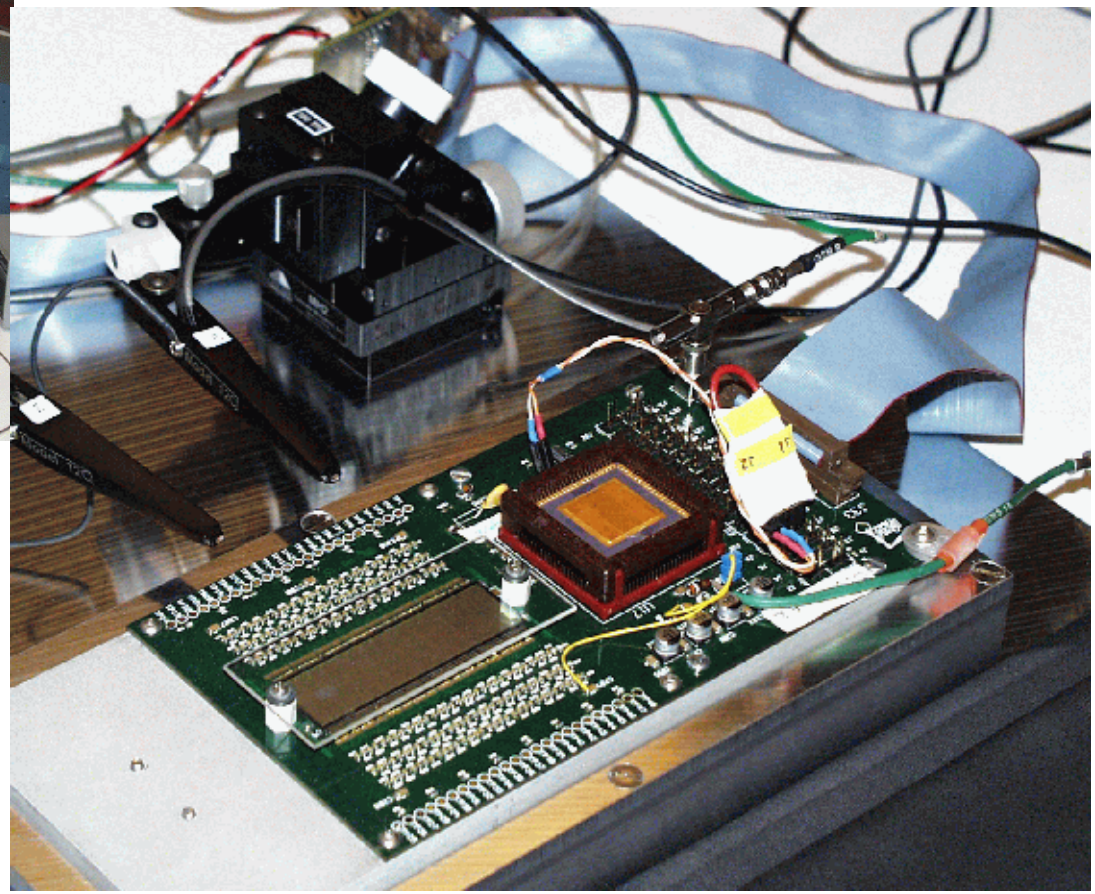
Three different types of module prototypes made:

- "Bare" modules, in which the multi-chip assembly consisting of the sensor and 16 FE chips is attached directly to a complex PC board. The intention of this prototype is to establish an electrical reference standard of the "best" performance achievable.
- Flex modules, in which the interconnections are performed by a Kapton+Cu Flex hybrid which is mounted on top of the sensor. This assembly is in turn mounted on a PC support card, which should only supply power and interfacing. Several such modules have been made using a first generation Flex manufactured at CERN.
- MCM-D modules, in which interconnections are made using deposited dielectric plus Cu layers on the sensor substrate. In this case, all of the connections are captured between the FE chips and the sensor prior to flip-chipping. Only one such module has been made so far, and it has not been tested in the US.
- The initial set of modules (four) was assembled by Boeing using Indium bumps in Summer 98. We have recently begun to receive IZM solder-bumped modules.
- Results will be shown from the five modules that exist now in the US.

Status of FE-B "bare" modules

- Two modules were flipped by Boeing in June, and assembled using the Genova Module Support Card (12 layer PC card which makes all of the necessary interconnections between 16 FE chips and MCC).





Some features of the first generation Module Support Card:

- Decoupling using 0.01 μF is present for all 9 bias points (8 DACs and MON_REF) on each FE chip.
- Decoupling using 0.01 μF is present for each of the 3 LV supplies on each FE chip.
- Hitbus from each chip is brought to a patch point for jumper-selection of this signal to PLL for self-triggered readout, but it is not buffered to transmit off of the board
- Only internal charge injection is supported (static VCal plus strobe). Modifications needed for external injection (external chopping of VCal).
- Three planes exist in the board: DGnd, AGnd, and AVdd. AVcc and DVdd are distributed by U-shaped bus.
- Detector connections (DGUARD and DGRID) are AC coupled to AGnd. A jumper-selected DC connection is needed. A 1 nF disk capacitor is used for decoupling.

An improved card has now been fabricated:

- Three larger decoupling caps exist for each FE chip (allows use of 0.1 μF), other decoupling dropped. Five power planes provide all critical voltages.
- Global HitBus OR for complete module created using external logic.
- All other minor problems fixed (except for possible improvements in bias connect)

Summary of the two “bare” FE-B modules:

- After some wire-bonding problems were fixed, both modules work perfectly from the digital point of view: all 16 chips have every channel working when using digital hit injection.
- When the detector is biased, and the FE-B DACs are set to standard conditions, the power consumption is very stable and reproducible (for 16 FE-B plus MCC):

  DVdd uses 400-450 mA at 3.5V (about 20 mA per FE-B plus 80 mA for MCC) = 1.4W

  AVdd uses 700-750 mA at 3.5V (about 25 mA per FE-B in front-end, rest in Hitbus buffers) = 2.3W

  AVcc uses 250 mA at 1.75V = 0.4W

  A total of about 4.6W maximum, with standard biassing of 40µW/pixel in analog FE
- One module uses a CIS Tile2 detector, and the other is a Seiko Tile1 detector. Both are 1M. The detector currents are quite high at -150V. The Tile1 uses about 45µA and the Tile2 about 200µA.
- The Tile1 module has only a few dead channels, with the exception of one chip (Chip 14) which has about 140 dead channels, mainly in the first two columns. Here, dead means that when doing a threshold scan, these channels produce essentially no hits. X-ray scans indicate these are due to regions with merged bumps.
- The Tile2 module has many dead channels, mainly in the chips on one side (a total of about 800 bad channels are found, most of them in Chips 0 and 4).

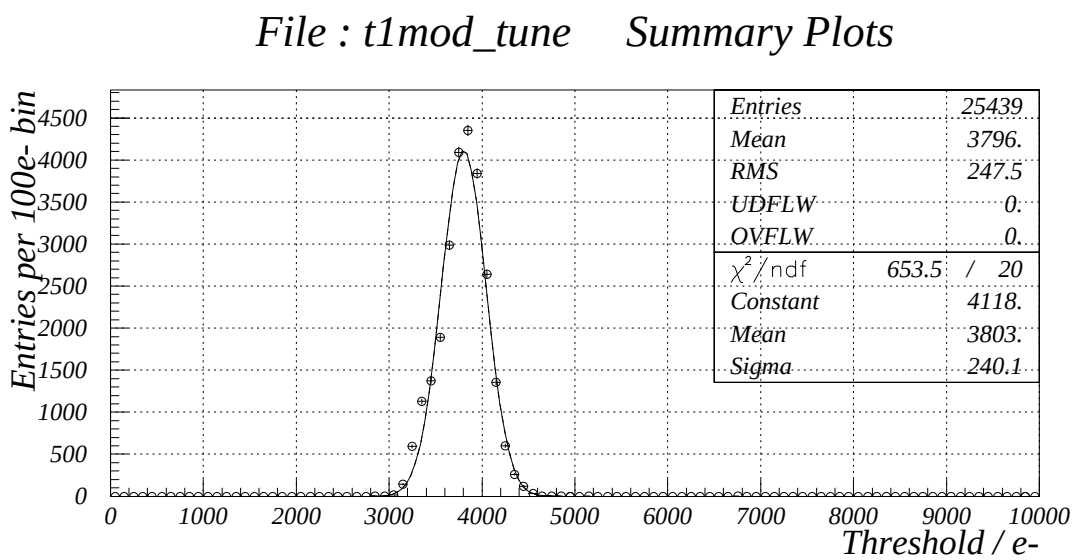
- Initially, behavior was quite poor when all chips were enabled and set to nominal thresholds. Very high noise was observed, with module sometimes entering a high current state in which all channels appeared to be oscillating. This behavior was considerably improved by adding more local LV decoupling (0.1 µF). This state has not been observed since on either module.
- Large number of dead channels was traced to poor bump-bonding (see talk of Gil). These bad channels have a significant influence on the performance of the chips that they occur on.
- These modules were constructed using thermal grease (Dow340) between the FE chips and the Aluminum support plate, with UV-cure epoxy applied to the four corners to hold the module in place. This is different from the single-chip assemblies, for which a silver-loaded epoxy was always used for attachment to a conductive AGnd plate on the PC card.

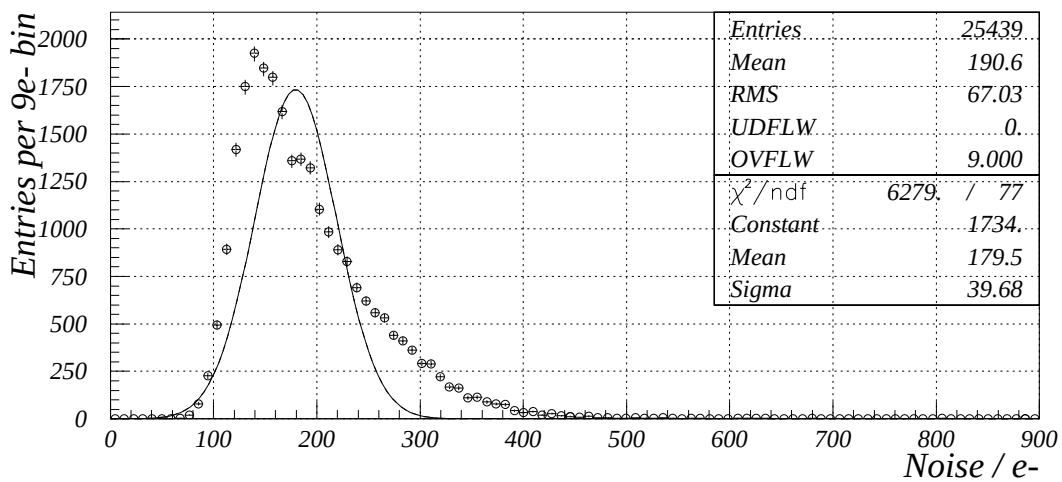
Modifications made to the Tile1 and Tile 2 module cards:

- Added piggy-back 0.1 µF capacitors by each chip in parallel with existing 0.01 µF capacitors.
- Removed wire-bonds from 9 bias nodes on each chip (8 current DACs plus MON_REF).
- Improved AGnd to DGnd connection near chips by soldering a wire across the ground side of the LV decoupling capacitors.
- Improved HV decoupling by using 47 nF surface mount capacitor.
- This essentially eliminated the instability problem. It was possible to operate the modules consistently with all chips tuned (TDACs set for minimal dispersion) and a threshold of about 3.5Ke. This was previously impossible.

Tile1 Module Results:

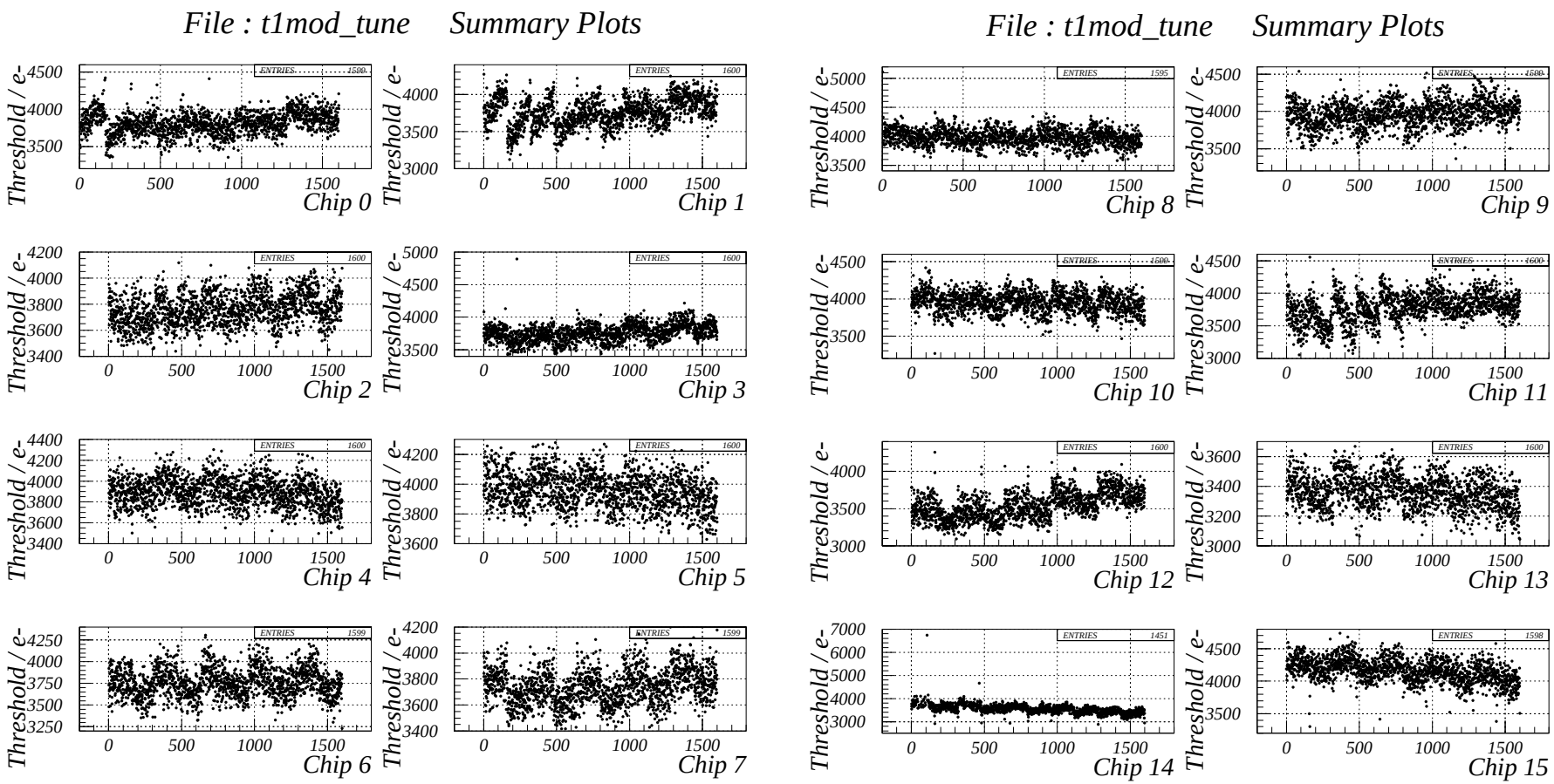
- Show summary of performance with all chips tuned, but only a single chip injected at a given time:





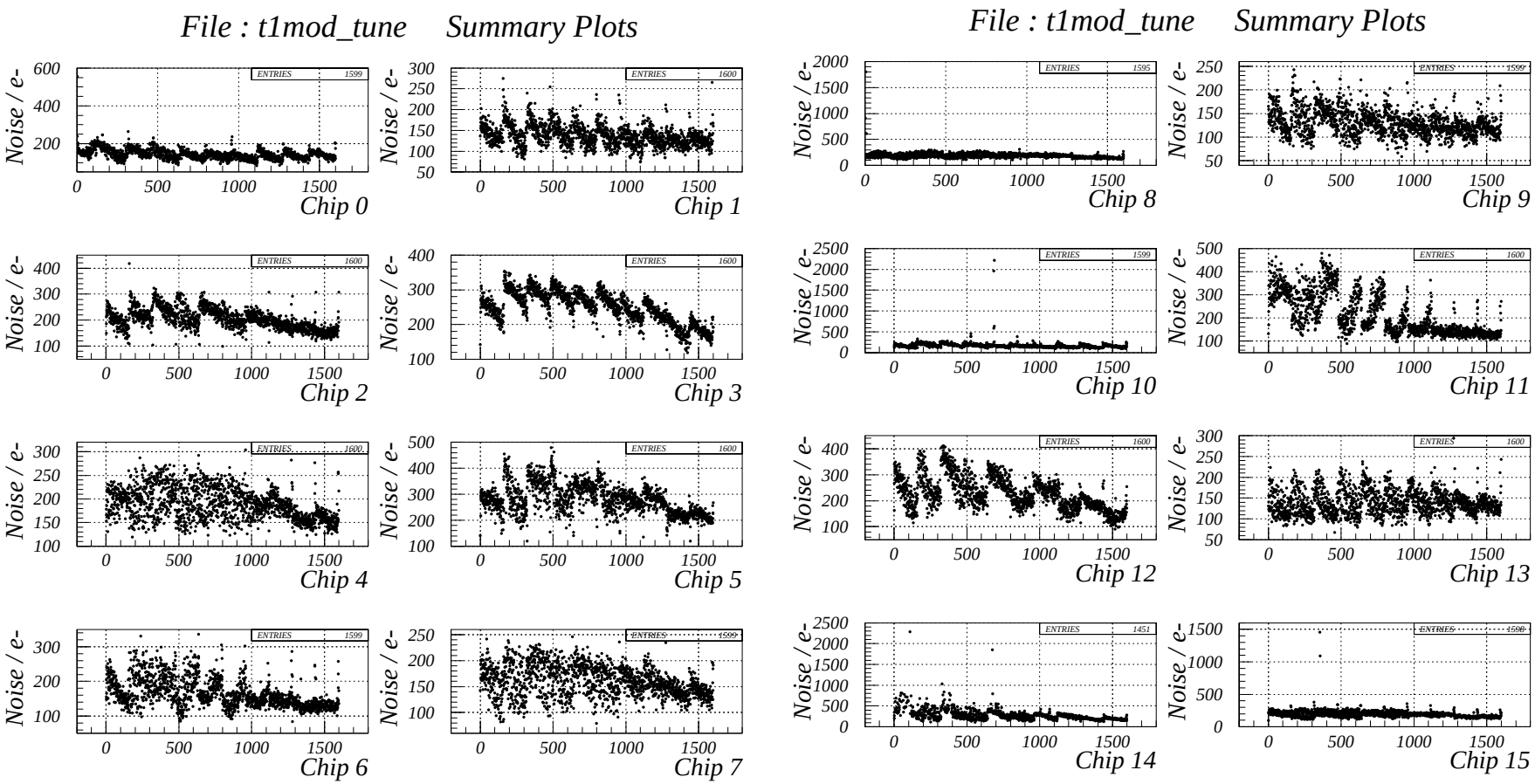
- Overall threshold dispersion, without tuning mean threshold of 16 FE chips, is 240e.
- Mean noise is about 200e, but some chips have noise extending up to about 400e.
- There are 25439 channels in this plot of the 25600 channels that should work in an FE-B module.

Behavior of threshold for the individual chips:



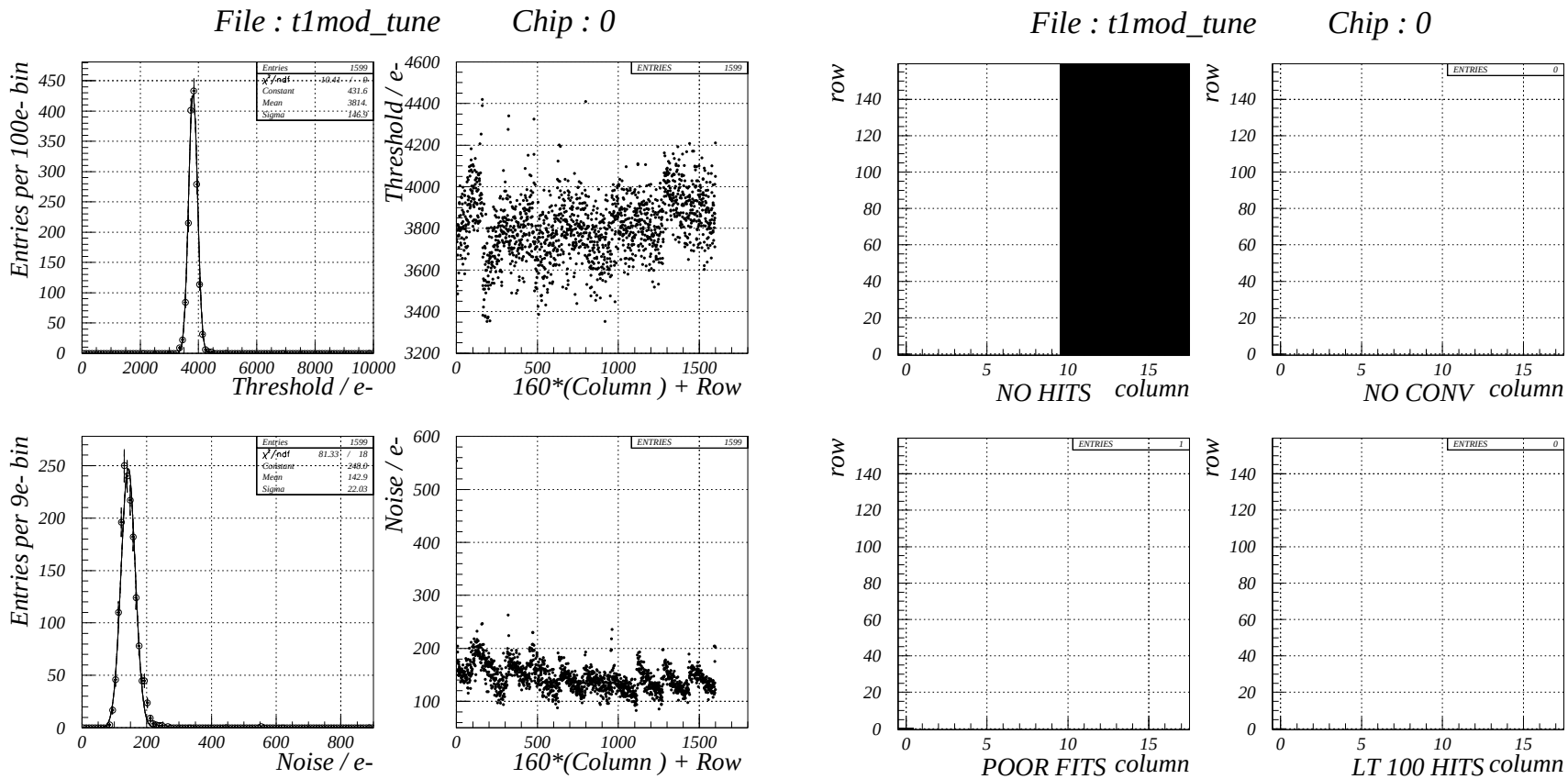
See that some of the chips do not show nice “tuned single chip” behavior, but rather show large systematic variations which increase the dispersion somewhat.

Behavior of noise for the individual chips:



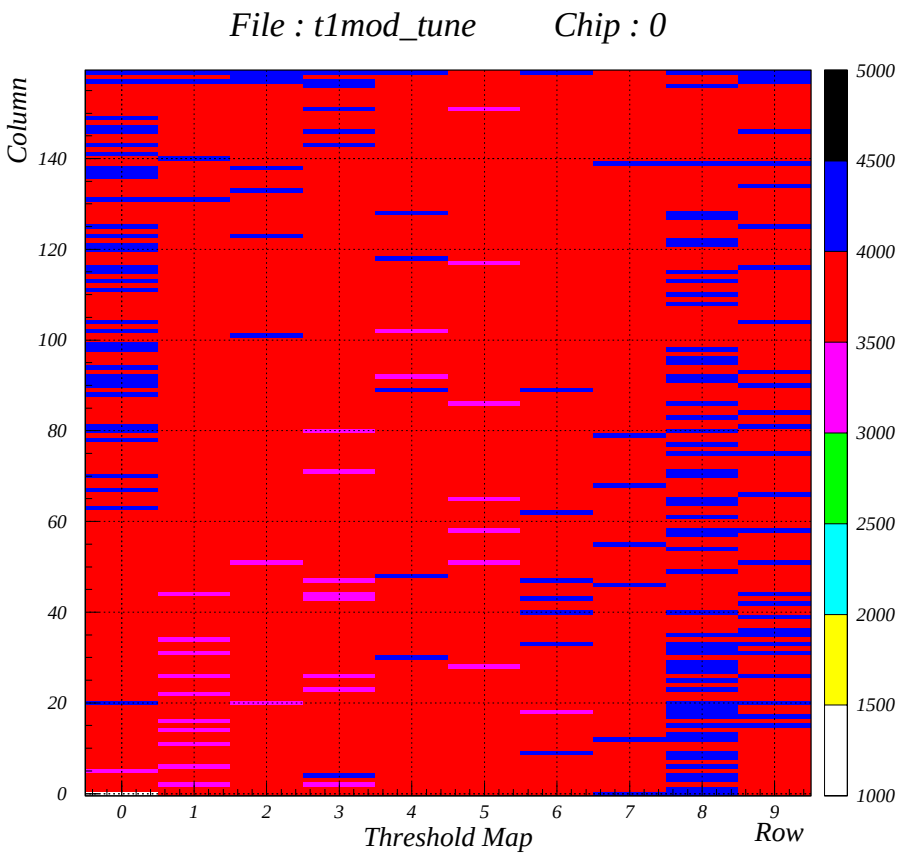
- Some of the chips have non-uniform noise behavior different than expected from single-chip behavior.

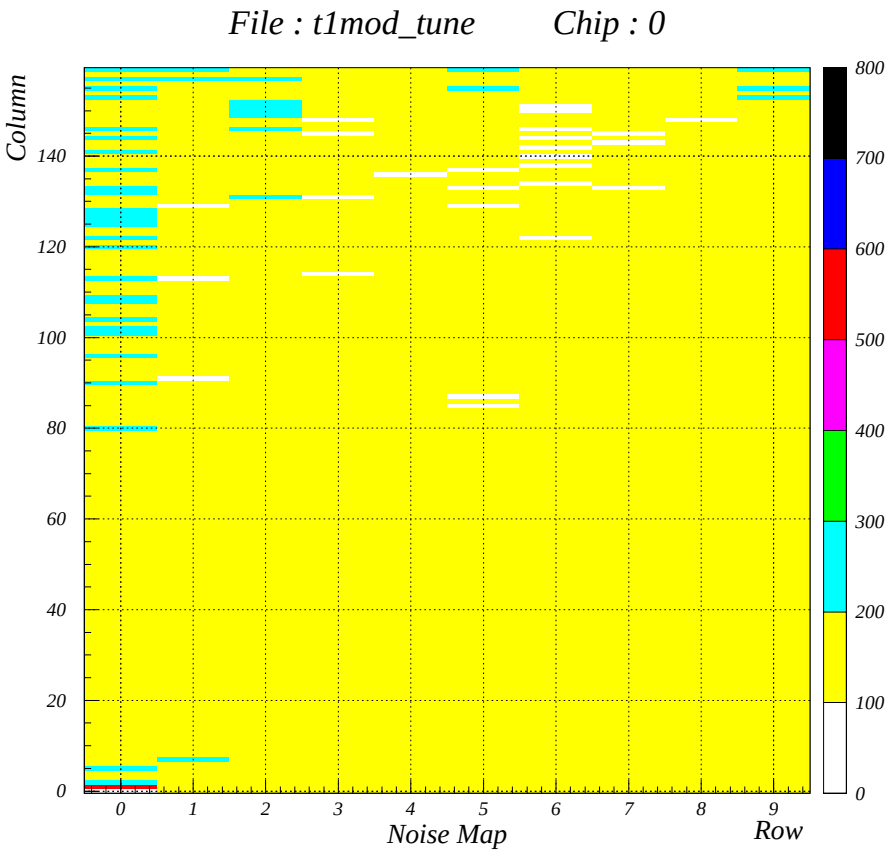
Threshold scan result for a typical “good” chip (Chip 0):



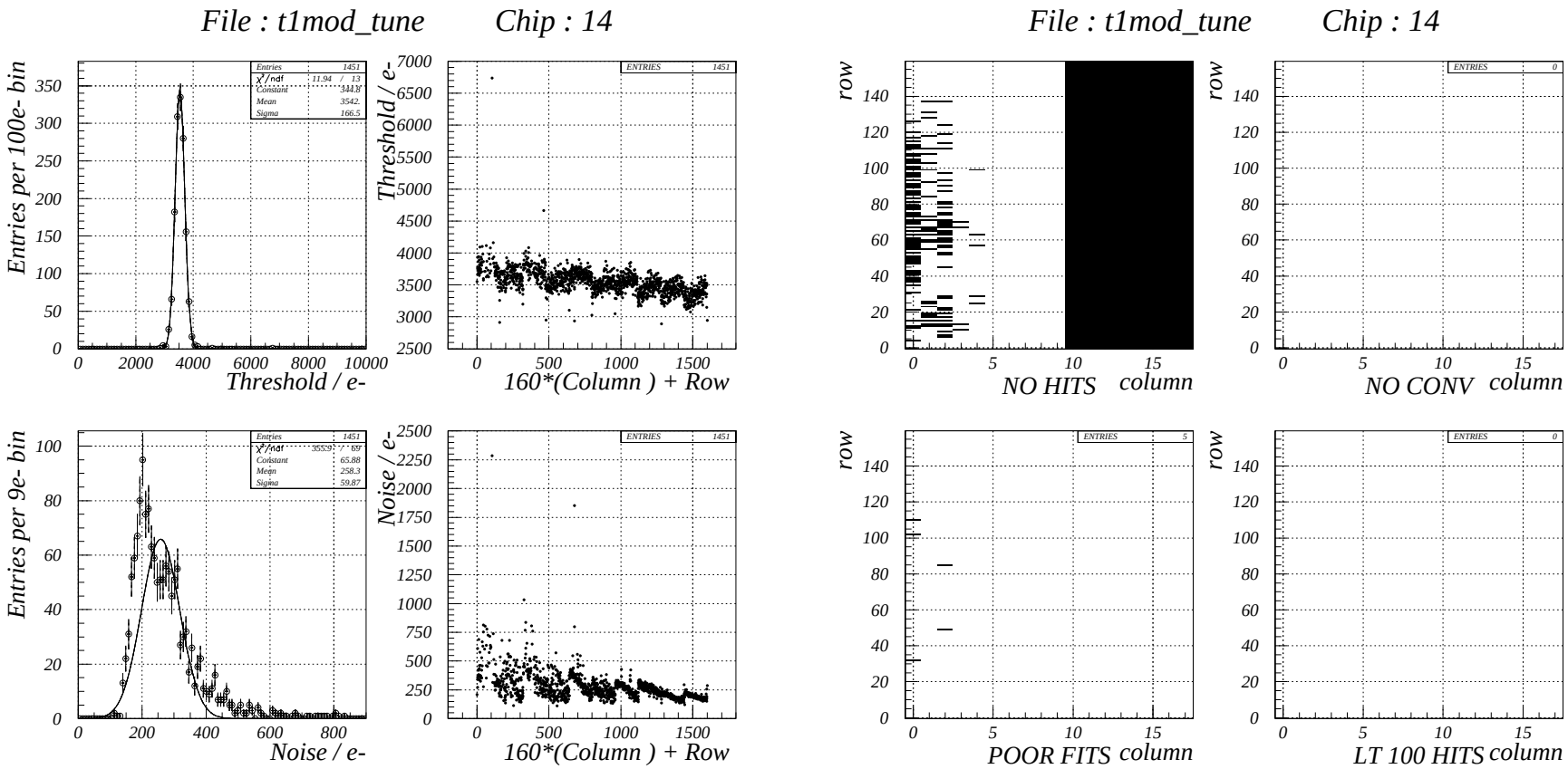
- Noise is worse than isolated single chip, but still acceptable. Threshold dispersion is OK but not great. Uniformity is not as good as for single chip assemblies.

- Threshold and noise map:

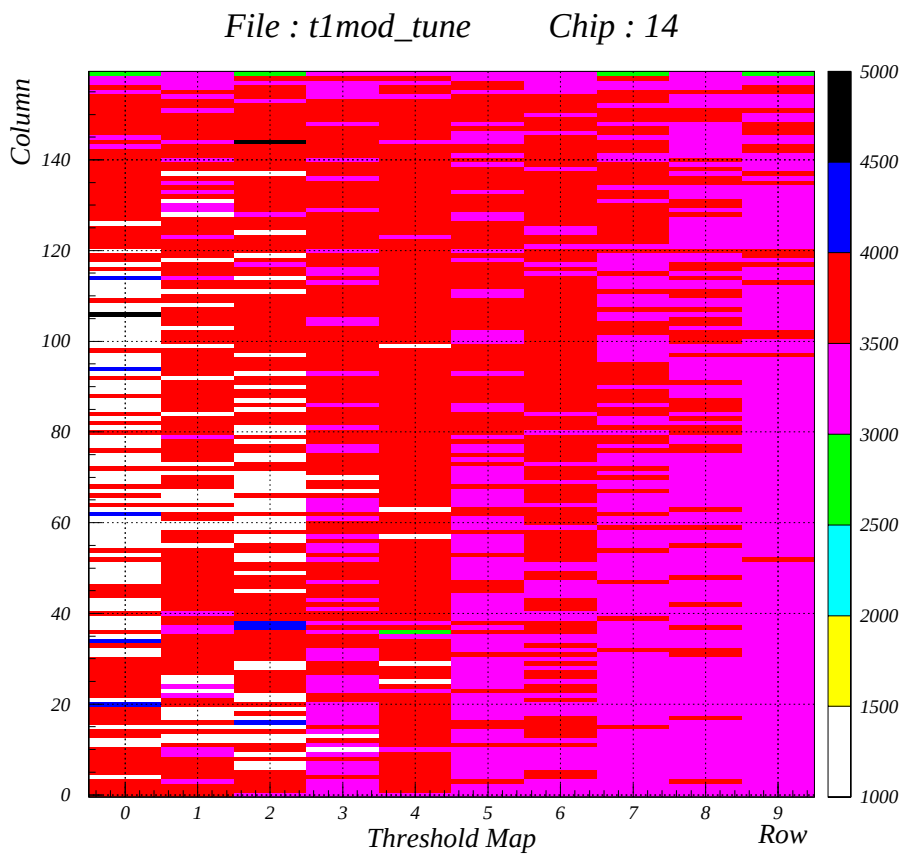


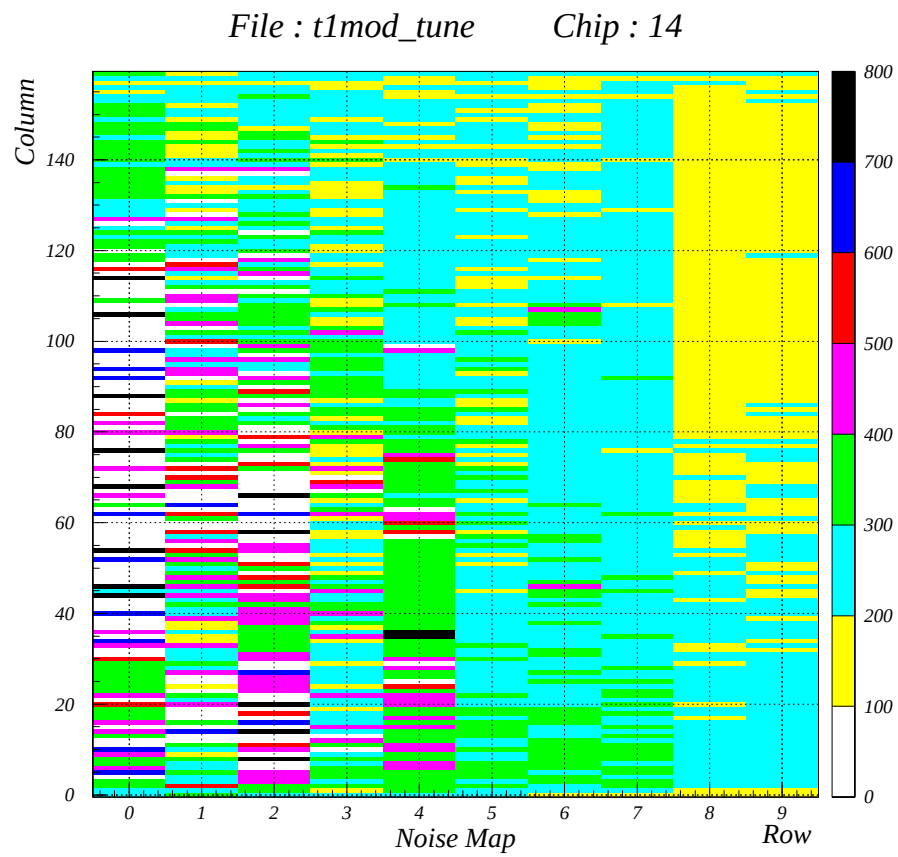


- Chip 14 is the only one with a significant number of dead channels:

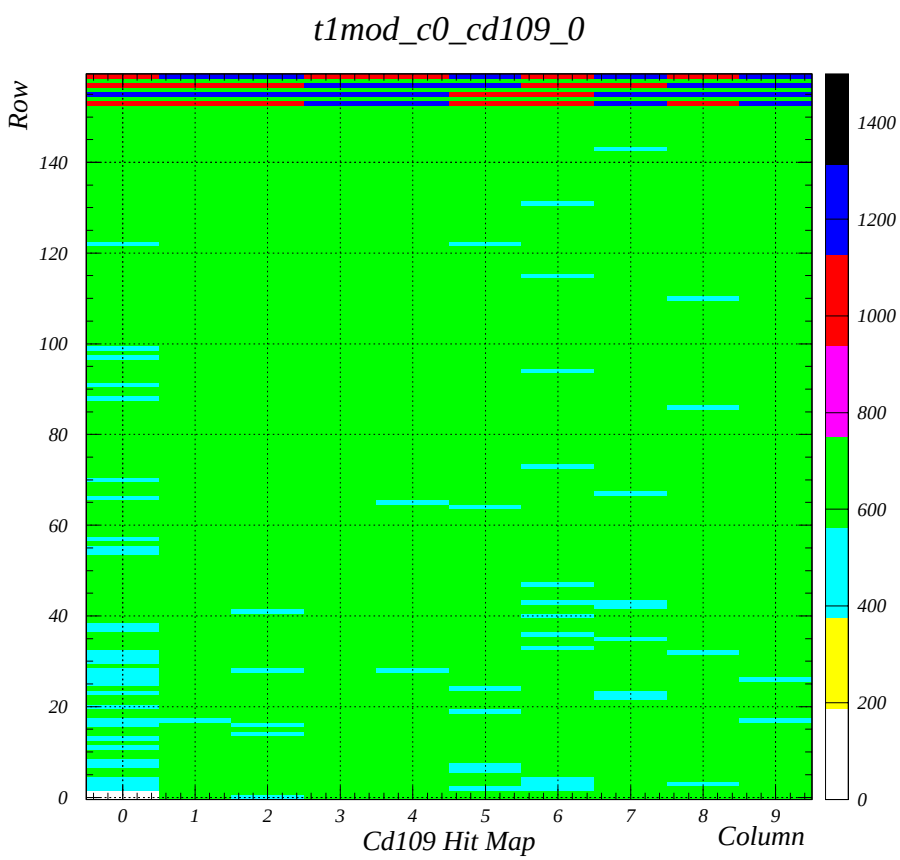


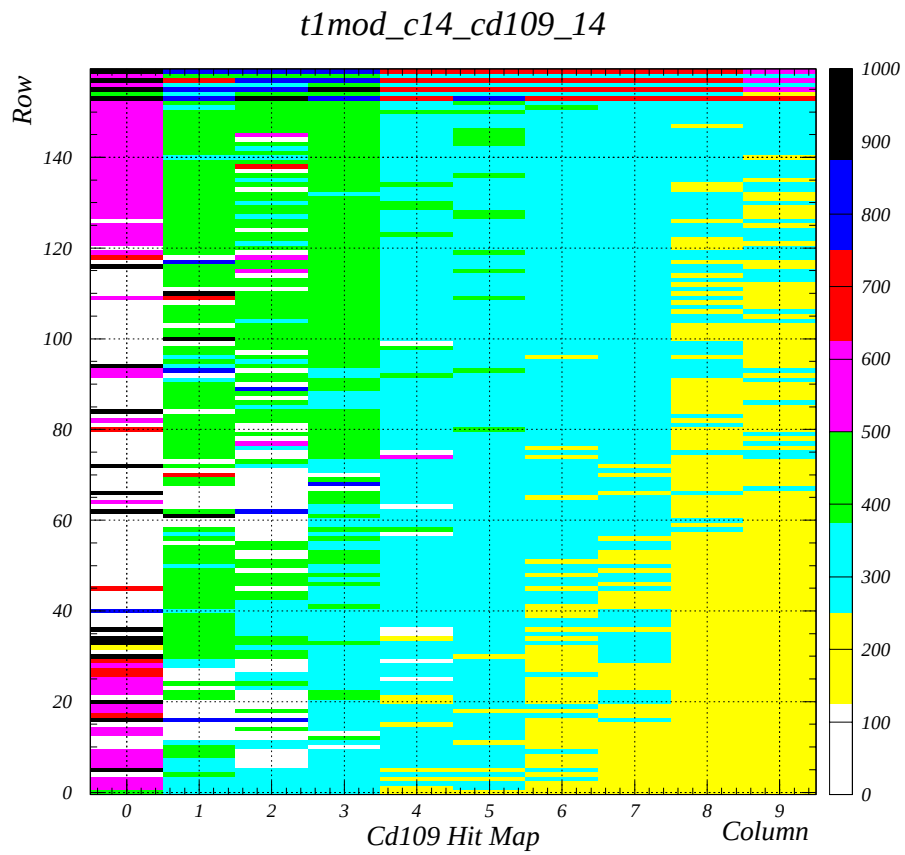
- Behavior near the dead channel region is quite poor:





- Source runs with Cd109 source have been made after tuning:



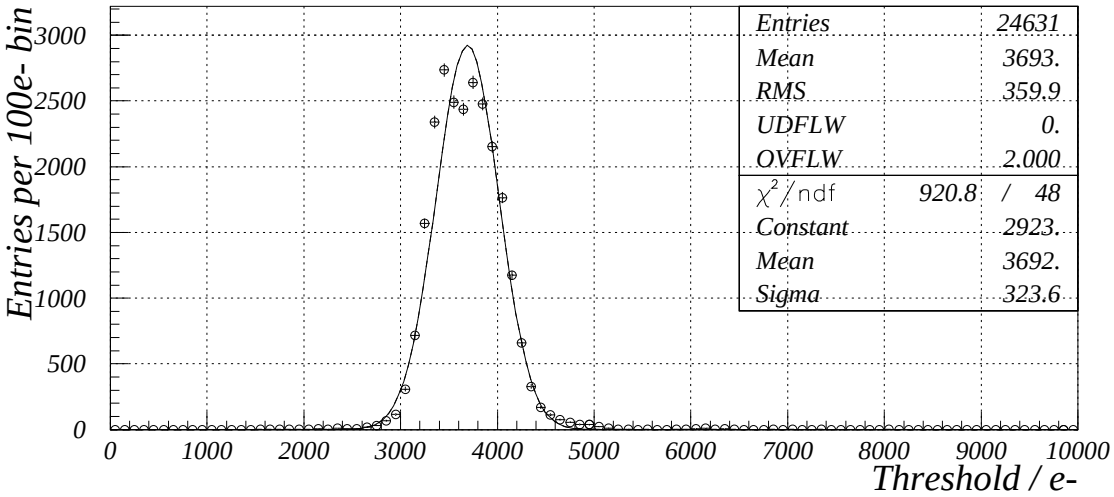


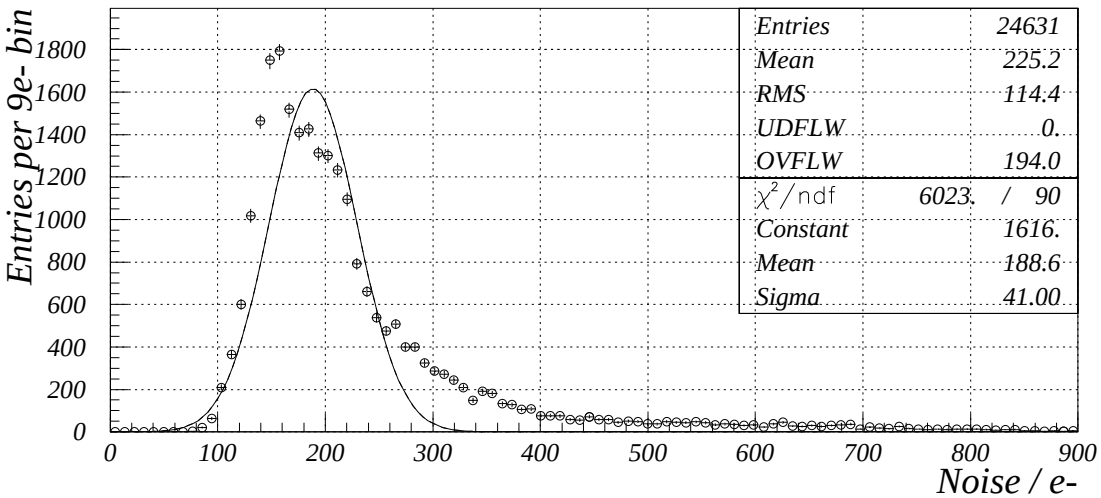
- Note Chip 0 and 8 in Tile have Column 0 400μ long, all others have 600μ.
- This module shows problems with “readout all” mode at nominal thresholds due to some instability (?). It is almost impossible to enable the entire chip. Instead source scans are made of parts of each chip and added to make full image.

Tile 2 module results:

Summary of performance with all chips tuned:

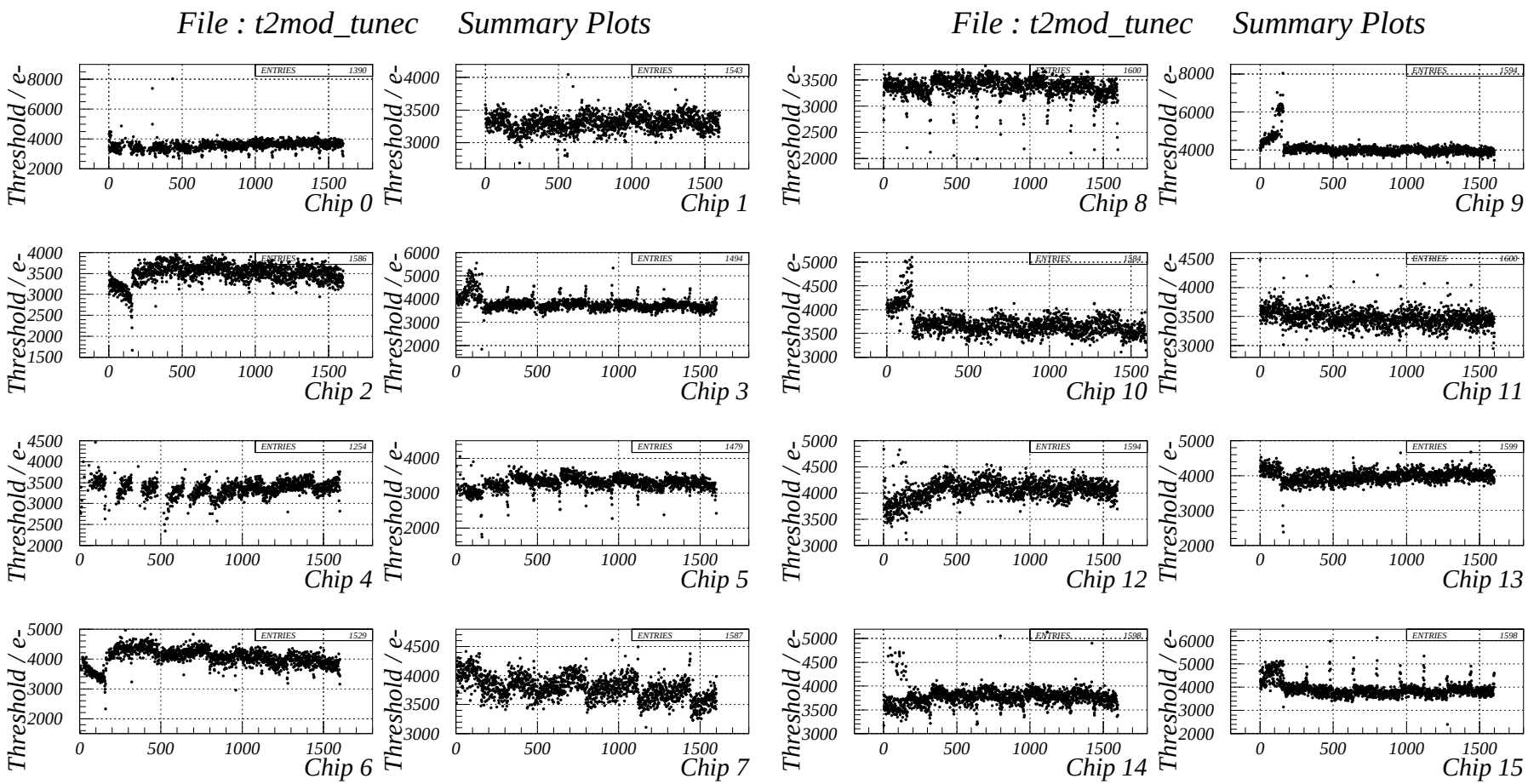
File : t2mod_tunec Summary Plots





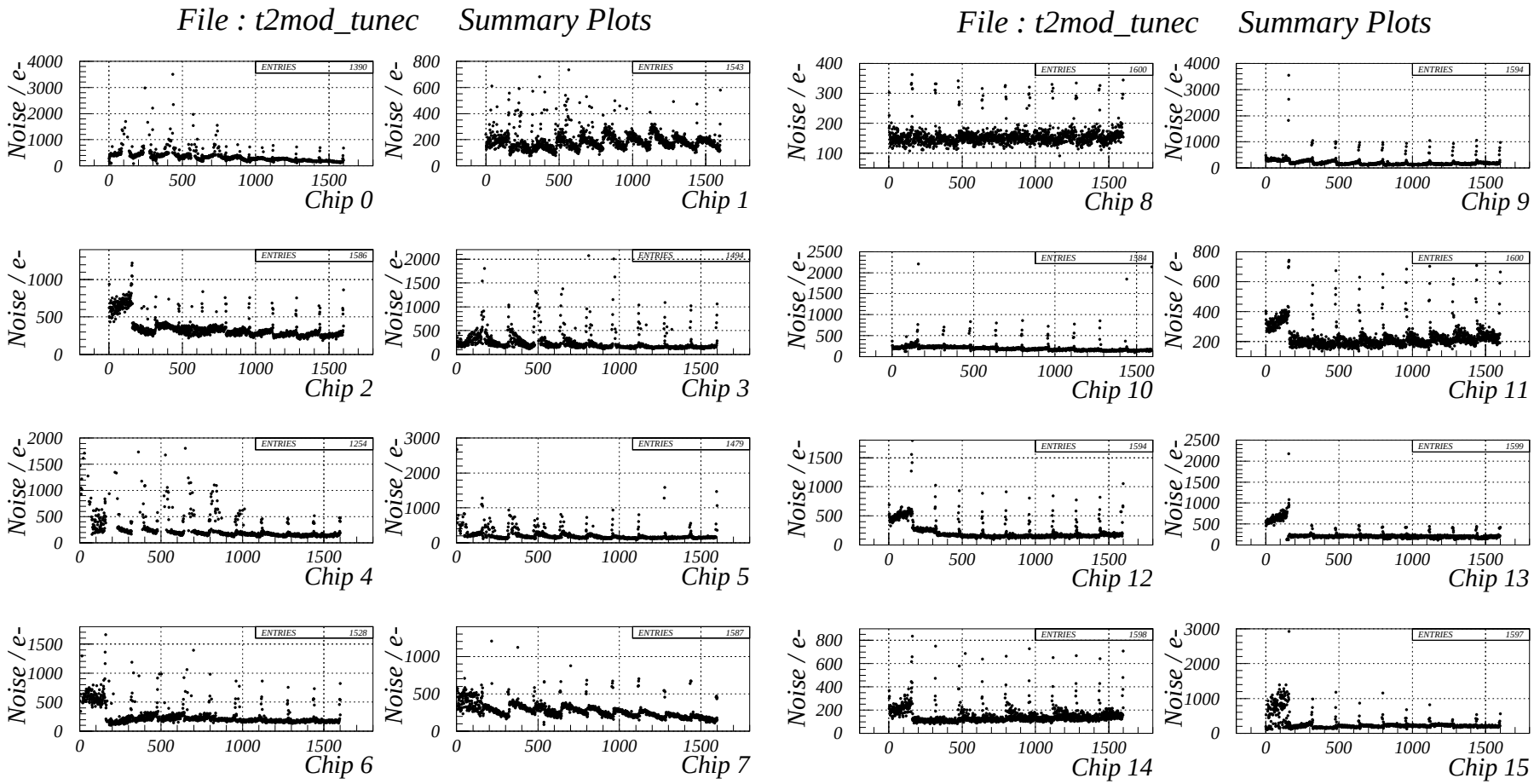
- Threshold dispersion is 320e, with no tuning of individual chip averages.
- Average noise is about 220e, with a tail going out to beyond 500e.
- Most of the tail in the noise distribution is for Column 0 channels, which are much noisier than expected in the Tile2 module (this feature is not present in the Tile1 module).

Behavior of thresholds for individual chips:



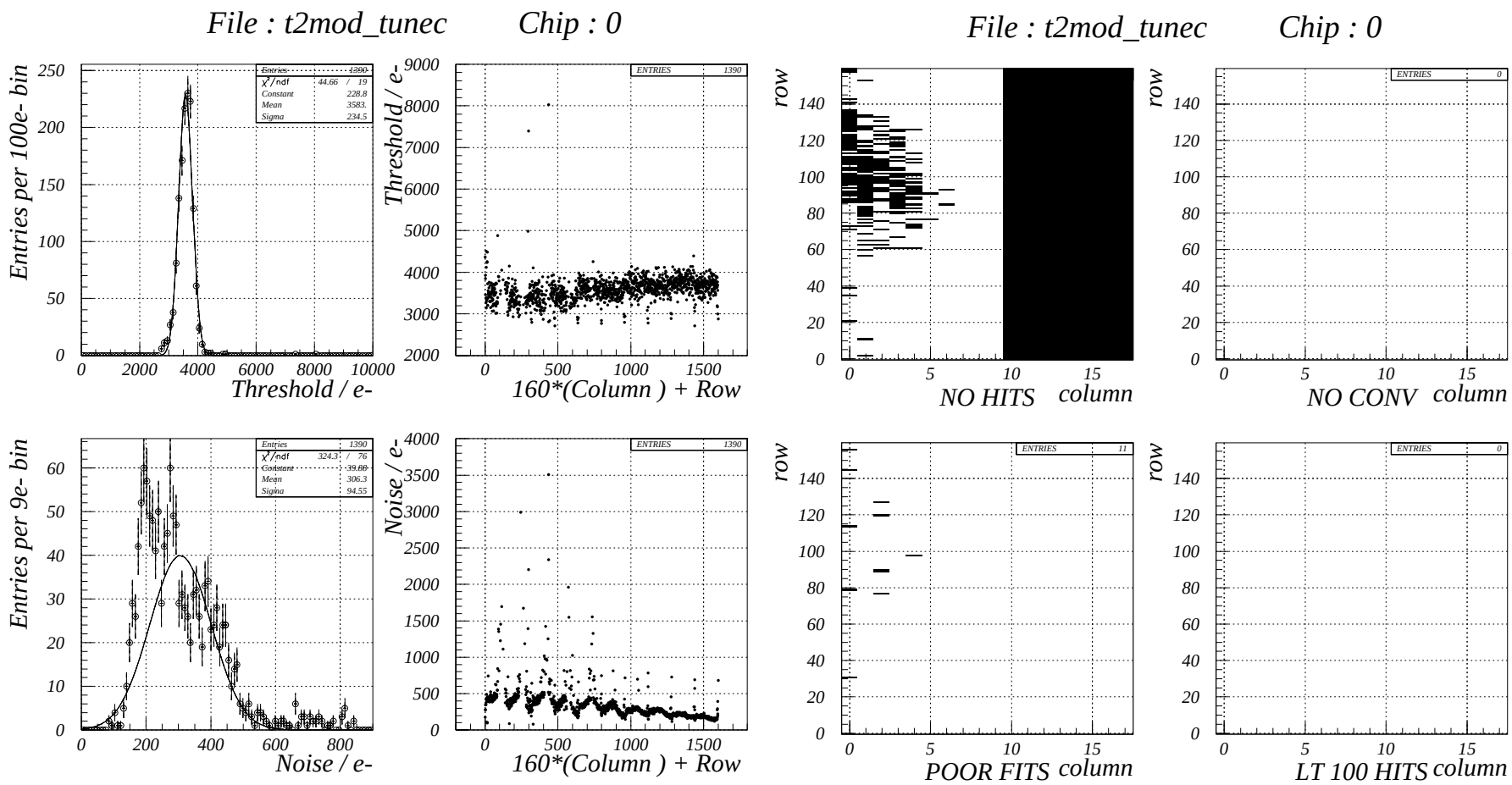
- Note poor behavior of column 0 in many of the chips.

Behavior of noise for individual chips:

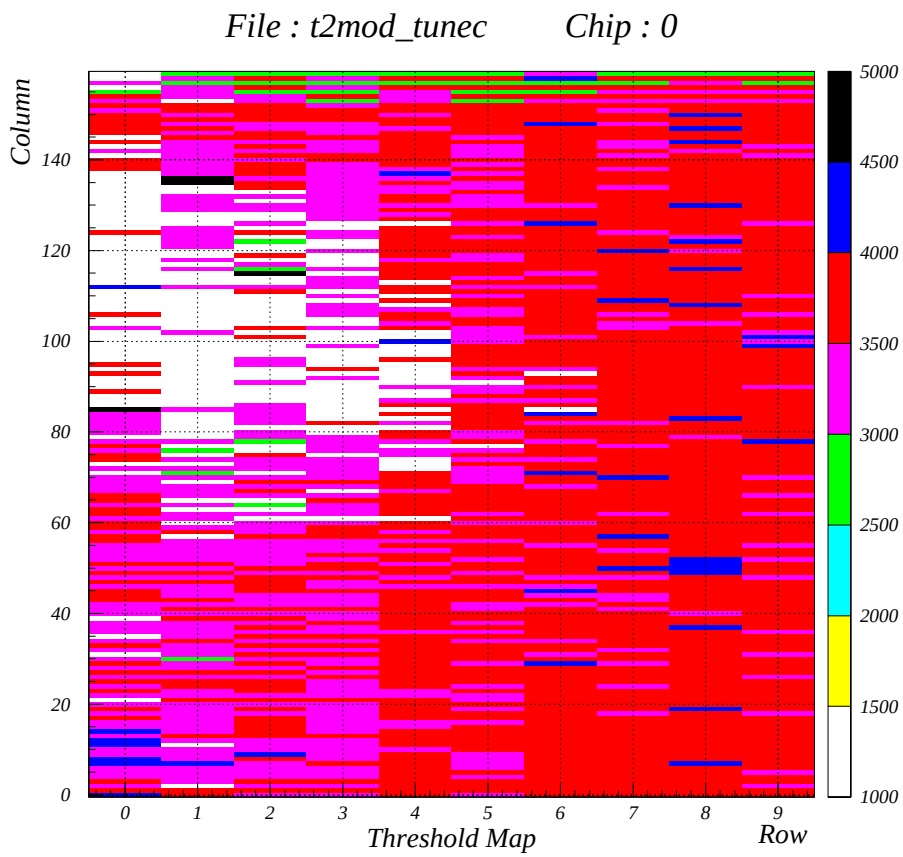


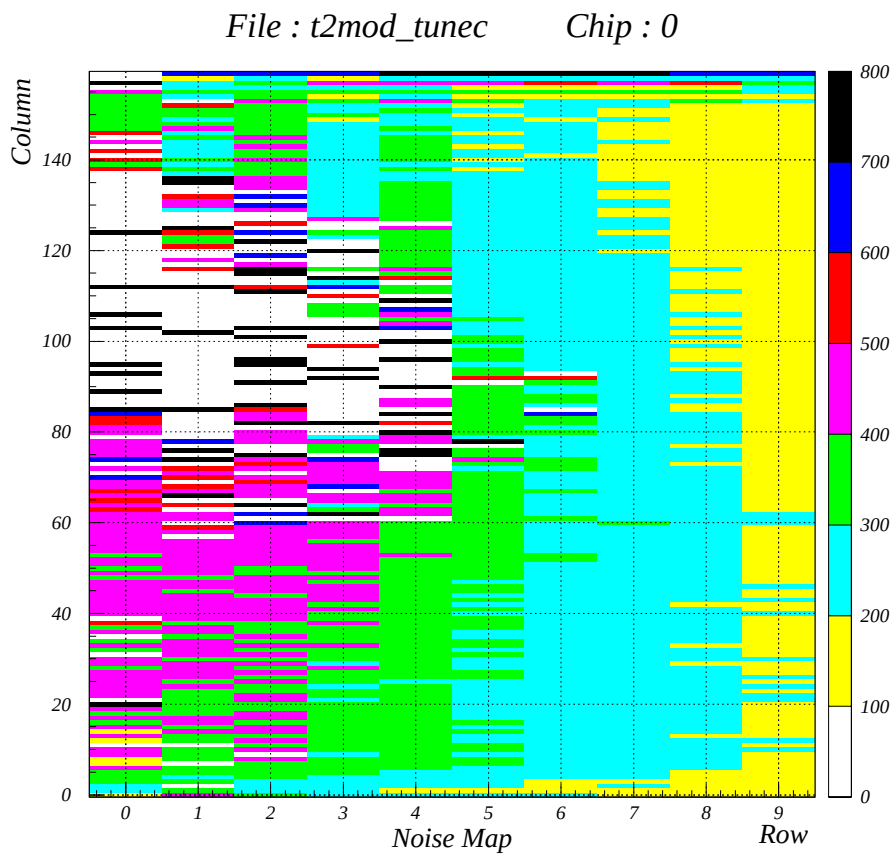
- Note unusually high noise in column 0 and in the ganged regions of the chips.

Example of chip 0, a chip with many merged bumps, tested with charge injection:



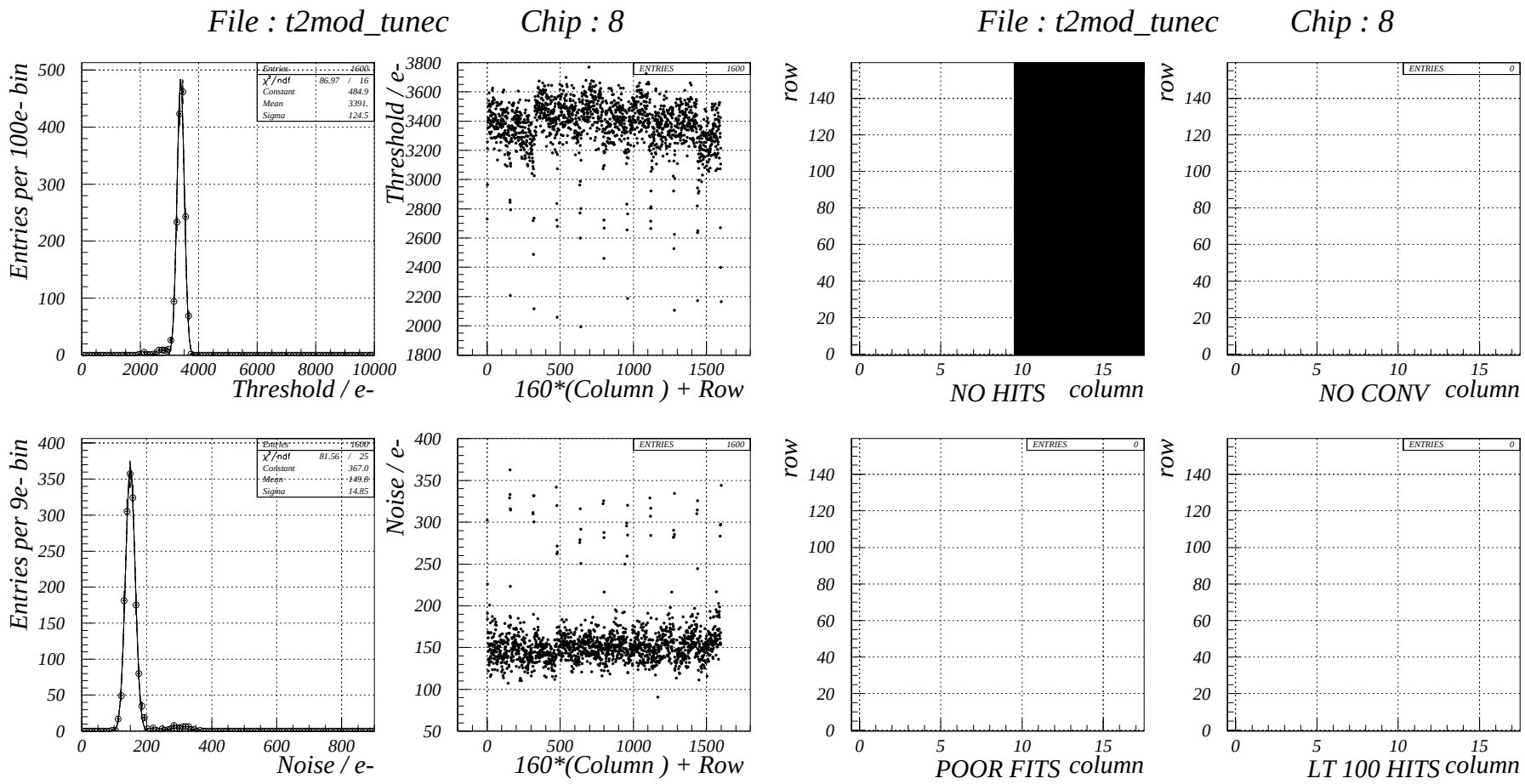
- Two dimensional map of threshold and noise behavior:





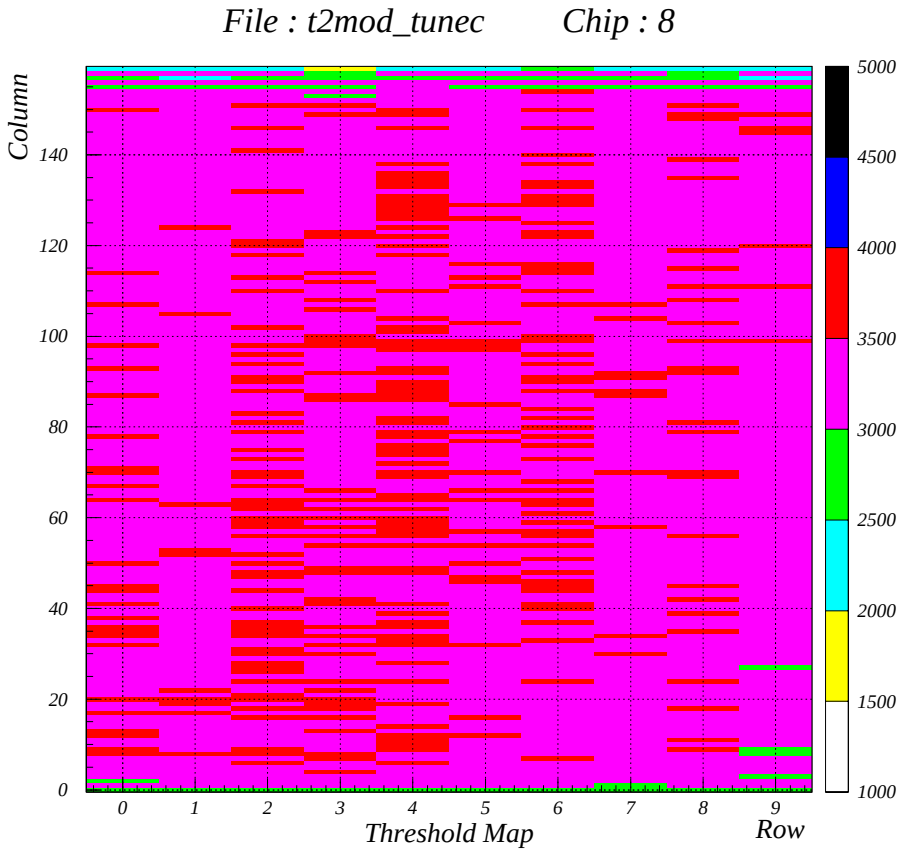
- Region near merged bumps has very poor behavior.
- It is difficult to operate this region in a “readout all” mode, as required for source tests and real operation in experiment.

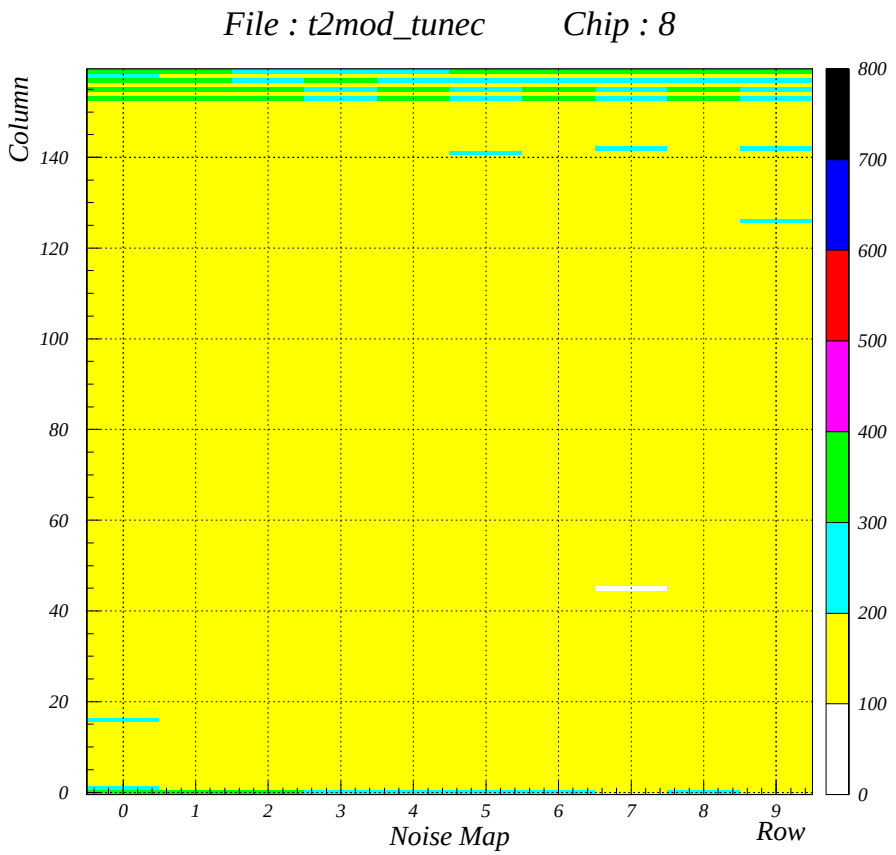
- Example of chip 8, an almost perfect chip:



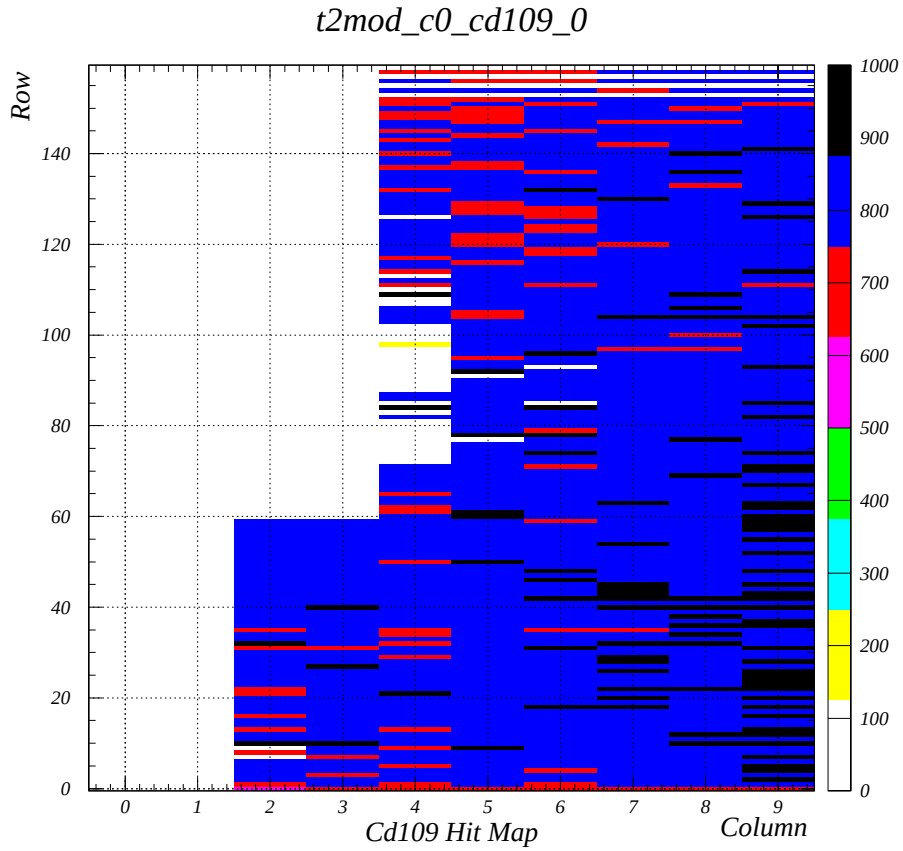
- This indicates that there is no intrinsic problem in the modules which prevents any chip from having good performance. Instead, it seems that for some collection of reasons, most chips do not achieve this expected level of performance.

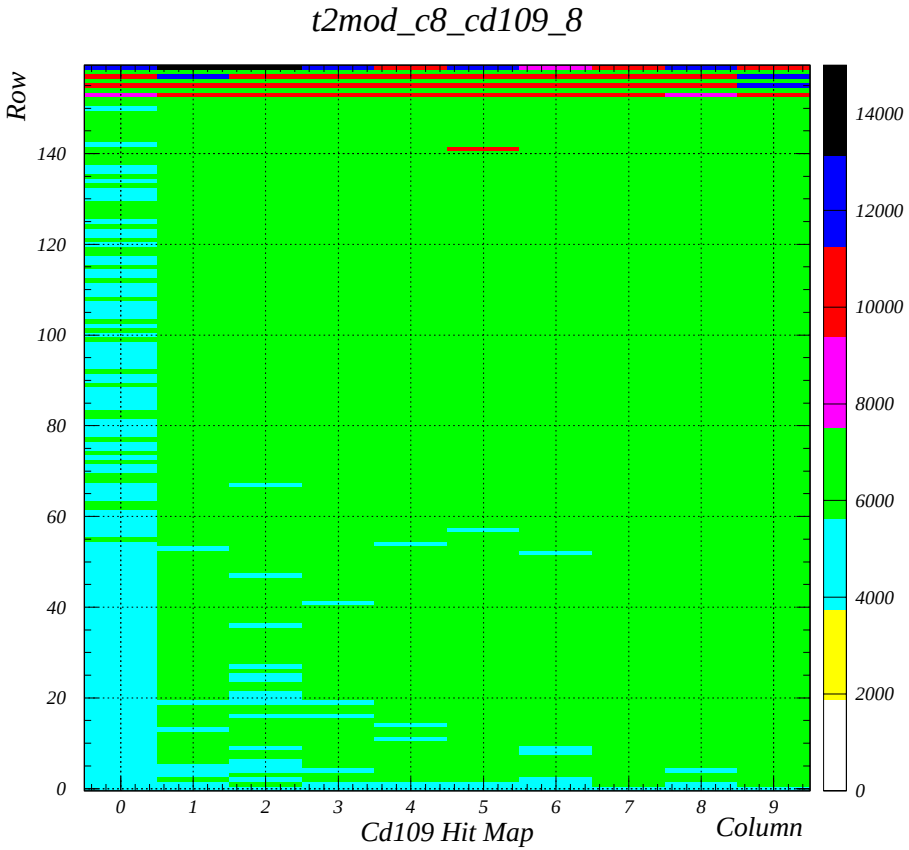
- Two dimensional map of threshold and noise behavior:





- Behavior with Cd109 source:





- This module shows no problem with operating in “readout all” mode, except on chips with large numbers of merged bumps, where it is necessary to enable only channels which have reasonable noise behavior.

General Observations on First Bare Modules

Two major differences relative to single chip operation:

- Significant noise increase for comparable operating point
- Instability of operation observed

FE Electronics issues:

- In FE-B, the pixel control logic operates on the AVdd supply, for convenience in supply routing. We can see that when the shift register is operated, large charges are injected into all of the pixels. When the measured noise level is very high, this disturbance can take some time (seconds) to disappear.
- In FE-B, the final stage of the discriminator is not complementary, and there is significant additional current consumption (about 10μA per pixel) when the discriminator is turned on. This is negligible when there are only small numbers of channels firing, but it drives the need for large local decoupling capacitors when the module is not very stable. Have observed that when single chips have large numbers of pixels firing, there is about 15mV modulation on AVdd.
- There are indications of non-ideal bump behavior (see later) from Indium bumps. In particular, the g_m of the input transistor, which sets a rough scale for the allowed series resistance, is 10^{-4}, so a resistance above 10K will cause significant increase in noise.

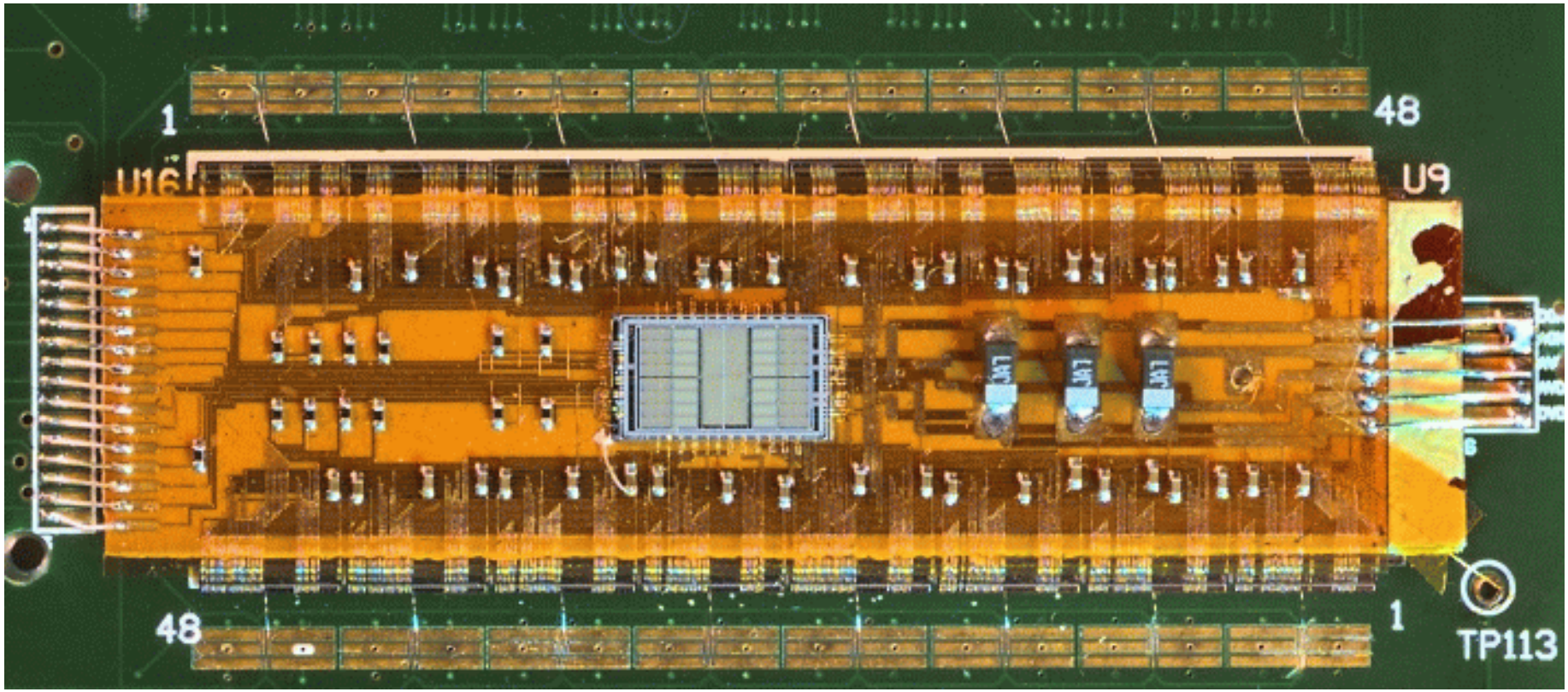
- There has been no high quality substrate contact in these tests. At best, chips are attached with conductive epoxy, but with no back-side oxide removal. In many cases, the back-side is insulated by thermal grease. Several back-side plated wafers are now being bumped for further exploration of the importance of this connection. Of course, these issues will be different in the buried oxide or SOI processes we will use for the final chips (the two rad-soft processes are both bulk CMOS)

High Noise:

- For most studies, the preamplifier feedback current was set to 5, corresponding to about 1.5 μs return to baseline for 20Ke charge. At this operating point, we typically observe about 110e of noise on both ST1 and ST2 detectors (single chip devices on the single chip support card).
- For the modules, minimum noise values in the range of 150-200e are observed. However, noise levels of up to even 400e or 500e have been observed. For some chips, these measured noise values change significantly from one threshold scan to the next in an apparently random way. Sometimes, there is even a corresponding “column-dependent” threshold shift observed.

Results on first LBL Flex module:

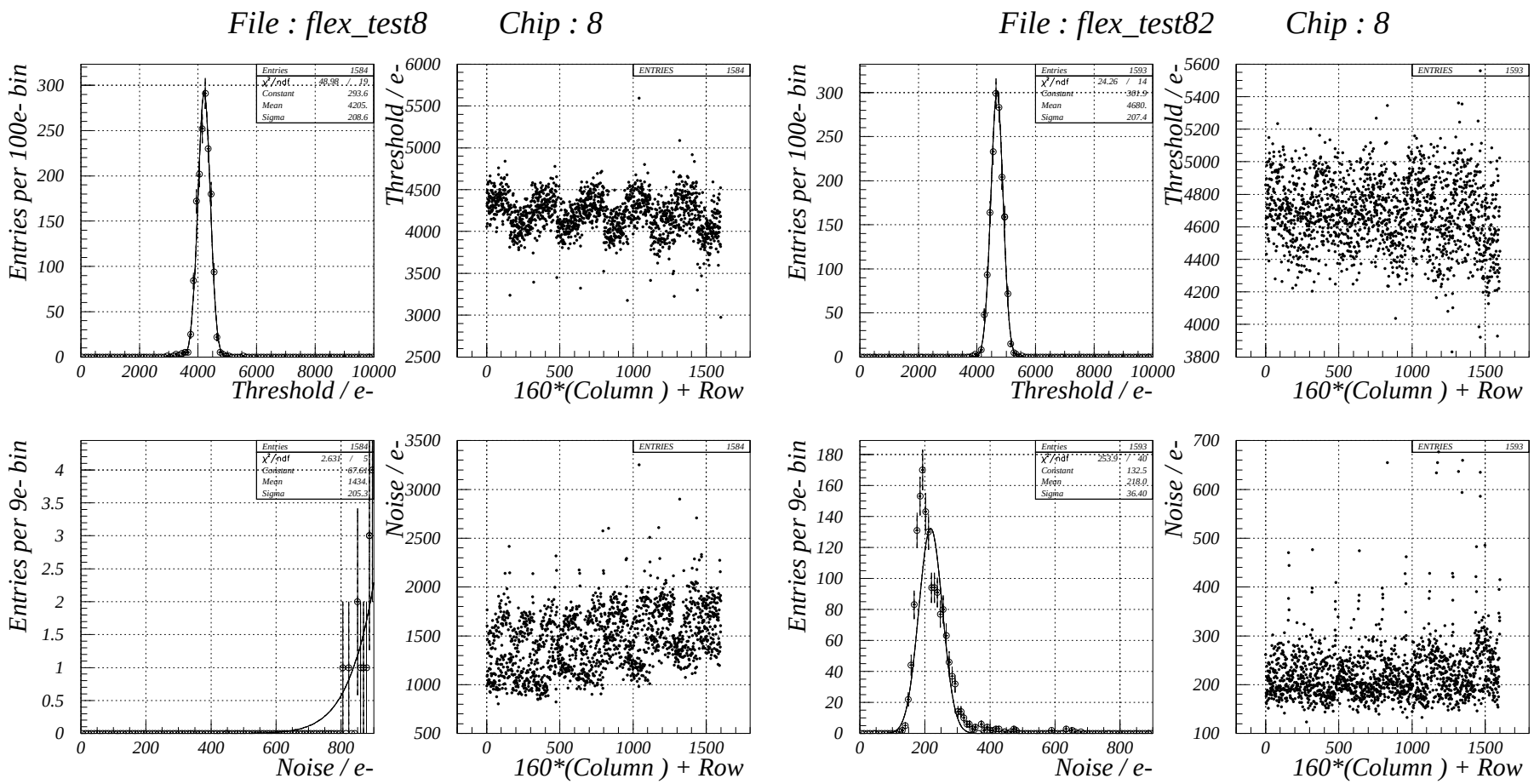
- Module was the last Boeing module, which was built using a CIS Tile1 detector and chips from a wafer that had been thinned to 150µ by GDSI. The thinning was done by cutting the wafer in half after bumping, protecting the bumps, and back-grinding. The dicing was done by GDSI. We had fun pulling the die off the dicing tape (tweezers don't work on such thin die...) The flip-chipping was done without any problems by Boeing.



Summary of Flex module behavior:

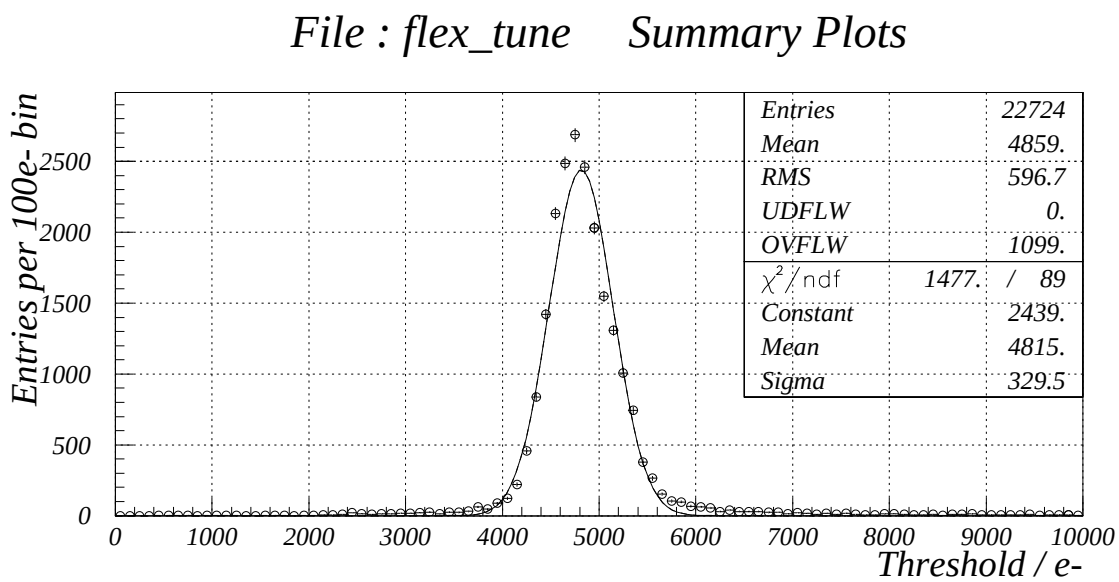
- All 16 FE chips plus the MCC work perfectly from the digital point of view
- Chip 15 does not respond to analog charge injection, although all analog nodes have correct signals and voltages when probed with picoprobe, and it operates correctly with a source in Hitbus mode.
- There are many bump-bonding problems, including several chips with regions of merged bumps. There are several very noisy chips that upset the operation of the entire module.
- No sign of high current state observed, in spite of the minimal decoupling (0.01 μF 0402 capacitors roughly for each chip), suggesting that better backside grounding is a contributing factor to this problem. However, if the module is operated with all chips operational (FE biasses correct), then it is very noisy.
- Noise levels are reasonable on some chips which have no serious bump-bonding problems, once the CINDAC (input transistor bias) is turned off on the noisy chips. Noise levels are very high on many other chips. Overall, this performance seems poorer than for “bare” modules, perhaps due to more limited decoupling, or perhaps due to problems from very thin chips. All results from this module are measured with CINDAC=1 on all chips except the one under study.
- Module was modified to add Hitbus source test capability (left off of the first generation Flex Support Card), and source characterizations were performed.

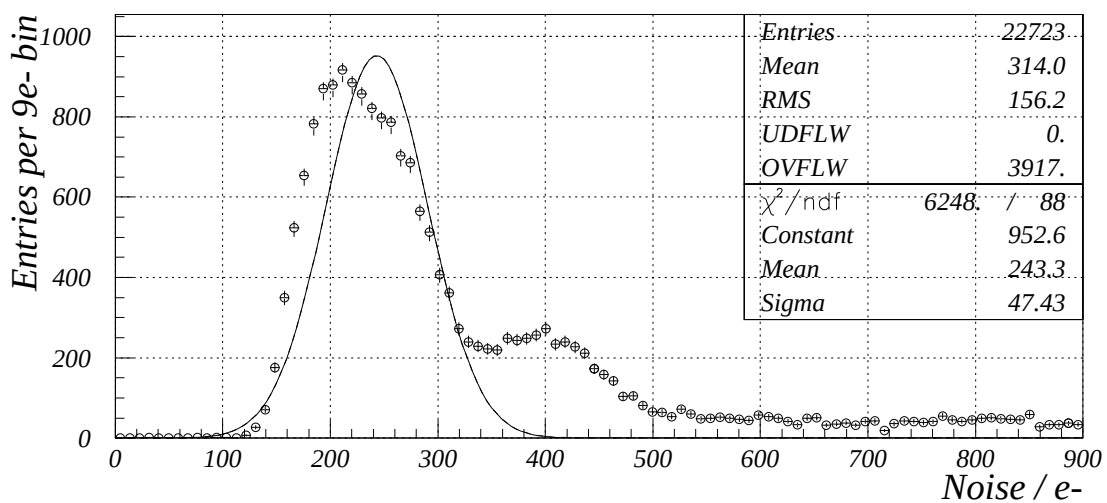
Comparison of behavior with all FE chips on, and all off except chip under test:



- Noise decreases dramatically from above 1000e to about 200e.
- The same improvement is obtained if the 3 worst chips on module are turned off

Summary of behavior of 15 characterizable chips:



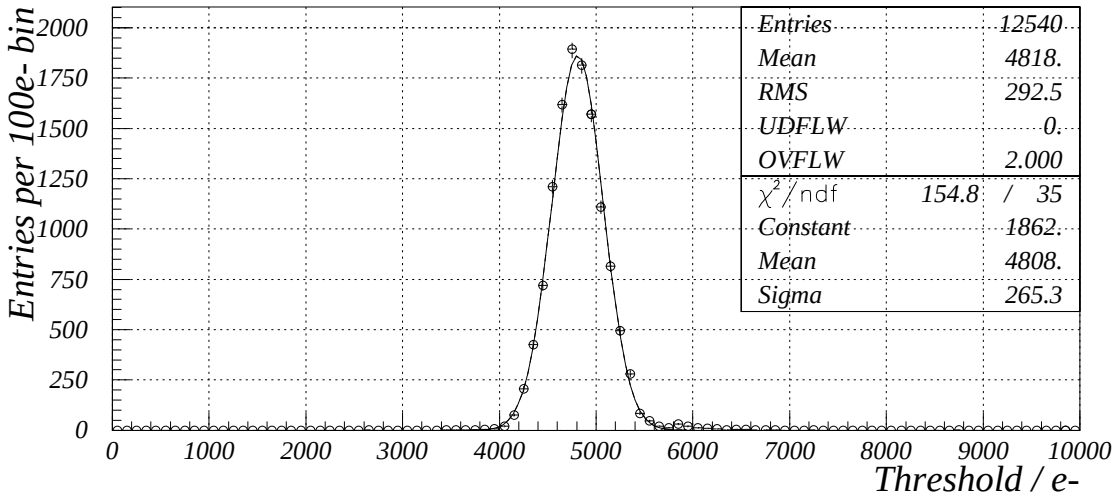


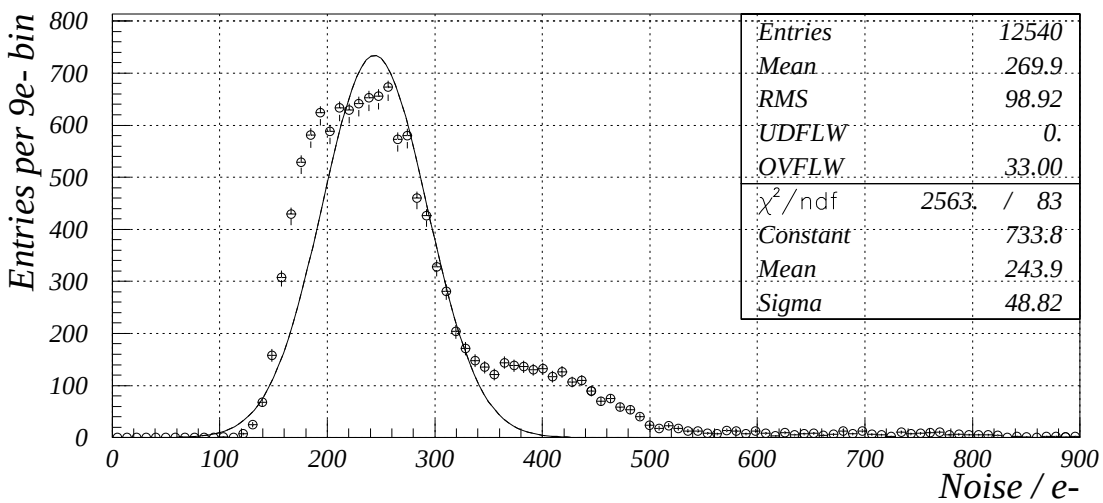
- Overall threshold dispersion is about 330e.
- Average noise is moderate for those channels in the plot, but there is a long tail, and there are several thousand off-scale entries.

- Note: all measurements made with CINDAC=1 on 15 of 16 chips

Summary of eight "good" chips (0,1,3,6,7,8,12,14):

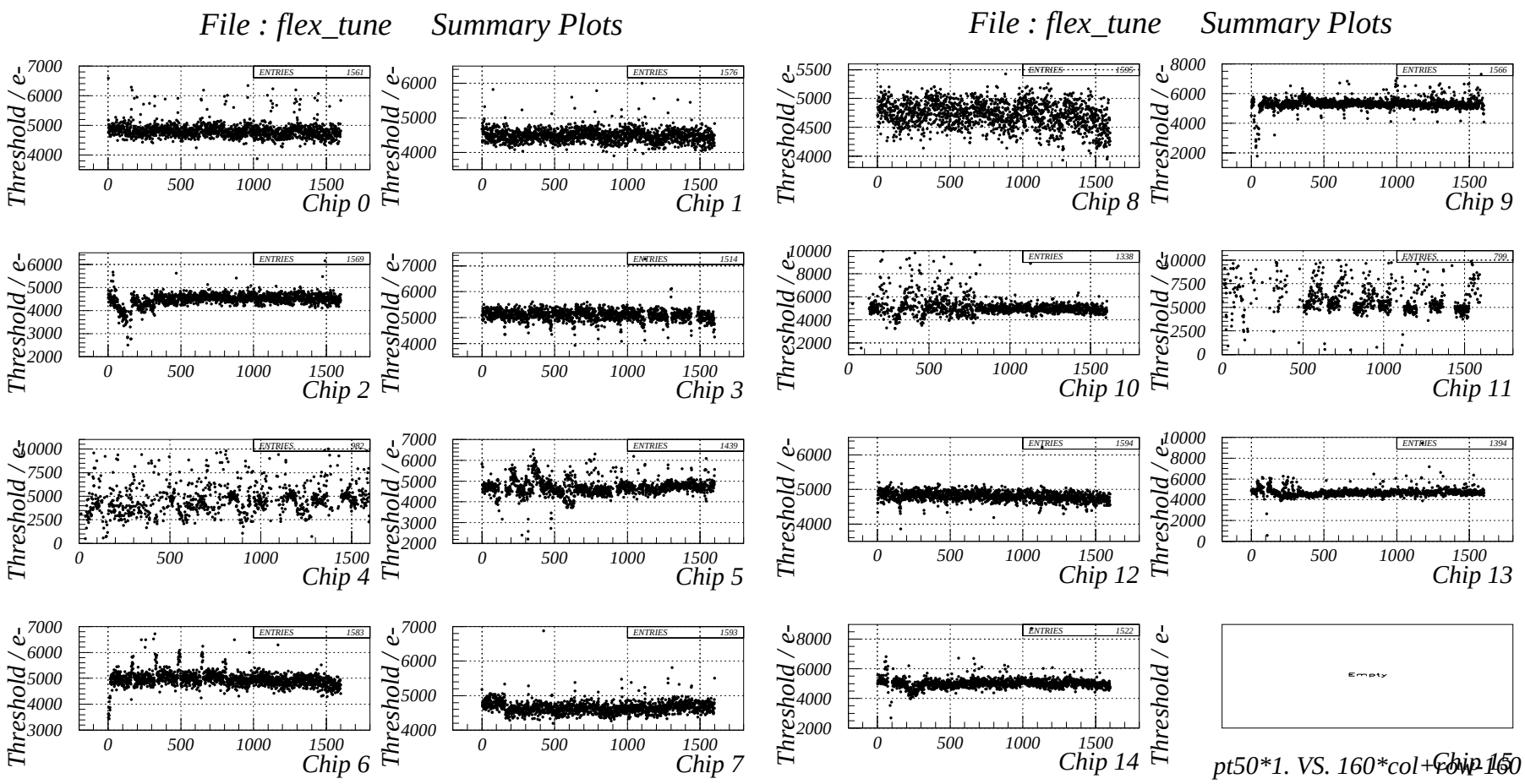
File : flex_tune_good Summary Plots



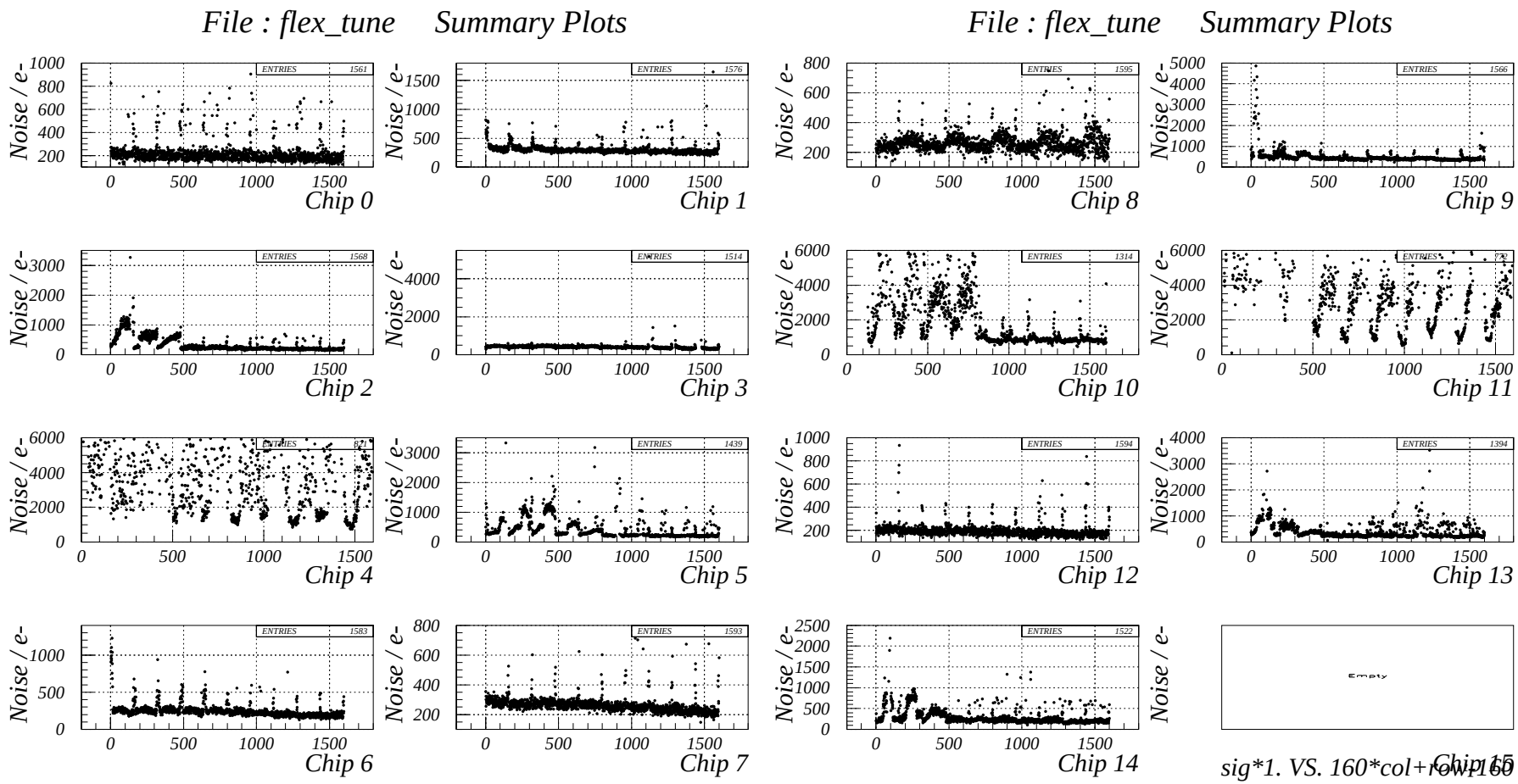


- Dispersion is reduced to 265e
- Very high noise tail has disappeared, with mean noise now 270e, and essentially no overflows.
- One of the good chips is right under the MCC (chip 12), so there is no indication that the presence of this bare die on top of the sensor causes any problems.
- Other good chips are at both ends of the Flex, so there is no indication of systematic problems due to power or signal bussing

Threshold behavior for individual chips:

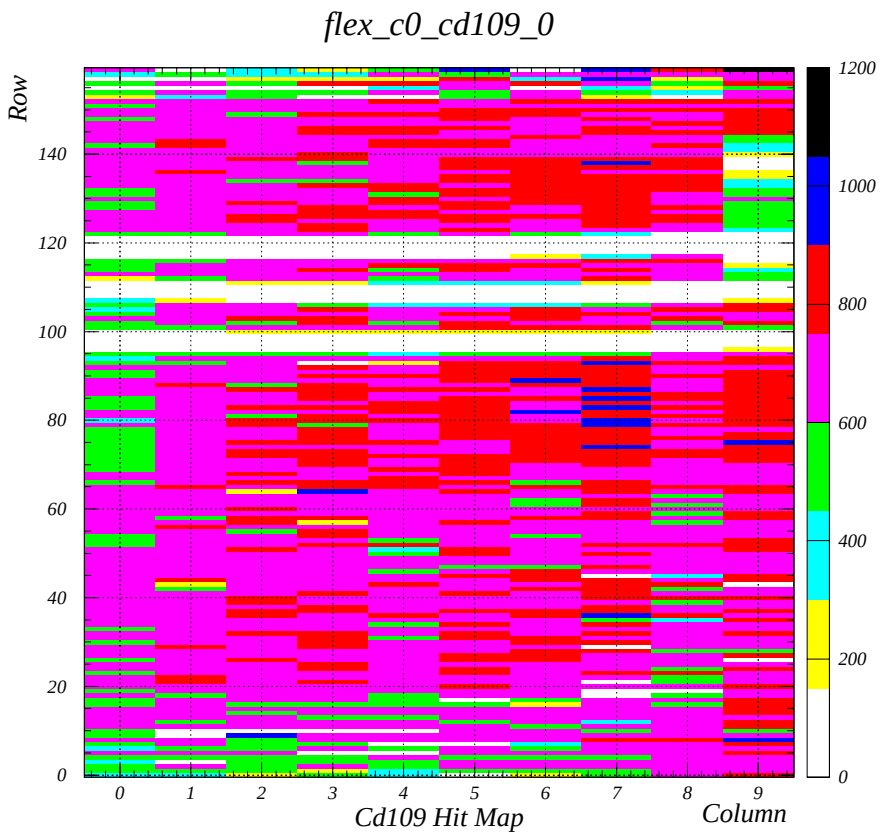


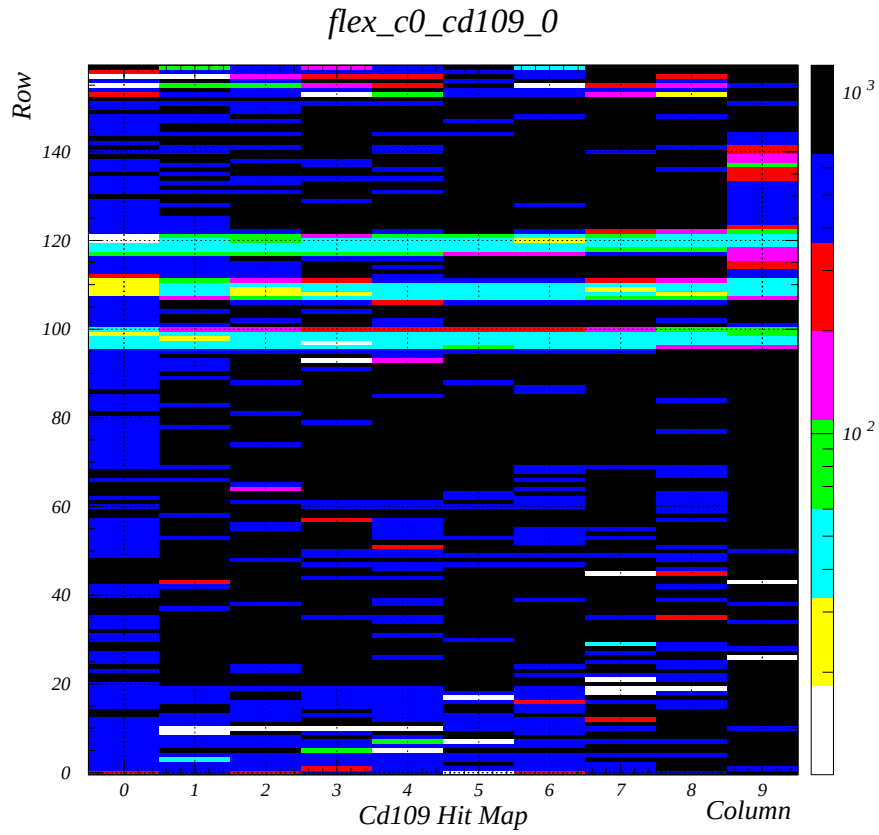
Noise behavior for individual chips:



- Chips 4,10,11 have extremely poor noise behavior, worse than anything seen before. Perhaps this is a problem with the thinned die.
- The good chips have noise behavior which is as good as that in “bare” modules.

Source characterizations with Cd109 source:



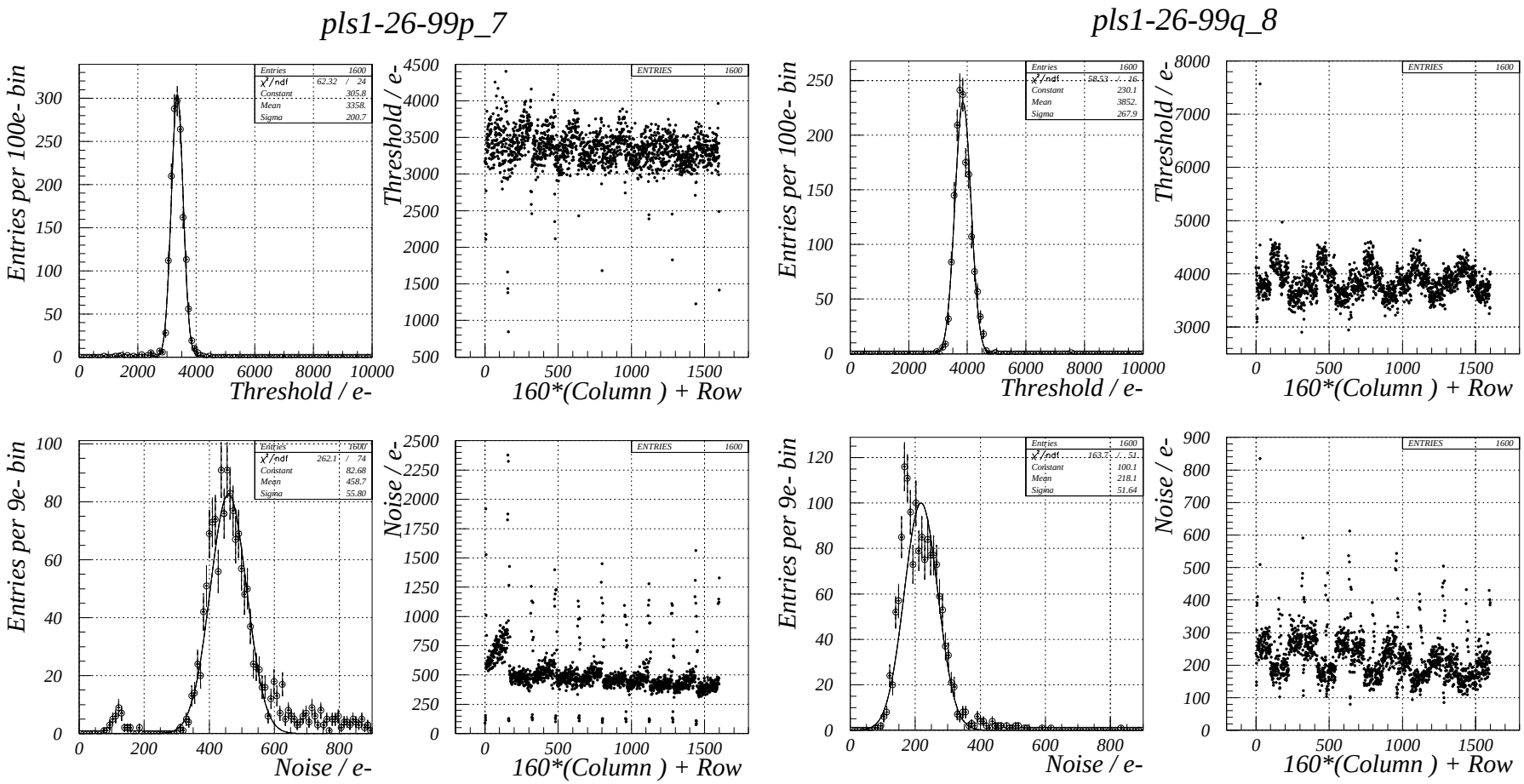


- The source is strongly attenuated in the material on top of the Flex. The three parallel lines are the leads of a Pt100. A termination resistor is visible in Column 9.

Results from first UOK Flex Module

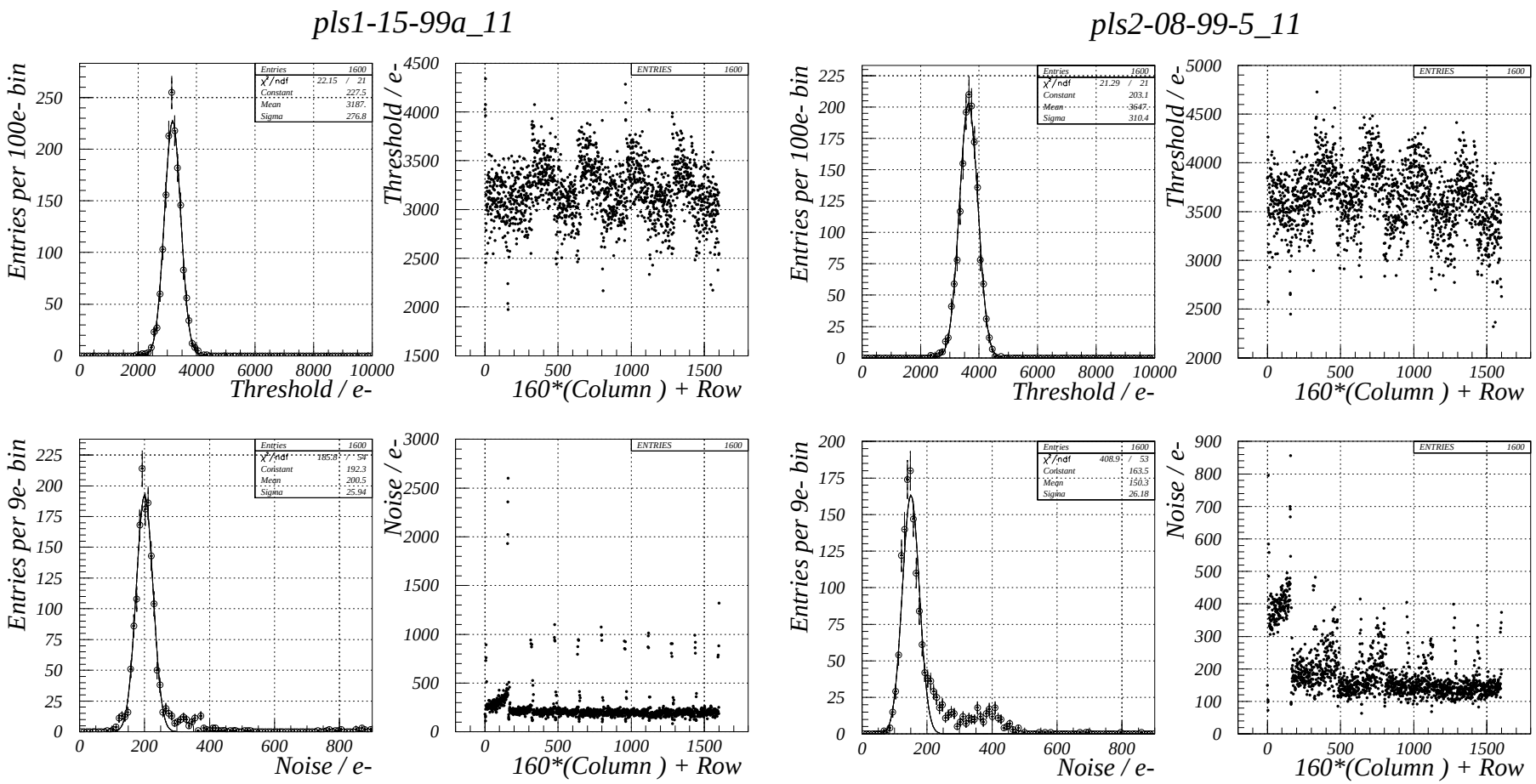
- Module was a 2M Tile 1 module bumped at Boeing. All assembly with Flex and Flex Support was done at UOK. The backside of the chips is electrically isolated from the Aluminum support plate by Kapton tape.
- Twelve chips work reasonably well, other chips have problems of varying severity.
- Small glitch in initial turn-on meant that module might have suffered a high temperature cycle of about 30 minutes, which could possibily explain relatively large number of chips which have problems.
- In this module, high current state observed when all chips operated at 4K threshold at the same time, and addition of 0.1μF instead of standard 0.01μF on LV supplies did not help this problem. This is different than the three LBL modules.
- All studies shown here were carried out by operating only one chip at a time (CINDAC set to 0 for others).

Threshold scans of two chips on the module:



- Some chips show relatively high noise always (500e), others show intermittent behavior of 200e or 500e).

Threshold scan of another chip twice:



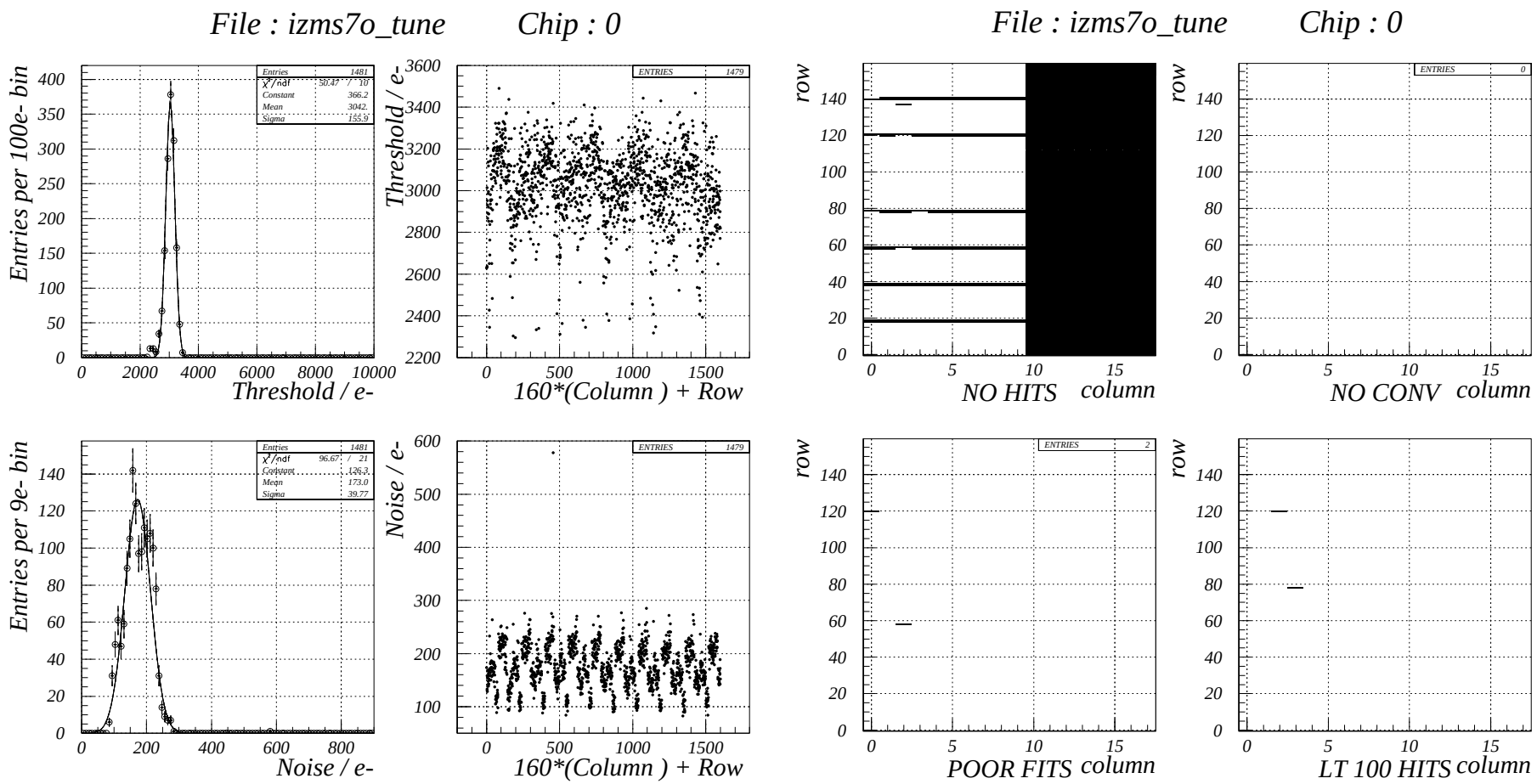
- Many scans of this chip always gave a noise of about 200e.
- Note the anomalous Column 0 noise behavior (expect less than 50% increase for 600μ pixel relative to 400μ pixel).

Single chip studies with different bump-bonding vendors

- Have compared two identical detectors, one with IZM solder bumps and the other with Boeing Indium bumps. The performance of the Indium bumped assembly was significantly worse, and shows clear evidence of resistive behavior.
- Sorting through our data on structures bumped by these two vendors, it is apparent that all of our good quality assemblies used solder bumps. In particular, there was a group of assemblies which we received in August, three identical ST1, and three identical ST2. All of the six assmblies had identical, and excellent, performance. The Boeing detectors typically show large noise and lack of threshold stability, neither of which are seen in IZM assemblies.

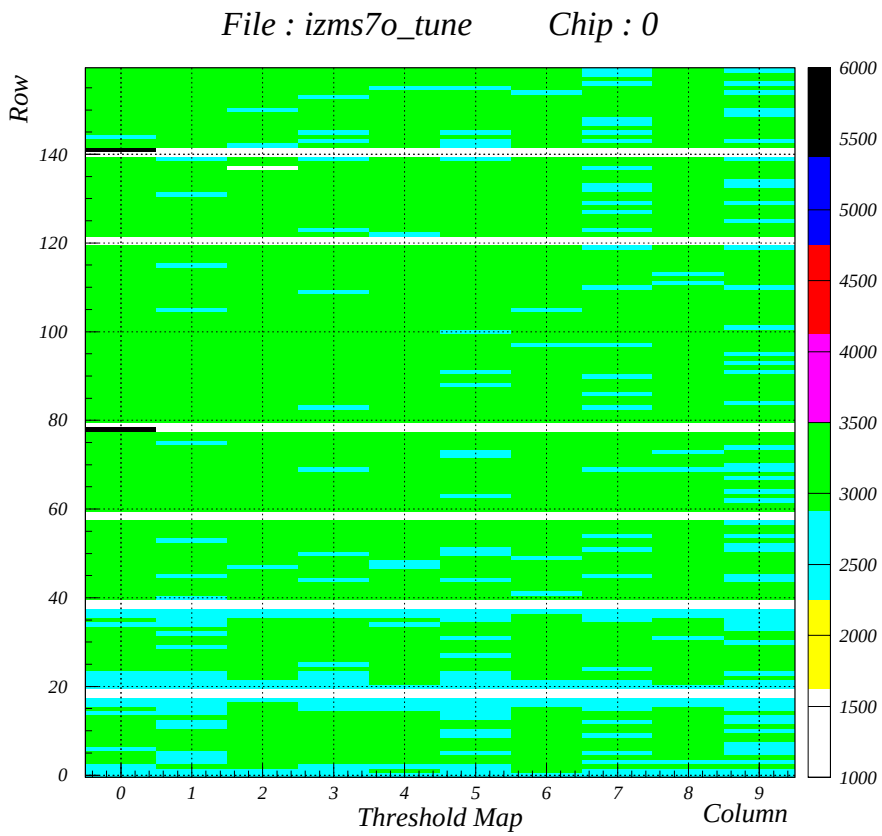
Measurement of IZM and Boeing S7O assemblies:

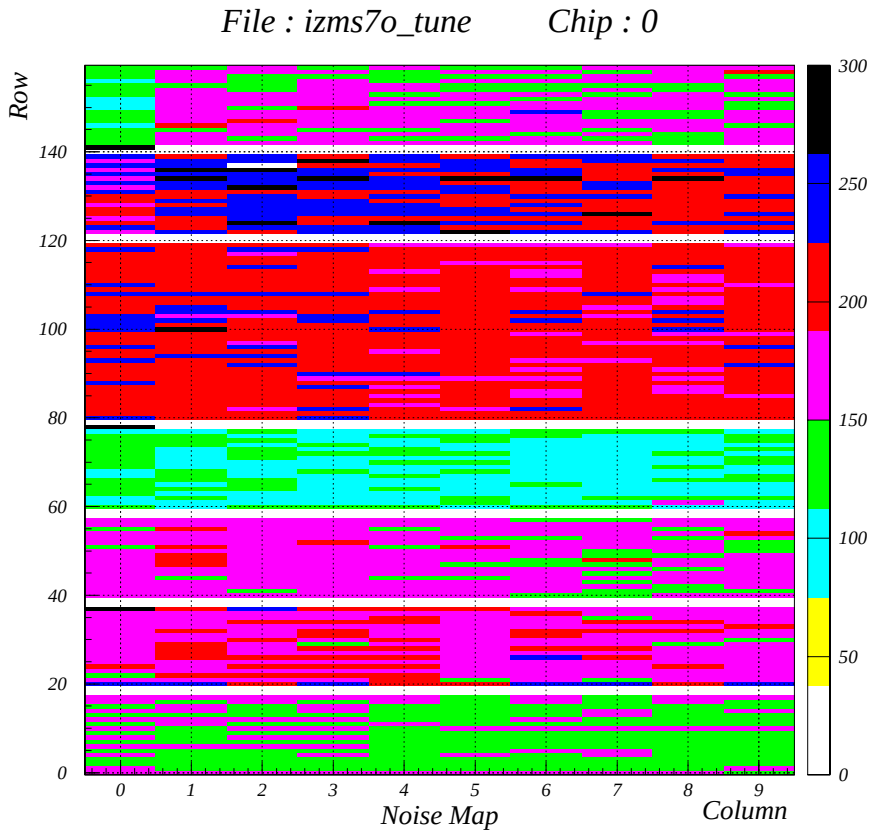
- IZM assembly has good performance, and was tested in H8 in August:



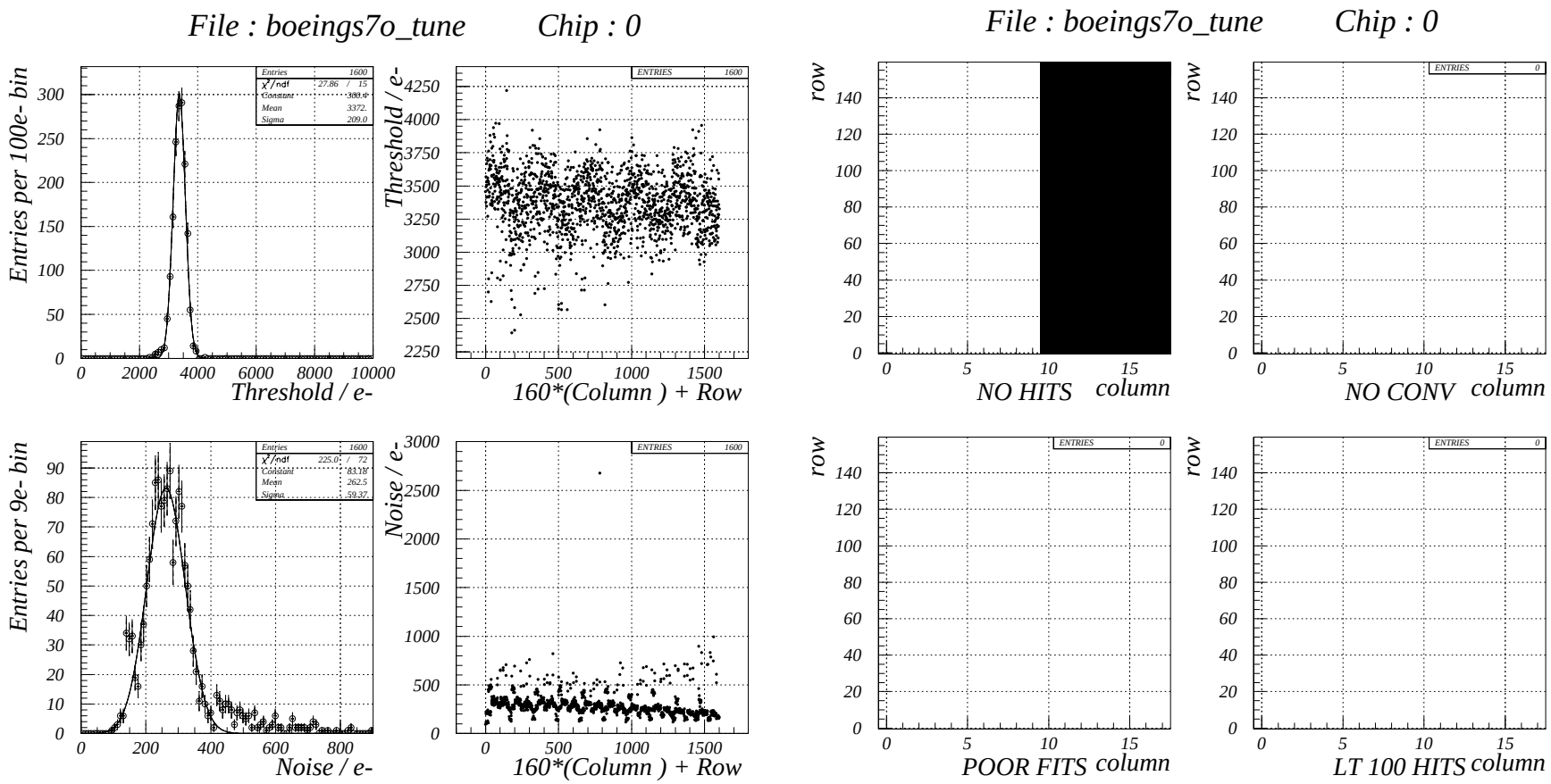
- Regions between each of the seven zones look dead, since those channels are all connected to a common metal guard ring.

- Threshold and noise maps look uniform within each zone, and behavior in the different zones matches that seen in complete single chips (at least for SSG and ST2):



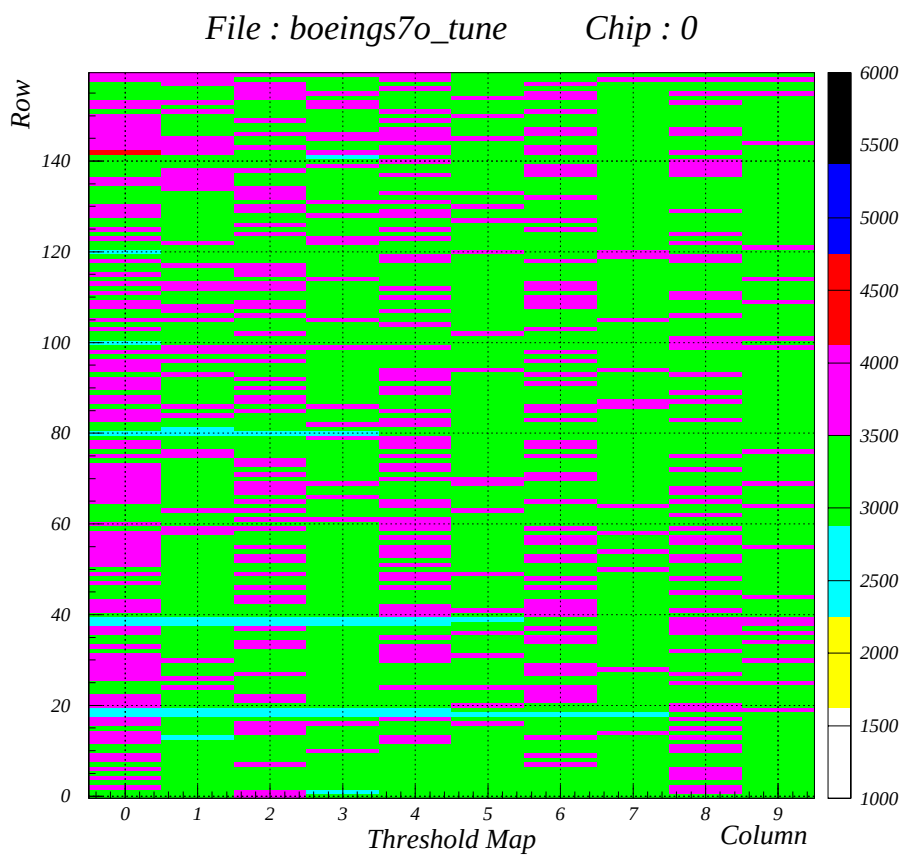


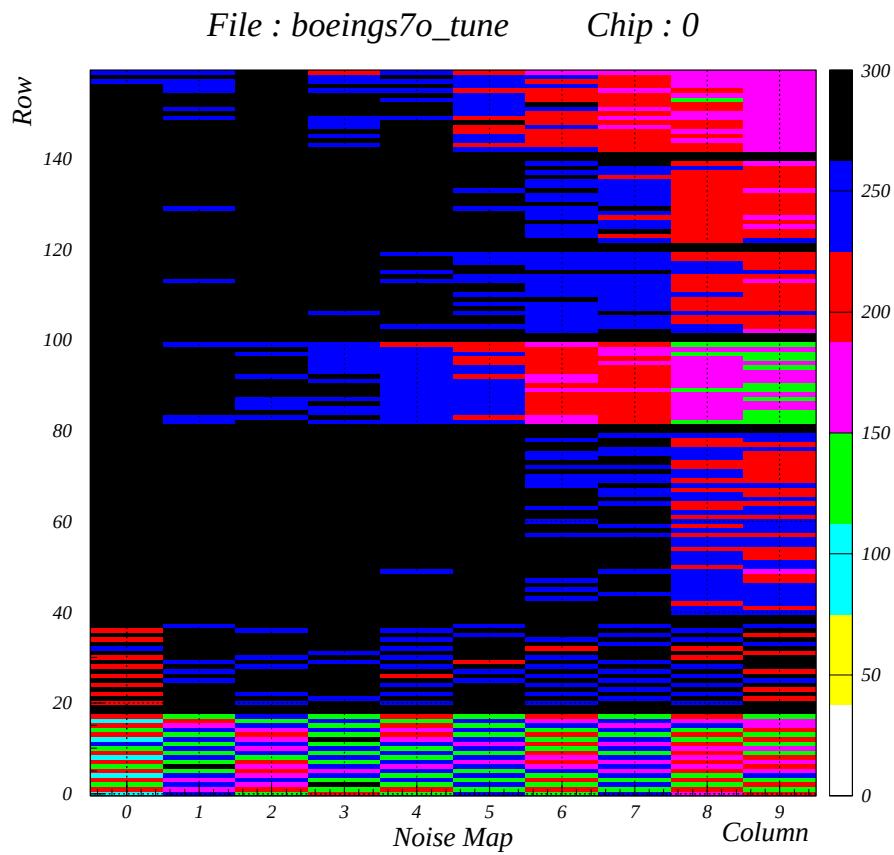
- For Boeing assembly:



- Noise is higher than for IZM assembly
- The regions between zones are not dead, but are only noisier than adjacent channels connected to the detector. For different channels which are connected together to work, the resistance must be large (more than 10 KOhm ?)

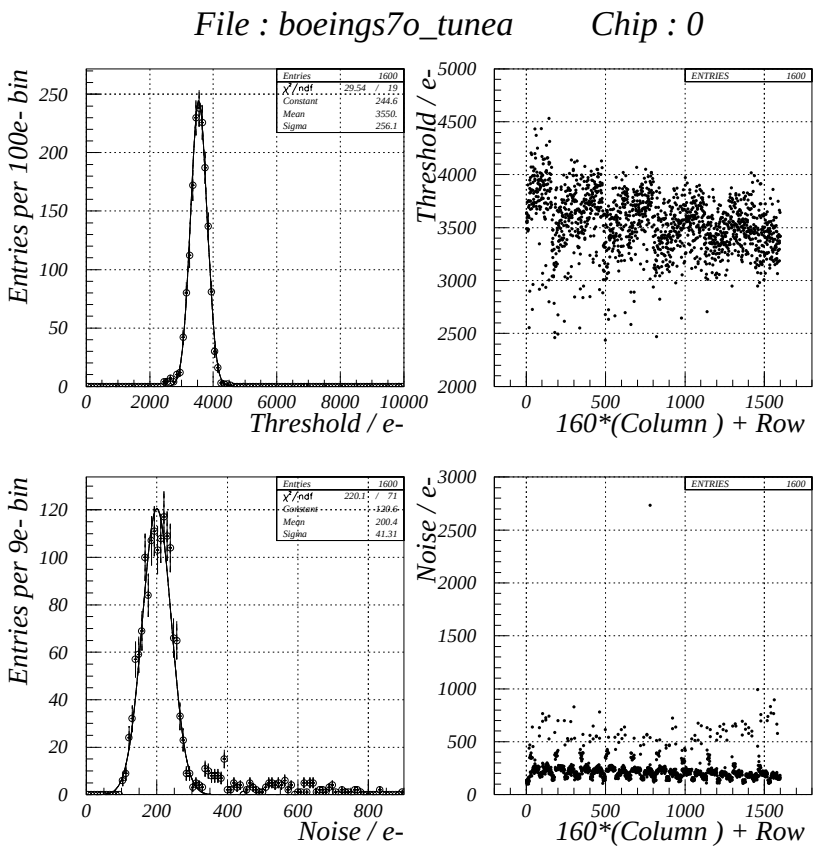
- Threshold and noise maps:

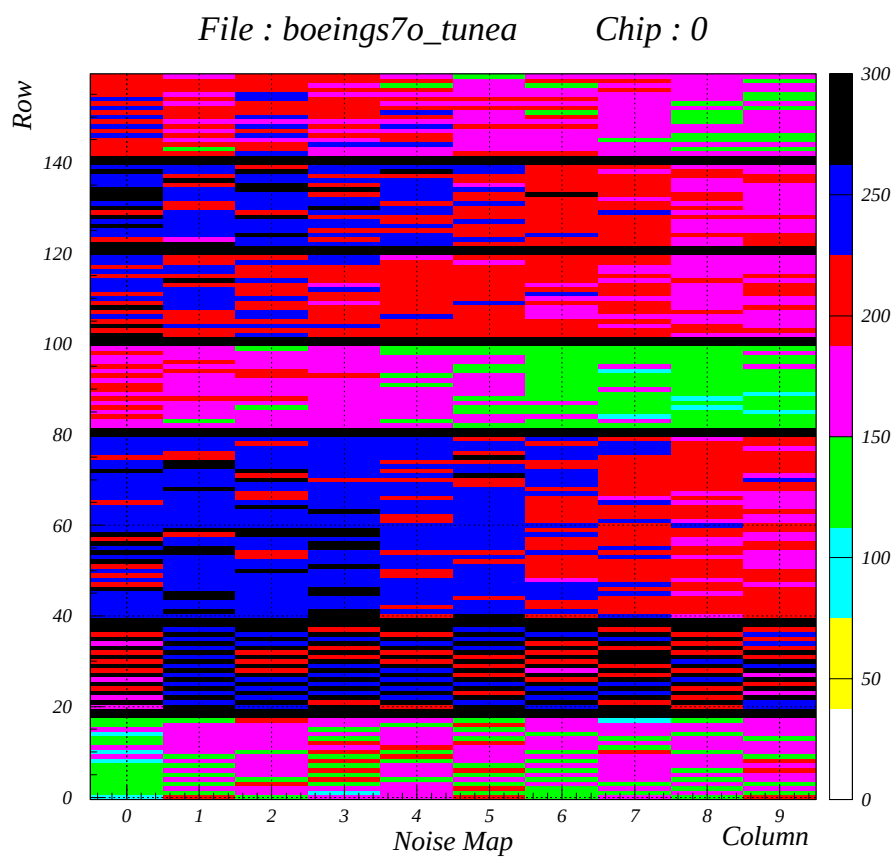




- See significant increase in noise, and it is now not uniform within a given zone of the detector.

- Perform additional threshold scans:





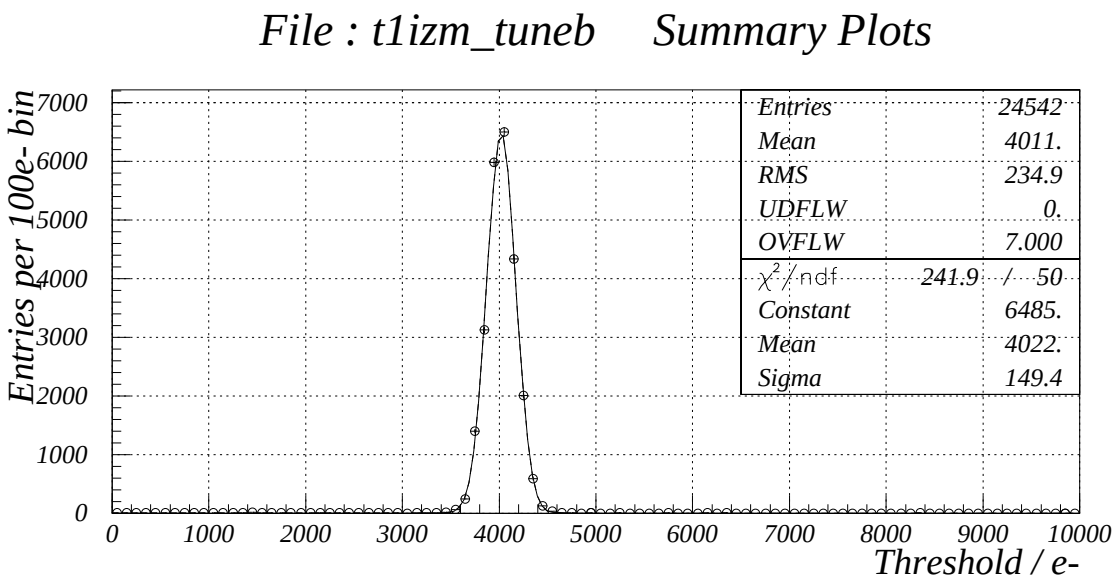
- In this particular scan, the noise is lower and more uniform. Several subsequent scans look more like the first scan (high level of non-uniform noise).

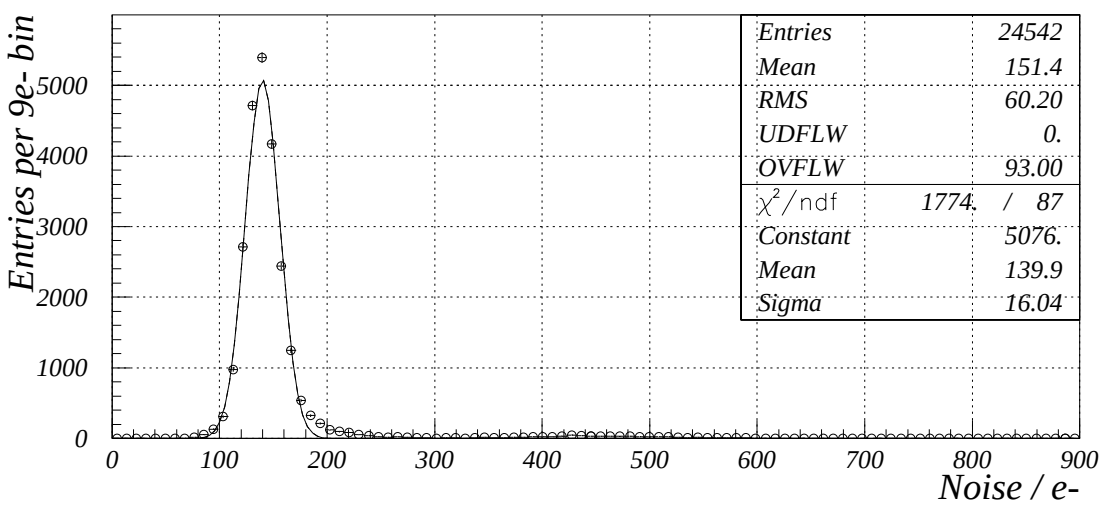
Results from First Solder-bumped Module

- Module was first tested last week. It is configured as a “bare” module, and is the first to use the second generation of module support card. It uses a CIS Tile1 detector (a second module with a Tile2 detector was broken in transport).
- It was X-rayed before assembly, and a large number of bumping defects were observed, primarily merged bumps. The match between defects observed with X-ray scan and problems observed in module is quite good, but not perfect. In addition, there are many channels not connected to the detector (no source hits observed), but their measured noise is similar to channels which work correctly. All of the chips were displaced outwards by 100μ (two rows), leaving two dead rows and two unconnected rows. This suggests significant Q/A problems at IZM.
- We continue to have problems wire-bonding assemblies from IZM, perhaps due to thicker Al oxide formation during high temperature steps in bumping.
- All 16 chips work perfectly from the digital point of view (digital injection). Threshold scans and source scans have been carried out on all chips.
- The good news is that this module behaves in a manner very similar to the single-chip structures. The noise level is only slightly higher (130-140e) than that observed in single chips (110-120e), and uniform, reproducible values are found for thresholds and noise. In spite of the large number of bumping defects, it has very acceptable performance. This demonstrates that many of our module problems up to now were related to the poor conductivity of the Boeing bumps.

Summary of threshold and noise performance:

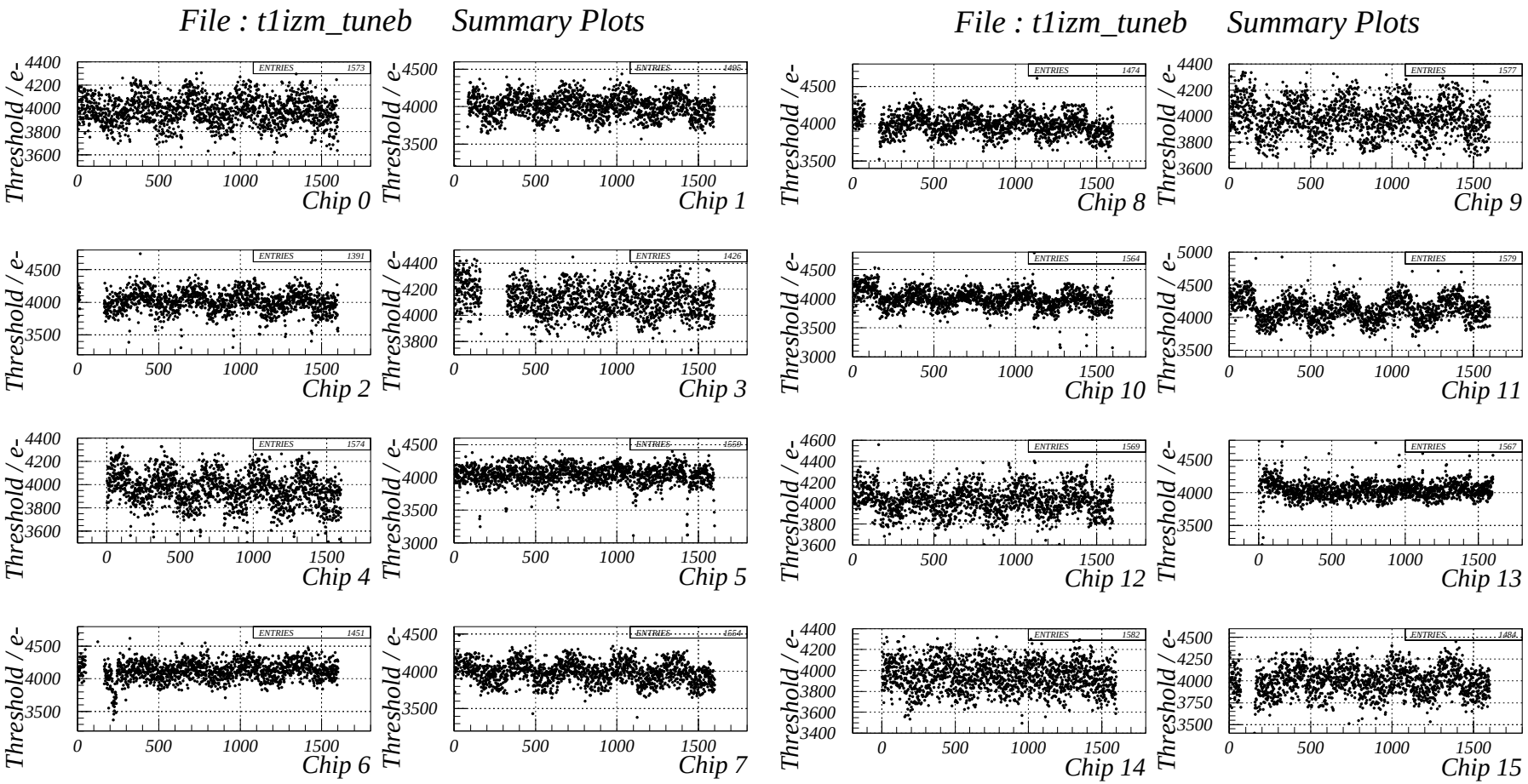
- Thresholds have been tuned to 4Ke for all chips:





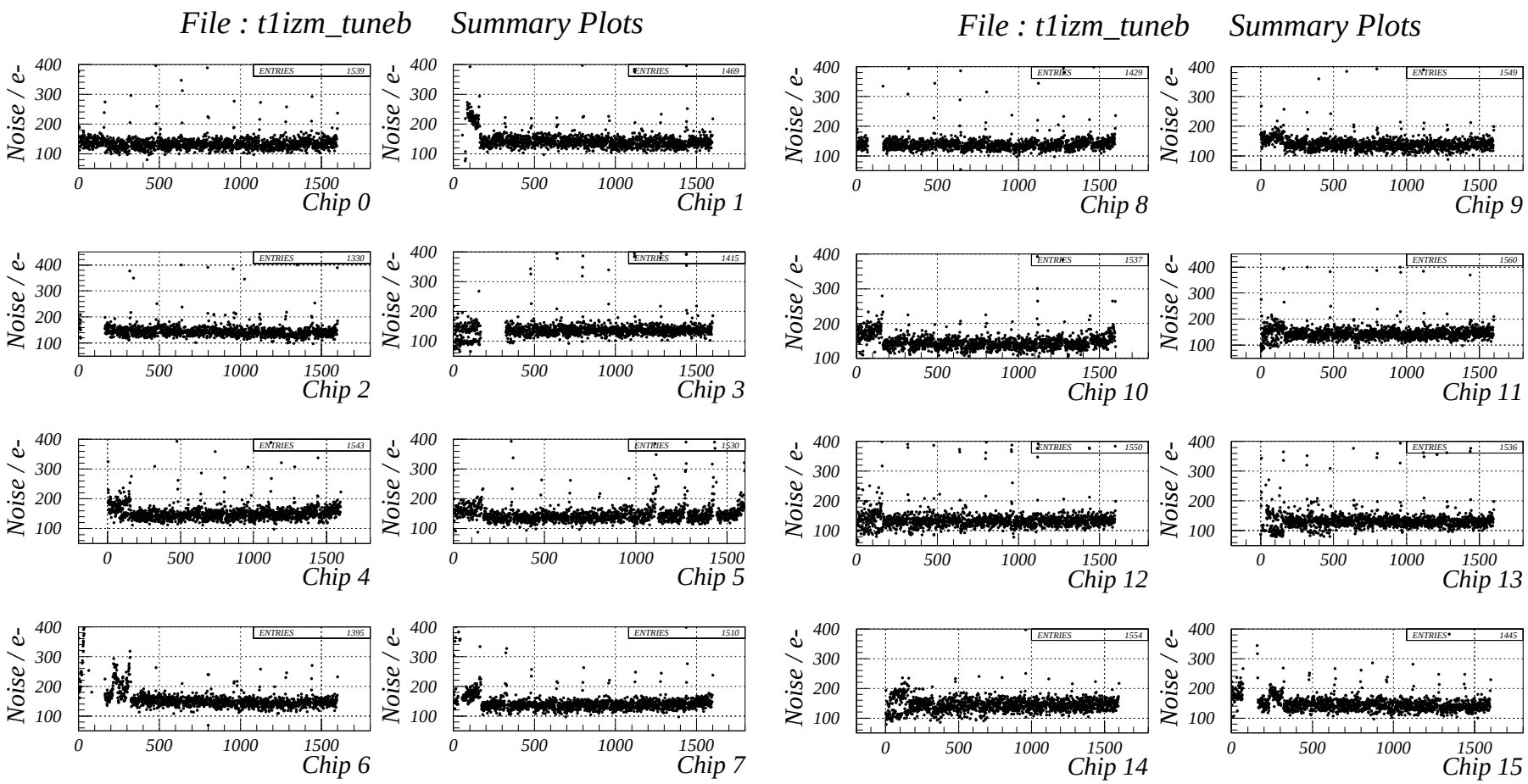
- Excellent threshold dispersion observed over the complete module (150e) after tuning overall thresholds of individual chips.
- Excellent noise performance observed over the whole module (140e).
- Approximately 1000 dead channels, many concentrated in some bad columns on several chips. The number of bad channels expected from X-ray scanning is more like 250, so this is a surprise.

Behavior of thresholds for individual chips (zoom):



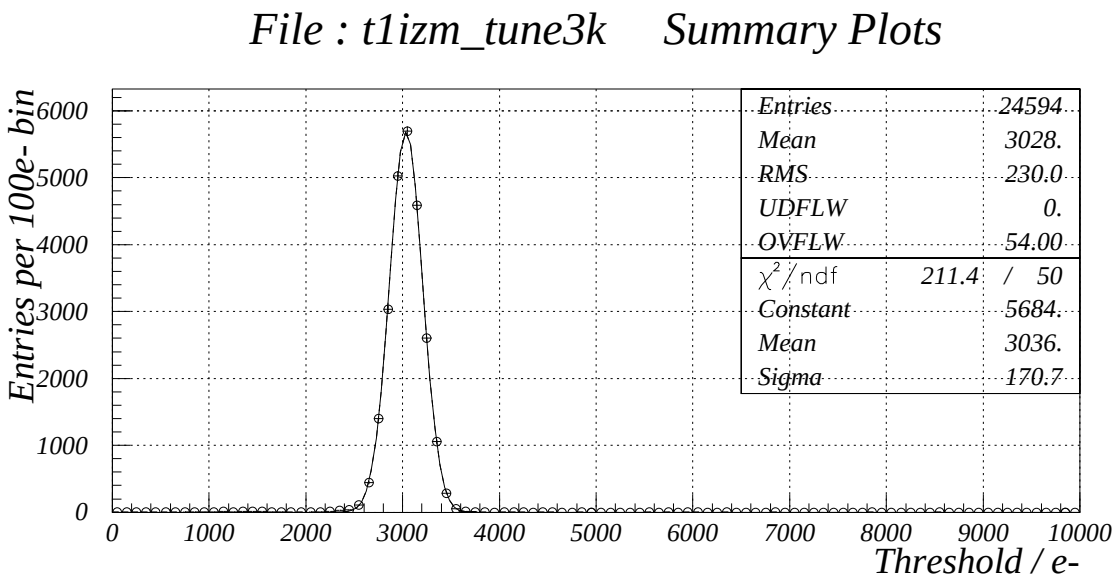
- Excellent uniformity is seen after tuning

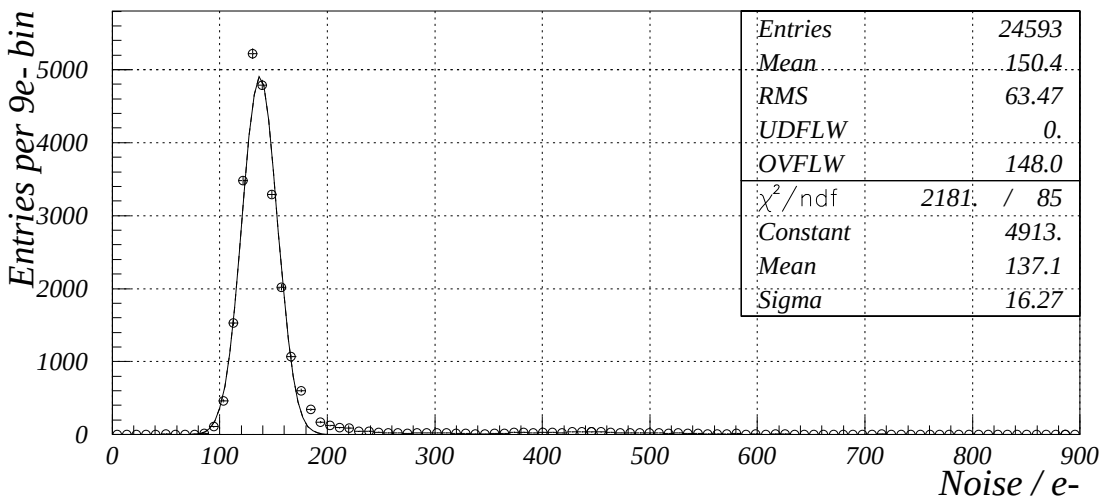
Behavior of noise for individual chips (zoom):



- Very uniform noise distributions, with the exception of the (very often) bad column 0 regions, which seem to have large numbers of bumping defects.

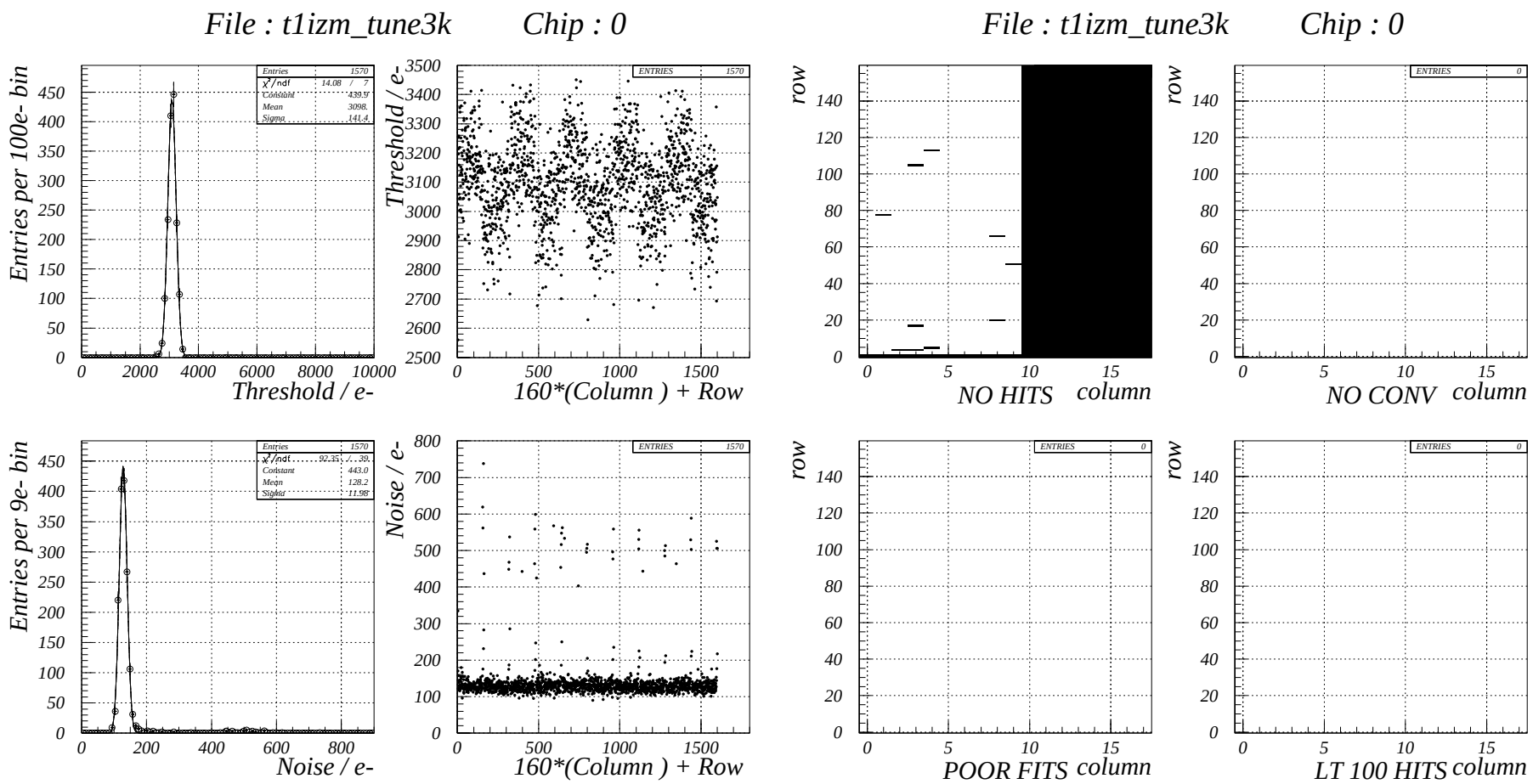
- Have also tuned thresholds to 3Ke (without retuning TDACs):





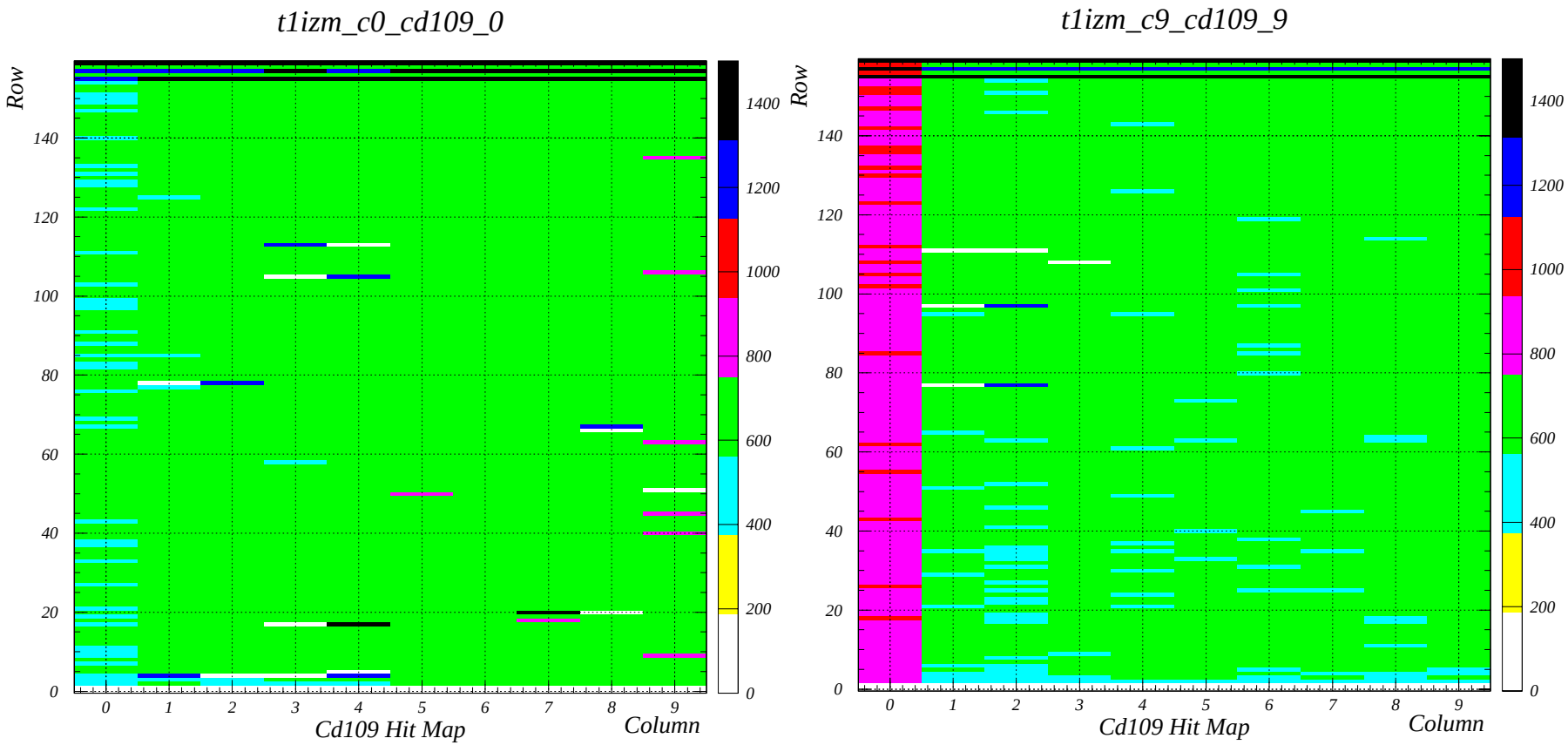
- Threshold dispersion increases slightly from 150e to 170e due to extrapolation (optimal performance requires retuning for each threshold)
- Noise performance is identical.
  - At this threshold setting, have taken HitBus source runs without any operational problems besides single isolated noisy pixels due to bump-bonding problems.

Behavior of single chips for 3Ke threshold:



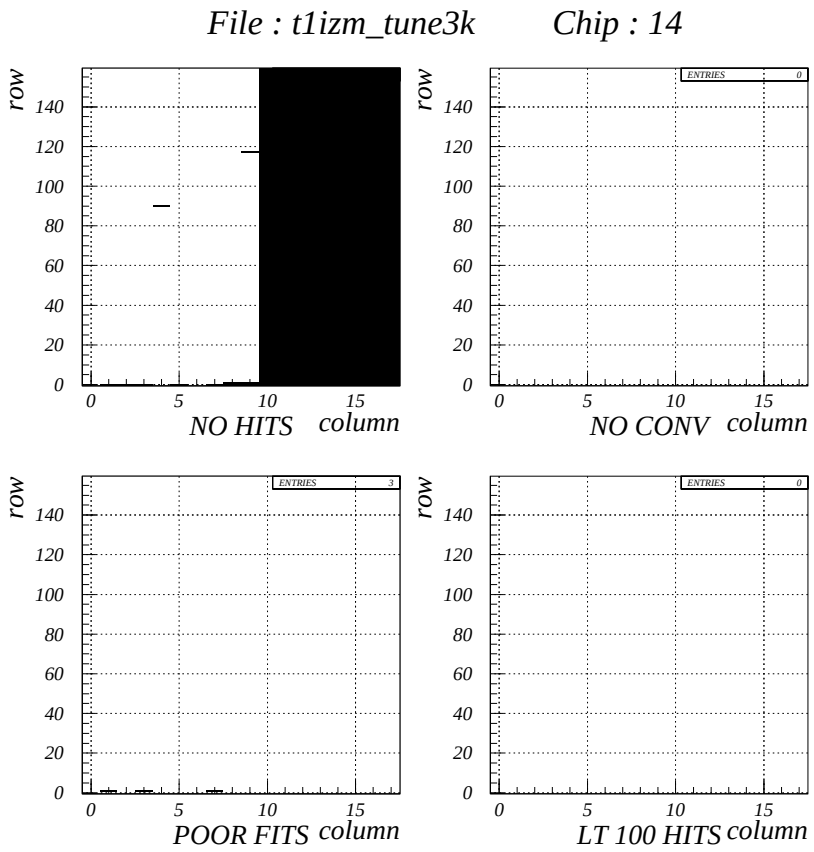
- Isolated dead channels (due to bump merging)
- Very uniform noise behavior. Threshold non-uniformities come largely from TDAC tuning at different threshold, and are small.

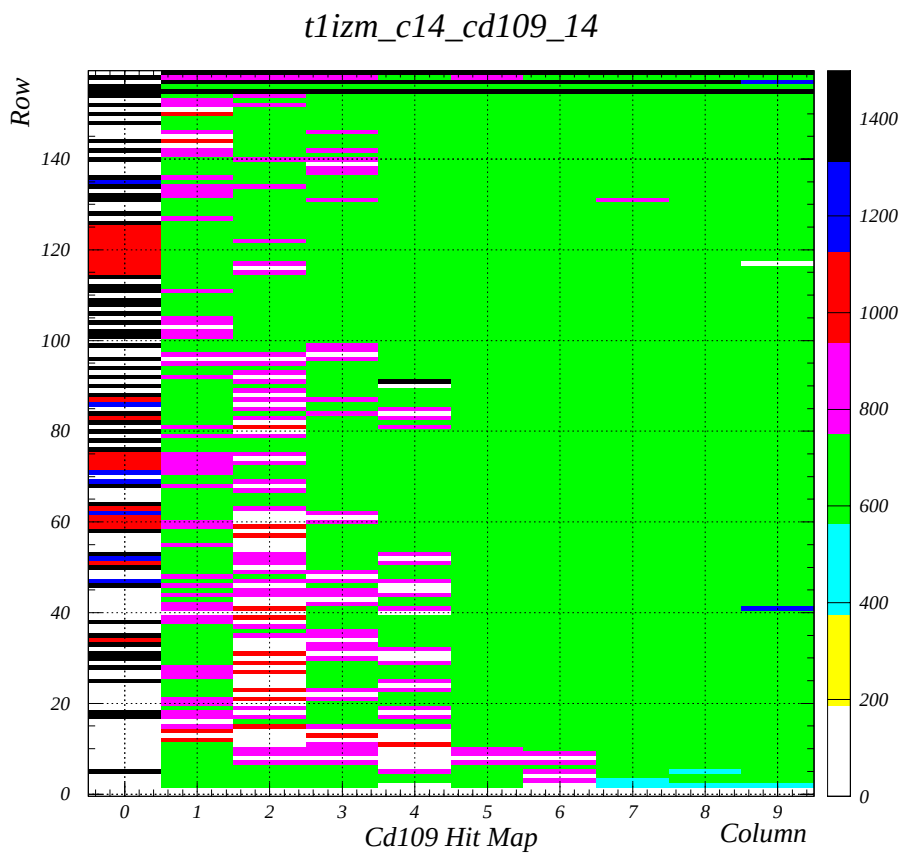
Behavior of good chips with a Cd109 source:



- Indications of merged bumps: dead channel next to a channel which counts extra hits.
- Column 0 pixels are 600μ long in all chips except those on the module edge (chip 0 and 8).

Behavior of bad (unconnected channels) chip with a source:





- Very few bad channels observed with charge injection.
- Very large number of bad channels observed with source. However, noise level is barely distinct from working channels. Perhaps this is in part because bumps are deposited only on electronics side, so additional capacitance is smaller.

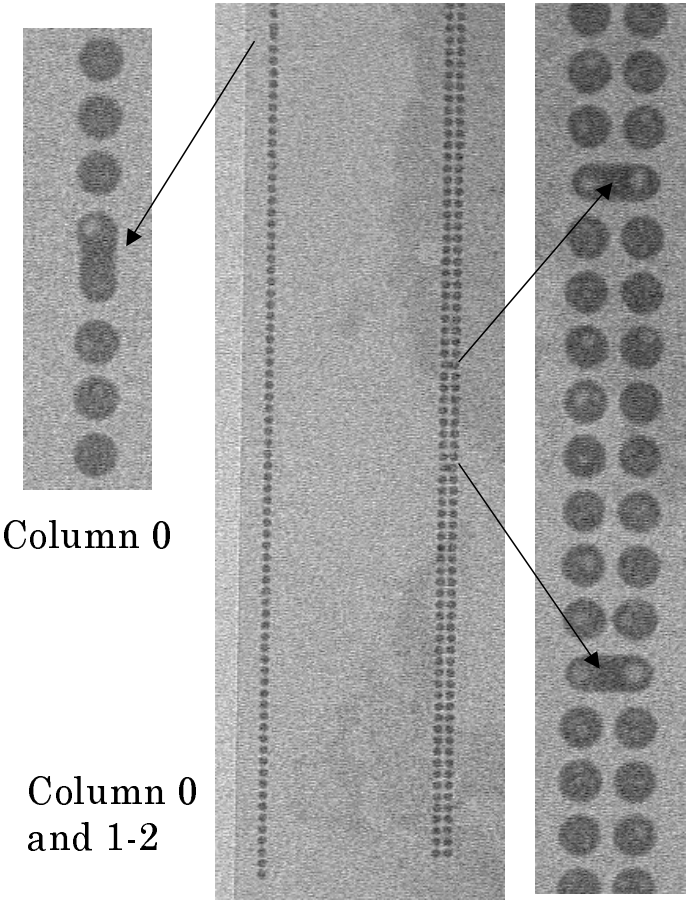
Operation of the module with all chips enabled:

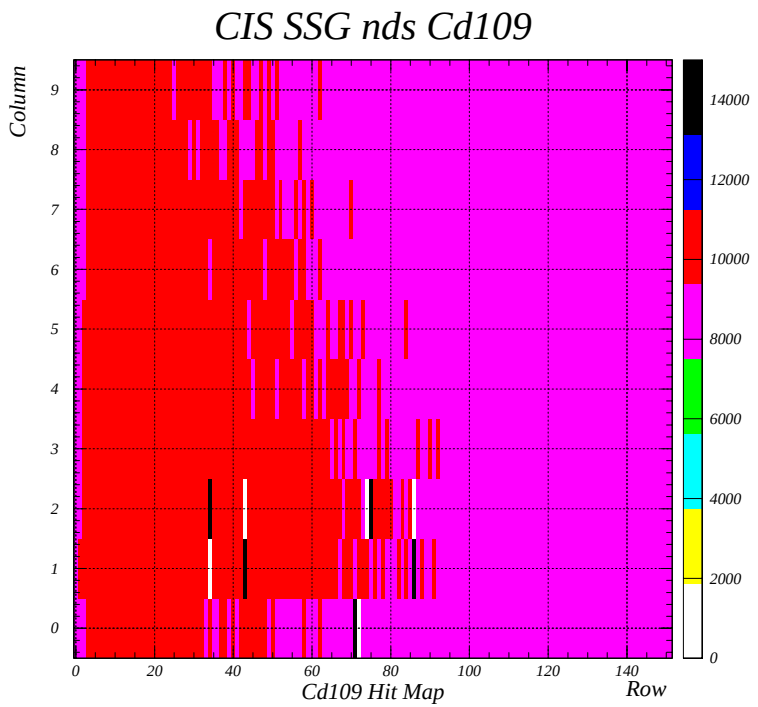
- After operation of single chips at 3Ke threshold with the Cd109 source, appropriate mask files were produced to eliminate “noisy” pixels. In this way, the overall counting rate for the FastOR of the entire module was reduced to less than 10 Hz with almost 25K enabled channels.
- Threshold scans under these conditions produced similar noise performance to that observed with only the injected channels on a single chip enabled for readout (the default calibration method).
- Source scans were done with readout enabled on all chips simultaneously (self-trigger rate is 70 KHz for this configuration using our Cd109 source).
- The resulting operation was stable, and produced reasonable source maps. Operation in full MCC mode was also successful.
- This is in some ways even more demanding than LHC operation because it is a self-triggered mode, where it is enough for one pixel to fire in order to cause a trigger and subsequent readout.
- Now we need to upgrade our software to process data from 16 chips simultaneously (monitoring 50K channels takes a lot of memory), and we can exercise modules completely.

X-ray Scanning of Bumped Assemblies

- Using a high-resolution X-ray scan system, have examined several devices. Merged solder bumps look like this:

Active Devices - SSG(Solder Bumps)





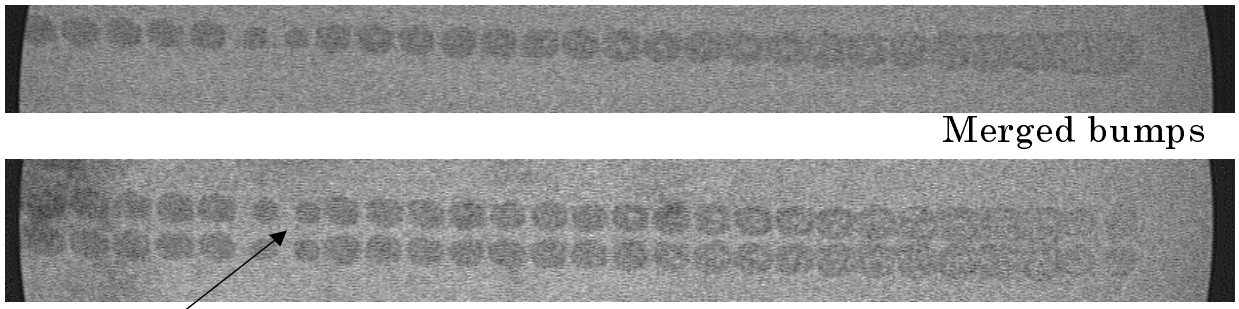
Complete correlation between pairs of dead and double rate channels with bridged bumps

M. Gilchriese - January 20,1999

8

- Boeing Indium bumps look different when there are problems:

Active Devices - S80(Indium Bumps)

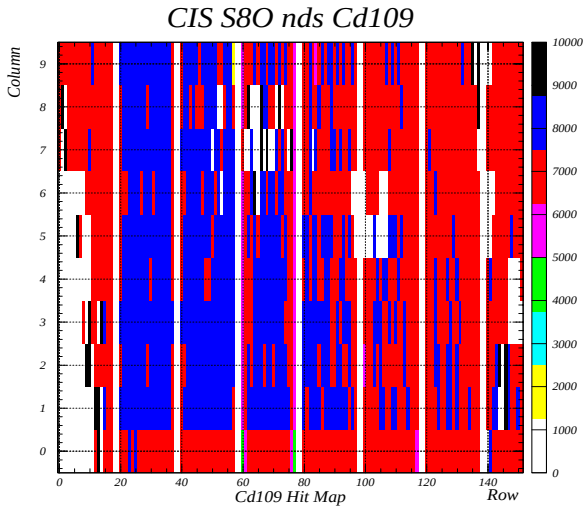


Column 0
Rows near 0

Merged bumps

Columns 1-2
Rows near 0

Unattached region



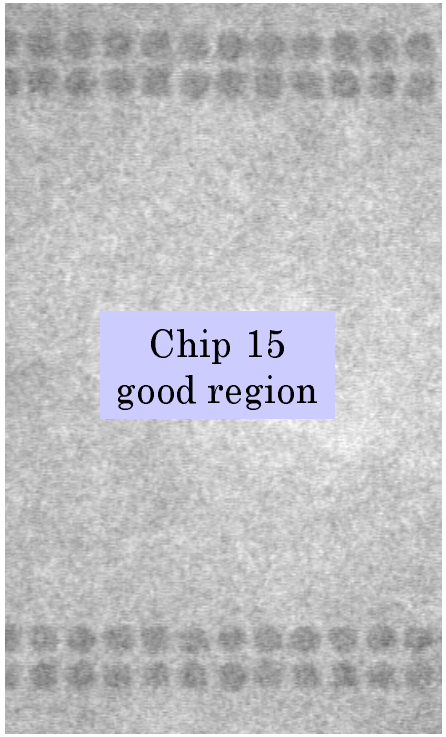
9

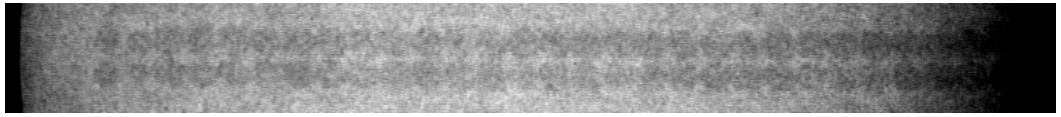
M. Gilchriese - January 20,1999

- In this case, many bumps can merge in a large region and produce extended groups of dead channels.

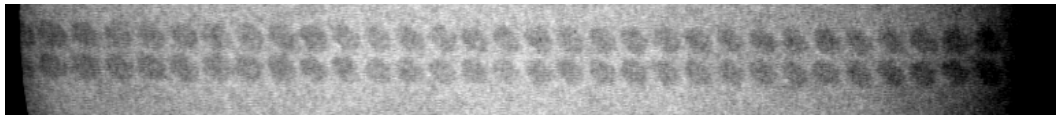
Original Tile2 Module X-rays:

Module(Indium Bumps)





Chip 4 column 3-4 bad region



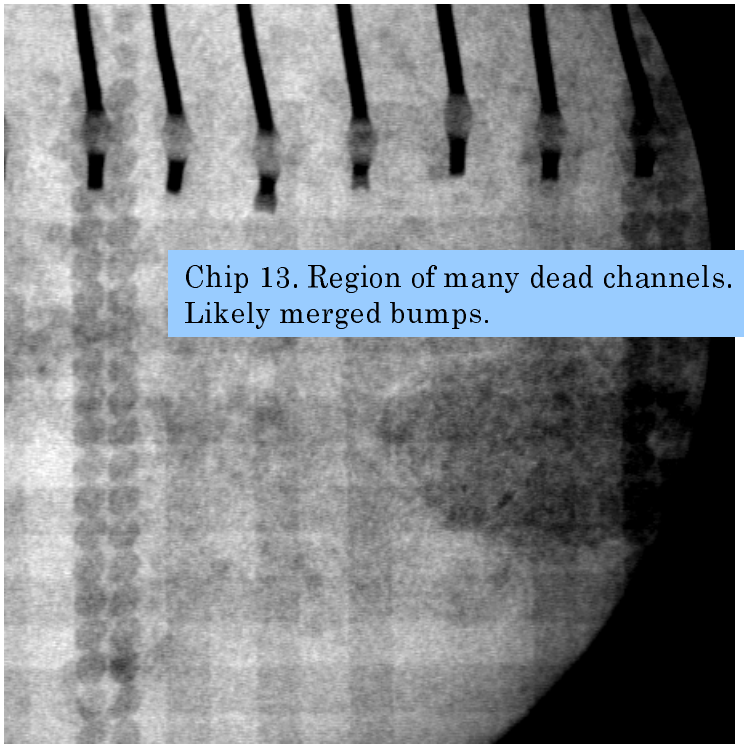
Chip 4 column 3-4 good region

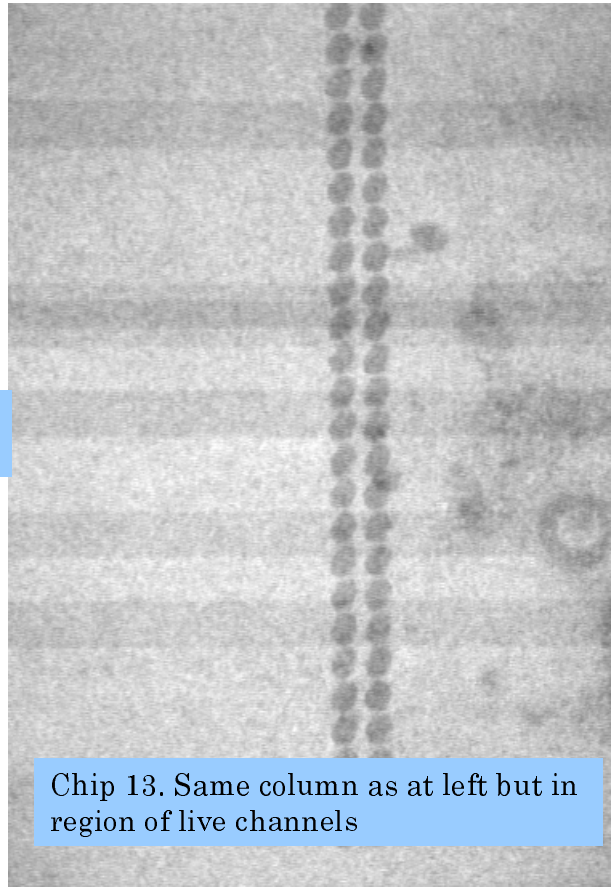
- Resolution not as good with module on top of aluminum plate
- But still clear correlation between dead channels and regions of merged/bridged bumps
- Simple mechanical modifications to support would be needed to improve resolution - mill out hole in plate.

Flex Module X-rays:

Flex Module

- Boeing indium bumps. Mostly see dead regions correlated with merged bumps. Still need to do more correlation with source scan.





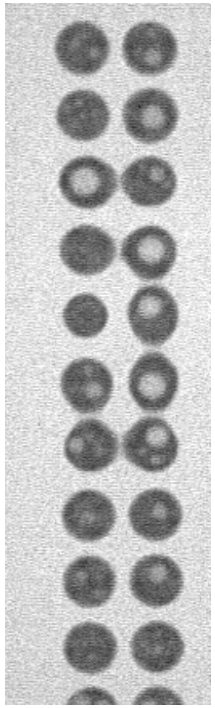
18

M. Gilchriese - January 20,1999

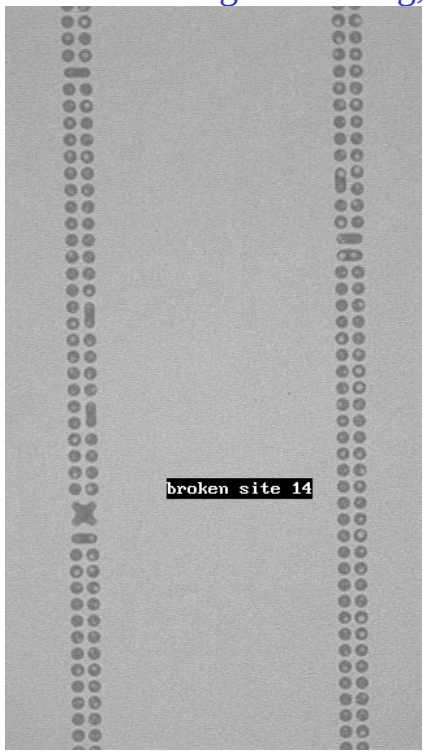
Tile 1 Solder-bumped Module X-rays:

IZM Bare Modules

- Looked at module broken during shipment and undamaged module. Both are bare.
- Scanned for bridges and missing. May miss some bridges(see 1st picture). Able to scan with module in gelpak.
- Assuming defects =2*bridged+missing, rate is 1-2%.



19



Die	Broken		Good	
	Bridged	Missing	Bridged	Missing
0	7	1	15	0
1	0	1	20	0
2	0	1	3	0
3	10	0	6	0
4	26	0	8	1
5	2	0	52	0
6	2	0	23	0
7	2	0	3	0
8	46	0	27	0
9	5	0	3	0
10	24	1	16	0
11	44	0	31	0
12	106	0	3	0
13	35	0	10	0
14	43	0	3	0
15	------	------	42	2
Total	352	4	265	3
Defects	708		533	
% defects	1.6%		1.2%	

M. Gilchriese - January 20,1999

Summary

- We have been slowly accumulating results from complete modules, primarily limited by the availability of the assemblies due to limited number of bumping vendors and their low output so far. This should change during 99.
- The yield of the assembly process is good, with all chips on a module normally fully functional (statistics is still low). We will learn more in the coming year as we produce 50-100 modules, some of which will have thinned electronics die.
- There have been many problems operating the initial modules received from Boeing with Indium bumps. This is partially due to the low quality of bumping (large number of merged bumps), which indicate to us that the Indium technology is quite challenging for our bumping pattern (tendency for slippage or over-compressed bumps). There are also significant problems arising from oxide layers within the Boeing bumps (nominally at the Al-UBM interface) which have caused noisy and unstable behavior.
- The first solder bumped module we have received indicates performance which is very similar to single chip assemblies. However, many bumping probems exist here too, and these measurements are still in an ideal electrical environment.
- Next step is completion of new Flex and Flex Support card, in parallel with significant number of solder-bumped modules. Some of these modules will have back-side gold-plating to make high quality substrate contacts as well. This should provide many good modules for studies over the next few months.