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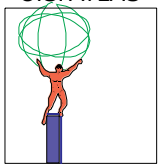

ATLAS PIXEL SYSTEM MODULE ASSEMBLY

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March 12, 1999

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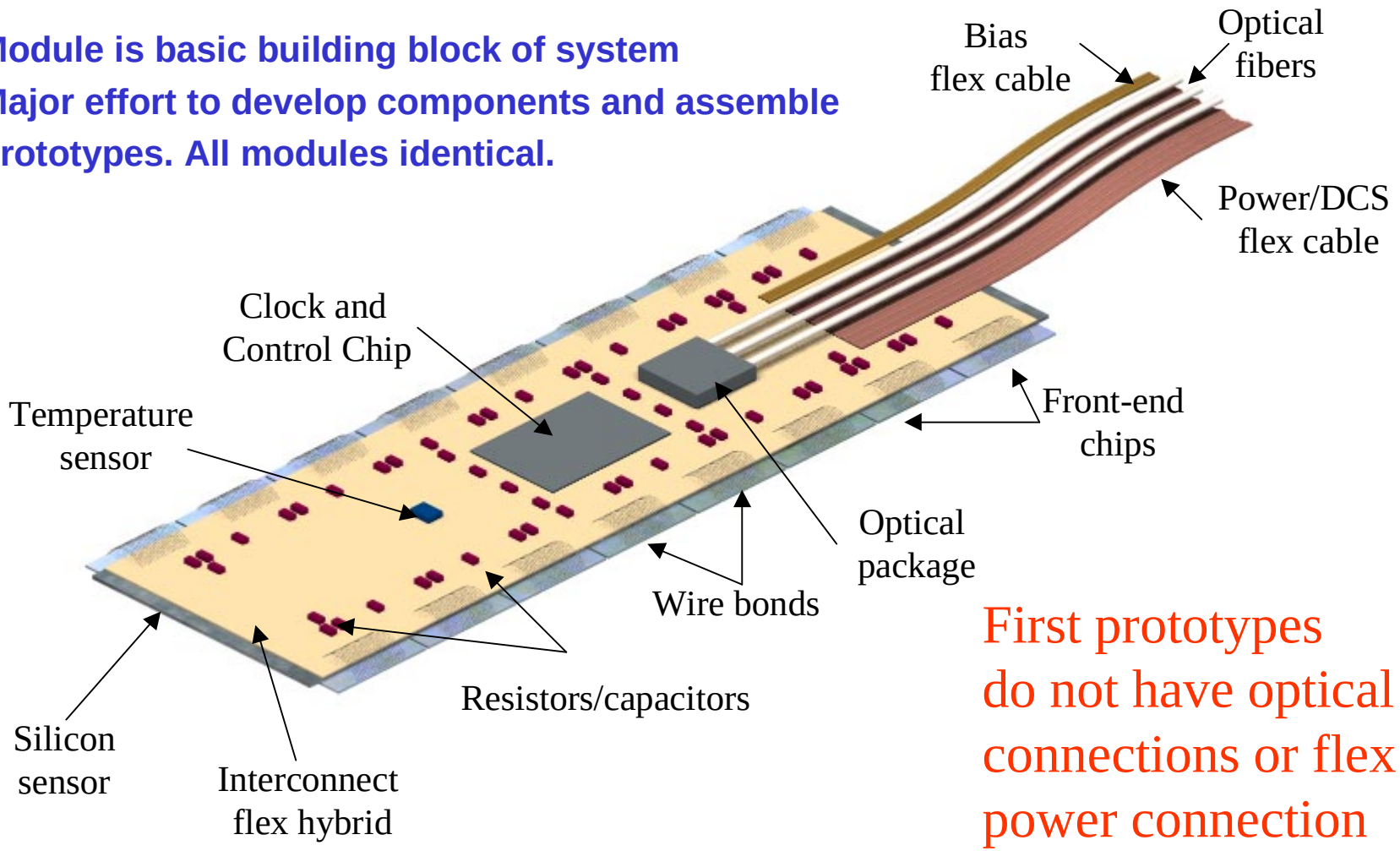
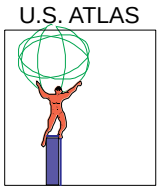
Pixel Module

Module is basic building block of system
Major effort to develop components and assemble prototypes. All modules identical.



First prototypes do not have optical connections or flex power connection



Items Covered in This Talk

- Bump deposition(or receiving metal) on IC and detector wafers
- Dicing, thinning and possibly backside metallization of these wafers
- Flip chip assembly to produce what we call “bare modules”
- Probing of bare modules(not done yet - production)
- Mounting flex hybrids with components on module
- Module burn in and testing
- Principal interfaces
  - Module attachment to mechanical structure
  - Cabling(power and optical links)

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Assembly Process - Example

ICs	
Yield(%)	Step
30.0%	Fab
99.9%	Ship
97.0%	Probe
99.9%	Ship
97.0%	Bump deposition
99.9%	Ship
99.5%	Inspection(bump yield)
99.9%	Ship
95.0%	Thin and metallize
99.9%	Ship
97.0%	Dice
97.0%	Sort
99.9%	Ship
99.0%	Inspect
Yield(%)	25%
	per die

Detectors	
Yield(%)	Step
100.0%	Fab
99.9%	Ship
90.0%	Probe
99.9%	Ship
97.0%	Bump deposition
99.9%	Ship
92.3%	Inspection(bump yield)
99.9%	Ship
97.0%	Dice
99.0%	Sort
99.9%	Ship
99.0%	Inspect
	76%
	per tile

Flex	
Yield(%)	Step
80.0%	Fab
99.9%	Ship
98.6%	Cut (from CLEOIII)
99.9%	Ship
100.0%	Probe
99.9%	Ship
95.0%	Mount components
99.9%	Ship
99.9%	Wire bond MCC (from CLEOIII)
97.0%	Probe/burn-in
99.9%	Ship
	72%
	per flex

Yield(%)	Module Assembly
99.0%	Flip chip/die
85.1%	Flip chip/module
99.9%	Ship
99.0%	Inspect
99.9%	Ship
99.0%	Probe bare module
99.9%	Ship
98.0%	Attach flex
95.0%	Wire bond FE's (with repair)
98.0%	Attach pwr/optics
99.9%	Ship
95.0%	Test/burn in
99.9%	Ship
	71%
	per module

Note on module yield model may be found at
http://www-physics.lbl.gov/~gilg/moduleyield.pdf

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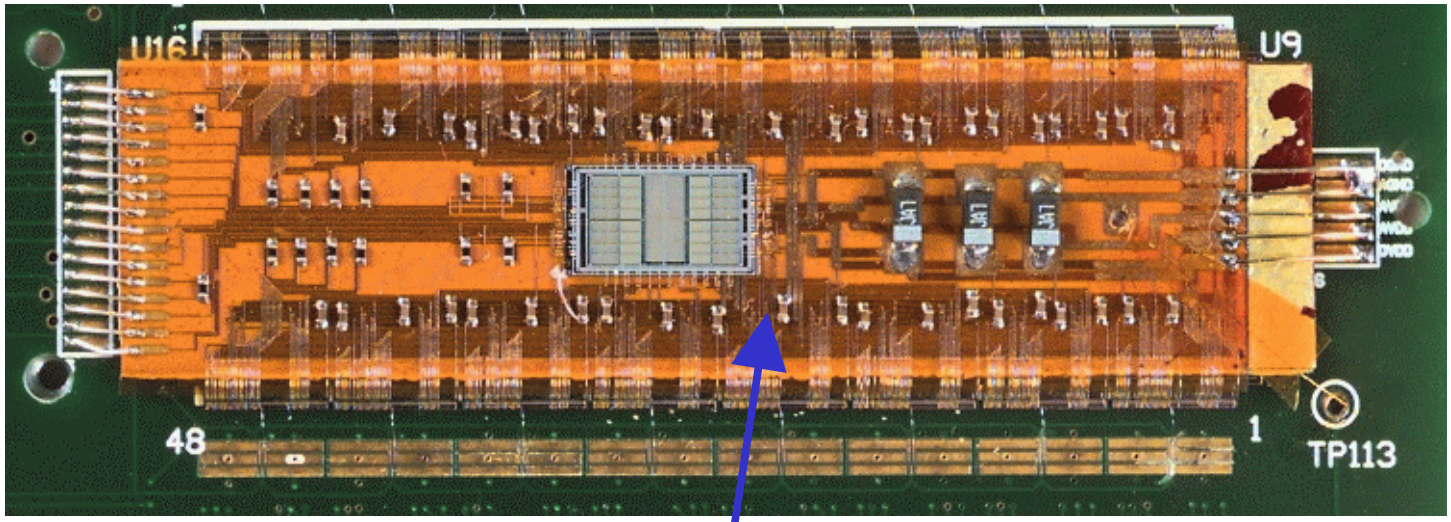
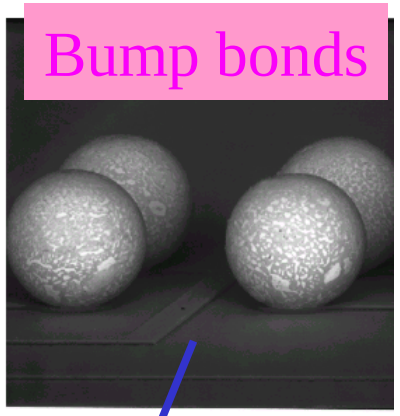
Pixel Modules

Module with flex hybrid and controller chip on PC board

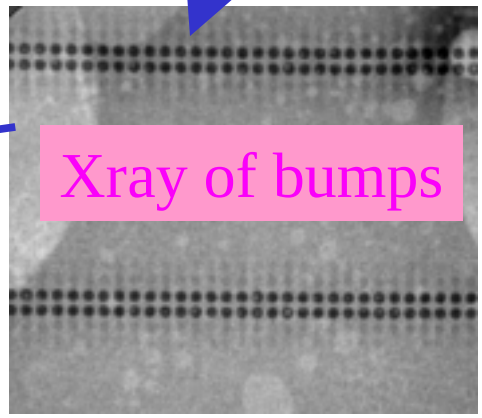


Bump bonds



16 chips with 46,000 bump bonds

Xray of bumps



Sensor

ICs

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Bump Bonding

- **Solder or indium bumps have been used so far in our prototype program.**
- **Different process flow for solder and indium and some small variations for fixed metal between vendors**

Vendors

AIT(In, solder)[1,4]

Alenia(indium)[2]

Boeing(indium)[2,3]

GEC(solder)[1]

IZM(solder)[2]

Sofradir(indium)[4]

Unitive(solder)[4]

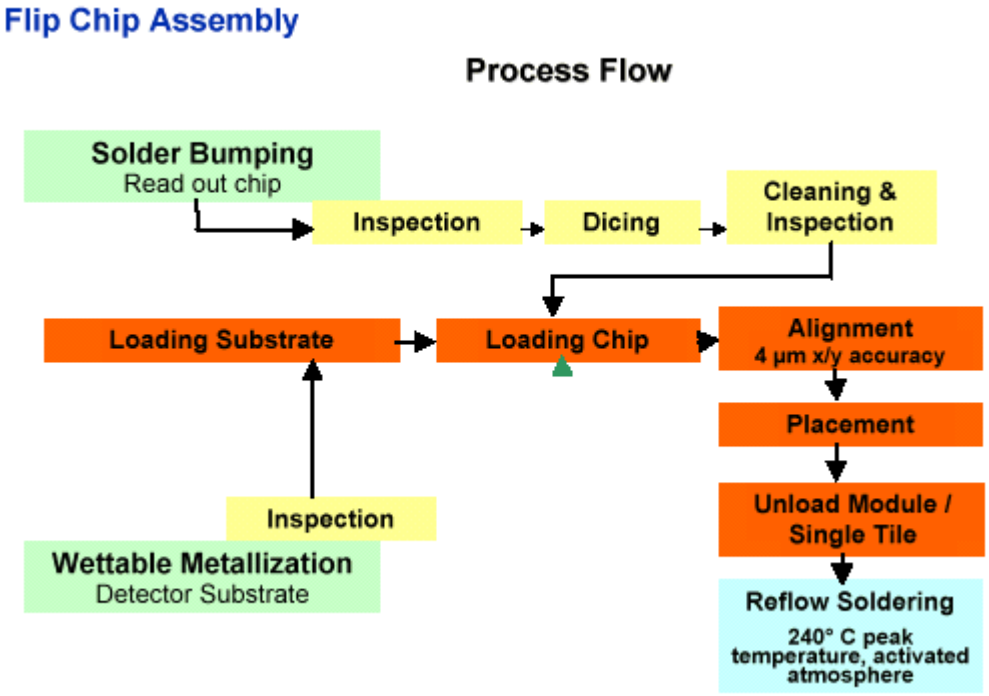
[1] Used by others

[2] ATLAS parts made

[3] No longer active

[4] Contacts in process

IZM



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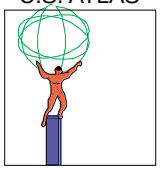

Bump Bonding- What Do We Know?

- Both indium and solder successful for prototypes but some concerns about indium(high resistance from oxides and flip chip misalignment)
- Defect rate for bump deposition is roughly 10^{-5} - 10^{-4} for both metals
- Visual inspection appears to be adequate to measure this(so far automated bump mapping systems appear to be beyond our means)
- Defect rate for flip chip assembly has varied greatly for prototypes from about 10^{-4} - 10^{-2} per bump connection.
- X-ray inspection established with two vendors(IZM and here in Bay Area) and is adequate to measure flip-chip yield
- Thinning of bumped IC wafers to 150 microns and subsequent flip chip assembly has been demonstrated(on one 16 chip module) for indium only at the moment. Have also thinned dummy wafers.
- Dicing of bumped wafers demonstrated with multiple vendors.
- Irradiated bumped(indium) detectors work. Bumping does not appear to affect detector properties adversely
- Tensile and shear strength measured. Creep studied. But all with low statistics. Both indium and solder.
- Preliminary price enquiry made to many vendors. Large differences in price(factor of 2)

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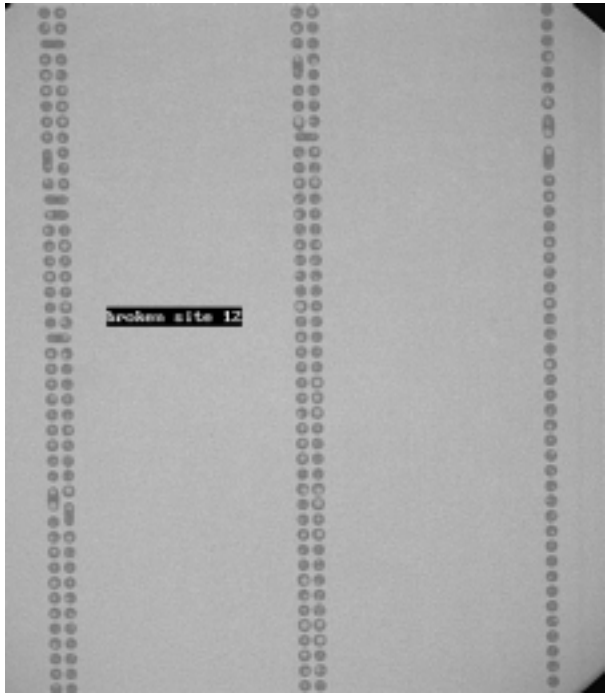
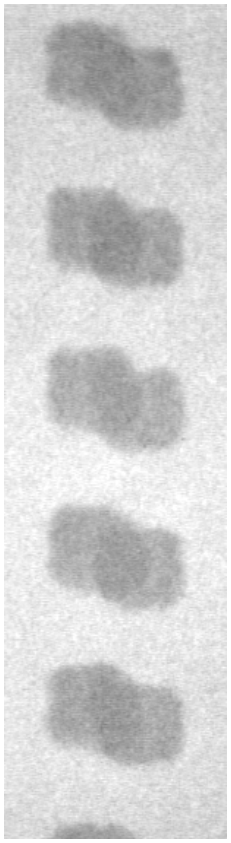
Examples



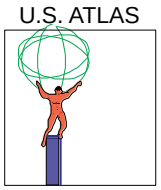
X-ray inspection of solder bump 16 chip module from IZM



Indium bump misregistration

More details on X-Ray inspection may be found at
http://www-physics.lbl.gov/~gilg/xrayfeb99.pdf

Flip-chip assembly of single detector to IC



Bump Bonding - What Don't We Know?

- Difference in electrical performance(resistance of bumps, height of bumps, ….) - underway now comparing indium modules with solder bump modules.
- Should we choose one technology - solder or indium? Or should we allow both(equivalent to having two vendors?)
- Irradiated detectors with solder bumps OK? Wait for rad-hard ICs
- Thin detector wafers - learn from 2nd prototype order
- More experience needed with thinning bumped wafers. More this year.
- Yield with good confidence for all steps - not until mid-2000
- Impact of possible need for backside IC metallization on process steps - underway now at IZM
- Strength of bonds with good statistics - underway in Italy(for indium, which is weaker)
- Production rate for both wafer bump deposition or flip-chip assembly.
- Do we need more than one vendor for schedule reasons? Clearly desirable to reduce risk.
- QA program must exist but we haven't come close to implementing this with vendors. Are agreed that substantial collaboration involvement is required. Develop QA plan this year.

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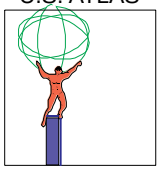

Bump Bonding Program

- Build many more modules - as many as we can afford
- Goal is to build 50+ active modules with prototype 2 sensors and FE-B/C and later FE-D/H chips by early 2000.
- This will be done at IZM and Alenia. Third vendor under consideration but not decided yet.
- 2nd generation dummy module program not yet fixed. Decide in June.
- Stay in touch with other programs(ALICE, FNAL pixels)
- Detailed work plan schedule up to production is (just) under development (primarily by me) following selection of flex module baseline 3 weeks ago
- Review in June

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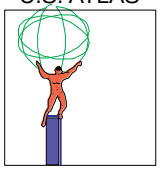

Module Assembly

- **Only two flex modules have been assembled to date, one at Oklahoma and one at LBL.**
- **A few more with flex v1.0 will be made in Europe shortly.**
- **These have been and will be made to address electronics performance issues not module assembly.**
- **Production aspects of module assembly simply have not yet been addressed.**
- **Will begin to address these issues in about May of this year in preparation to prototype assembly tooling and procedures with modules made from 2nd prototype sensors, Flex 1.x and 2.0 and FE-B(first) and then FE-D chips.**

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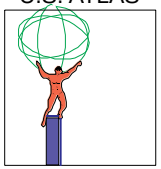

Module Assembly Plan

- **Within the U.S., LBNL is responsible for module assembly but this relies on delivery of tested parts.**
- **We plan to have either direct responsibility in US or defined point of contact for all aspects during the development phase(through about mid-2000). We expect almost every step to also occur in Europe so coordination is important.**
  - **IC wafer probing(Einsweiler, Richardson, + labor)**
  - **Sensor wafer testing(Seidel, Hoeferkamp, UNM postdoc, Alam)**
  - **Bump deposition and inspection(Gilchriese)**
  - **Dicing, thinning and metallization(Gilchriese, Palaio)**
  - **Flex production and testing(Skubic, Boyd, Timm, + labor)**
  - **Flip-chip assembly and inspection(X-ray)(Gilchriese + labor)**
  - **Bare module probing(Einsweiler, Richardson, LBL postdoc, LBNL engineering)**
  - **Module assembly tooling(Goozen, Zizka, Anderssen)**
  - **Module assembly - mechanical, wire bonding(Goozen, Zizka + labor)**
  - **Assembled module testing(Einsweiler, Richardson, LBL postdoc, LBNL engineering initially, but migrates to other groups)**
  - **PLL upgrades and software(Richardson, Fasching, UW supported engineering)**
  - **Optical interface/tests(Gan, Kagan, OSU engineering)**
  - **Power cable interface/tests(Anderssen + testing group)**
  - **Module attachment interface(Anderssen)**
  - **Radiation testing(Taylor)**
  - **Database contact(Ciocio)**
  - **QA plan(Taylor, Gilchriese)**
  - **Overall coordination(Gilchriese)**