On-Detector Pixel Electronics Schedule

K. Einsweiler, LBNL

Overview of FE Electronics milestones

Present US deliverables include only FE chips, so for now, only discuss this schedule.

Comments and Summary

Overview of Milestones

Pursue two rad-hard vendors (TEMIC/DMILL and Honeywell SOI) through the final prototype stage:

- The initial milestones were for test devices in the two processes of interest, to establish that the processes themselves were useful for pixels. On this basis, the Honeywell Bulk CMOS process was disqualified as not suitable for doses in excess of 10 MRad.
- The next set of milestones applies to the real prototypes (demonstrator FE chips referred to as FE-D and FE-H). The critical steps are to complete the design (submit for fabrication), receive the fabricated parts, and complete the evaluation of those parts.
- The final set of milestones describes the schedule for converging on a single vendor (we do not see any defensible reason for two vendors, with the exception of the B-layer). There would be a second prototype run of a final design that should be acceptable for ATLAS pixels.

DMILL Test Device milestones:

- Test devices have been submitted several times for DMILL, but the relevant devices are those after the transfer of the process from LETI to TEMIC.
- The prototype array “MAREBO” was submitted in July 97 and returned in Jan 98. This array included a FE design similar to what we are using in FE-D, with a simple shift register readout in the column, and no circuitry at the bottom of the column.
- This was a run made before CEA certified the successful transfer of the process, and it suffered from low yield on NMOS due to poly bridges in certain topologies, problems with the drain/source doping of the PMOS which made them noisy and less rad-hard, and very poor beta for the NPN’s.
- Nevertheless, it has been extensively studied and irradiated. The performance after 25 MRad is difficult to extract, but it is possible to show decent noise and threshold performance, as well as timewalk performance, from a single array.
- An improved version of this test array has been resubmitted to DMILL in Dec. 98. It includes both the CMOS and bipolar FE designs, and includes several cells with capacitive loads and leakage current injection capability. This structure will be irradiated to perform more detailed characterizations of FE performance before and after irradiation.

HSOI Test Device milestones:

- Single transistors on PM bars have already been evaluated for both the production SOI and the enhanced SOI process from Honeywell. The enhanced process seems to behave well up to 50 MRad with threshold shifts of only about 100 mV, and g_m losses of less than 20%.
- Test structures, including a complete FE design with preamp, discriminator, pixel control circuitry, bias circuitry, current DACs and current reference, was submitted on a production HSOI multi-project run in Nov. 98, and the wafers will be available shortly.
- These circuits will be characterized before and after irradiation to confirm the behavior of full designs. Although this run is not in the target process, we have not been able to detect any electrical performance differences for the enhanced SOI process compared to the production process.

Test Device Schedule:

Milestone	Baseline	Current
Complete Design DMILL Test Device		12/15/98
Complete Fab DMILL Test Device		4/30/99
Complete Evaluation DMILL Test Device		7/1/99
Complete Design HSOI Test Device	4/16/98	11/1/98
Complete Fab HSOI Test Device	8/26/98	3/31/99
Complete Evaluation HSOI Test Device		7/1/99

DMILL Prototype milestones:

- Have agreed within the collaboration that given our limited resources and the desire for common designs, we should pursue a sequential prototype strategy, with first a DMILL version, and then an HSOI version.
- The DMILL version, referred to as FE-D, is almost complete. We recently had a first design review at CERN (2/23/99), and the top level blocks are all within a few weeks of being finished.
- Effort is concentrating on completing detailed simulations of top level blocks. This means SPICE and Verilog in most cases, for example for all of the digital readout.
- We expect that this process, including a Verilog simulation of the complete chip, and partial and full DIVA DRC and LVS, should be complete by about 4/15/99.
- This would provide us with wafers by about 8/15/99. We will of course negotiate with TEMIC for the fastest turnaround consistent with our budget.
- The wafers would be available just barely in time to construct complete assemblies for irradiations at the CERN PS in October, but probably too late to test complete assemblies in the CERN H8 beam before the end of Sept. We will also have access to lower energy testbeam at the CERN PS or in Bonn at their 1.5 GeV electron beam later in the calendar year.
- Full evaluation of irradiated assemblies cannot be done before Spring 00.

HSOI Prototype milestones:

- So far, only LBL has experience within our design community with the HSOI process. We have built up a decent Cadence technology file and DRC plus LVS rules for DIVA.
- We are struggling to get the necessary agreements in place with our European colleagues (Bonn, CPPM, Genova) to allow them to design with this process. Unfortunately, the US Govt makes this difficult.
- We hope to have the outside institutions up to speed by April 99, so they can begin contributing to the “porting” of the FE-D design to HSOI.
- This port will allow us to relax some of the restrictions on the present DMILL design, and so the schematics of various parts will not be identical. We also need to establish a simple standard cell library, and work with the vendor to develop a better understanding of corner models for the process.
- There will be some improvements possible in the design due to the improved layout rules and added metal layers. We will probably increase the readout architecture performance for high occupancies, and possibly prototype two FE designs in parallel.
- Our present planning suggests that the FE-H submission would take roughly 6 months after the FE-D submission to complete the design and layout work.

Prototype Schedule:

Milestone	Baseline	Current
Complete Design DMILL Prototype	2/26/99	4/15/99
Complete Fab DMILL Prototype	7/23/99	8/15/99
Complete Evaluation DMILL Prototype	12/9/99	6/1/00
Complete Design HSOI Prototype	4/2/99	10/1/99
Complete Fab HSOI Prototype	8/25/98	2/15/00
Complete Evaluation HSOI Prototype	2/15/00	6/1/00

Second Rad-hard Prototype milestones:

- A complete evaluation of both FE-D and FE-H chips, including irradiating complete single chip and module assemblies, and systematic performance measurements in the CERN H8 testbeam, will be performed.
- This cannot be completed prior to about June 00 due to availability of chips and testbeams.
- After this information has been digested, it will be possible to have a thorough review of the two designs and vendors, and make a choice. This choice must include technical performance issues, yield issues, cost issues, and any other differences that appear during the evaluation period.
- Both cost and limited engineering resources argue strongly against fabricating production chips with more than one vendor. The possible exception to this would be the necessity of achieving higher performance in the B-layer, which might be uniquely achievable using the HSOI process (denser layout rules, 4-metal interconnect possibilities, and potentially greater radiation hardness, but possibly higher cost).
- Only after we have actual yield information from our prototype runs, and after we have made the vendor choice, can we establish a secure cost estimate for the FE electronics. Until then, it is necessary to assume rather large contingencies.

Second Rad-hard Prototype Schedule:

Milestone	Baseline	Current
Review Design Approaches of First Prototypes	1/19/00	6/15/00
Make Rad-hard Vendor Selection	2/29/00	7/15/00
Complete Design of Second Prototype	7/7/00	9/15/00
Complete Fab of Second Prototype	11/29/00	1/15/01
Complete Evaluation of Second Prototype	3/29/01	6/15/01

Summary

FE Electronics:

- As in almost all silicon projects, the critical path is determined by the FE electronics development schedule.
- This work has been proceeding well, with no major technical problems. However, it is clear that we continue to suffer from schedule slippage (or overly optimistic scheduling).
- This is due to a combination of the difficulty in projecting accurate schedules for custom IC designs, and by the shortage of engineering resources and the constant turn-over in engineering manpower.
- We are constantly trying to improve the engineering manpower, but we seem to reach at best a rough equilibrium condition.
- The present schedule does not allow for much additional slippage without starting to have a real impact on the overall construction schedule.

Overall Electronics:

- LBL currently has an overall coordination role in FE Electronics. This includes on-detector electronics, along with power supplies and opto-links. There is a critical lack of “project engineering” in these areas, and it is very unlikely that the host lab (CERN) will provide any significant assistance. Outside of CERN, only LBL has the requisite experienced manpower to assist.
- We have begun to expand our roles somewhat into other areas where US expertise can have a major impact on the project, and where there are critical needs that are not being met by our European colleagues. This includes collaborating on the MCC and work on opto-links (packages and electronics). If work in these areas proceeds well, we would plan to update our list of deliverables appropriately.