# OSU/ATLAS Electronics Status Report

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**LBL ATLAS Review**
March 11, 1999

- Introduction
- Block Diagram of DORIC4
- Schematics/Simulation
- Design Work in Progress

# OSU ATLAS GROUP

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## Introduction

- DORIC4 works → start with working design (analog + digital)

  Advantage: balanced digital architecture

  → minimizes crosstalk

  Disadvantages:

  → sensitive to PIN bias noise

  → designed for radiation tolerant BIPOLAR

  → NPN only

  → drives transistors with high current

  → hard to integrate with other CMOS electronics

- OSU plan of action

  Make RAD hard version of DORIC4

  → retain architecture - convert from BIPOLAR to CMOS

  → use n-FETS and p-FETS where necessary

  → new input amplifier for better S/N ratio

  → test new PIN bias noise cancellation network

# *Status*

- Status

  Conversion from BIPOLAR to CMOS underway

  Using SPICE (MOSIS/BISIM3 AMI 0.8$\mu m$ extraction) to model the CMOS circuits

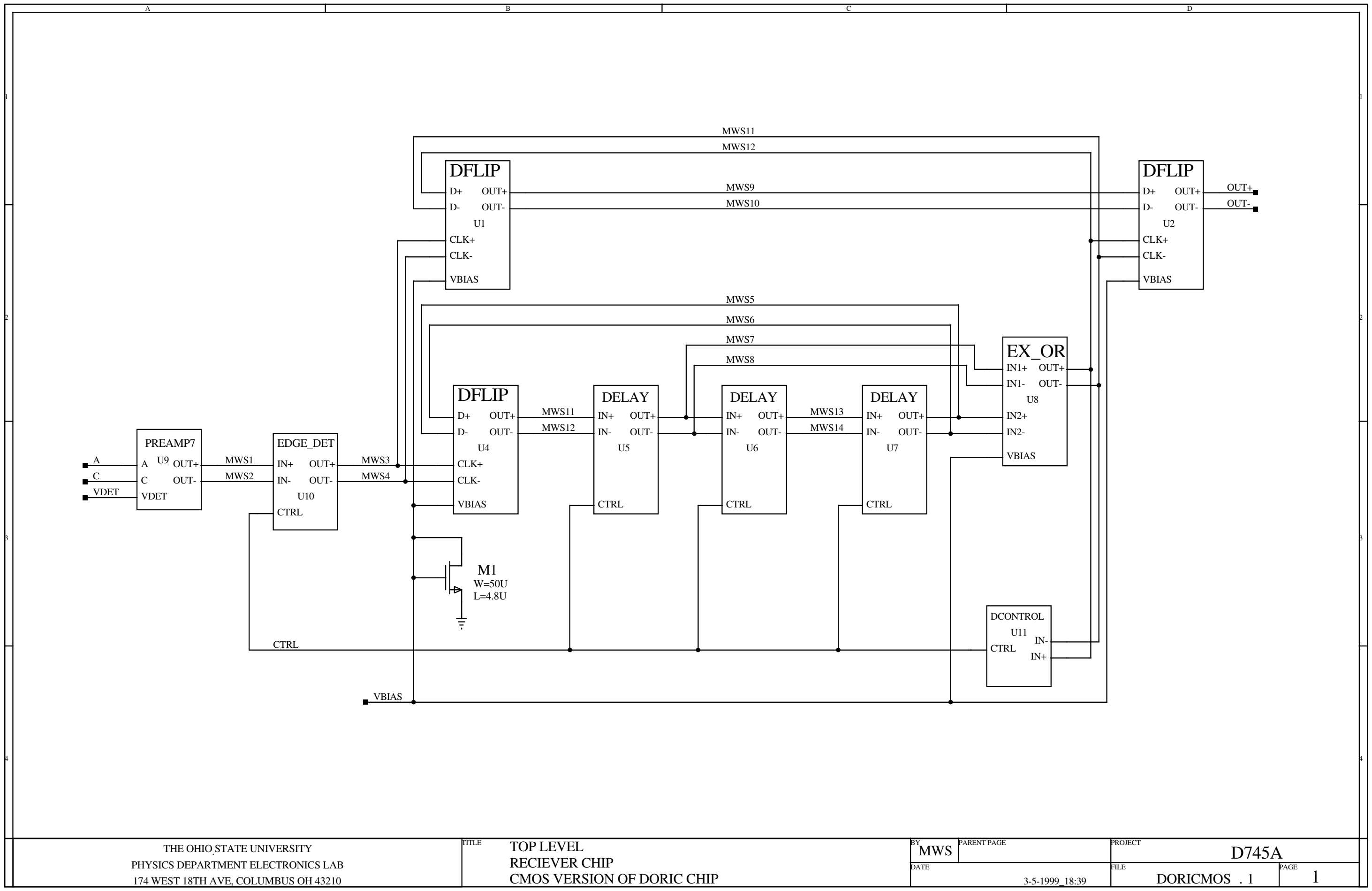
  Getting models from Honeywell for SOI process

  $\rightarrow$ non-disclosure agreement being negotiated

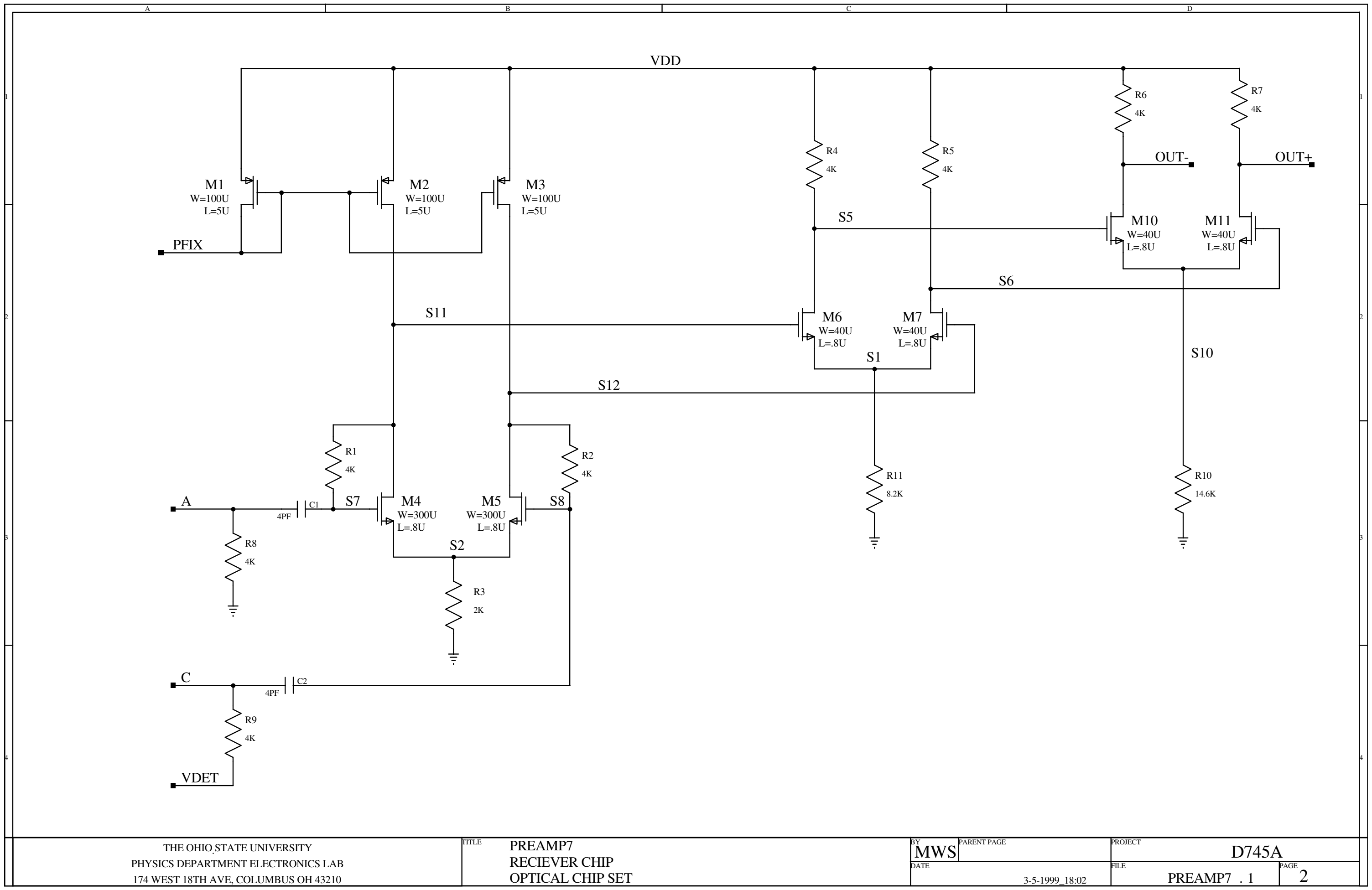
  Designed a balanced low noise preamplifier

# *Block Diagram of Doric4 Sub Section for Simulation*

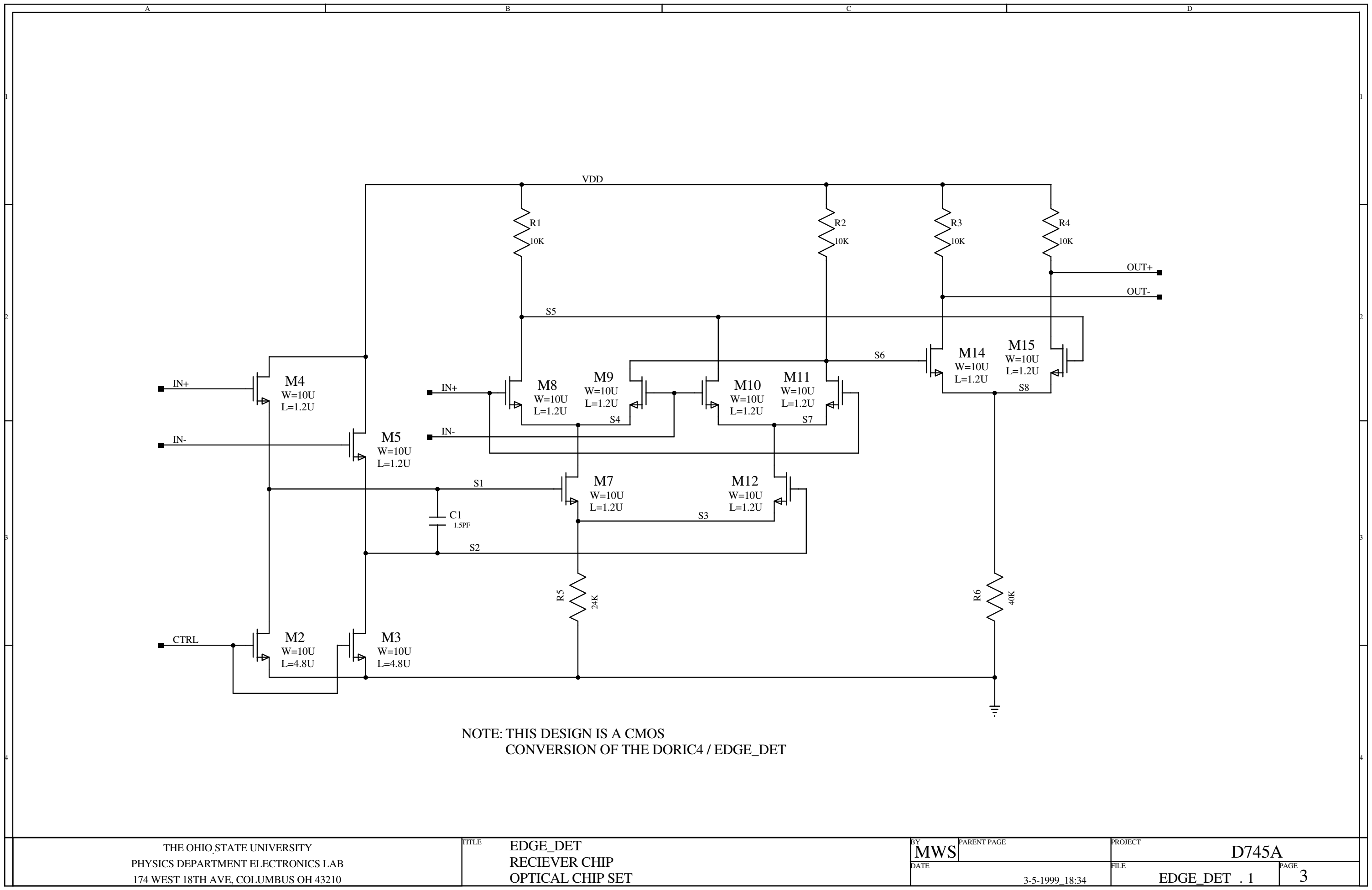
## Copy of DORIC4 architecture



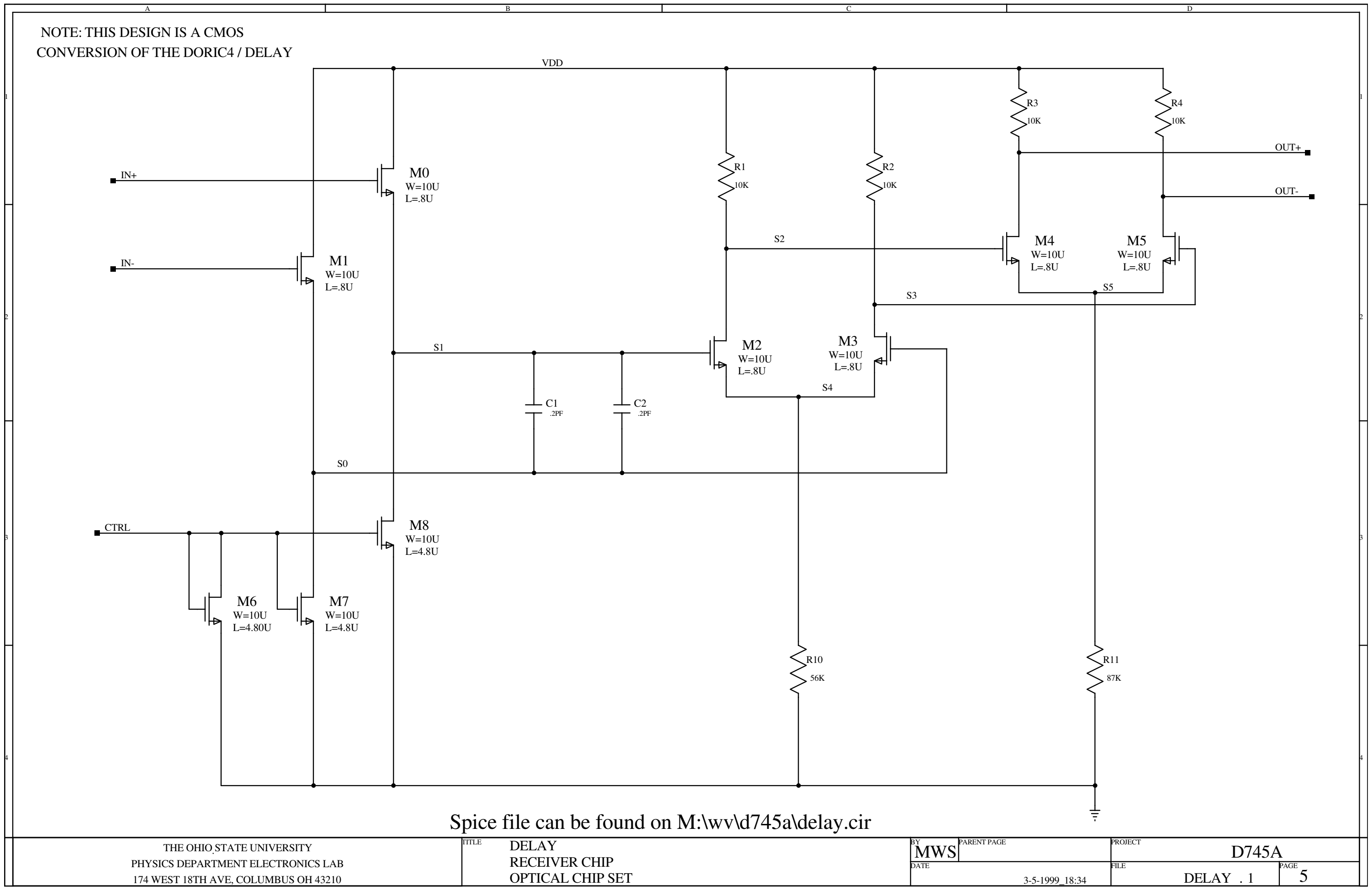
# CMOS Version of PREAMP Circuit



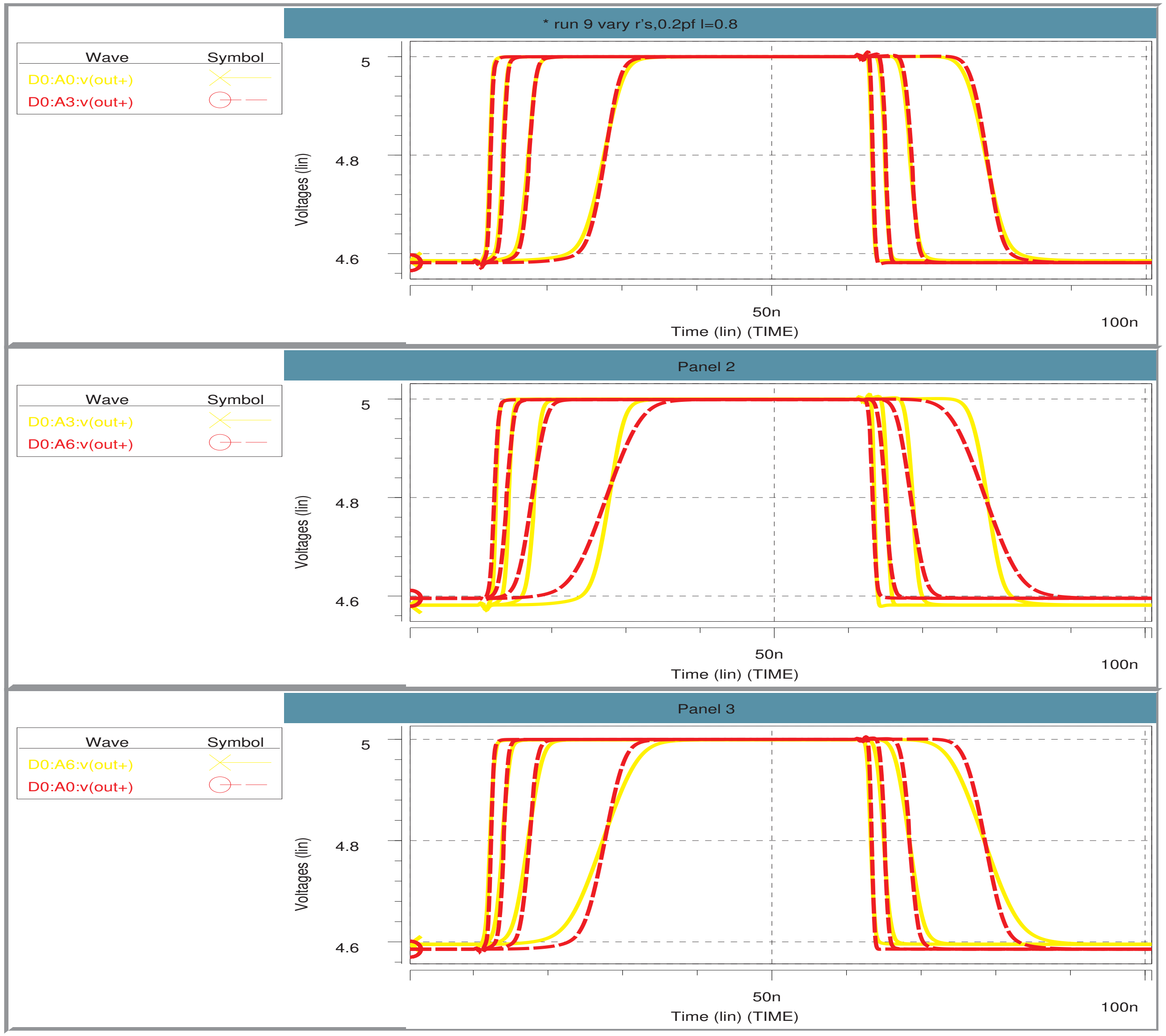
# CMOS Version of Edge Detect Circuit



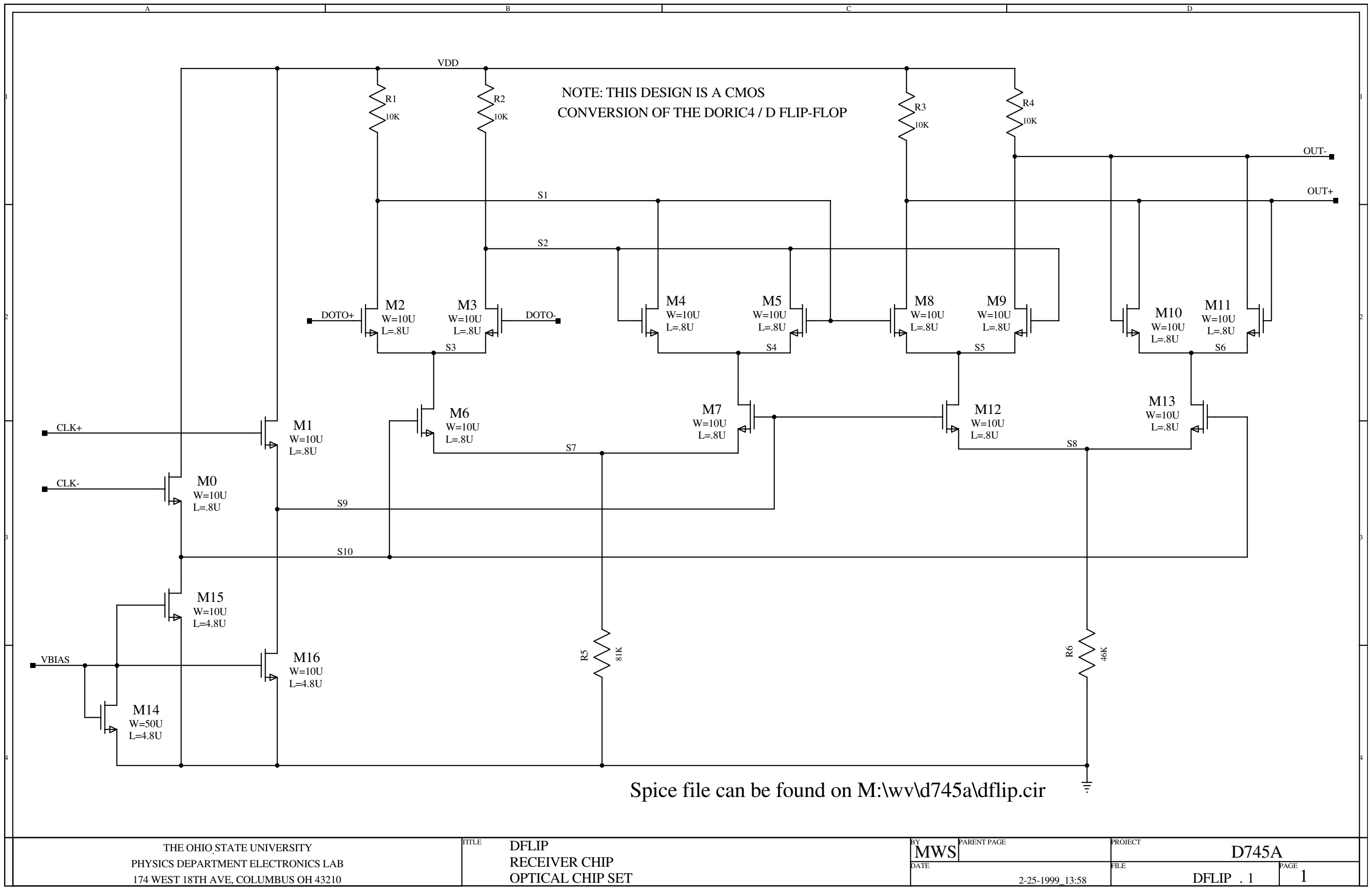
# CMOS Version of Delay Circuit



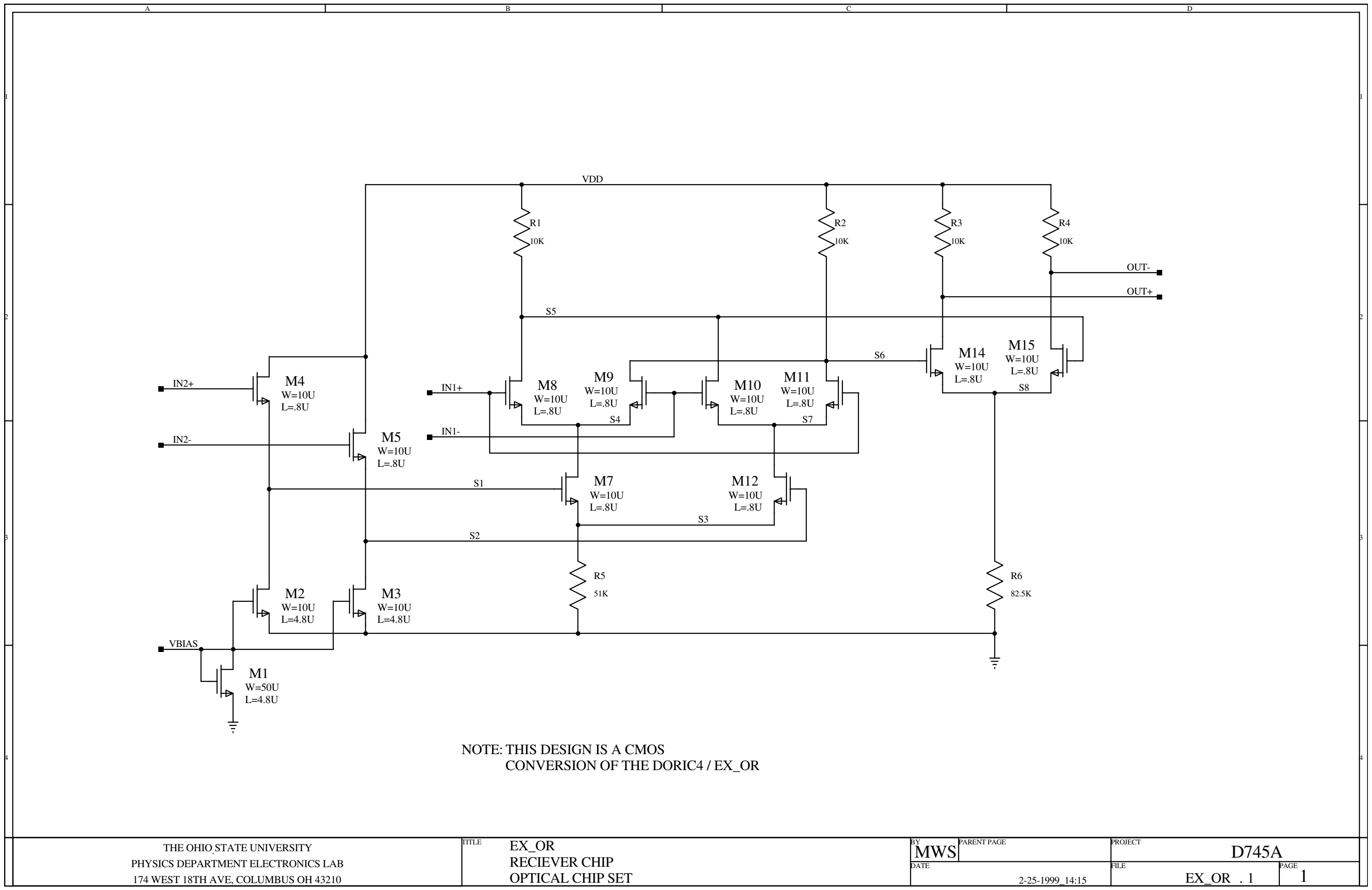
# Spice Simulation of CMOS Delay Circuit



# CMOS Version of D Flip Flop



# CMOS Version of Exclusive OR



# Design Work in Progress

- DCONTROL

  Controls duty cycle of recovered clock

  Holds duty cycle at 50%

- Output Drivers

  LVDS

  CMOS

- Simulate entire system

  tolerance of resistors (R can vary by 50%)