WBS 1.1.1.3 Pixel System

Opto-links, and On-detector Electronics

Major Topics:

- Opto-links (WBS 1.1.1.3 and 1.1.1.4): Status and Issues
- On-Detector Electronics and Test System (WBS 1.1.1.3): Status and Issues

Concentrate on technical status and next steps:

- Motivate near-term schedule and goals

Describe cost and schedule status, particularly for FY02

- Discuss FY02 manpower estimates, costs, and milestones

Summary and Conclusions

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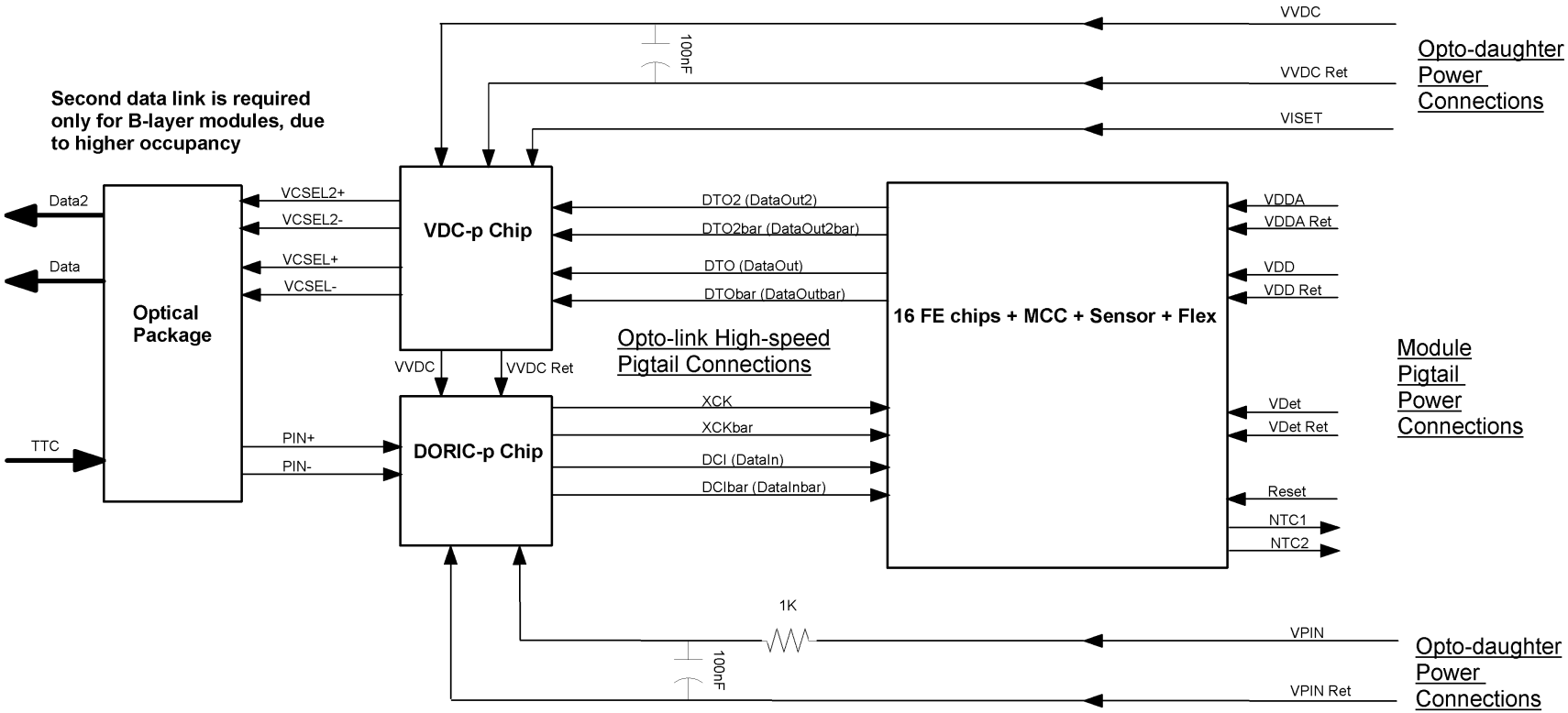
On-Detector Electronics, Opto-links, Power Distribution

System Design:

- **Pixel Array (Bonn/CPPM/LBL):** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is ìrequestedî by sending LVL1 signal with correct latency. FE chip then transmits corresponding digital hits autonomously.
- **Module Controller (Genova):** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements module level command/control. The 16 FE chips on module connect to MCC in star topology to eliminate bottlenecks and increase fault tolerance.
- **Opto-link (OSU/Siegen/Wuppertal):** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 40 or 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Opto-package is now 8:1 Taiwan package, plus two matching optolink chips with LVDS interfaces. Fibers are rad-hard silica-core stepped-index multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling on module. Low-mass power tapes used to reach patch panels at end of support (PP0, 1m) followed by Al round cable to transition on cryostat wall (PP2, 7m), then conventional cables to USA15 cavern. Filtering, transient protection, and possibly local voltage regulation would be performed on intermediate patch panels.

Summarize all connections required for module operation:



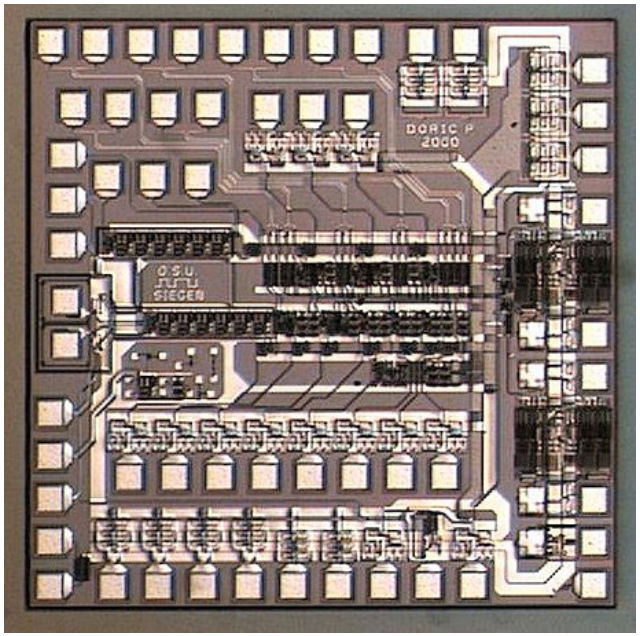
- There are five power supply voltages with their separate returns, and one control voltage that uses VVDCRet as a reference.
- VVDC powers both the DORIC and the VDC, and VPIN will need to connect directly to the opto-package instead of routing through the DORIC.
- Present concept is that DORIC, VDC and their passive components, plus the Opto-package are placed on Opto-card. Interface requires 3-4 LVDS signal pairs.
- Taiwan 8:1 opto-package will be matched by 4 channel DORIC and VDC.

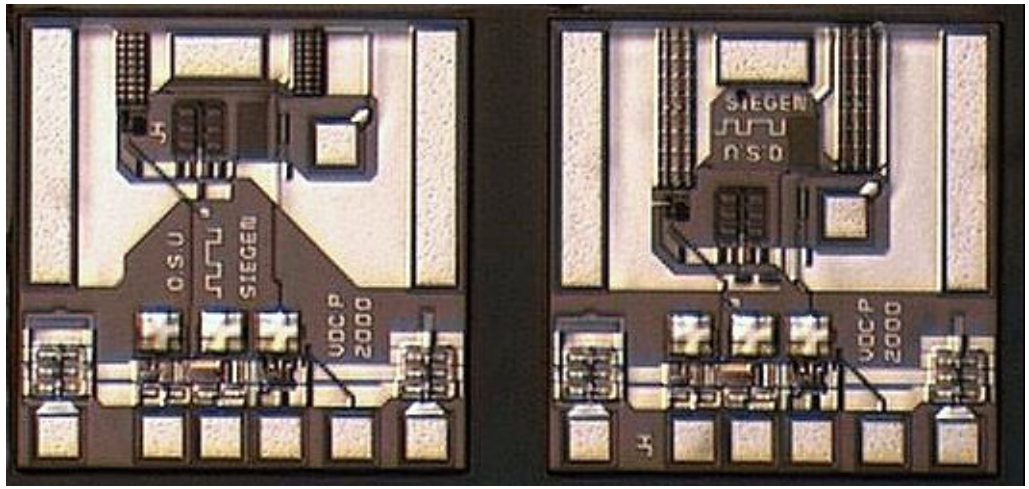
Pixel Opto-links:

- All AC signals (clock/commands/data) are transmitted optically to modules:
- **Receiver:** Fiber output is converted using an epitaxial Silicon PIN diode. The output (small current signal) is sent to the DORIC chip, which receives the 40 MHz crossing clock and a bi-phase mark encoded command stream as a single 40 Mbit/s serial stream. It uses a delay-locked loop to extract the clock (providing a high quality 50% duty-cycle clock) and decode the command stream. Note the command stream includes the synchronous LVL1 trigger commands, plus other synchronous commands, and slow configuration commands. An LVDS electrical interface is used to the MCC chip.
- **Driver:** The VDC chip converts LVDS data output streams from the MCC into current pulses suitable for driving the VCSELs chosen for data transmission. For pixel applications, the outer layers plan to use a single 40 or 80 Mbit/s output stream, and the B-layer will use two 80 Mbit/s data streams. The 80 Mbit/s link consists of sending a bit on each 40 MHz clock edge. The VCSEL drive current is adjustable using a remotely-controlled voltage. This allows in situ I/L curves, and also periodic operation at high bias to force rapid annealing of VCSEL radiation damage.
- SCT groups (RAL/Oxford collaboration) have designed and produced two basic chips in pure bipolar AMS design. They work well, but do not withstand pixel doses. For several reasons, pixels have converted designs to rad-hard CMOS.

Status of Pixel DORIC and VDC:

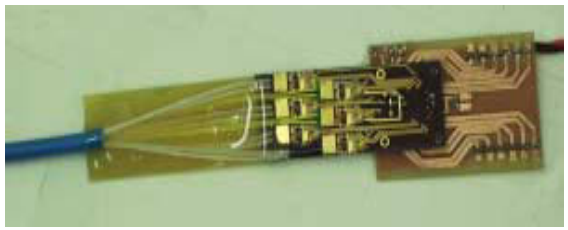
- OSU and Siegen converted SCT design from AMS bipolar to DMILL CMOS. Chips included in FE-D1 submission. VDC-D1 worked fairly well, DORIC-D1 had several design errors related to poor modeling of parasitics.
- Second generation fabricated in FE-D2 submission. DORIC-D2 now works fairly well, but only when used as a bare die very close to opto-package:





- VDC-D2 shows problem with behavior of dim current (should be constant 1mA).
- DORIC-D2 suffers from preamp DC offsets, and general has a somewhat higher error rate than the SCT DORIC-4A chip.
- Irradiations with DORIC-D2 and VDC-D2 at CERN PS showed many problems at higher doses. We have concluded that DMILL is no longer a candidate process.

- In Feb MPW, submitted first 0.25µ prototype VDC-I and DORIC-I, based on DMILL design, and including fixes for these errors.
- VDC-I1 has better dim current behavior, but excessive power consumption (22mA for 10mA VCSEL current), and modulation of supply current by 2mA between dim and bright output states (injecting noise into DORIC power supply).
- DORIC-I1 has better DC offset behavior, but excessive noise in preamp due to high gain and too short time constant in preamp baseline restoration. DLL control loop oscillates without external decoupling, and circuit requires transmission of particular sequence to ensure initial lock to 40MHz.



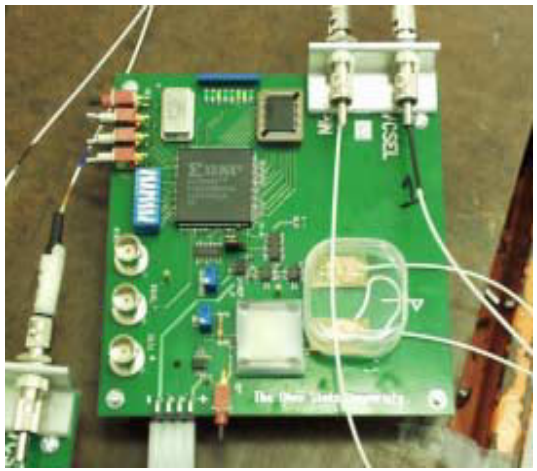
Opto-board with 6 opto-links

Bi-phase marked optical signal

25 m fibers/wires

Decoded data

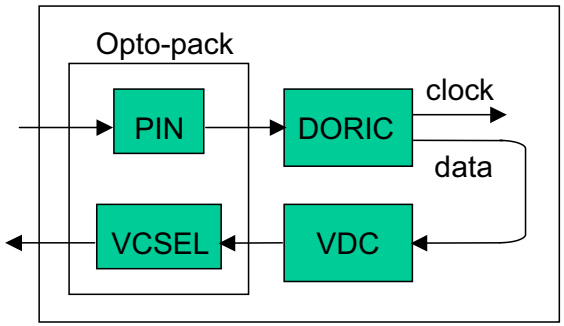
Bit error test board in control room (6 boards)



Components ready for Sept irradiation at CERN PS.

Six complete optolinks were irradiated to dose of 40MRad. Individual chips were irradiated to dose of 50MRad

Opto-link



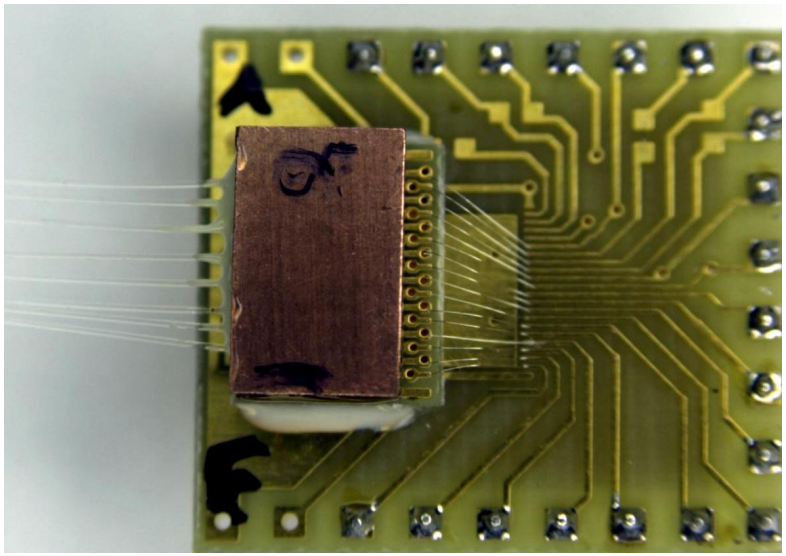
- Results of irradiation showed little degradation at doses of 40-50 MRad.
- Convened 3 day workshop at LBL in Sept on opto-chips to work more closely with OSU, taking advantage of Peter Denesí knowledge of opto-electronics. He has extensively simulated OSU designs, and we will help to improve the designs. Characterized DORIC timing performance (jitter, odd/even effects), looked OK.
- Improvements made in designs for DORIC-I2 and VDC-I2 for FE-I engineering run. Run includes the first 4-channel VDC design, and prototype single-ended preamp for DORIC as test structure as well.

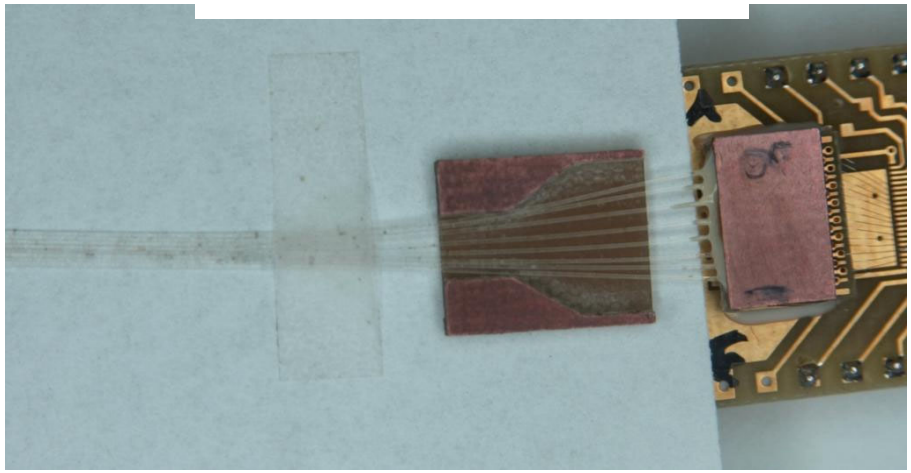
Remaining Issues:

- Two significant issues in transition to 0.25µ process, neither yet addressed. Third issue raised by alternate opto-package based on PIN/VCSEL arrays
- PIN bias may reach 10V at end of lifetime, and present DORIC design uses on-chip AC-coupling and differential preamp for readout, violating process limits. This requires switch from differential to single-ended preamp design for DORIC.
- VCSEL may require 2.3V or more of bias to achieve 20mA current at end of lifetime, forcing VDC supply to operate at process limit of 2.7V with no headroom.
- VCSEL arrays require switch from common anode (NMOS current source between VCSEL and ground) to common cathode VDC (PMOS current source between VVDC and VCSEL).
- Need to resolve these issues soon, and implement improvements in circuits.

Status of Opto-package development:

- Pixel integration issues forced the design into an ìend of staveî or ìsectorî level opto-interface, instead of the module-level interface used by SCT. This strongly suggested a more ambitious opto-package design.
- Both Taiwan and OSU have worked on different approaches to this problem.Review in June 01 selected Taiwan 8:1 package as baseline.
- Agree to use SCT-qualified PIN (Centronics) and VCSEL (Truelight). These elements have been (partially) evaluated in neutron, gamma, and proton beams.

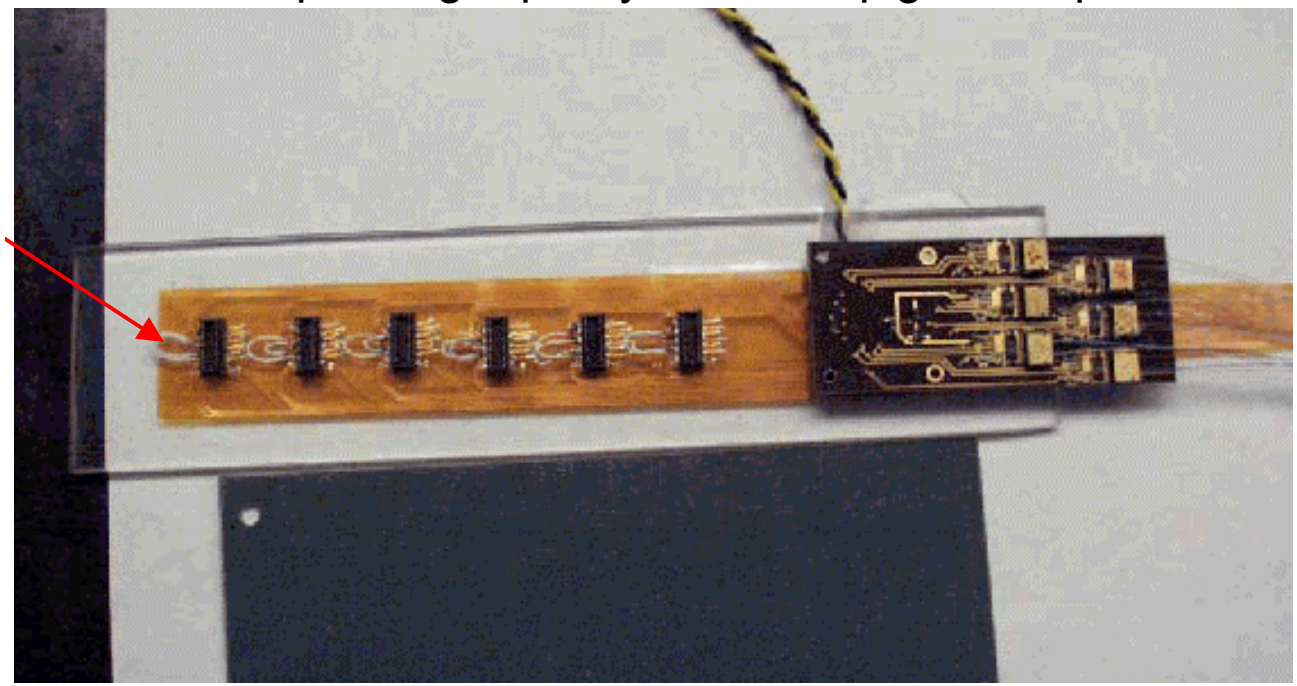




- Package is about 10mm wide and 8mm deep. Compact design requires multi-channel DORIC and VDC in order to develop a compact opto-card.
- Alternate package is based on PIN and VCSEL arrays and a connectorized package with MT-8 termination, eliminating fanout and splicing.

Opto-Card Concept for Mounting Opto-links

- Original concept was to keep fast timing signals in optical form until very close to the pixel module. Given the very challenging services integration in the pixel detector, especially the barrel, this has proven to be impossible.
- Present design groups opto-links at the ends of the Global Support structure (attaching them to PP0). This consolidates fiber interface and opto-packages onto a single card with electrical connection to PP0. This separate unit can be fully tested and burned in prior to installation. In addition, all opto-links are at a radius of 15cm, decreasing problems due to SEU effects at smaller radii. This does require high quality electrical pigtails to pixel modules to avoid EMI.

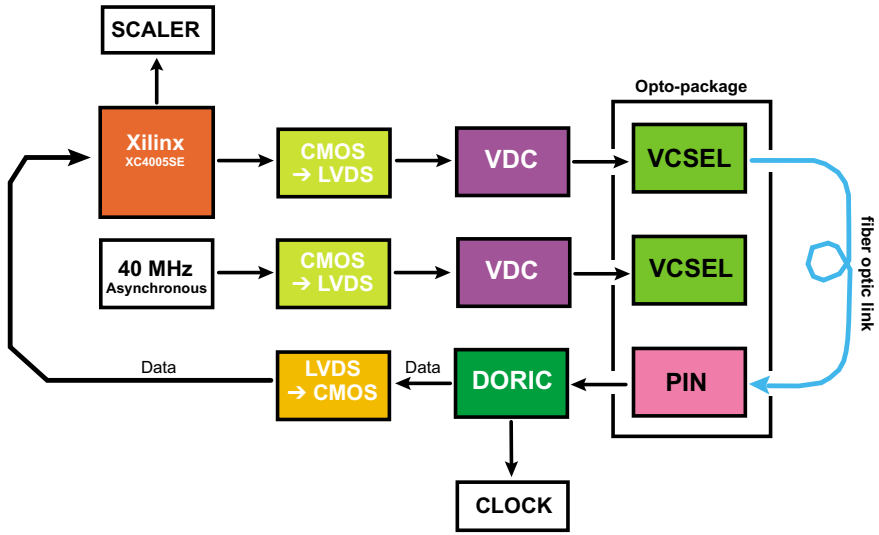


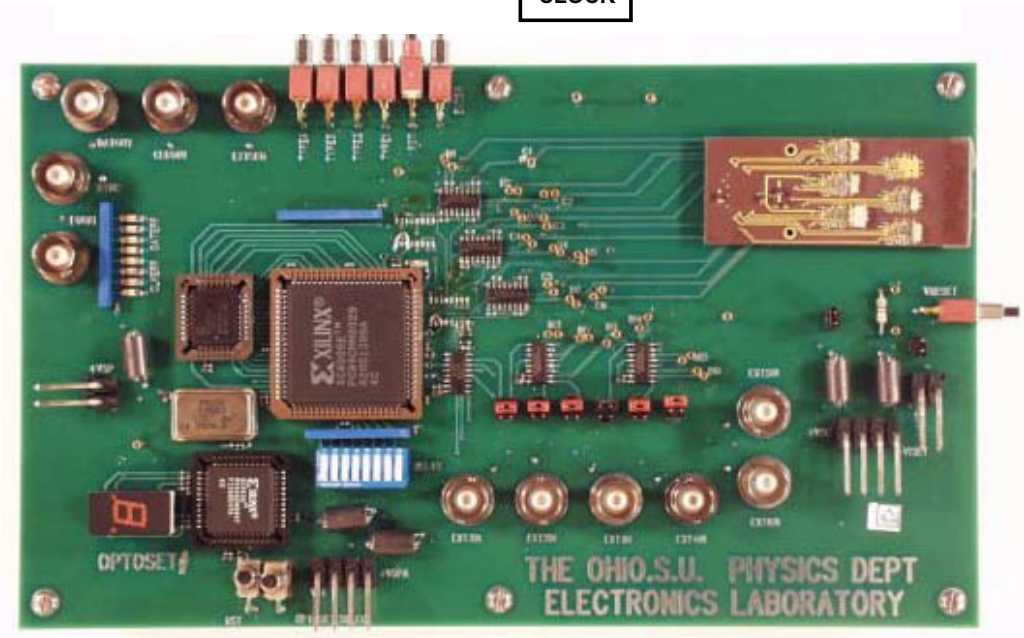
First testing of Optocard prototype with 6 Taiwan links mounted on PP0 prototype.

First optocard prototypes do not respect all mechanical envelopes.

Test System for Opto-chips and Opto-links

- OSU has built a first prototype of a high-performance opto-link tester, designed to be used for testing a complete opto-card.





- Use VDC and VCSELs as data source, and DORIC and PIN as data decoder/receiver.
- Can loop-back within the same opto-package for now since opto-packages are rare.
- Final system would use off-detector elements coupled by realistic fiber ribbon to opto-card under test.
- This means using a BPM chip and VCSEL array to generate input data, and a DRX chip and PIN array for receiving output data.

Irradiation qualification:

- Collaborative effort of SCT and pixels (Wuppertal from pixels) have performed systematic irradiation studies of optical fibers and opto-elements (PINs and VCSELs) up to pixel fluences. Results show no significant risks, provided PIN is operated with adequate bias voltage (up to about 7V), and provided VCSELs are operated with sufficient bias current (up to about 20mA).
- Only known issue at this time is single event upsets caused by interactions in the very thin epitaxial layer of the PIN diode. Irradiations at PSI showed a significant effect, but at the new radius of the opto-cards, this should not produce a BER of more than about 10^{-9}.
- Pixels has recently significantly upgraded the MCC command set to be highly fault tolerant. Critical commands (particularly LVL1) are successfully decoded under any single bit error, and are only mis-interpreted under double bit error.

Next Steps:

- Continue to optimize 0.25μ designs to improve noise performance and power consumption (links are already functional, but need improved margin).
- Prototype multi-channel DORIC, and move towards improved opto-card design, including more difficult B-layer case (14 80Mbit/s data links plus 6 TTC links).
- Begin operating real modules with opto-link interface in system test.

Deliverables

US Roles

- Contribute to design of opto-chips (VDC and DORIC) in 0.25μ processes. Present electronics effort is dominated by OSU group, and expect this to continue. German groups more active in testing and evaluation.
- Contribute 50% towards opto-chip fabrication. Baseline in cost estimate is conservatively assumed to be DMILL (???)
- Probe 50% of opto-chips.
- Supply fraction of opto-cards corresponding to number of modules in the disks.

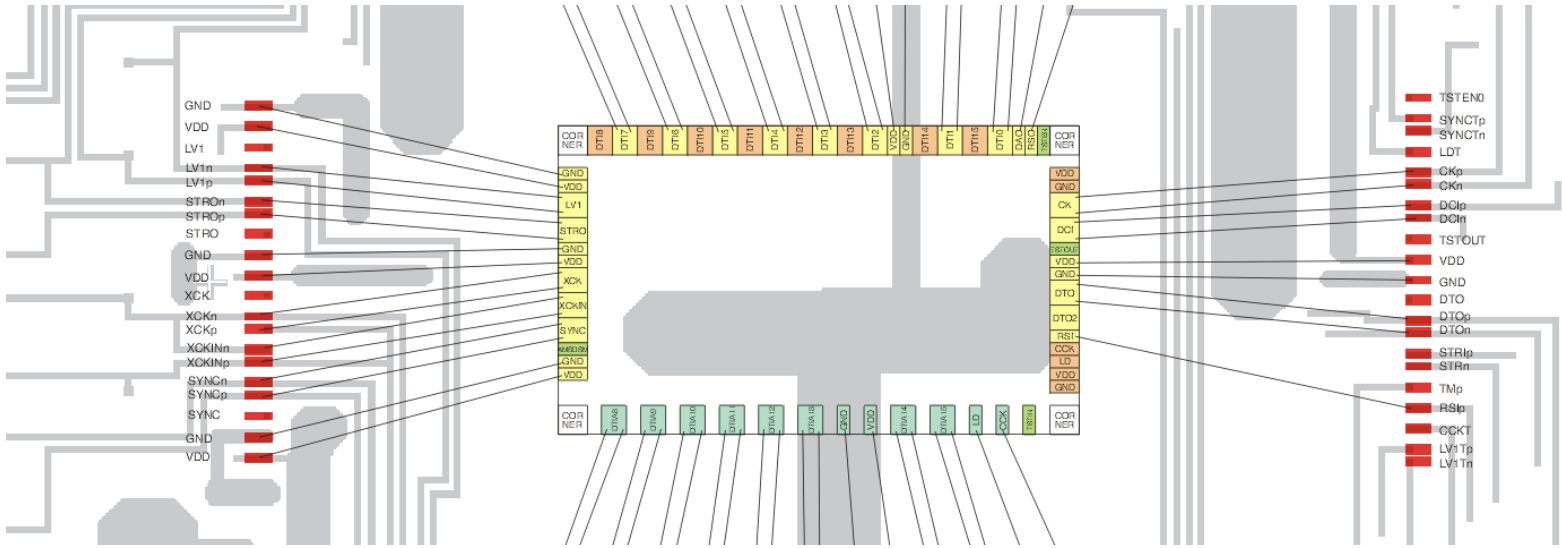
Electronics Challenges and Requirements

Main challenges are in FE chips:

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Cope with reduced signal of 10Ke and sensor leakage current of up to 50nA per pixel at end of lifetime. For the B-layer, this corresponds to a lifetime of about 2 years at design luminosity.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of about 3Ke with good enough timewalk to have an ìin-timeî threshold of about 4Ke (hit appears at output of discriminator within 20ns of expected time). This requires a small threshold dispersion (about 300e) and low noise (about 300e).
- Associate all hits uniquely with a given 25ns beam crossing. Contributions to this timing come from timewalk in the preamp/discriminator, digital timing on FE chip, clock distribution on module, and relative timing of different modules.
- Meet specifications with nominal analog power of 40μW/channel and nominal total power for FE chip of 200mW (worst case budget is 70μW and 350mW).

Status of MCC chip:

- First version fabricated by Genova in AMS technology. Chip is roughly 70 mm^2, and 400K transistors. Other than a few very minor errors, it works well.
- Second generation fabricated in DMILL process. Chip is 100 mm^2. Observed yield is poor (less than 10%), and design never worked properly at 40MHz.
- New version in 0.25µ included in FE-I engineering run. Includes a small changes in Verilog description based on test results from MCC-D2 and minor evolution of requirements. Includes 128 word FIFOs instead of 32 word FIFOs.
- All functionality now included, such as programmable delay for Strobe generation, and dual output to drive 1/2 links in 40Mbit/s or 80Mbit/s mode, total of 160Mbit/s.
- New pinout adopted to allow wire-bonding chip to Flex within strict mechanics envelope. All pads placed on three sides only (all 16 data inputs on one side):



FE Electronics Prototypes

Several generations of prototypes have been built:

- First ìproof of principleî chips were built in 96.
- First realistic prototypes were designed in two parallel efforts in 97/98, producing a rad-soft HP prototype (FE-B) and a rad-soft AMS prototype (FE-A/FE-C). These were 18 column, 160 row chips with 50µ x 400µ pixels.
- Prototypes of critical elements made in both rad-hard processes (TEMIC DMILL and Honeywell SOI) to study performance and radiation hardness.
- Initial rad-hard activity focussed on common design DMILL chip (FE-D), followed by common design Honeywell chip (FE-H).

Features of initial rad-hard FE design:

- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

Initial Radiation Hard Strategy

Pursued essentially identical designs with two vendors:

- **ATMEL/DMILL:** Began first work on FE-D in Summer of 98. FE-D1 run was submitted to TEMIC on Aug 10 99. Design contained some ìsimplificationsî in digital readout from FE-B design to fit into DMILL constraints, as well as some improvements. Performance targeted at outer layers, with 400μ pixel and 24 EOC buffers per column pair.
- Comments: Initial version of front-end chip (FE-D1) showed very poor yield, concentrated in two circuit blocks. Second set of wafers for initial run were processed (FE-D1b), and showed same behavior. Extensive testing pointed towards technology problems. Second run was made, with two versions and minor bug fixes (FE-D2). No improvement observed, and vendor was dropped.
- **Honeywell/SOI:** Began serious work on FE-H in Fall 99. At this time, only LBL and CERN had TAA agreements in place to do design. In addition, Honeywell was in process of revising Layout Rules, which caused significant delays. A number of minor improvements relative to FE-D, taking advantage of better device density and third metal layer. Design was made more robust, and performance was targeted at B-layer as well (400μ pixel with 32 EOC buffers).
- Comments: Had completed almost all layout work and were just starting verification in July 00, when we learned of cost increase to $20K$/wafer in large quantities. This made continued work impractical, and this path was abandoned.

Deep Sub-micron Approach:

- One of dominant effects of irradiation of CMOS devices is creation of trapped charge in the critical gate oxide layers. Below about 10nm oxide thickness, the charge trapping largely vanishes due to quantum tunneling effects. Modern 0.25µ processes are the first to operate fully in this regime (they have 5-6nm oxides).
- The RD-49 collaboration has studied details, confirming that if one controls leakage paths using layout, then a commercial 0.25µ process can be very rad-hard (circuits tested to 30MRad). Many technical concerns addressed, but basically little experience with full-scale devices, so some concerns still remain.
- All experience so far with analog and digital designs suggests that the silicon behaves almost exactly like the SPICE BSIM3 simulations. Nevertheless, given our lack of experience with these processes, we are planning several prototypes.
- CERN has negotiated a frame contract for LHC with IBM for their CMOS6 0.25µ process which extends through 2004. This fixes prices and terms for engineering and production runs, and would provide the basis for our production procurement. We can also access the TSMC 0.25µ process in production quantities via the MOSIS consortium as a back-up should problems arise.
- This path places us into commercial mainstream, where we can be assured of low prices and availability in the future. Depending on R&D in 0.18µ and smaller feature sizes, it provides a technology path for upgrades to the B-layer. By 2005, roadmaps suggest ìbaselineî process would be 0.10µ 9-metal, operating at 1.0V.

Development program for FE-I 0.25μ FE chip

- Serious effort began in Sept 00, with 3 day design workshop at LBL. We benefitted from many discussions with Fermilab BTeV group (Mekkaoui and Huff) and RD-49 people (Snoeys, Anelli, Faccio, Cervelli), and clearly previous work helped us start more rapidly.
- Decided to pursue design path which is, in principle, compatible with submission of common design to either IBM or TSMC.
- This involved extensions to the ìstandardî RAL design environment for TSMC compatibility. It also required upgrades to the standard cell library for TSMC compatibility, separate digital substrate connection, and satisfying density rules for lower layers.
- Serious concern about getting rapid start in complex, new process was addressed by a series of test chips.

Test chip program in 0.25μ

Digital Test Chip:

- First TSMC submission done Jan 8 01 was a digital test chip, including various blocks from readout.
- This included several basic blocks from readout, such as pixel differential SRAM and readout sense amps. It also included three different shift register designs, organized in long strings, for SEU testing.
- It also included first analog blocks such as DAC and current reference, and LVDS I/O. A very first version of the preamp was included.
- Due to several last minute problems with verification tools, this chip was submitted without LVS, and it contained many basic connectivity errors. In the end, we did manage to demonstrate that the pixel RAM was working, but all analog blocks were useless because of power supply shorts.
- We learned a great deal from this, despite problems.
- Improved digital readout design includes 8-bit timestamps, and fully static and differential storage and readout in pixel matrix. TOT processing is now included at the bottom of column. It is a much more ìtop-downî design, where all major logic blocks (hit logic in pixel, CEU and TOT processor, EOC logic, and readout controller) use place and route, and where possible, high-level synthesis.

Analog Test chips:

- Second pair of submissions was an analog test chip to IBM (Feb 28 01) and TSMC (Mar 5 01).
- This chip included all major analog blocks for FE-I in fairly mature form.
- The preamp block had approximately final layout, and included the present set of 14 SEU-tolerant FF bits for threshold trim (5-bit TDAC) and feedback trim (5-bit FDAC), as well as Kill, Enable, HitBus, and Select FF for control.
- The preamp uses the same ìDC feedbackî technique contained in our previous chips, somewhat modified due to the constraint on minimum W/L for enclosed NMOS (no long NMOS). The new design uses a single power supply, which simplifies the services, but complicates the design. It is now a two stage design, with a rather low preamp gain, and is fully differential from the preamp output onwards.
- The test chip included 20 pixels, each with a selectable capacitive load and programmable leakage injection. All of the bias generation was on-chip, including a total of 15 8-bit current DACs, internal VCal injection with a new chopper design where each pixel had its own chopper.
- The TSMC version of the chip returned in mid-May. The IBM version was not received until the end of June due to multiple shipping errors in CERN wafer handling.
- Two TSMC irradiations and one IBM irradiation were performed at LBL.

Analog Test Chip summary:

- After about two months of characterization work, we reached the following major conclusions:
- The detailed electrical performance of TSMC and IBM are rather different. In particular, the epi-substrate doping is much higher in IBM, leading to very high parasitic capacitances for PMOS wells. This significantly limited the timing peformance of the IBM test chip.
- Our present design has major problems with threshold dispersion. These appear in the initial threshold tuning of the chips, were untuned dispersions in the range of 1500e - 2000e are observed. In addition, although the dispersion can be tuned to an acceptable level with the 5-bit TDAC, after irradiation to several MRad, the channels have re-dispersed back to roughly their original untuned dispersion.
- Our ability to understand the test chips quantitatively was severely limited by the lack of basic capacitor arrays, and the rather poor information on parasitic capacitance provided by IBM.
- However, in all areas besides threshold dispersion, the influence of radiation (60MRad and 120MRad for TSMC, and 60MRad for IBM) had only very minimal effects on the operation of the design. Even trim DACs with LSBs in the 100pA range showed only modest changes.

FE design revisions in response to ATC results

- After significant analysis of the threshold dispersion problem, we concluded it is due to VT matching problems, but they are distributed throughout the design. About 1/3 of the problem is in the preamp, the rest is in the second stage. No minor design modifications seem likely to significantly improve this problem.
- For this reason, we have left the basic FE design unchanged, but we have significantly increased the preamp gain by reducing the feedback capacitance. We estimate that the baseline design (FE-I1A) has about 1.8 times the gain of the IBM test chip, and the high-gain version (FE-I1B) has about 3 times the gain. This extra gain should translate into reduced threshold dispersion.
- In addition, the feedback design involved the use of PMOS with their wells not connected to VDDA. In the IBM process, these long PMOS added about 60fF parasitic capacitance directly on the preamp output. In the present design, there is no source follower present, so this has a large effect (risetime degraded by more than a factor of 2). We have devised an improved feedback design which requires one small PMOS instead of two long PMOS, reducing this parasitic by roughly a factor 4. This gives us quite acceptable timewalk performance in simulation.
- Untangling these problems required several months of work. In addition to the difficulty of integrating the complete chip, this has resulted in 2 months additional delay in submission compared to predicted date from June (9/26 used in ATLAS project plan). This gives total delay of 4 months compared to original schedule.

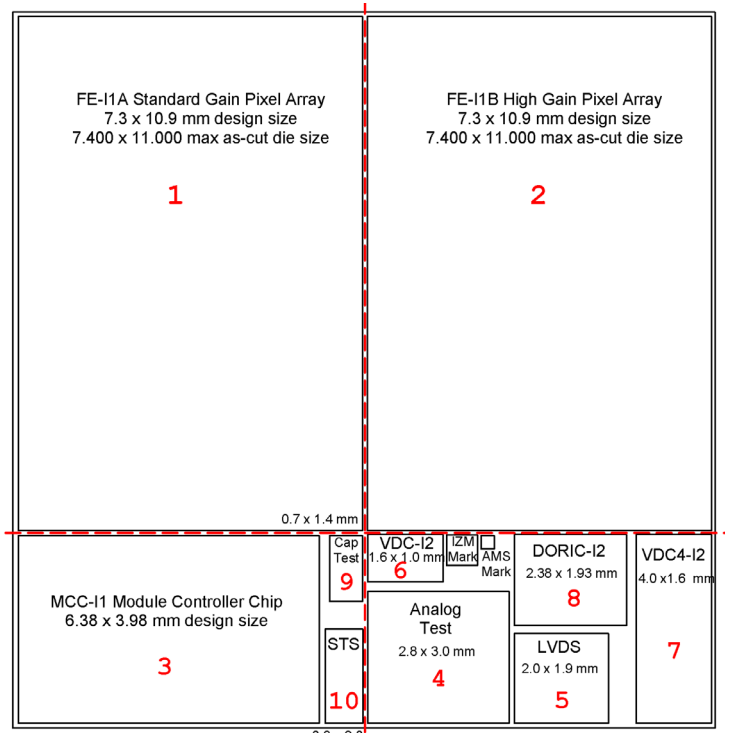
Verification process for FE-I

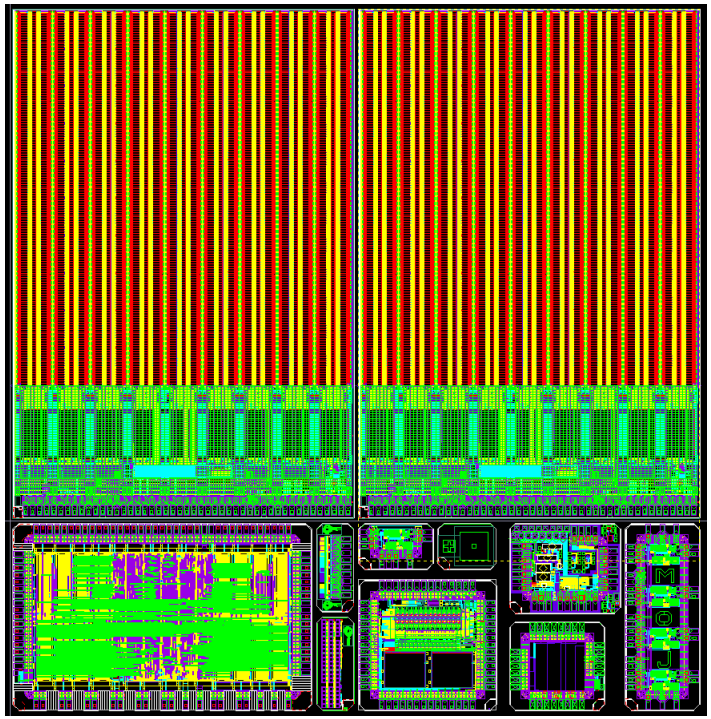
- Analog design has been verified with very extensive HSPICE simulations. This includes threshold and noise performance, TOT behavior, timewalk, cross-talk, leakage tolerance, etc. Much effort went into comparison of the simulated and measured results for our TSMC and IBM test chips, and in general, the agreement is quite good. We have added post-layout parasitics, including capacitances and diodes (especially the NWell diode created by PMOS). We need to gain more experience with matching issues, but we have the impression that the CERN data is a good guide.
- Complete design has been verified for functional behavior using Verilog, based on standard cell library for functional descriptions of some blocks. This will not include wire loading effects in a very realistic way, but the CERN/RAL standard cells are not very sensitive to such effects (min size rad-tol inverter can drive 1pF load with about 2ns risetime !).
- We have created a ìlittle chipî which is a sub-set of the full chip, including only one block of 16 pixels per column, and including only 2 EOC buffers per column. This complete chip has ìonlyî 300K transistors (compared to 2.5M for the complete FE-I). This chip has been used extensively to LVS/DRC and simulate.
- Digital design has been verified for timing performance using TimeMill and PowerMill tools. These tools accept a SPICE netlist and BSIM3 models, and perform a highly accelerated simulation, using adaptive criteria to simulate digital blocks rapidly while still simulating analog blocks accurately.

- TimeMill and PowerMill simulations were done of a complete column pair, including all post-layout parasitics. Simulations were also done of the complete little chip, with and without parasitics.
- PowerMill toolset also allows detailed understanding of power consumption of design at block level. Initial results suggest that we are somewhat above our digital budget, but not far from spec. Nominal and worst case budget for VDD is 25mA and 40mA, whereas Powermill suggests 25-30mA of idle current and about 50mA of current at full occupancy.
- Schematic level simulations of column pair and little chip were successfully performed for ìworst caseî of 1.8V supply, -3σ models, and 60MHz clock. Simulations of column pair and little chip were successfully performed, including all parasitics, for typical conditions. This is a smaller set of timing simulations than ideally preferred, but these simulations started very late.

What is included in the FE-I Engineering run ?

- Complete module chipset, including two versions of FE-I1 and new MCC-I1.
- Next generation of opto-chips, including VDC-I2, VDC4-I2, DORIC-I2.
- LVDS Buffer chip for use in support cards
- Test chips, including Analog Test Chip, modified CERN STS (standard test structure) and CapTest chip including capacitance measurement circuit for about 60 different M1/M2/M3 structures.
- Alignment marks for bump-bonding vendors.





- LBL has taken responsibility for global integration and verification of reticle.

Present status of FE-I engineering run

- All designs are integrated into reticle which is 15.00 x 14.70mm. Reticle size and layout information has been transmitted to IBM.
- PO is in place for the initial six wafer run, and all TIDs should have been done from the six contributing pixel accounts (this took one month!). Second set of TIDs will be done for the modest additional charge for six extra wafers in the near future.
- Complete DRC checking has been done for all designs. We have realized that each different tool (we use Diva, Calibre, and Hercules) has strengths and weaknesses. Not all errors are found using foundry tool (Hercules) !
- DRC Waivers have been completed and will be sent to CERN today for transmission to IBM.
- IBM Waiver Acceptance Committee meets once per week, and must approve our waiver requests before the GDS file will be accepted.
- Expect to send GDS file to CERN for transmission to IBM on Friday Nov 9.
- We hope that the wafers might be available in late January, but this depends on how busy the foundry is, and on what impact the holiday season has on their turn-around. IBM has hinted the turn-around could be quite a bit faster than 8 weeks, so even first week in January is possible.

Comments on overall LBL role

- We are the critical player in this area.
- For the FE-I chip, the only collaborating institute is Bonn. They have a senior physicist/designer and one EE student working on the chip. They have made significant contributions in the analog blocks, and assembled the analog test chip. However, they have required significant help from our analog designer to complete some of this work properly, and we do not anticipate a large role for them in future submissions (their blocks are done and work well).
- We are working closely with OSU to try and improve the quality of the opto-electronic designs (now in their 5th generation and still have not converged on high quality product). This is proving more challenging than had been anticipated...
- We have developed the extended 0.25μ design kit used for all of the chips in this run. In addition, a major effort has been invested in designing a high quality pad library for both all digital and mixed-mode chips.
- We have taken responsibility for all of the final verification, reticle assembly, and technical contact role for the submission. This is significant extra work and responsibility.

Next Steps towards a production FE-I

- Preparations for testing the returning wafers will accelerate. This includes layout of simple support cards and design of probe cards, in addition to the ongoing development of the test system hardware and software (to be discussed later in this talk).
- There are simulations to finish up for the submitted FE-I, including completion of PowerMill analysis of digital power consumption, and matching analysis of final FE designs. These simulations will establish a reference for comparison to actual chip performance.
- We intend to continue working on an improved FE design, which will not be as sensitive to VT matching in the threshold control. This is expected to lead to a new Analog Test Chip submission in Spring 02. The difficulty here is that our rapid schedule and usage of 5-metal designs implies that we will need to go back to TSMC and MOSIS. However, we were somewhat surprised by the magnitude of the differences between the performance of our present design in TSMC and IBM, and therefore we are suspicious of using TSMC to develop a next-generation front-end for FE-I2.
- The above plans may be significantly augmented, depending on what additional issues appear in the real FE-I chips during testing and operation.

Testing Plan for FE-I1 Engineering Run

For FE-I wafers, single chips, and modules with MCC-I:

- New TPLL and PICT are planned route for FE-I wafer probing. They will allow very complete characterization of the FE-I chip and its many new features.
- Expect to deliver new systems to Bonn and LBL in time for wafer probing (but just barely...). Any further slippage in their fabrication schedule will make this difficult.
- Expect to deliver final TPLL and TPCC to the rest of the collaboration starting in about Feb. 02. This is later than initially planned, but should be just in time for the arrival of bump-bonded FE-I parts.
- New single chip support cards and module adapter card will be fabricated during next two months. New FE-I pinout and new Flex Support Card from Bonn for Flex4 seem well-defined enough for LBL to go ahead with board layout immediately.

For MCC-I:

- As soon as the first FE-I wafer is diced, Genova will receive MCC-I die for packaging. This will allow first testing of MCC-I with the full MCCEx system.
- Once tested die are available, some will be sent to LBL to complete testing of the TPLL VHDL code for the MCC-I. This will complete preparation of new test system.

- Genova intends to deliver a single wafer to a commercial IC testing firm in order to have them run a series of test vectors on it and characterize good chips. This wafer will be diced to provide large number of known good MCC-I die for Flex4 loading.

For opto-chips:

- After dicing of first FE-I wafer in LBL, die will be delivered to OSU for further packaging and distribution, as was done in the past for FE-D opto-parts.

For LVDS Buffer Chip:

- Peter Denes will develop a simple probe card test setup for wafer testing.
- Will then package directly into SOIC28 plastic packages and distribute for use on support cards.

For Analog Test Chip

- Will update existing single-board test system used up to now at LBL. Plan to continue packaging parts in PLCC-68 package. This work will start next week, because the analog test chip pinout is now frozen.

Organization of testing for 0.25μ chips

Engineering run:

- Processed by IBM as two back-to-back runs of 6 wafers each, where the second run does not include any NRE costs. Delivery of second group of wafers should follow within a few weeks of the first group (beginning and end of Jan 02 ?).

Wafer probing:

- Proposal for first 6 wafers is to divide them into 2 groups of 3, and probe half in Bonn and half in LBL. One of the LBL wafers would then be completely diced as soon as possible, and would provide large numbers of die for each design type. One of the Bonn wafers would be given to Genova for commercial MCC-I testing. Remaining two sets of 2 wafers would be sent to IZM and AMS respectively.
- Opto-die harvested from fully diced wafer would be sent to OSU/Siegen/ Wuppertal for testing. LVDS Buffers would be packaged by LBL for use with support cards.
- Second group of 6 wafers would be probed immediately after their arrival, but kept in reserve until first bumping results from first wafers are analyzed ?

Thinning, Dicing, and Die probing:

- Wafers are ordered ìunthinnedî with native 700µ thickness. Expect that if dummy module program validates thinning vendor(s), and dummy modules made with thinned die have good yields, then all bumped wafers will be thinned prior to dicing.
- All bumped FE-I die should be re-probed after thinning and dicing, and flip-chip should only be done using ìknown good bumped dieî. Expect Bonn to handle IZM die and LBL to handle AMS die.
- If all goes well, initial 2+2 wafers (roughly 200 FE-I per wafer) could produce as many as 15+15 modules. We should be prepared for this possibility, although real numbers may be much smaller.

Bare module probing:

- All bare modules returned from bumping vendors should be tested prior to being assembled into flex modules with Flex 4 hybrids.
- Many groups are working on performing bare module probing (Bonn, CPPM, LBL, Milano). These setups should be validated using dummy modules tomake sure there are no mechanical issues. Assuming we get many modules back, many groups should test modules.

Milestones for FE-I (taken from ATLAS schedule)

Milestones exist for FE-I1 evaluation:

- FE-I1 submission: 9/01
- Wafers back: 11/01
- Wafers Probed: 12/01
- Bumped assemblies available: 2/02
- Complete lab/irradiation tests: 6/02
- Complete beam/system tests: 10/02

Milestones for FE-I2:

- No milestone for analog test chip, since this is relatively new development
- FE-I2 FDR: 6/02
- Submit FE-I2: 7/02

Milestones for FE-I Production:

- FE-I PRR: 3/03
- FE-I production submission: 4/03

Question: does this slip by two months ?

- Critical path will be front-end improvement program, but believe answer is yes.

Thoughts on FE-I2 schedule

- The digital functionality of the FE-I1 chips includes everything that we believe is necessary for ATLAS, including some ìcontingencyî (e.g., TOT processor allows digital timewalk corrections by one crossing to compensate for possible marginal front-end performance).
- We may need to further optimize digital power consumption, depending on how the numbers come out. Within the matrix, this is already quite optimized. For the EOC buffers, power reduction would require returning to an asynchronous design, similar to that used in earlier chips.
- There may be system issues such as digital cross-talk. The digital readout uses differential transmission of timestamps to pixels and differential readout busses with reduced signal swing, with optimized layout for EMI cancellation. We have tried hard to optimize all power distribution nets and shielding (all 5 metal layers were really needed due to 70% maximum fill density). We have also included about 6pF of smart VDD decoupling in each pixel to minimize transients on digital supplies.
- Expect main issues will be in front-end performance. The present design has excellent performance in every aspect except timewalk (where it is quite good but not excellent) and threshold control. We are naively expecting dispersions of about 1000e and 600e for the two versions of FE-I. With 5-bit TDACs, these can be easily tuned to less than 100e RMS, but we know that small changes in the global threshold or in radiation dose will re-disperse the tuned thresholds.

- Present FE designer (Laurent Blanquart) will begin to work on an improved second generation design later this month. Expect that this should take several months (comparable to design and layout effort for initial front-end design).
- Problem is prototype path. For IBM, no signs of interest in LHC community in 5-metal submissions (stupid initial decision to use 3-metal to save money has locked community into this path - MOSIS 0.25μ runs are all 5-metal !). Converting our design back to 3-metal is very painful. Pad library and front-end design are fully optimized for 5-metal fabrication. For TSMC, we would need to develop improved pad library based on designs used for Feb run (probably useful in any case), and understand more deeply the differences between the two processes.
- Only alternative is to submit a full FE-I2 run with an alternate front-end design, without the benefit of prototyping in a test chip first.
- We will argue this out over the next few weeks and chose our direction for next-generation FE prototyping...
- If we follow ìmost conservative scheduleî path, this would involve a TSMC prototype chip submitted say in March 02, returning in mid-May (same dates as this year). This chip could be fully evaluated in about 1 month. Depending on the results, and on how compatible that new design would be with the existing chip infrastructure (room for circuitry, bias requirements, control requirements), integration of the design could be quite rapid.
- Believe that a schedule slippage of 2 months is plausible (FE-I2 submission in 9/02), but this will depend on schedule pressures from overall ATLAS/LHC too...

Test System for FE Chips and Modules

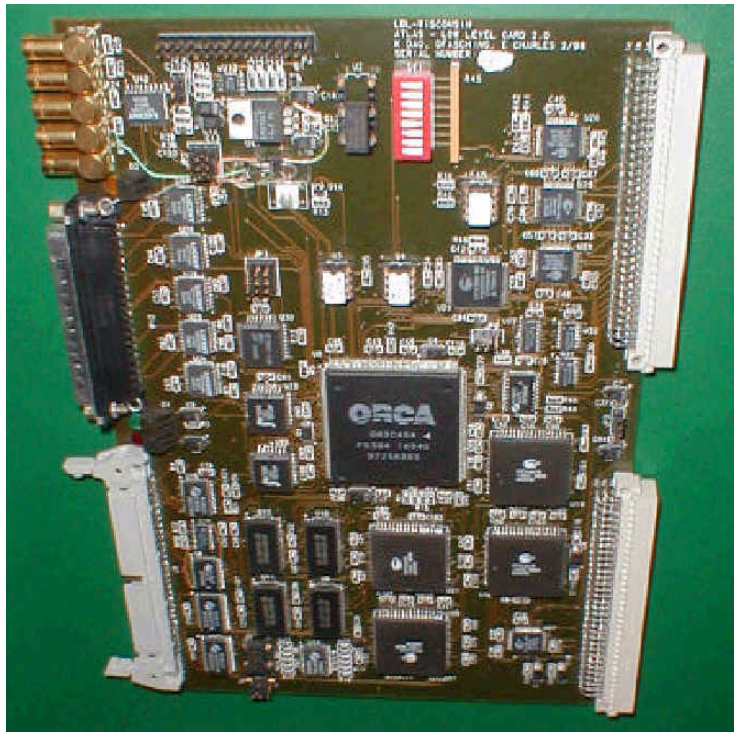
History:

- LBL/Wisconsin developed original test system in 97/98 for use with initial rad-soft pixel ìdemonstratorî prototypes.
- This system has been successfully used for wafer probing, and characterizing single chips and modules in the lab and in the testbeam.
- A total of 16 such systems are presently in use throughout the pixel collaboration. They are the standard with which all chips and modules are evaluated.
- The use of a common, high-performance test system for this full range of activities has allowed greater efficiency and easier comparison of results.

Overview:

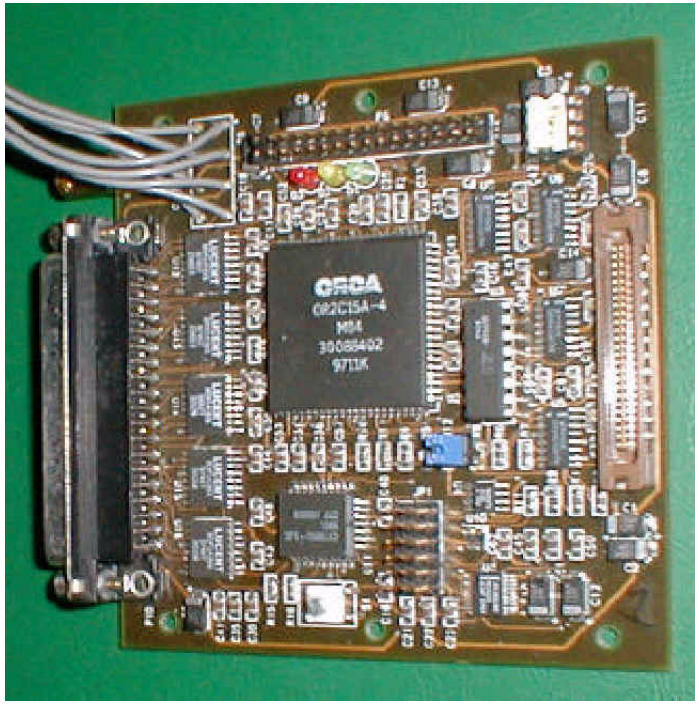
- The system consists of a PC host running National Instruments software environment and one or more VME boards (so-called PLL).
- Each VME board drives a local control card (PCC) over a long cable (20m), which in turn drives the individual test cards (support cards) over a short cable (1m).
- There are now several generations of test cards supporting the different applications from wafer probing to single chip testing to bare module testing and the first two generations of Flex modules.

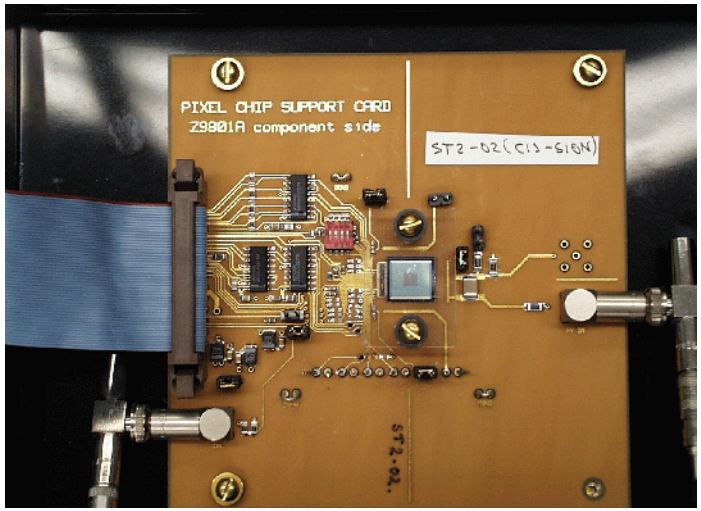
Components of Current Test System:

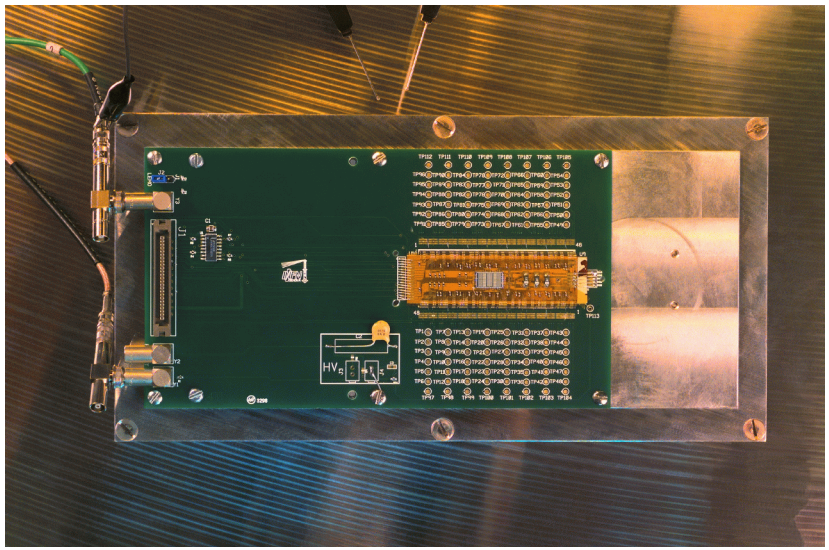


PLL

PCC





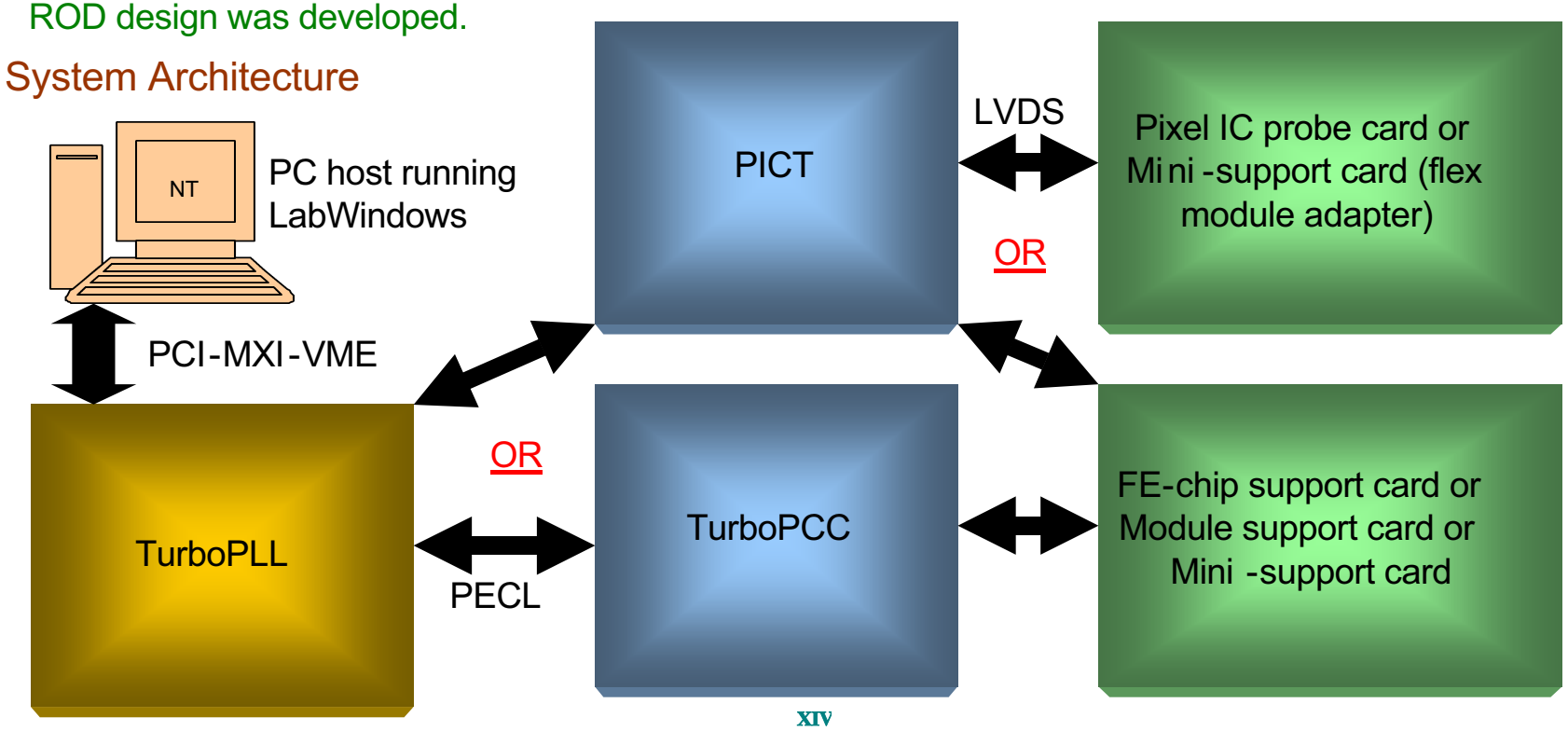


Upgraded Test System

- New generation under design. Incorporate experience with present system, and optimize to cover complete range of production needs with one modular set of hardware and software, keeping same basic interfaces to provide flexibility.
- Includes upgrades for greater range of test capability (vary amplitudes and timing), plus optimized buffering and variable frequency testing:

Architecture is directly based upon the original PLL approach, which had proven so ideally tailored to our needs and which represents the model upon which the ATLAS ROD design was developed.

System Architecture



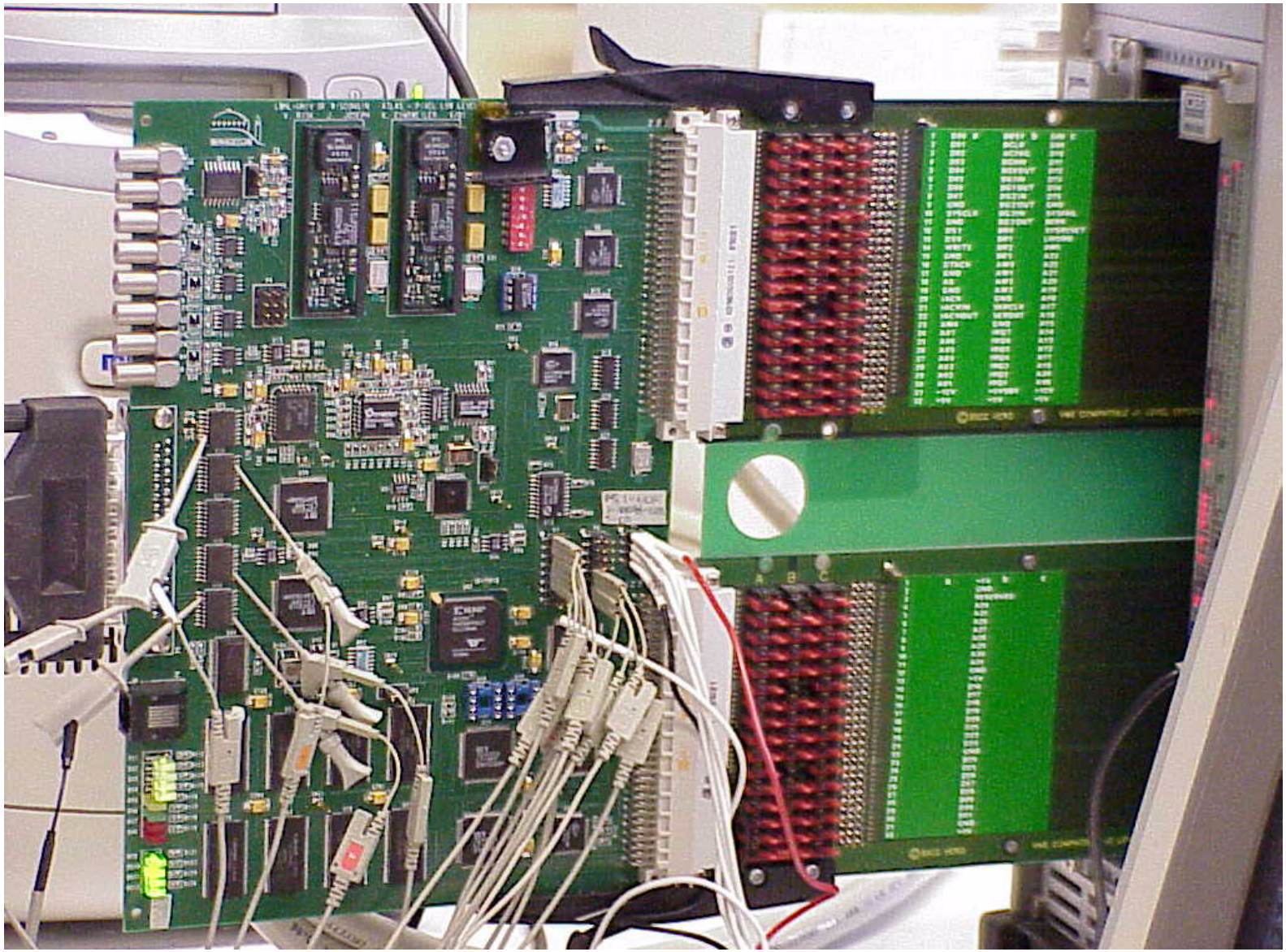
Design Goals:

- New system uses current generation FPGA for much more programming flexibility (old FPGA completely full, making code revisions very difficult).
- New system allows complete evaluation of operating margin available in each chip. Optimized cuts can then be used to select die and modules that should continue to work properly after full lifetime radiation doses.
- Cover wider range of needs, including parametric testing at all stages from initial wafer probing, to module testing, and module burn-in.
- System designed to allow operation over wide range of supply voltages, from a minimum of 1.6V up to 4V, to cover testing of 0.8μ and 0.25μ (and below) chips.
- New system should be operating in time for complete characterization of 0.25μ FE-I wafers and chips, but this schedule is now extremely tight...

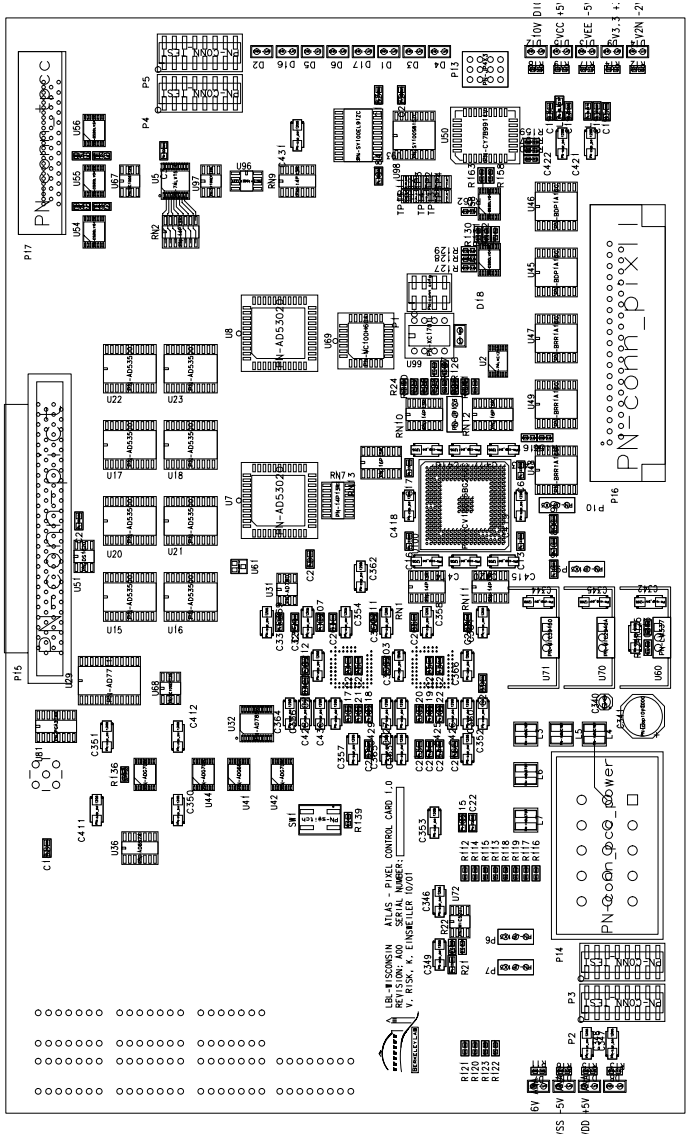
Schedule:

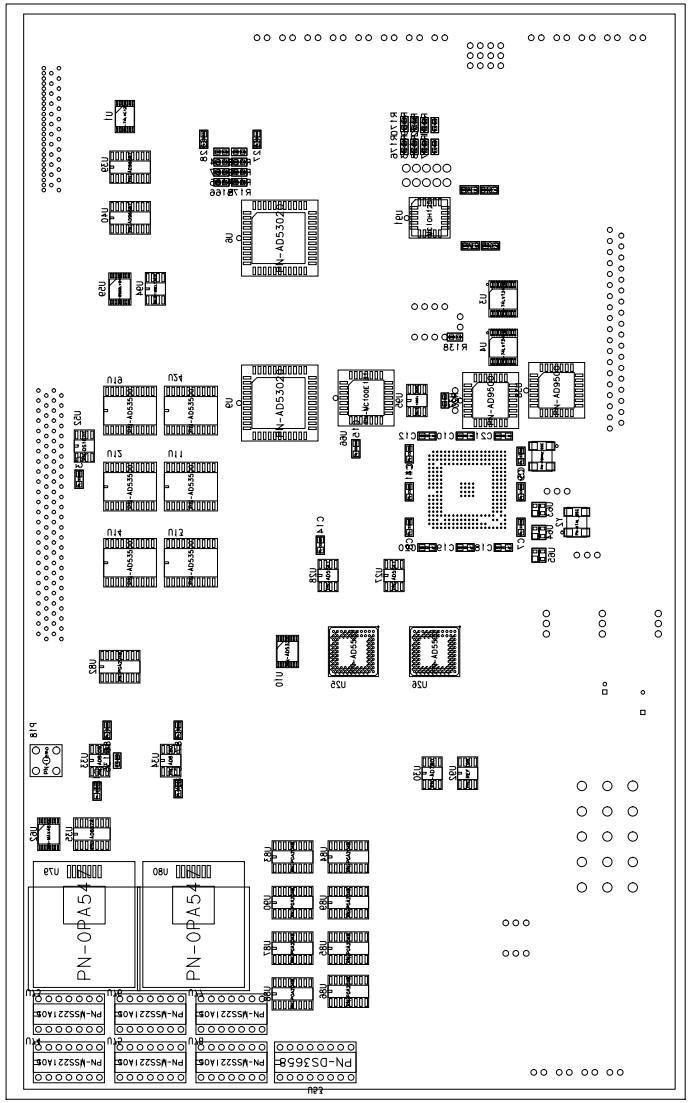
- TurboPLL design is complete. First version fabricated in May 01. Known errors/ omissions include: lack of circuitry for 80Mbit/s stream decoding, plus minor part geometry errors (front-connector and negative regulator inverted). For now, initial three boards are loaded, and will be debugged for first FE-I testing. The known errors will be handled with minor revision of board in Dec 01, prior to production run of 20 boards.
- TurboPLL VHDL ported from previous system, and testing now almost complete. Integration of output FIFO functionality required to decouple board clock and chip clock has required more VHDL improvements than expected. Expect to complete debugging and implement FE-I/MCC-I upgrades during November. Upgrading of PC host software has been proceeding in parallel.
- Expect revised boards to go out for fab by mid-December. Will load boards commercially, and should be shipping boards to collaboration by late Feb 02.
- PICT design is complete. Board layout in progress, with about 10 days to go before submission for fabrication (before Thanksgiving ?) Would initially load 3 boards for first FE-I testing, and expect to have boards in lab by mid-December.
- VHDL work is ongoing (and fairly simple). Complete command set defined, and PC host software being written now. Expect to have functional system by Jan 02. Difficulty will be to deliver working system to Bonn in time for initial wafer probing.

TPLL in Pixel lab:



Status of PICT Layout:



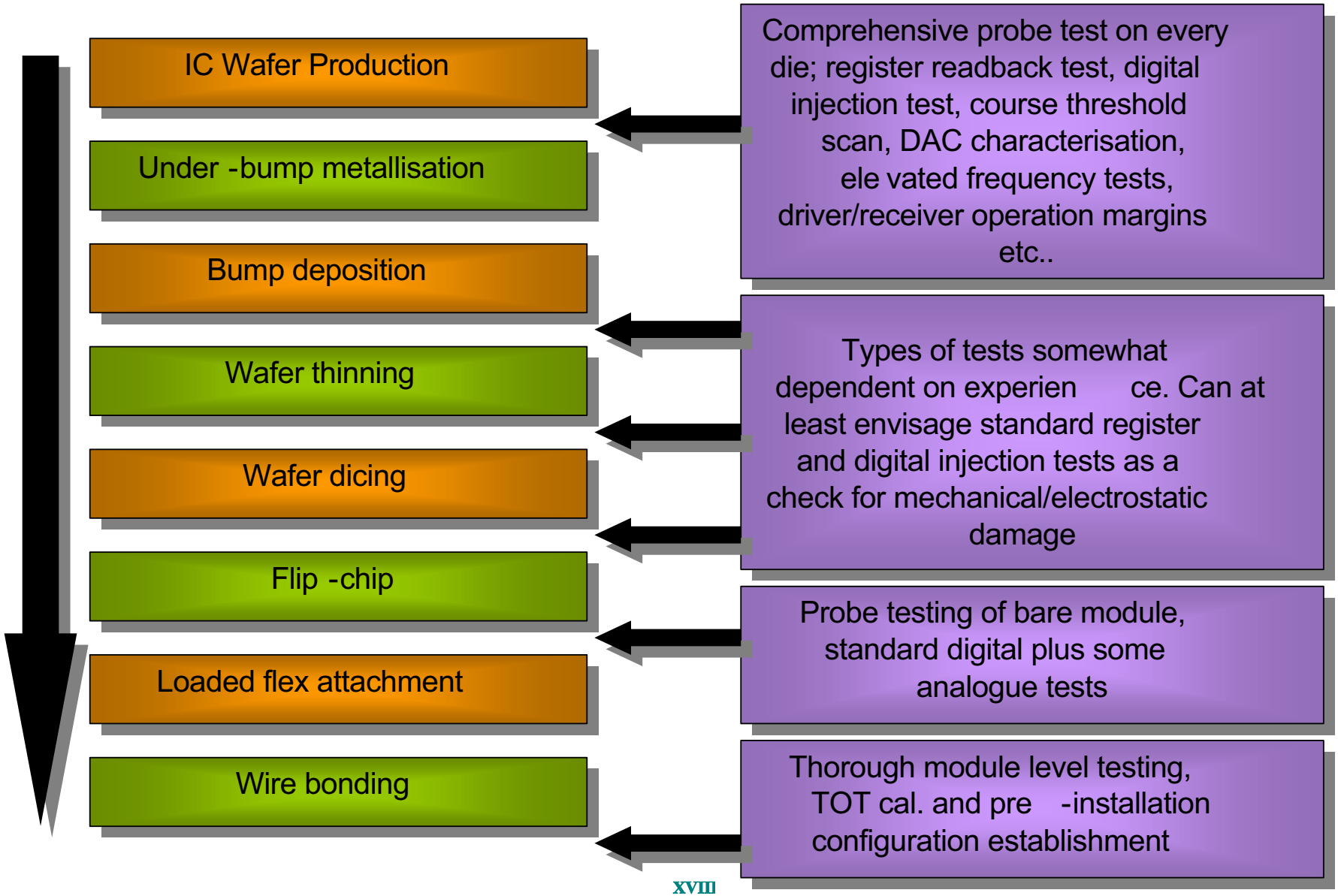


- PLL and Power enter on right (bottom), PCC and PICT output is from left (top).
- Not all passives placed, and routing not yet started, Plan for 12 layer board.

Evolution of testing systems

- Present testing has emphasized single chips or single modules. This is what the PLL/PCC design was optimized for. Simple tests are being done with 2 modules using brute force approach of two PLL and PCC.
- Next major step is basic system test with a sector or a half-stave, using ROD. Given present state of pixel opto-links, propose to proceed with copper-based BOC. This is called the SimpleBOC, and uses LVDS links over twisted pair cable for two groups of 7 modules. It would operate comfortably over 10 meters. The module end would be plug-compatible with the opto-daughter card interface, and would plug into PP0. This copper link could be transparently replaced by real opto-links as the necessary hardware/software becomes available.
- This scale of test system will evolve into the object used during macro-assembly (module mounting onto sectors, and assembly of sectors into disks).Not yet clear how important ROD-based testing will be during assembly. Alternative approach would be to use PLL-based system to exercise individual modules.
- Intend to build a 10% scale system for commissioning purposes beginning in about 2004 in the SR building at CERN. Not clear when/whether the center of gravity of system testing would move from macro-assembly institutes to CERN. The CERN system might not be set up significantly before delivery of barrels and disks to CERN.
- Final step is the full readout system for ATLAS.

Production Testing Plans



- New system addresses range of needs from wafer probing to module burn-in.

On-detector Electronics Deliverables:

US Responsibilities include:

- FE chip design, testing and production (LBL): Contribute roughly 20% towards the common procurement of the series production. Test roughly 50% of FE ICs.
- Opto-link chip design, testing and production (OSU): Contribute approximately 50% towards the common procurement of the series production.
- Design and provide hardware/software for lab/testbeam single chip and module testing, production FE wafer probing, production module testing/burn-in (LBL).

LBL engineering personnel estimate:

Person	Months in FY02	Months in FY03
Laurent B	12	12
Peter D	2.5	2.5
Emanuele M	4	2
Gerrit M	5	3
Bryan H	3	1
John J	4	1
Valerie R	3	
Chinh V	4	3
Engineer Total	37.5	24.5
George Z	2	2
Helen C	1	1
Technician Total	3	3

- IC tasks include FE-I1, FE-I2, and FE-I3 (production chip). Continuing manpower is concentrated on front-end issues, assuming that other parts of the design are basically very close to production quality.
- Board tasks include completion of TPLL/PICT/TPCC plus SimpleBOC in FY02, and completion of production burn-in system in FY03.
- Continue to assume that all chip testing and most board testing is performed by physicists, with use of engineering manpower only has needed for technical problems.

- Project resources in present budget:

PROFESSIONAL	FY 96	FY 97	FY 98	FY 99	FY 00	FY 01	FY 02	FY 03	FY 04	FY 05	Calculated Total	Entered
Software Prof.	.0	.0	.0	.0							.0	.0
Engineer - EE	.0	.0	.0	.0			2.1	1.2			3.2	.0
Engineer - ME	.0	.0	.0	.0							.0	.0
TECHNICAL												
Design & Draft	.0	.0	.0	.0							.0	.0
Electrical Technician	.0	.0	.0	.0			.2	.1			.3	.0
Mechanical Technician	.0	.0	.0	.0							.0	.0
Admin. Supervisor	.0	.0	.0	.0							.0	.0
Other Admin	.0	.0	.0	.0							.0	.0
TRADES												
Contract Labor	.0	.0	.0	.0				.5	.3		.8	.0
Shops	.0	.0	.0	.0							.0	.0
Technical Services	.0	.0	.0	.0							.0	.0
Student	.0	.0	.0	.0			.3	1.0	.3		1.6	.0
TOTAL LABOR	.0	.0	.0	.0	.0	.0	2.6	2.8	.5	.0	5.9	.0

Trades Legend:
Contract Labor = Job Shopper
Shops = Fabrication (in-house facility) from raw materials
Technical Services = Rigging, electricans, etc.

- Additional resources from base program:

PROFESSIONAL	FY 96	FY 97	FY 98	FY 99	FY 00	FY 01	FY 02	FY 03	FY 04	FY 05	Calcu-lated Total	Entered
Software Prof.	.0	.0	.0	.0							.0	.0
Engineer - EE	.0	.0	.0	.0			2.0	1.8	.5	.5	4.8	.0
Engineer - ME	.0	.0	.0	.0							.0	.0
TECHNICAL												
Design & Draft	.0	.0	.0	.0							.0	.0
Electrical Technician	.0	.0	.0	.0							.0	.0
Mechanical Technician	.0	.0	.0	.0							.0	.0
Admin. Supervisor	.0	.0	.0	.0							.0	.0
Other Admin	.0	.0	.0	.0							.0	.0
TRADES												
Contract Labor	.0	.0	.0	.0							.0	.0
Shops	.0	.0	.0	.0							.0	.0
Technical Services	.0	.0	.0	.0							.0	.0
Student	.0	.0	.0	.0							.0	.0
TOTAL LABOR	.0	.0	.0	.0	.0	.0	2.0	1.8	.5	.5	4.8	.0

Trades Legend:
Contract Labor = Job Shopper
Shops = Fabrication (in-house facility) from raw materials
Technical Services = Rigging, electricans, etc.

- In principle, we could reduce our needs for FY02 and FY03 slightly from these estimates.
- Significant reduction would require giving away tasks, mainly in the board area.
- This would not be simple. The present situation is a result of our ability to deliver complete systems (hardware, firmware, software). Only Genova has this capability in the collaboration, and they have been saturated with MCC work.