ATLAS Pixel Sensors

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Features of the Experiment	Impact on the Sensor Design
10-year fluence @ innermost layer $>10^{15}$ cm^{-2} ⟨1-MeV n⟩	Guarantee stable operation @ high voltage; operate below full depletion after inversion.
$\sim 10^8$ channels (1192 sensors) plus spares; want to test these under bias before investing chips on each	Implement integrated bias circuit.
All of the other subsystems located outside the pixels	Minimize multiple scattering; minimize mass.

Many of the sensors' detailed features follow from extensive study of radiation damage effects. Summarize those:

2 types of damage:

- non-ionizing energy loss in the silicon bulk
- ionization in the passivation layers

Principal effects + impact on design:

- change in dopant concentration leads to type inversion + increase in $V_{depletion}$
  - segment n-side to operate inverted sensor partially depleted
  - design for high operation voltage
- increase in leakage current
  - cool sensor to avoid increase in noise, powe consumption
- decrease in charge collection efficiency
  - maintain good S/N; minimize capacitance

Parameterize the effective dopant concentration N_{eff} to predict the depletion voltage as a function of temperature and time:

$$V_{dep} \propto |N_{eff}| = |N_a + N_C + N_Y|, \text{ where}$$

$$N_a = g_a \cdot \Phi \cdot \exp(-t/\tau_a), \text{ “beneficial annealing”},$$

$$N_C = N_{C0} \cdot [1-\exp(-c\Phi)] + g_c\Phi, \text{ “stable damage”},$$

$$N_Y = g_Y \cdot \Phi \cdot [1-(1+t/\tau_Y)^{-1}], \text{ “reverse annealing”},$$

$$\tau_Y = 9140\text{s} \cdot \exp(-0.152T),$$

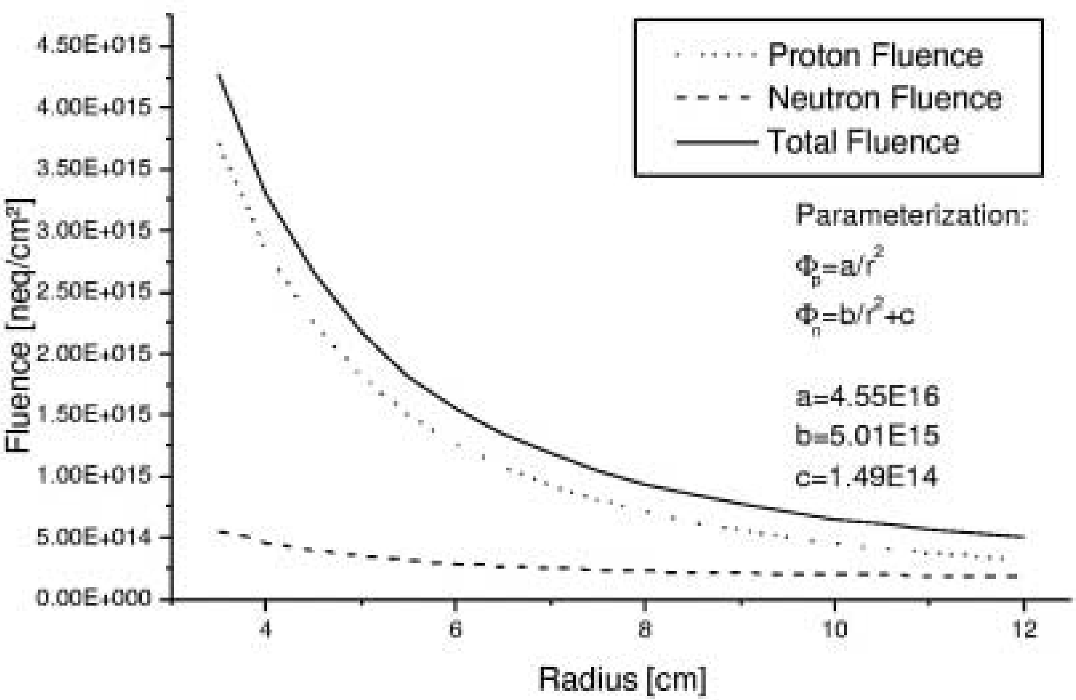
Φ is fluence, t is time, T is temperature, and

g_a, τ_a, N_{C0}, c, g_c, and g_Y are known parameters.

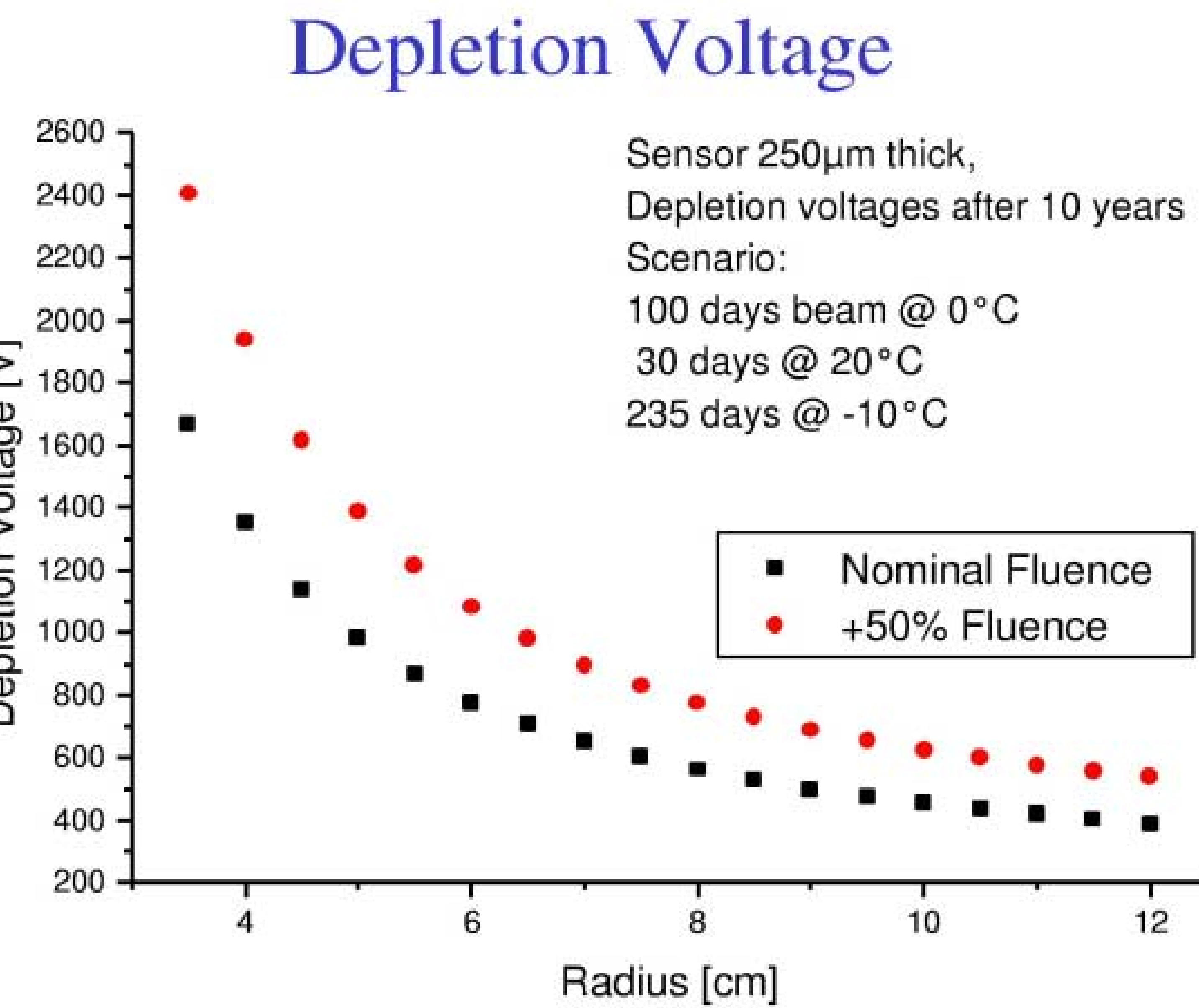
Total fluence has been predicted for each component's lifetime assuming luminosity ramp-up from $10^{33}cm^{-2}$ to $10^{34}cm^{-2}$ during Years 1-3:

ATLAS Scenario

- 100 days beam @ 0°C, 30 days @ 20°C, 235 days @ -10°C
- 250μm thick sensor
- B-Layer: Fluence 2.8E15, 85% charged, radius 4.3cm (old position
- Layer 1: Fluence 6.6E14, 70% charged, radius 10.1cm (old positior



xample prediction of depletion voltage ersus radius, for 10-year fluence:



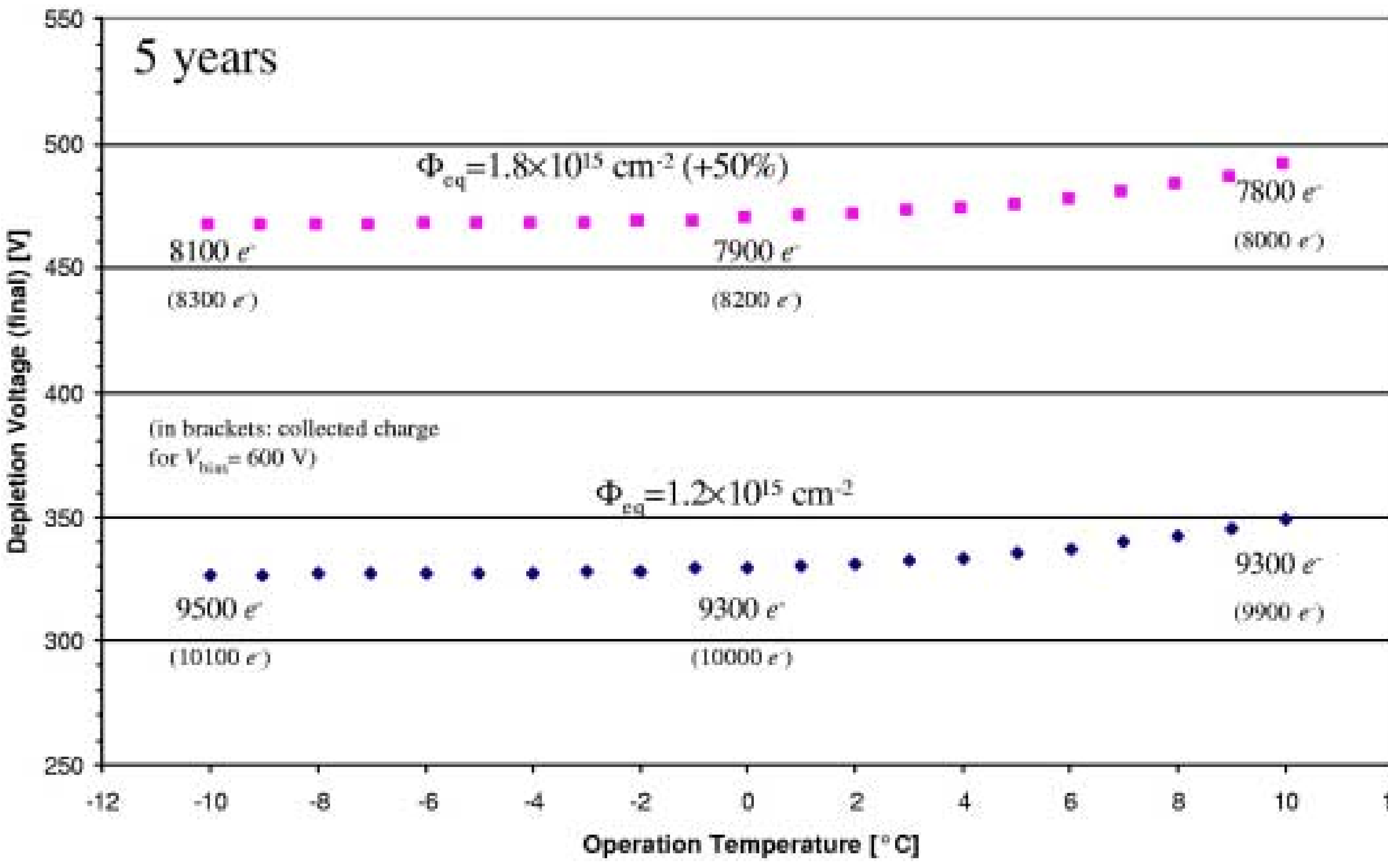
Simulations were made to select operating temperature and access time:

Depletion Voltage $V_{dep}(T_{op})$ - B-Layer - 5 years

Radiation level for B-layer: Φ_{eq}(5 years) = 1.2×10^{15} cm^{-2} resp. 1.8×10^{15} cm^{-2} (+50%)

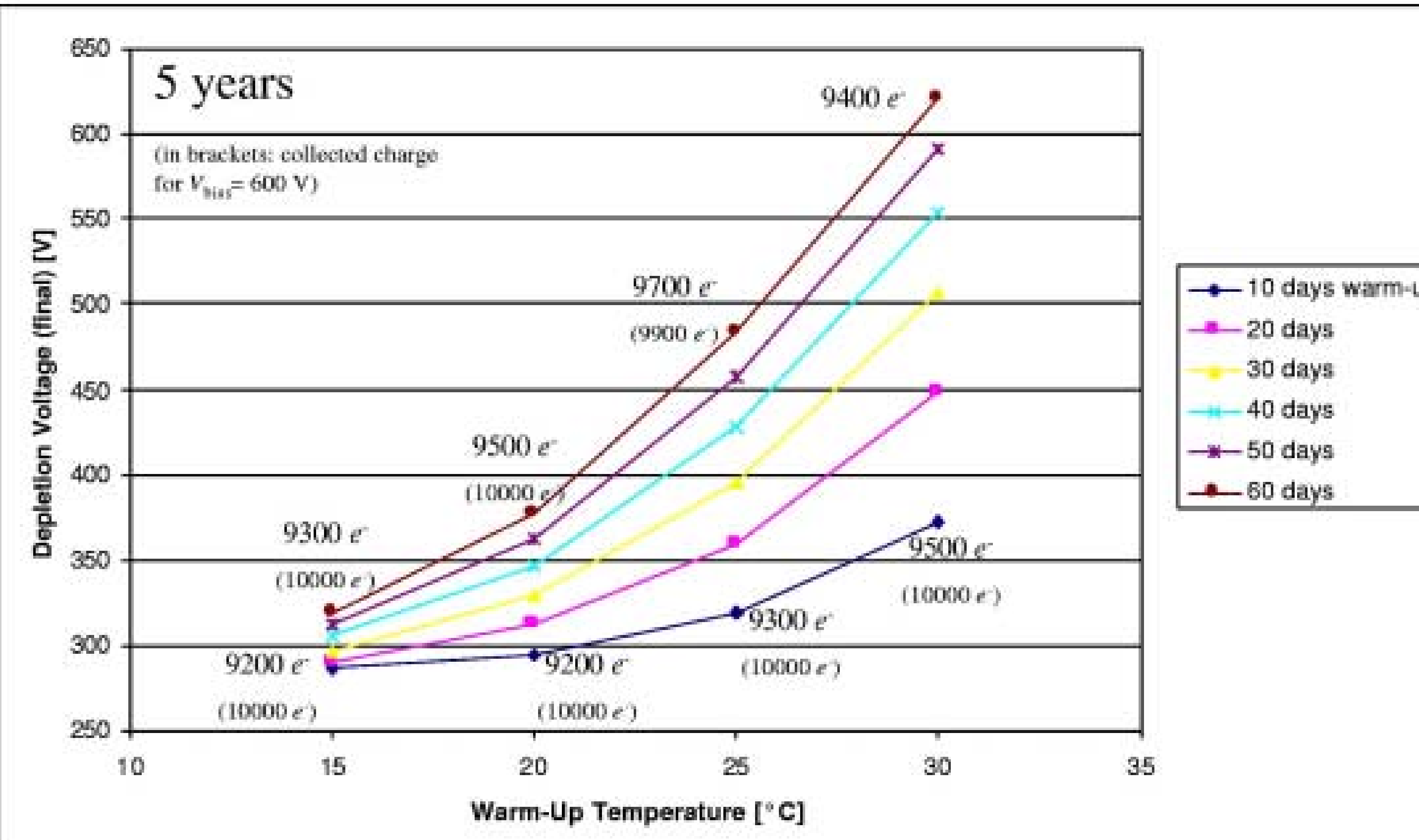
Scenario: 100 days beam at T, 30 days at 20°C, 235 days at -10°C per year

Sensor thickness 200μm, oxygenated silicon, $V_{bias}=V_{depl}+50$ V, max. 600 V



Depletion Voltage $V_{dep}(T_{warm\text{-}up})$ - B-Layer - 5 years

- Radiation level for B-layer: Φ_{eq} (5 years) = 1.2×10^{15} cm^{-2}
- Scenario: 100 days beam at 0°C, n days warm-up at T per year, rest at -10°C
- Sensor thickness 200µm, oxygenated silicon, $V_{bias}=V_{depl}+50$ V, max. 600 V



Conclusion:

100 days' operation @ 0 °C

30 days' warm-up @ 20 °C

235 days' storage @ -10 °C

General Features of the Production Sensor Design

- Rectangular sensors:
  2 chips wide x 8 chips long -
  - Each chip: 18 columns x 160 rows
  - Each pixel cell: 50 x 400 μm^2
  - Active area: 16.4 x 60.8 mm^2
- n^+ implants (dose $>10^{14}/cm^2$) in n-bulk to allow underdepleted operation after inversion
- Thickness: 250 μm

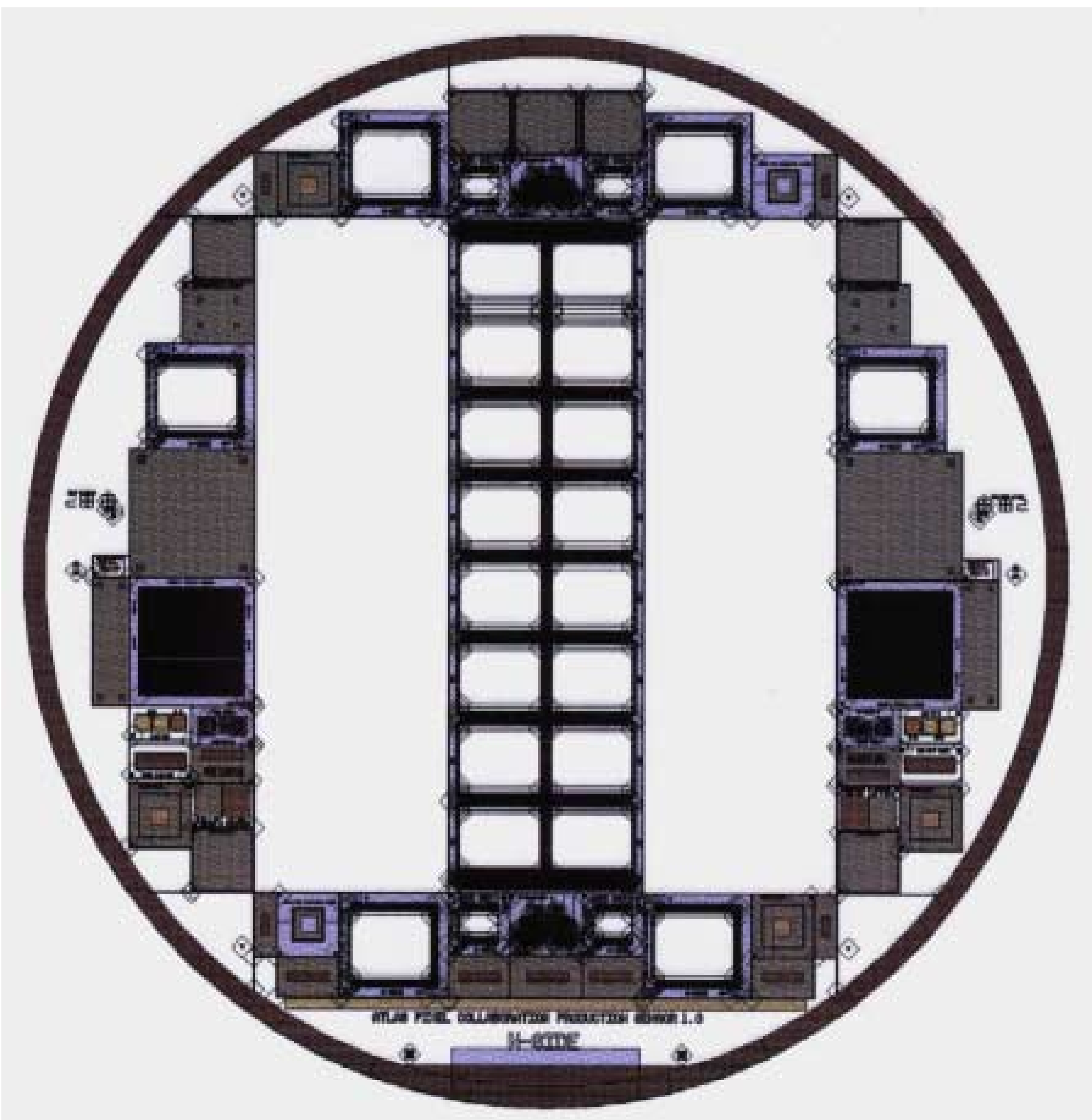
Route to the Design

- First Prototypes -
  - Designed in ‘97, fabricated by CiS + Seiko, studied in '98-'99
- Second Prototypes -
  - Designed in '98, fabricated by CiS, IRST, and TESLA, studied in '99-2000
- Pre-production Sensors -
  - Designed in '99-2000, ordered in Aug. 2000 from CiS + TESLA for delivery in Feb. 2001
- Production Sensors -
  - To be ordered following acceptance of pre-production; approx. Sept. 2001.

The Production Wafer

4-inch diameter, 250 μm thick, with:

- 3 full-size Tiles
- 6 single-chip sensors
- various process test structures to monitor oxide breakdown voltage, flat-band voltage, oxide-silicon interface current, p-spray dose



Features of the Full-size Sensors (“Tiles”)

Pitch 50 x 400 μm^2

47232 cells per sensor

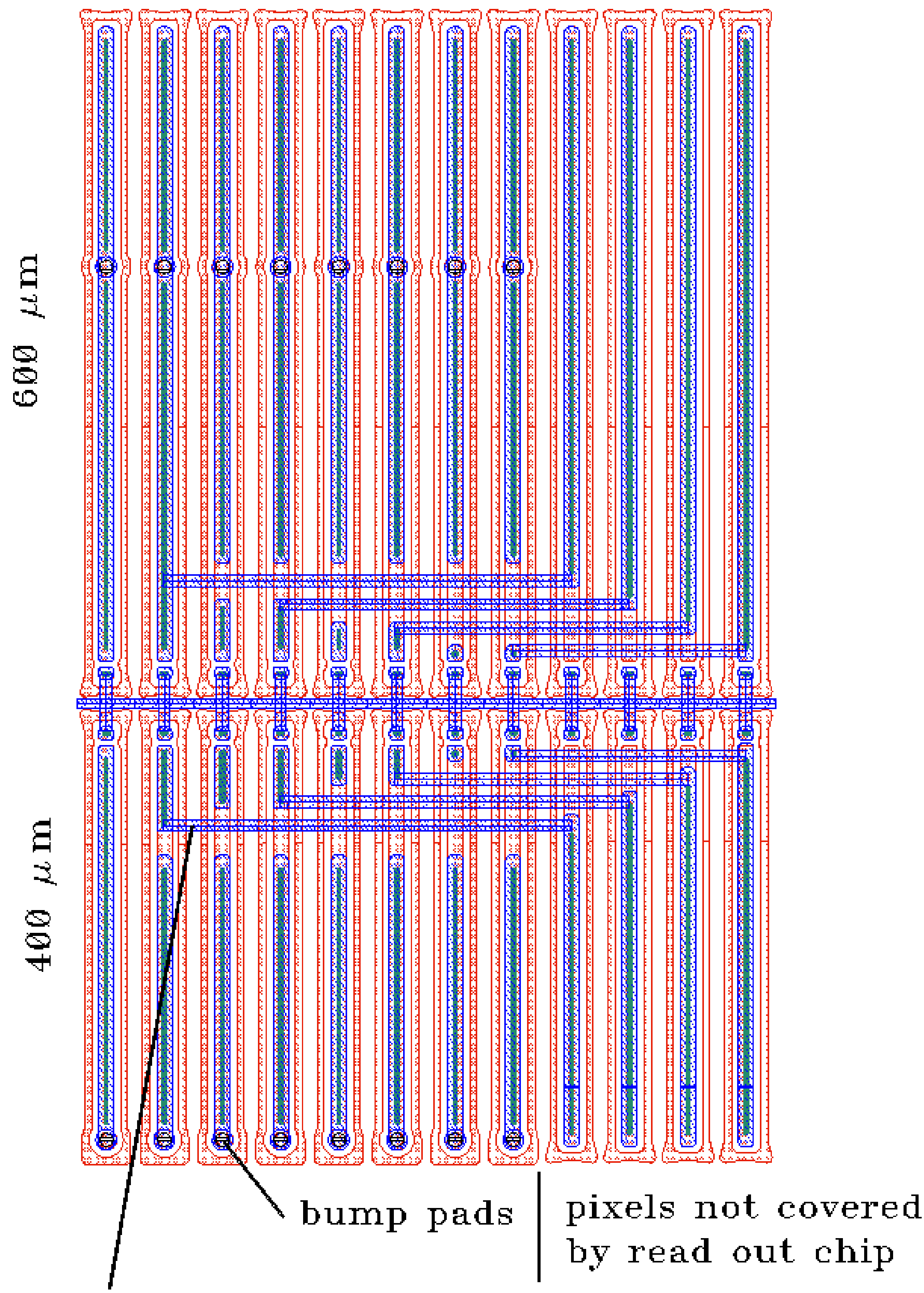
Area 18.6 x 63.0 mm^2

Active area 16.4 x 60.8 mm^2

cells in regions between chips are either

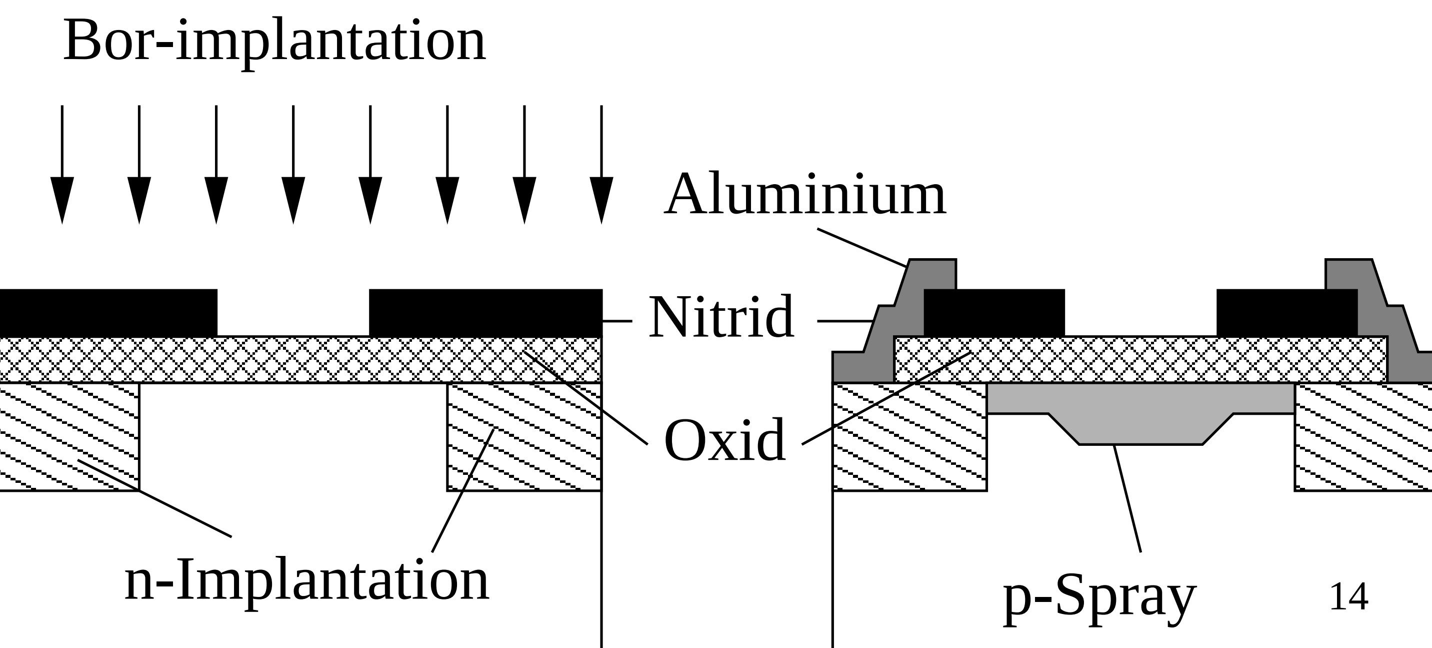
- elongated to 600 μm to reach the nearest chip, or
- ganged by single metal to a nearby pixel that has direct R/O

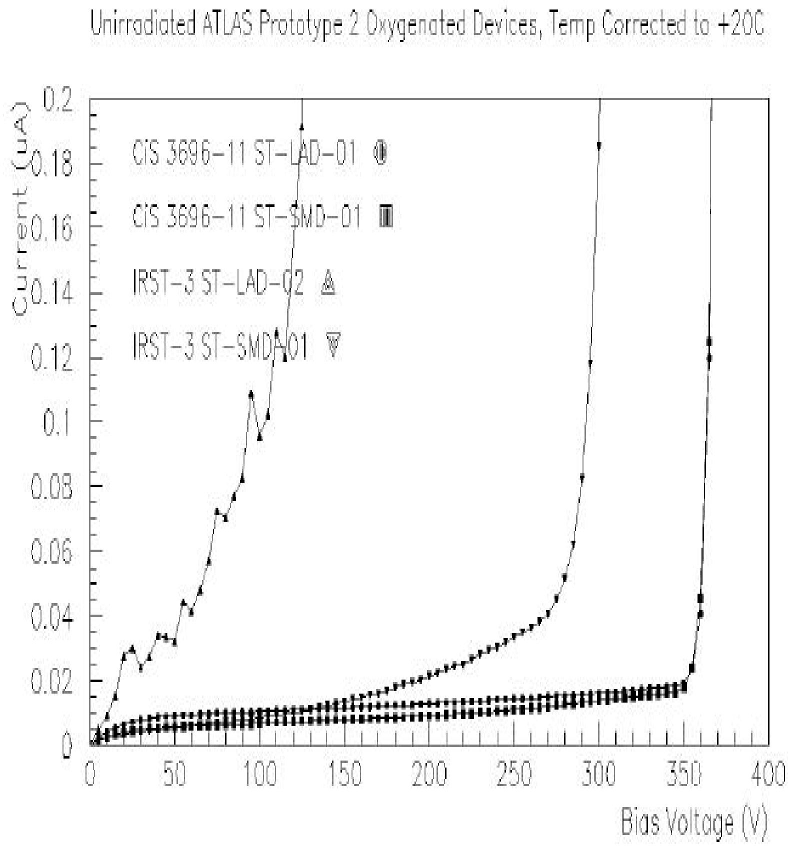
Elongation and Ganging of Implants in the Inter-chip Region



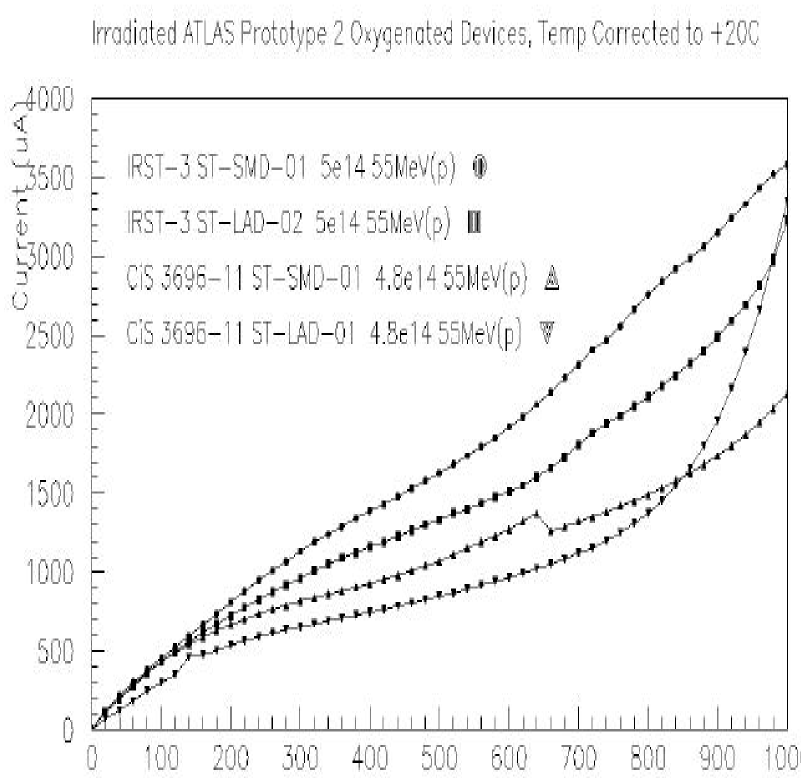
medium [(3.0 ± 0.5) x $10^{12}/cm^2$] dose
nplant applied to the full n-side without
asks, then overcompensated by the high
ose pixel implants themselves.

he p-spray is *moderated*: it attains a lower
oron dose near the lateral p-n junction,
hereby reducing the electric field. The
urface charge at the junction is optimized at
he saturation value (1.5×10^{12} /cm^2) and is
ightly higher in the center (3.0×10^{12}/cm^2)
or safe overcompensation. The higher dose
the center also reduces the capacitance.

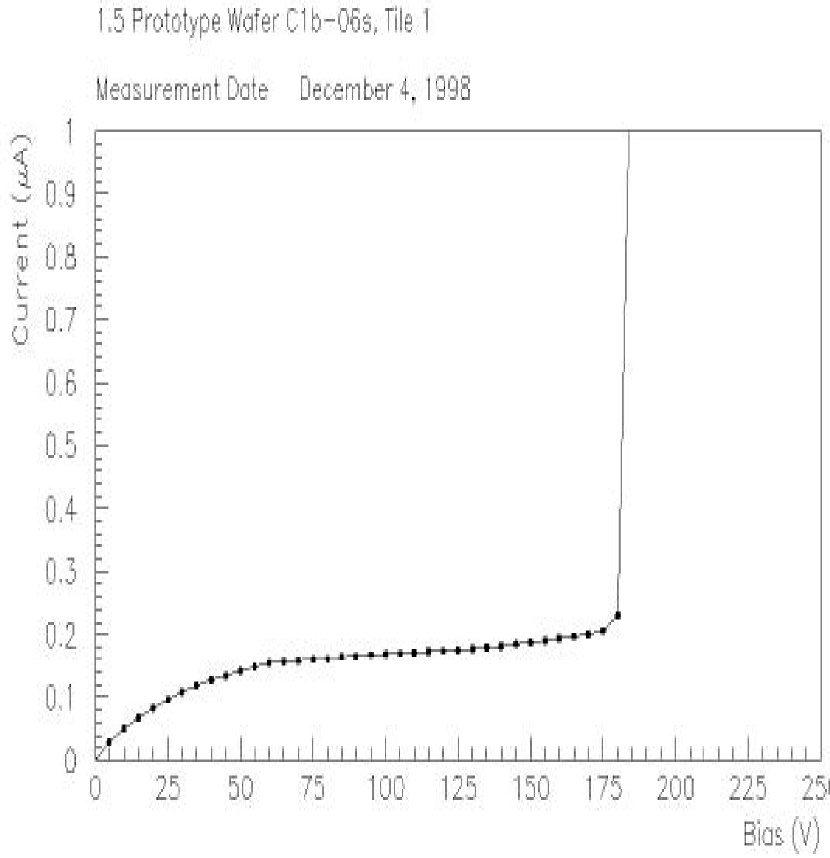




he same sensors irradiated to 9 $\times 10^{14}$ 1MeV n/cm^2:
reakdown voltage

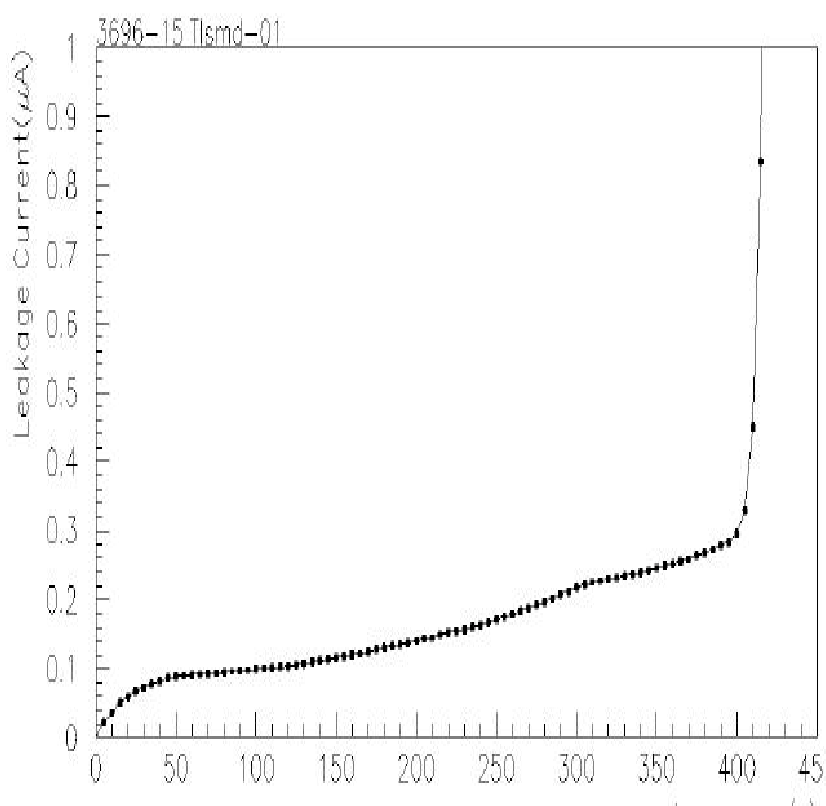


(Prototype 1): 180 V



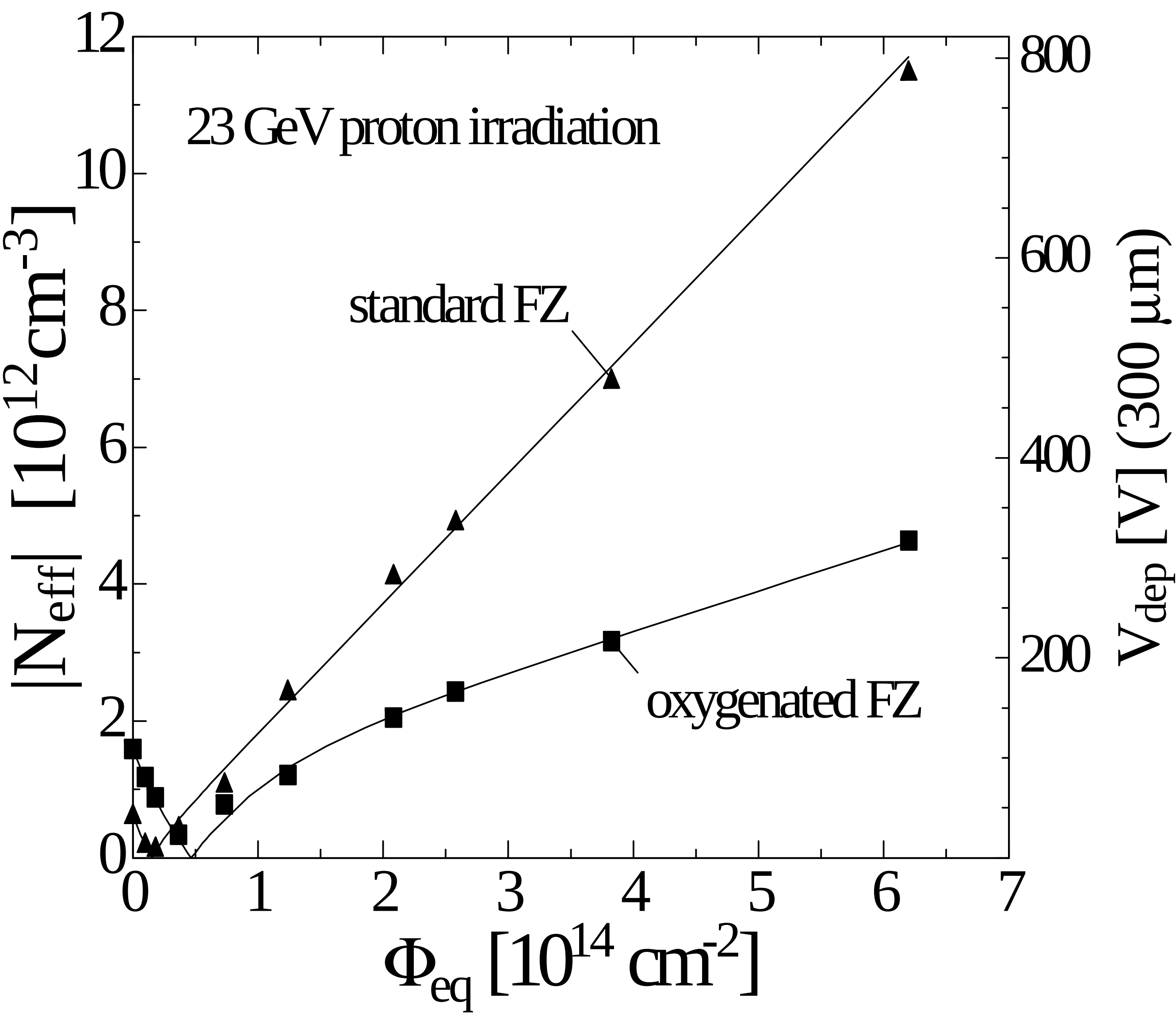
reakdown voltage for tile with moderated p-spray

Prototype 2): 410 V

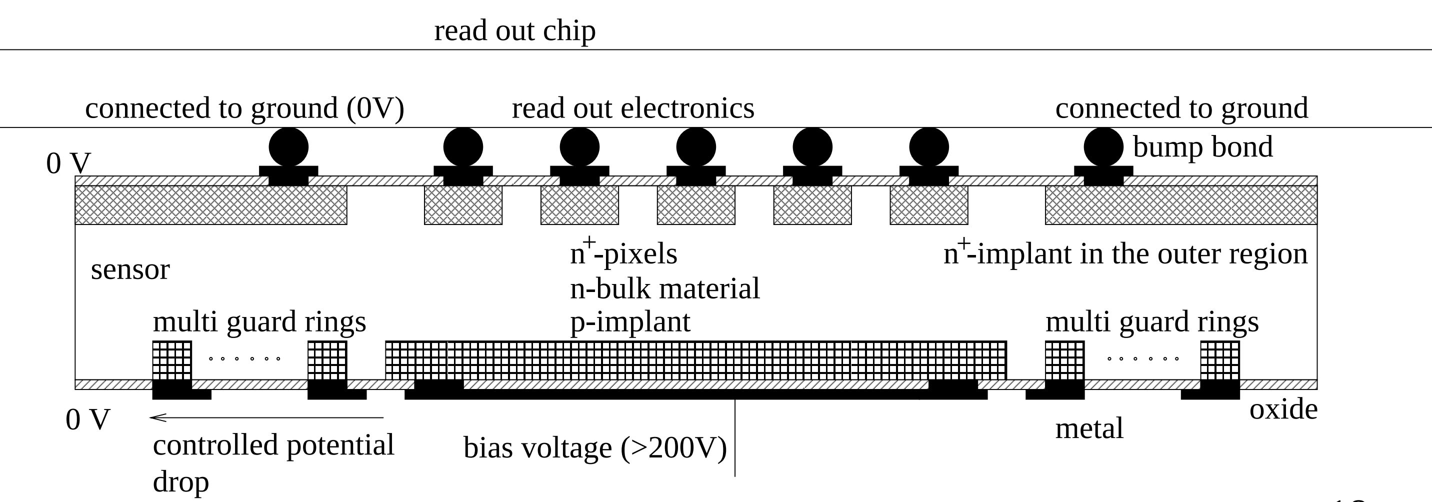


Substrate: oxygenated

rom the ROSE Collaboration: Oxygen-nriched (24 hours in 1150°C environment) licon is significantly more radiation hard han standard silicon as tested with protons or ions. V_{dep} is 2x lower after $10^{15}/cm^2$.



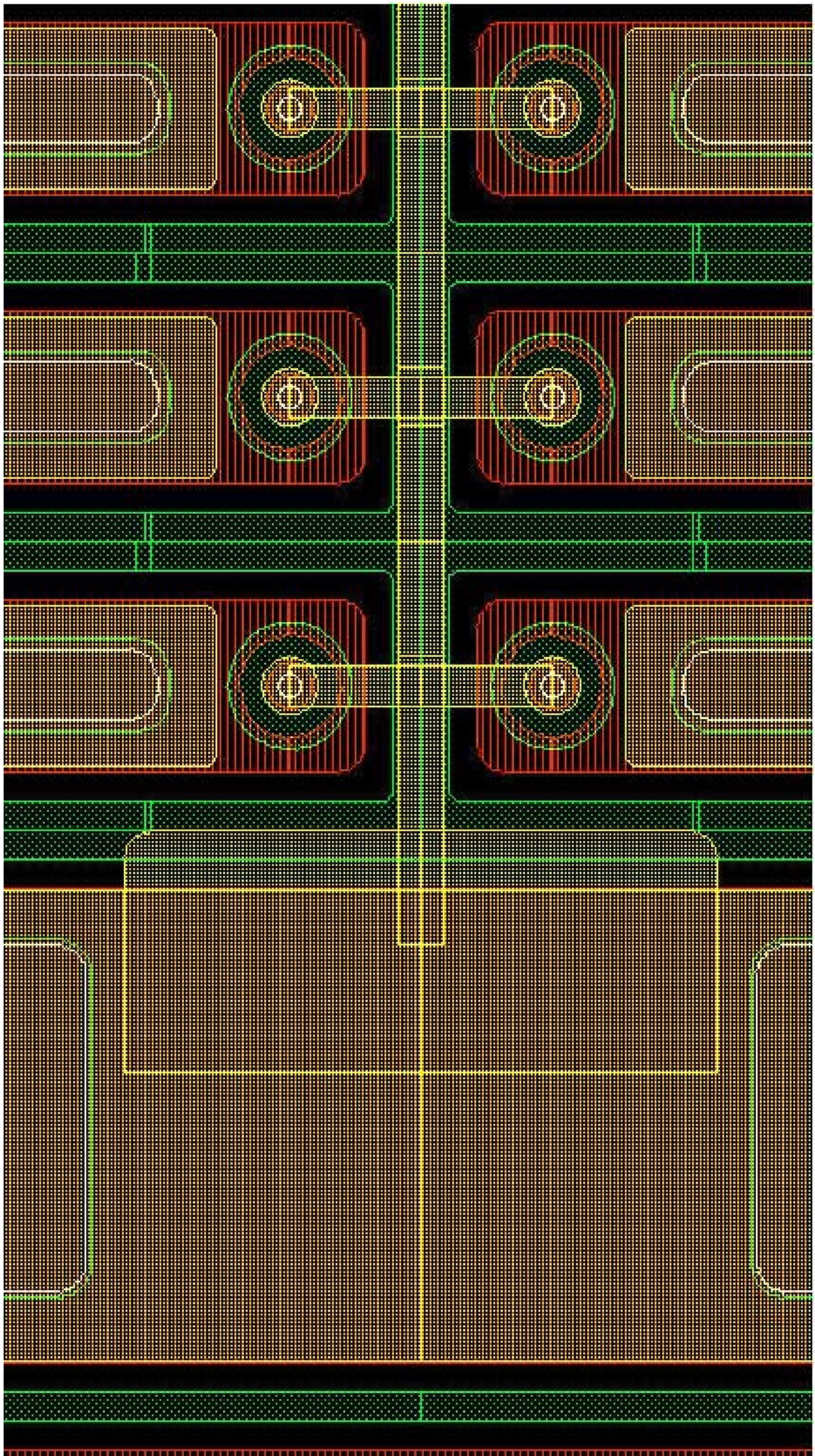
- on the p-side: a 17-ring structure of p^+ implants. Pitch increases with radius. Meta overlaps implant by 1/2 gap width on side facing active area. (See Bischoff, et al., NIM A 326 (1993) 27-37.)
- on the n-side: no conventional guard ring. Inner guard ring of ~90 μm width surrounded by a few micron gap. Region outside gap is implanted n^+ and grounded externally. Recal that the chip is only a bump's diameter away. This design guarantees no HV arc from n-sid to chip.



For high yield on assembled modules, we want to test sensors prior to attaching chips - so we want to bias every channel on a test stand without a chip and without contacting implants directly. A bias grid is implemented:

- Bus between every pair of columns connects to small n^+ implant “dot” near each pixel
- When bias is applied (through a probe needle) to the grid, every pixel is biased by punchthrough from its dot.
- p-spray eliminates need for photolithographic registration, permits distance between n-implants to be small $\rightarrow$ low punchthrough voltage
- Bias grid unused after chips are attached but maintains any unconnected pixels (i.e., bad bumps) near ground

Bias Grid



requirements

- thickness - 250 μm
- thickness non-uniformity, wafer to wafe - +10 μm, -30 μm
- thickness non-uniformity across each wafer - < 10 μm
- bow - ≤ 40 μm
- crystal orientation - <111>
- resistivity - 2-5 kΩ-cm
- resistivity uniformity, wafer to wafer - ±30 %
- substrate free of deep levels (C-V independent of frequency f for 20 Hz < f < 10 MHz)
- substrate oxygenated @ 1150 °C, 24 hrs

(measured at 20 °C)

- initial operating voltage - 150V or V_{dep} + 50V, whichever is higher
- initial leakage current @ V_{op} - < 2 μA per tile
- current slope at V_{op} - $I(V_{op})/I(V_{op} - 50V) < 2$
- initial oxide breakdown voltage - ≥ 50V
- ΔI ≤ 30% after 30 hours operation in dry air at V_{op}

- implant spacing ≥ 5 µm
- implant width ≥ 5 µm
- contact hole diameter in oxide or nitride ≥ 5 µm
- contact hole spacing in oxide or nitride ≥ 20 µm
- metal width ≥ 8 µm
- metal spacing ≥ 5 µm
- contact hole diameter in passivation ≥ 12 µm
- contact hole spacing in passivation ≥ 38 µm
- mask alignment tolerance within same side ±2µm
- mask alignment tolerance between front and back sides ±5 µm

Processing parameters:

- n^+ implantation dose > $10^{14}/cm^2$
- p-spray effective dose in Si - $(3.0 \pm 0.5) \times 10^{12}/cm^2$
- p-side contact dose > $10^{14}/cm^2$

Radiation hardness

To be tested on 2-4 test structures of 3 types, per batch, after 10^{15} p/cm^2 (CERN PS) and 50 kRad low energy electrons (Dortmund):

- $V_{op} \geq 600$ V
- I(600 V) < 100 µA @ -10 °C
- ΔI < 30% after 15 hours @ -10 °C

Pixel Sensor Testing

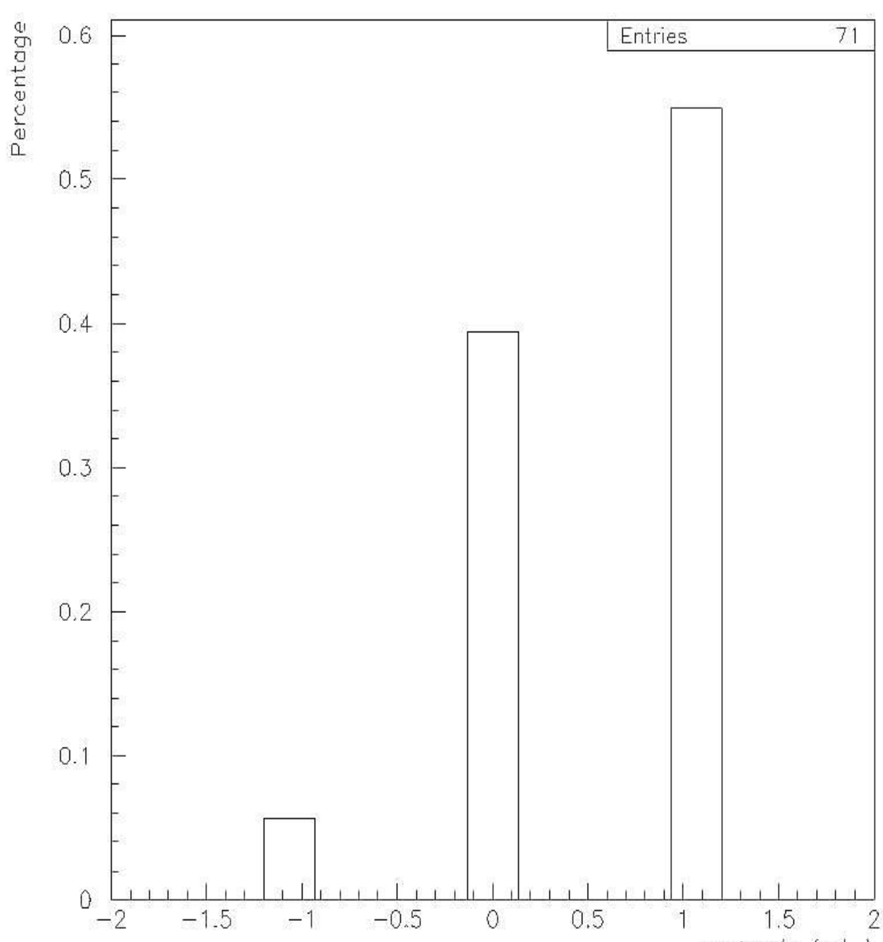
static studies of irradiated + unirradiated devices

test beam studies of sensors with amplifiers.

Examples...

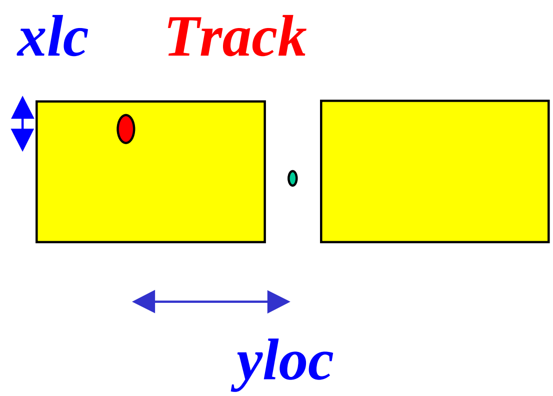
Static tests

- Quality assurance procedures applied to Prototype 2 assigned a flag $Q_{flag} \in (-1, 0, +1)$ to each tile on the basis of its breakdown voltage.
  - $Q_{flag} = -1$ for $50V < V_{breakdown}$
  - $Q_{flag} = 0$ for $50V < V_{breakdown} < 150V$
  - $Q_{flag} = +1$ for $V_{breakdown} > 150V$
- Typical results for CiS (predict production yield):



Beam test study of charge collection uniformity

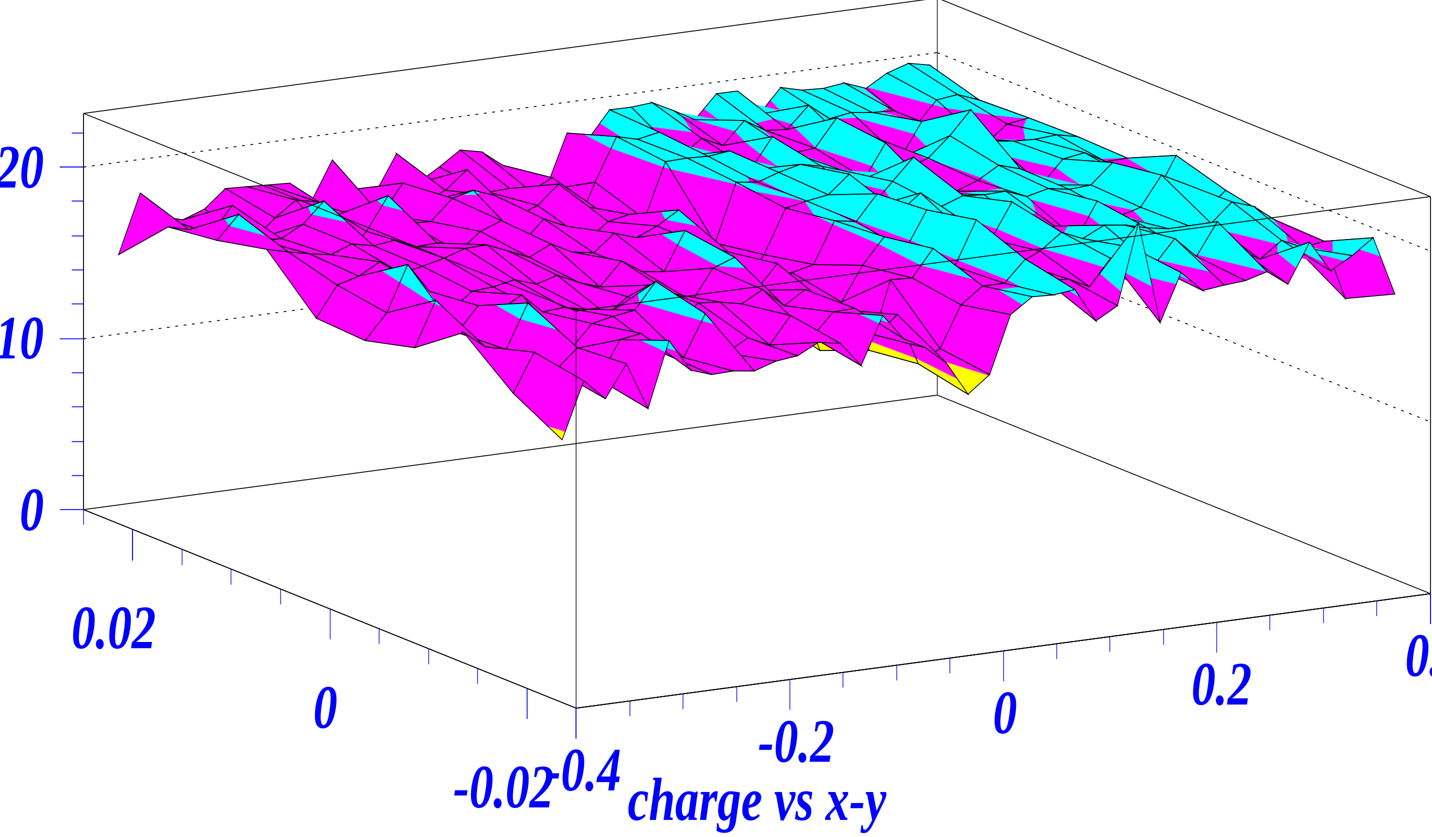
For an oxygenated Prototype 2 wafer @ $V_{bias} = 400$ V, $\Phi = 5.6 \times 10^{14}\ n_{eq}/cm^2$:

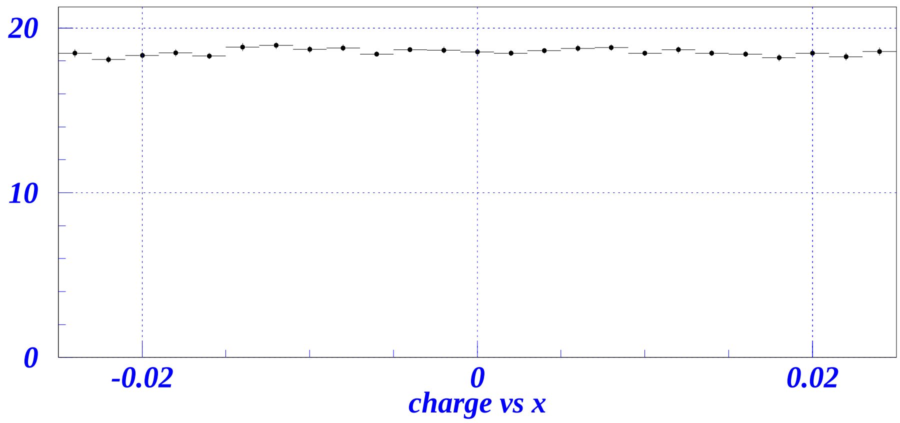


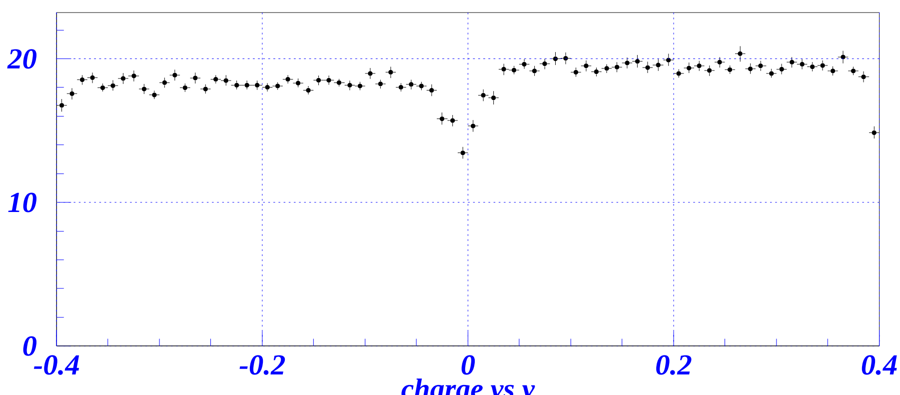
track position extrapolated to the pixel detector using strip detector telescope

average cluster charge computed for each position bin

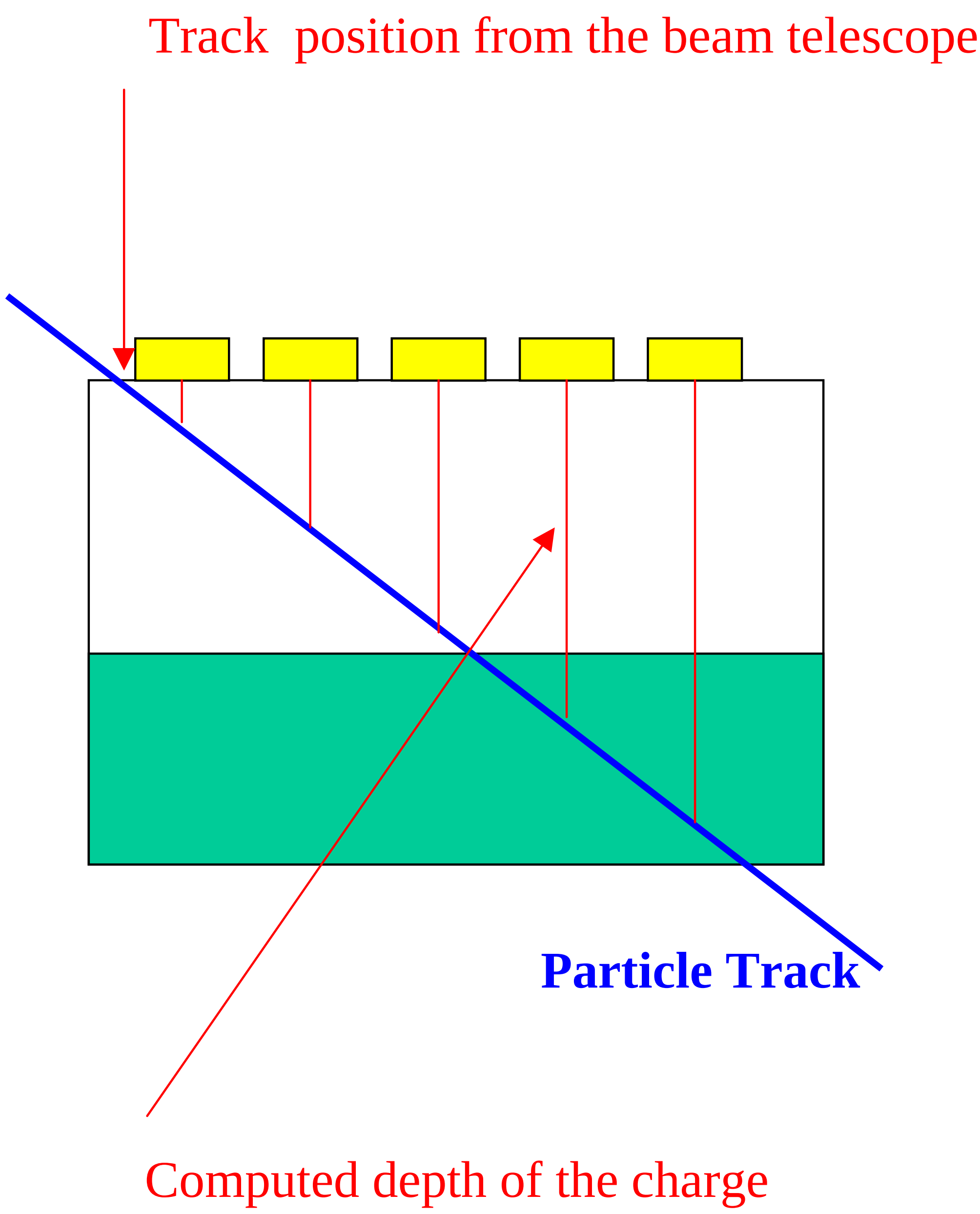
~18000e^- signal:

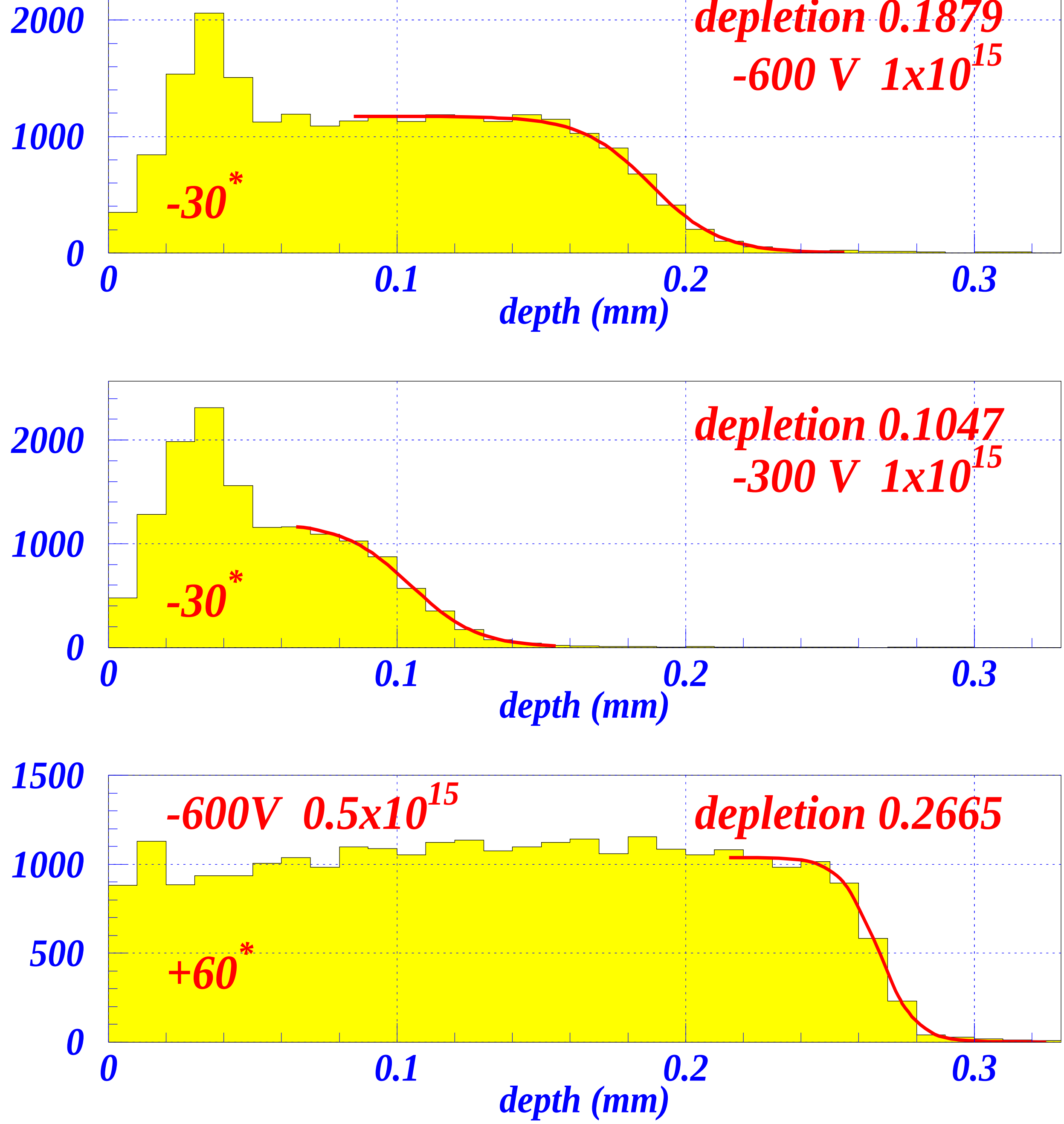

20
10
0
0.02
0
-0.02
-0.4
-0.2
0
0.2
charge vs x-y


20
10
0
-0.02
0
0.02
charge vs x


20
10
0
-0.4
-0.2
0
0.2
0.4

Beam test study of depletion depth



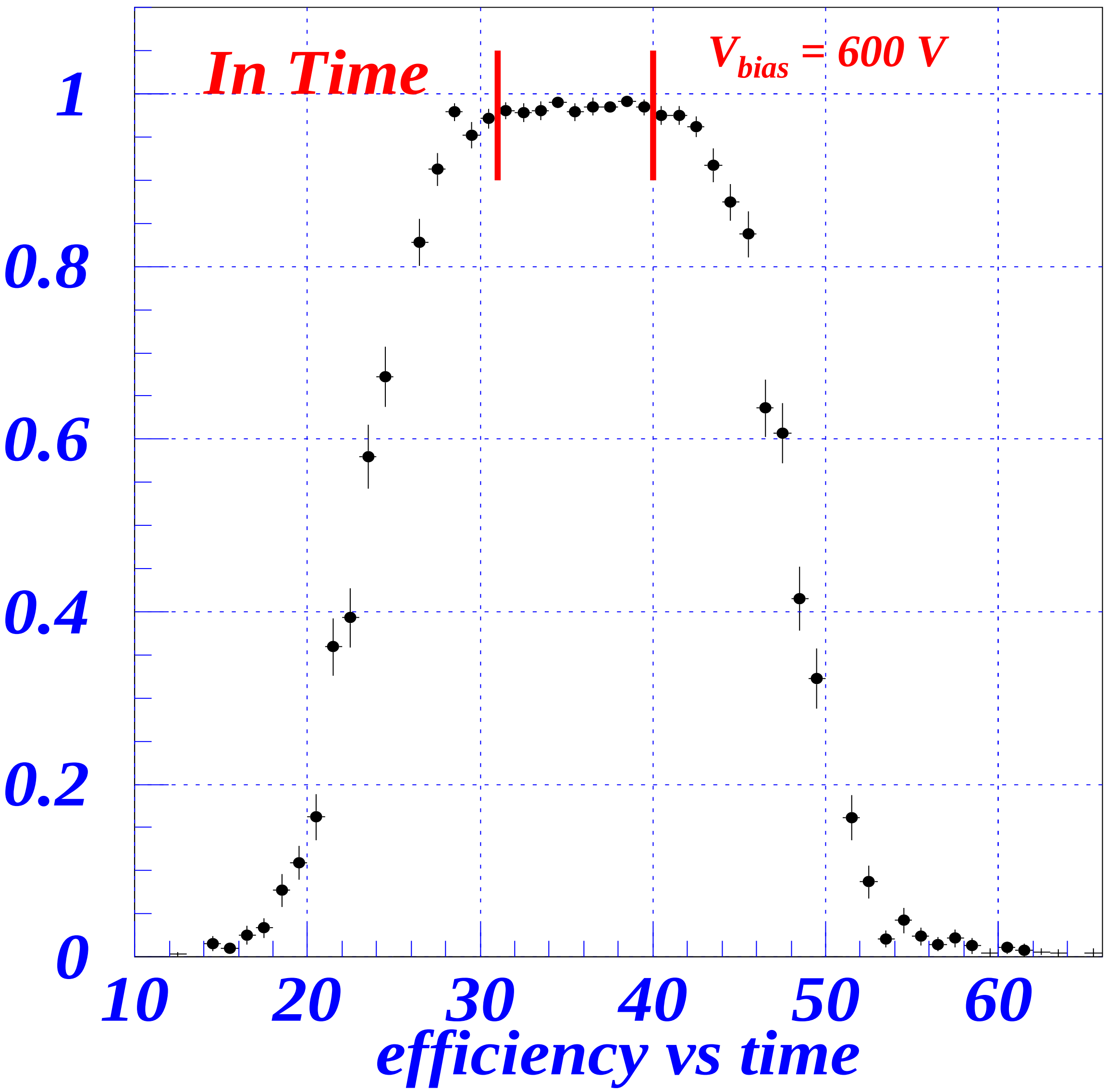


fter 10^{15} n_{eq}/cm^2, V_{dep} = 190 μm @ -600 V
for non-oxygenated substrate

Preliminary:) 250 μm thick oxygenated
sensor fully depleted @ -400 V after 5.6

Beam test efficiency study

8.4% efficiency after $\Phi = 10^{15}\ n_{eq}/cm^2$, for 000e$^-$ threshold:



Beam Test Study of Spatial Resolution

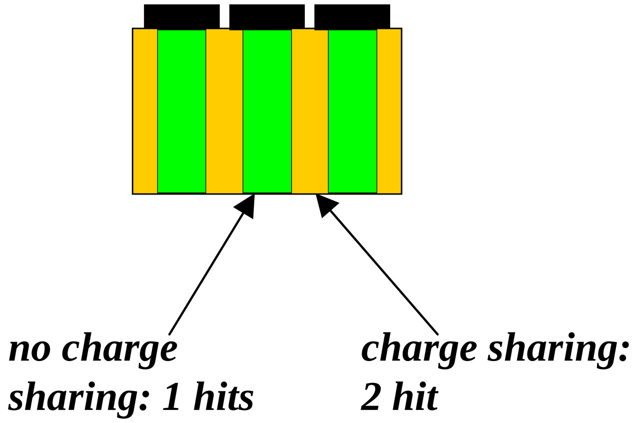
Resolution at 0^o for 3000 e^- threshold:

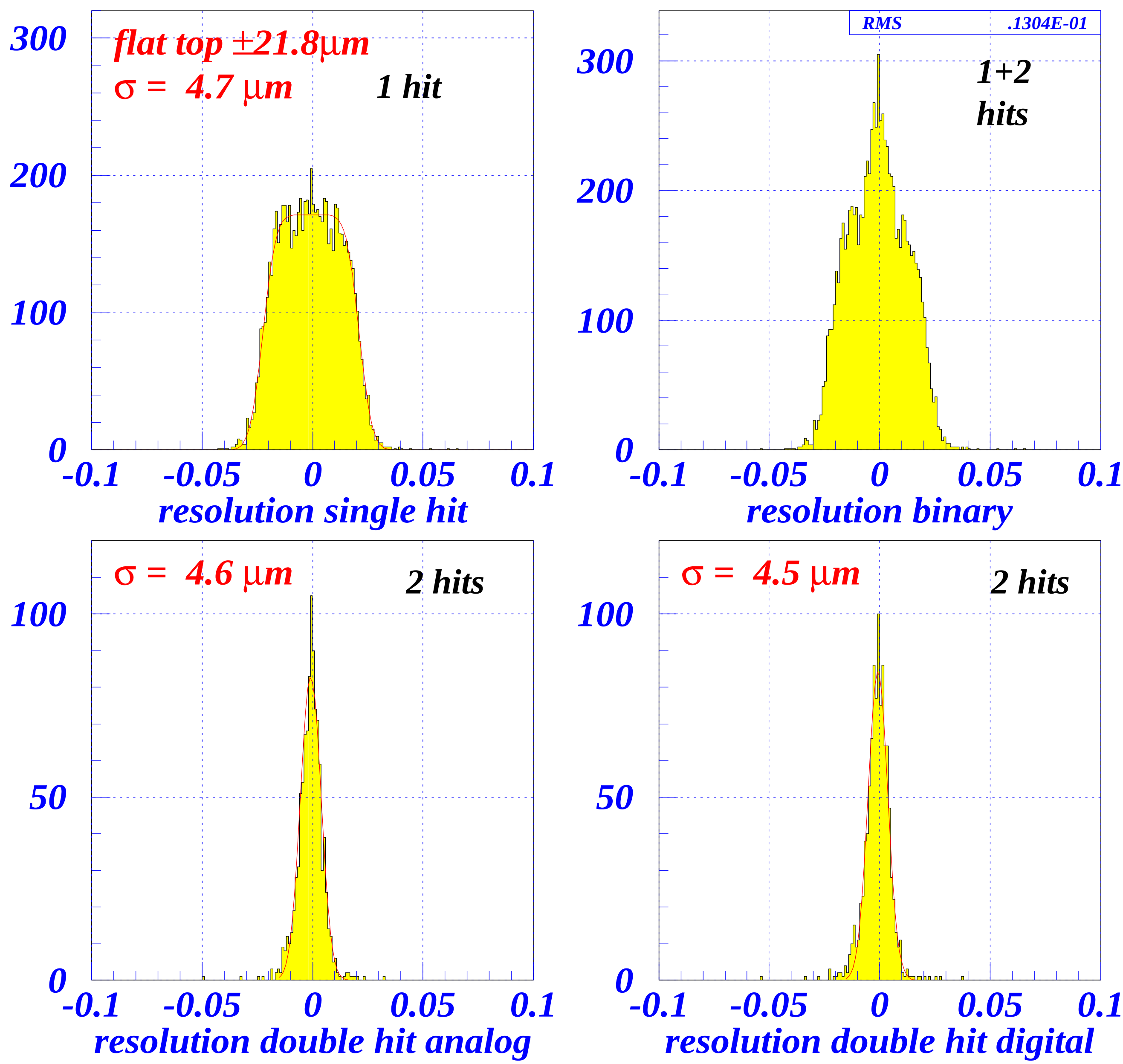
- depends on ratio (2 hits):(single hits)
- sharing within ± 3 μm
- ~ 15 % double hits

Larger charge sharing region for larger angles

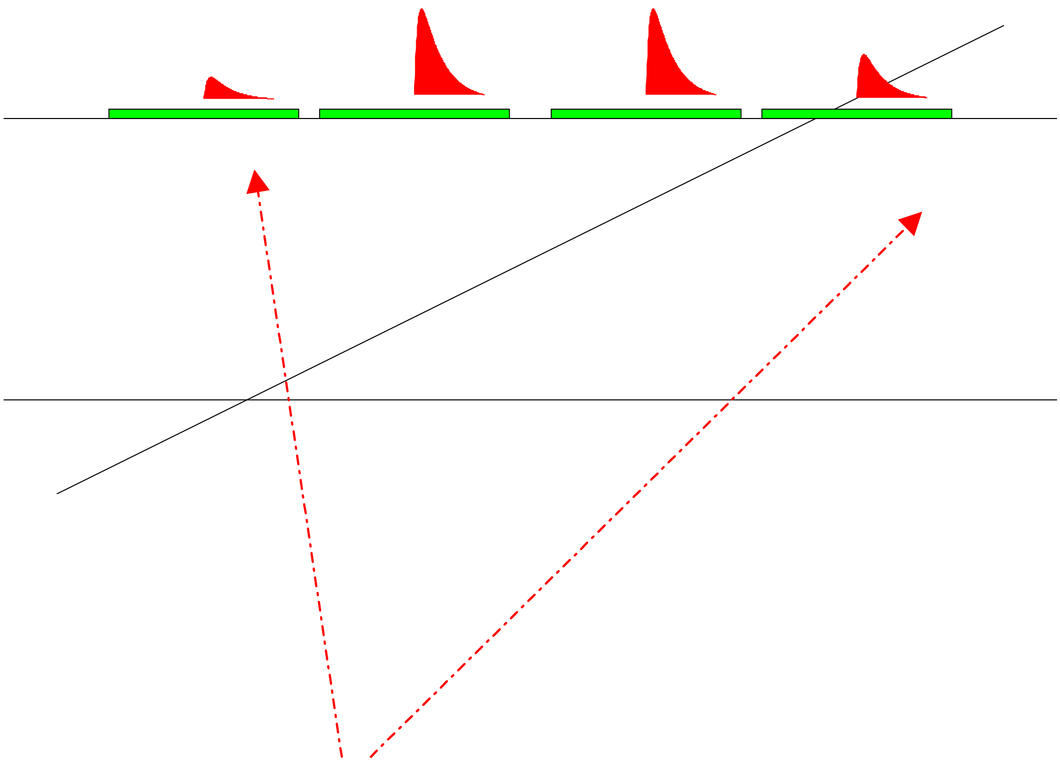
Depleted region reduction due to rad damage affects the multiple hits rate

Magnetic field modifies charge sharing through Lorentz angle

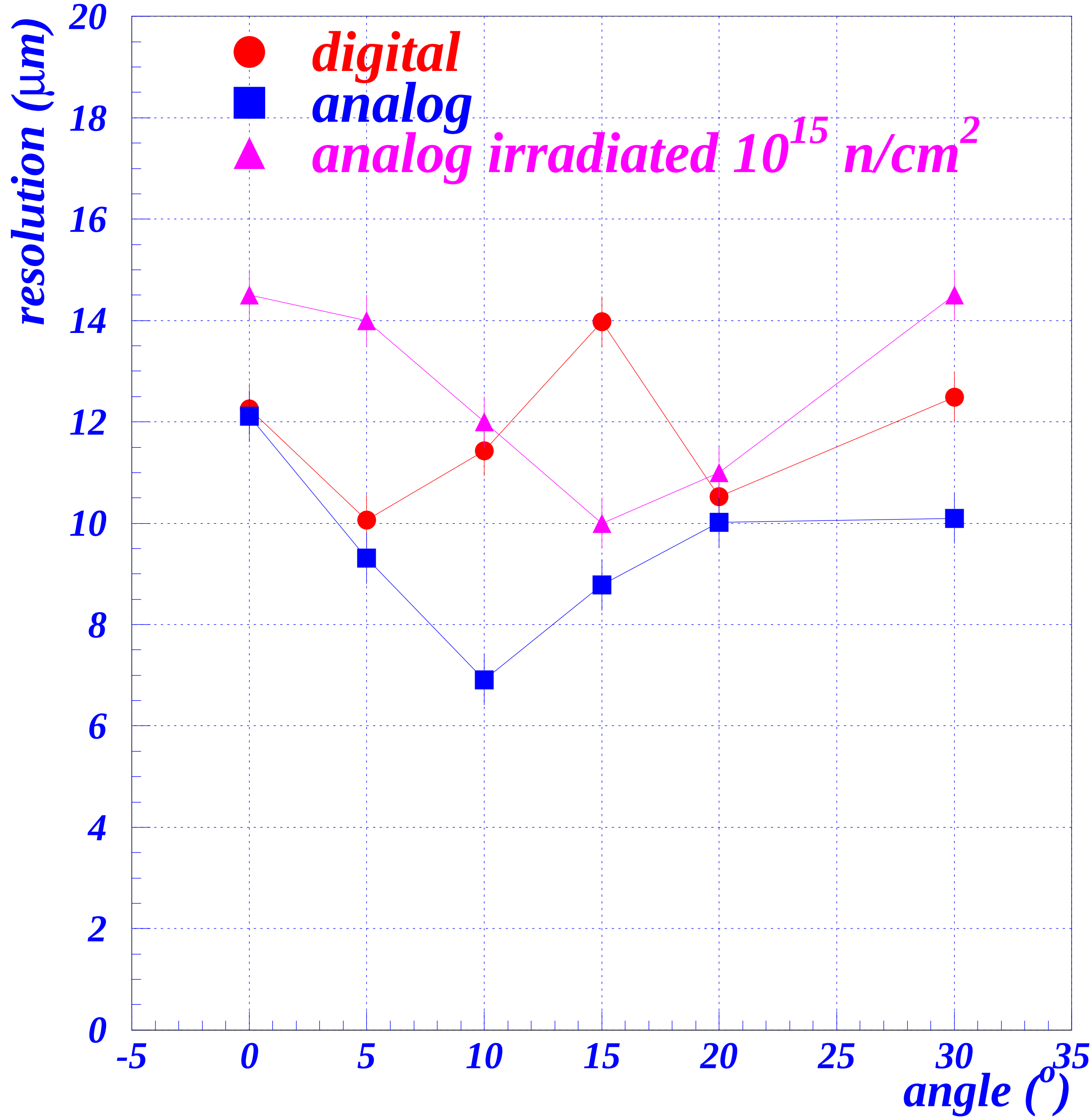

no charge
sharing: 1 hits
charge sharing:
2 hit


flat top ±21.8μm
σ = 4.7 μm
1 hit
300
200
100
0
-0.1
-0.05
0
0.05
0.1
resolution single hit
RMS .1304E-01
1+2
hits
resolution binary
σ = 4.6 μm
2 hits
50
resolution double hit analog
σ = 4.5 μm
2 hits
resolution double hit digital

Beam test study of resolution as a function of azimuthal angle



Charge interpolation on the external pixels in the cluster improves spatial precision



Analog (Time over Threshold) measurement of the charge improves resolution.

Anticipated Production Sensor Testing Program

On all wafers:

- visual inspection by microscope, before and after all other measurements
- I-V of every tile, every single chip, and diode with guard ring (for V_{break})
- C-V on diode with guard ring (for V_{dep})

Once per batch:

- bow
- versus time
- thickness

On a representative sample of control structures, a few per batch:

$V_{flat\text{-}band}$, oxide charge, p-spray dose, electron
obility, V_{break} of oxide and nitride layers,
ter-pixel resistance, inter-pixel capacitance,
nplant and metalization resistivities

On irradiated test structures:

V_{op}, I_{op}, ΔI vs. time, V_{break}, oxide properties,
at-band voltage, oxide charge, p-spray dose,
ectron mobility

Sensor Costs

U.S. ATLAS E.T.C.
WBS Profile Estimates

ng Source: **All**   **Funding Type:** Project   10/24/00 2:12:16

tions: All

S er	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Tota (k$)
	Sensors	0	0	0	0	0	97	167	39	0	0	30
2.1	**Design/Engineering**	0	0	0	0	0	35	35	0	0	0	7
1.2.1.1	**Test design**	0	0	0	0	0	35	35	0	0	0	7
.1.1.2.1.1.1	**Design - New Mexico**	0	0	0	0	0	35	35	0	0	0	7
2.3	**Production**	0	0	0	0	0	62	132	39	0	0	23
1.2.3.1	**Barrels, Disks and B-layer(s**	0	0	0	0	0	62	132	39	0	0	23
.1.1.2.3.1.1	**Preproduction**	0	0	0	0	0	16	0	0	0	0	1
.1.1.2.3.1.2	**Production**	0	0	0	0	0	0	93	0	0	0	9
.1.1.2.3.1.3	**Testing**	0	0	0	0	0	46	39	39	0	0	12

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Sensor schedule:

S	Task Name
.1.2	**Sensors**
.2.1	**Design**
	Test Design
	Compl. Spec for production order release
	Production release order effort
	ATLAS PM approval of production procurement
.2.3	**Production**
	Start preproduction fab
	Preproduction Fab/Test
	First preproduction wafers delivered
	Outer Sensors Production
	First Outer production wafers delivered
	Outer Sensors Testing
	Outer Sensors Testing Complete
	Outer Sensors Need to Begin Module Production
	B-Layer Production
	First B-layer wafers delivered
	B-layer sensor testing
	B-layer sensors needed to begin modules