Status of Pixel Detector

Leonardo Rossi - INFN Genova

Overview

- **Generalities**

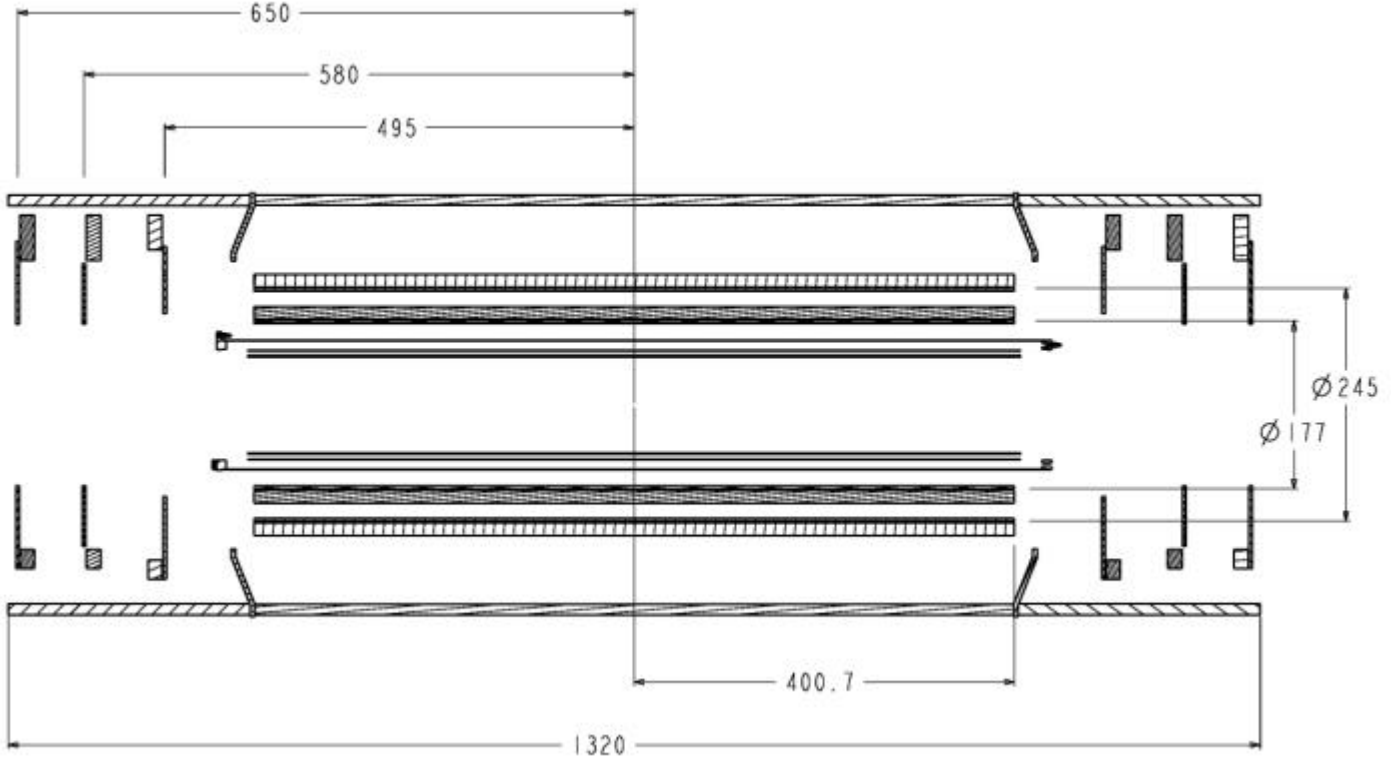
major recent achievements and problems:

- **sensors**
- **module hybridisation**
- **rad-hard front-end electronics**
- **schedule and layout update**
- **mechanics, cooling and integration**

Generalities

- **Pixel is the innermost ATLAS detector, is devoted to track and vertex reconstruction and primarily aims at heavy quark and lepton tagging.**
- **The detector is highly modular and use of same solutions all over the system is pursued (e.g. same modules, same local supports, same material for supports, etc.)**
- **The detector is designed for 3-hit coverage over -2.5<h<2.5, with 3 barrels and 3(+3) disks (transition at h~1.5). If less than 3 hits performance (B_tag) suffers @any *L*.**

- **The layout has been recently changed to cope with rad-hard electronics delay (see later).**



• **Pixel cells are 50x400 mm everywhere but in the B_layer (innermost cylinder, independently replaceable, dominates the impact parametr resolution) where the length is 300 mm.**

•**The pixel collaboration is made of 22 labs from 7 countries. The major players are France, Germany, Italy and US.**

• **Management is done through working groups (e.g. electronics, modules, sensors), the PDSG (1 per lab+experts) and the RPDSG (Rossi, Wermes, Olcese, Delpierre, Einsweiler, Gilchriese, Wunstorf).**

• **Preparation for production happens through two kind of reviews:**

  • **FDR (Final Design Review), where the design is evaluated by external reviewers, with special attention to interfaces**

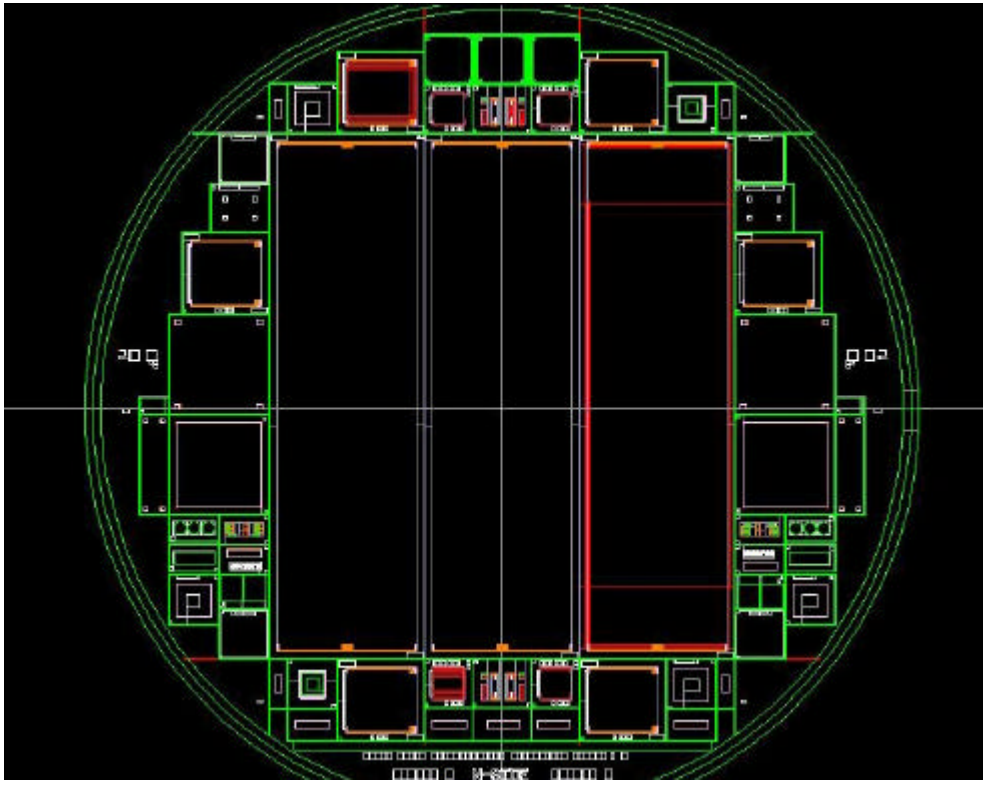
  • **PRR (Production Readiness Review), where the (same) reviewers go through the production issues too. After a successful PRR a call for tender can go out and then the (pre)production order can be issued.**

• **The FDR precedes the PRR by at least 3 months**

Recent achievements

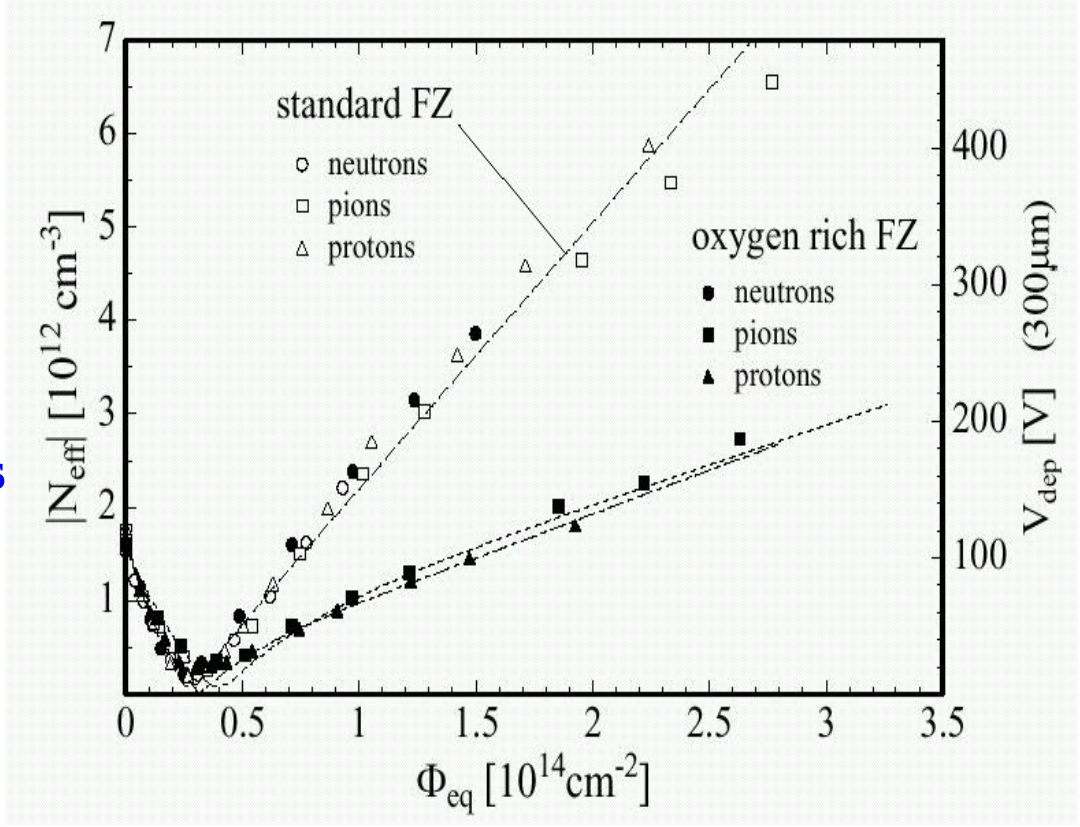
Sensors

- FDR (12/99) and PRR (2/00) have been passed
- Call for tender out (5/00). Formal steps took more time than expected (1st experience for pixel groups).
- Order in July for 30+30 4” wafers, each wafer 3 tiles (+test structures) >50% of wafers with 3 tiles working, rest with 2 tiles. Delivery 1/01, approval by 3/01, then order for production.



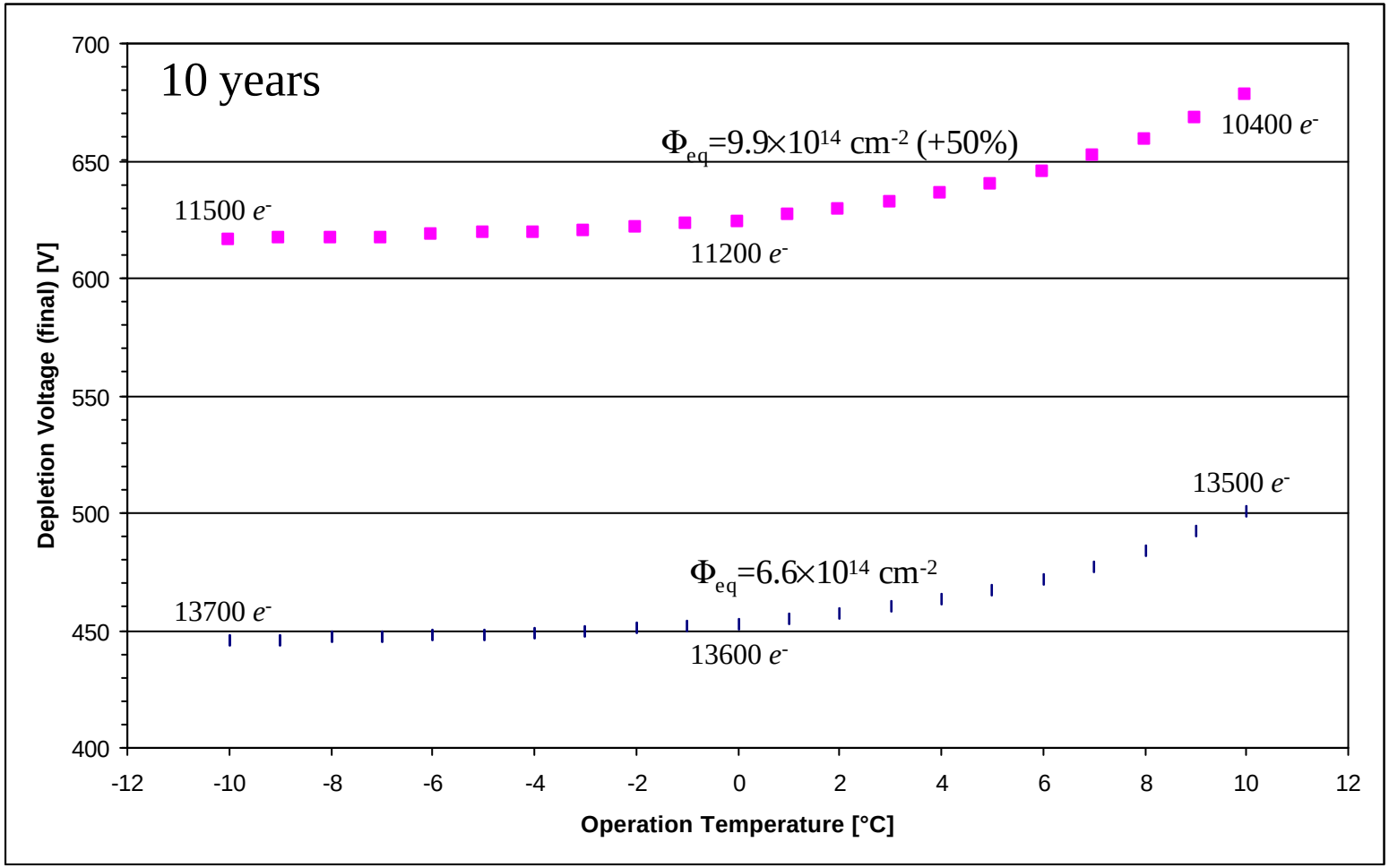
Oxygenated sensors: calculations and measurements

- **Use of oxygenated wafers to produce sensors may give considerable advantage (see RD48, ROSE Collaboration).**
- **Main advantage of those sensors is the smaller slope of the reverse annealing curve (responsible for the increase of V_{bias} at high dose) and the saturation of reverse annealing. Also important is the reduction of stable damage.**
- **They can therefore survive higher doses (of charged particles) or run at higher T or/and survive longer warm-up times.**
- **The advantage is larger for innermost layers (as the positive effects have been only measured for charged particles, not for neutrons).**



Damage Projection - Atlas Pixel Detector - 1st Layer

- Radiation level for 1st layer: Φ_{eq}(10 years) = 6.6×10^{14} cm^{-2} resp. 9.9×10^{14} cm^{-2} (+50%)
- Scenario: 100 days beam at *T*, 30 days at 20°C, 235 days at -10°C per year
- Sensor thickness 250µm, oxygenated silicon, $V_{bias}=V_{depl}$+50 V, max. 600 V



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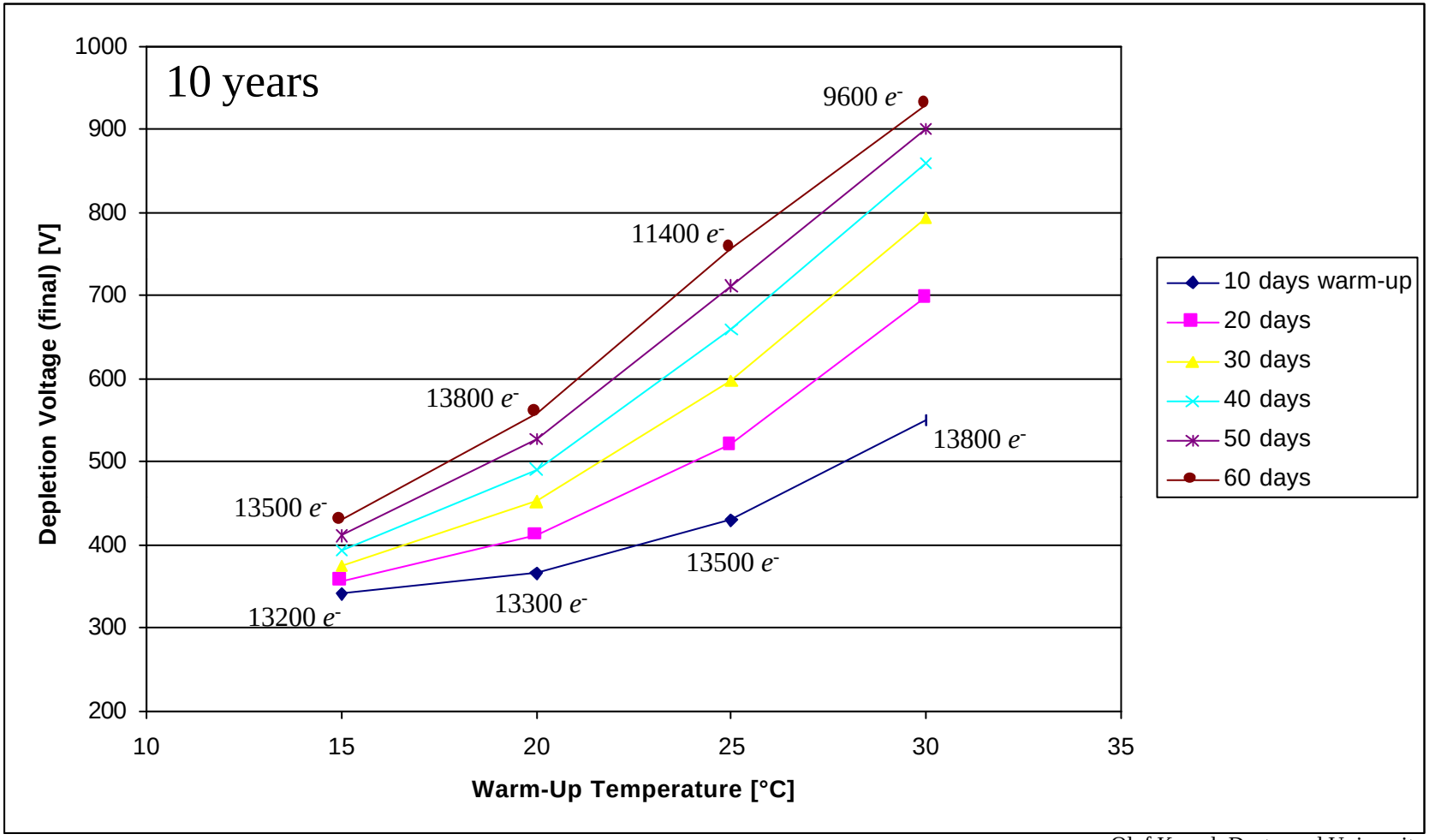
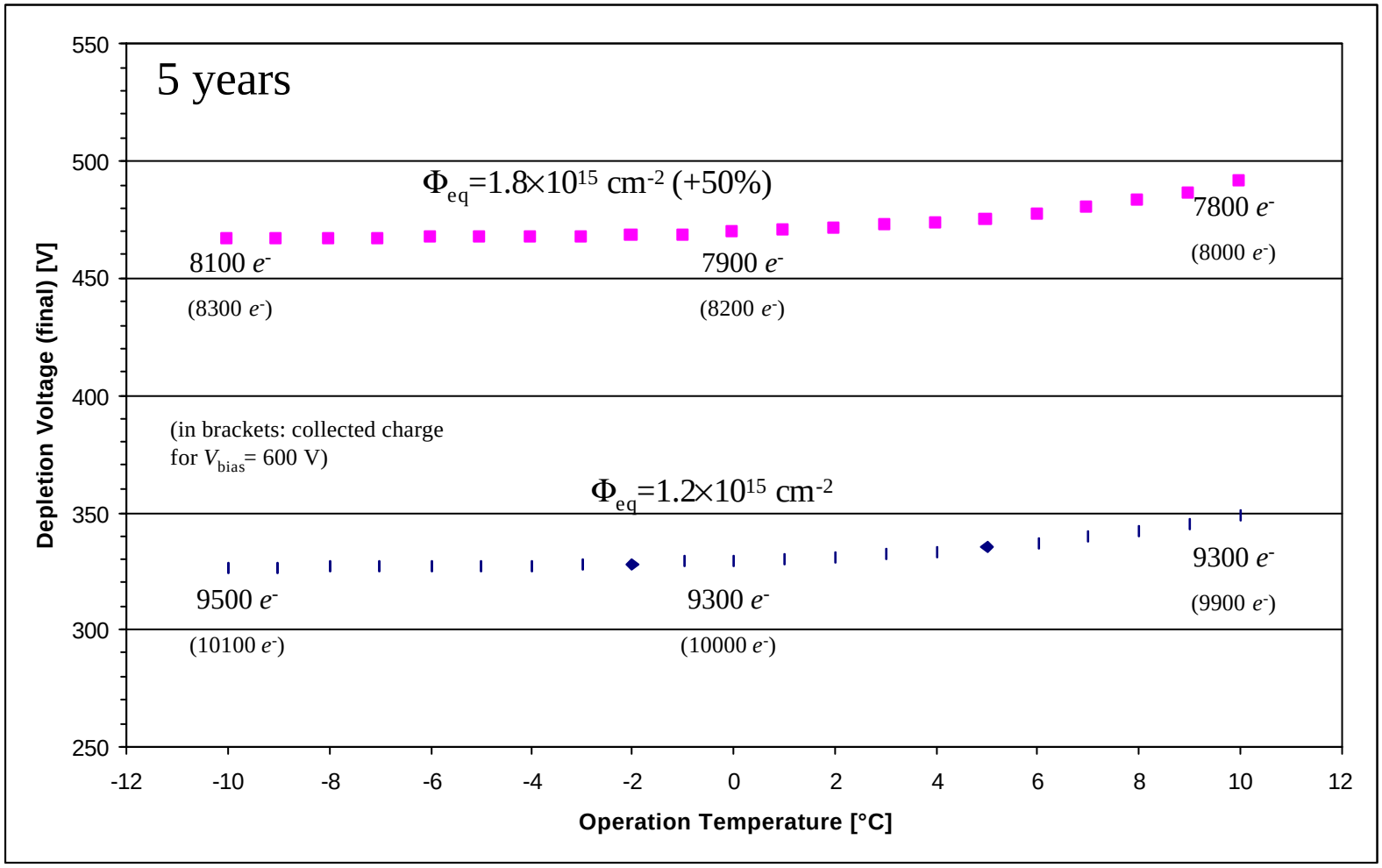


Damage Projection - Atlas Pixel Detector - B-Layer

- Radiation level for B-layer: Φ_{eq}(5 years) = 1.2×10^{15} cm^{-2} resp. 1.8×10^{15} cm^{-2} (+50%)
- Scenario: 100 days beam at *T*, 30 days at 20°C, 235 days at -10°C per year
- Sensor thickness 200µm, oxygenated silicon, $V_{bias}=V_{depl}$+50 V, max. 600 V



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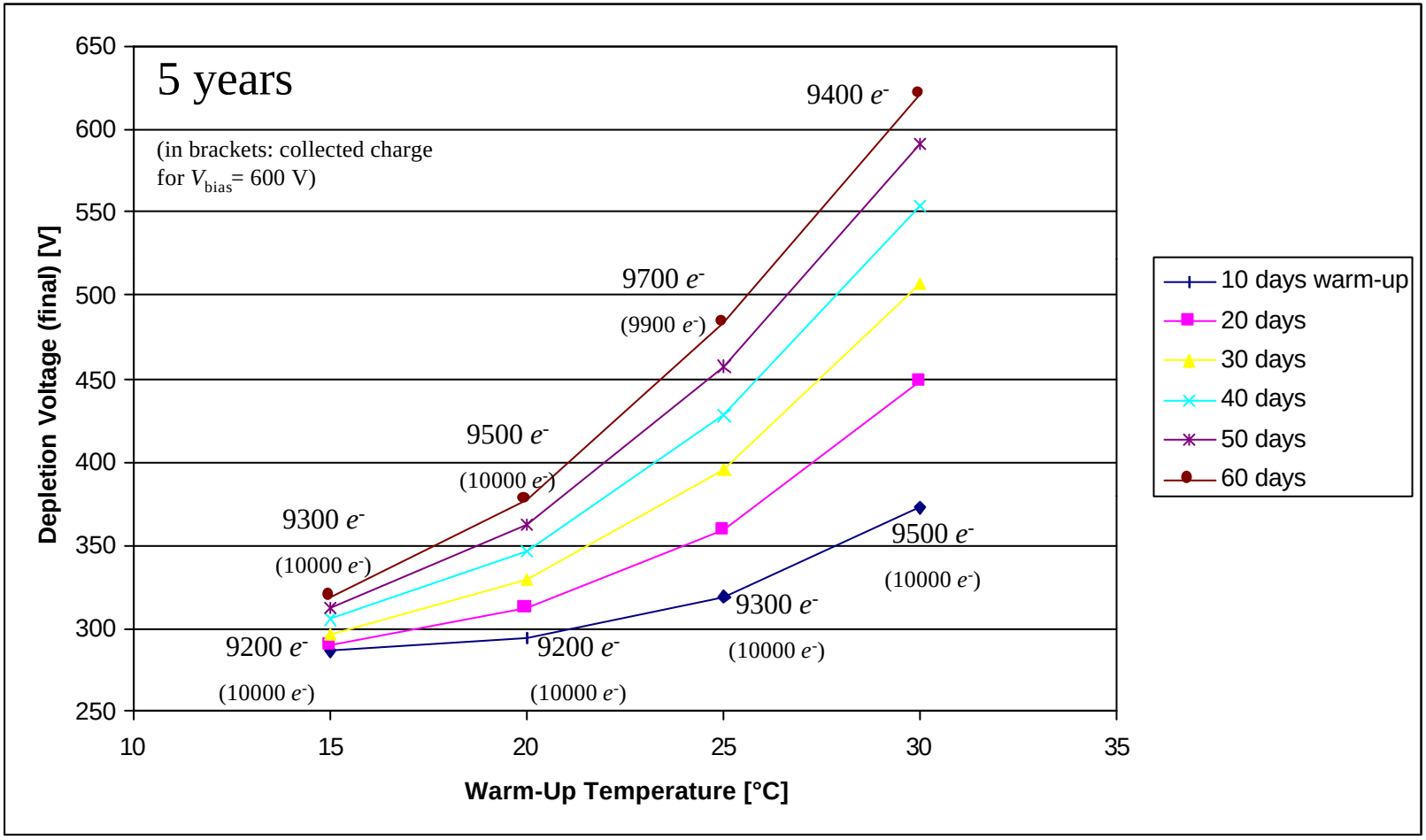
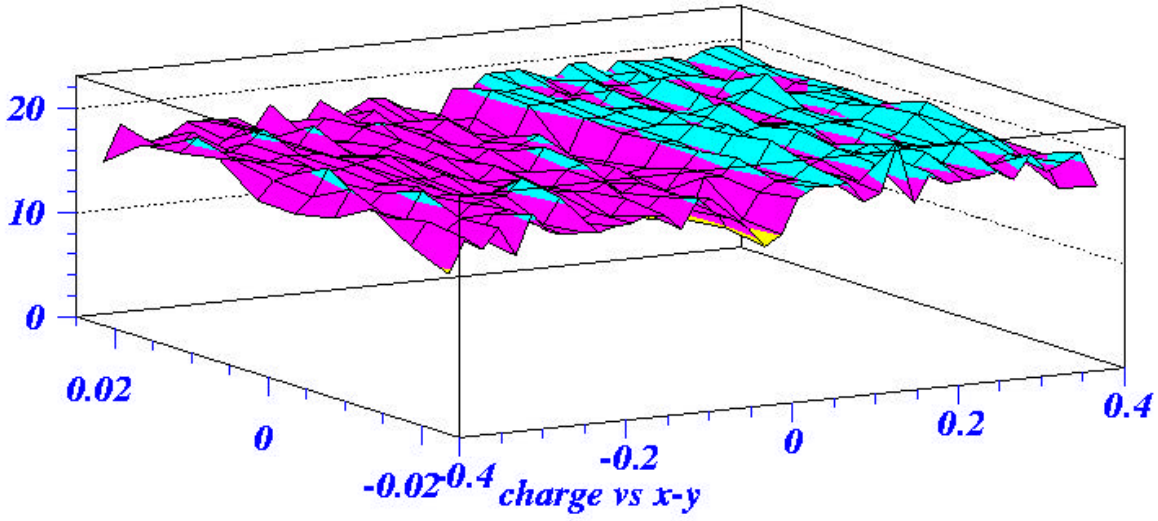
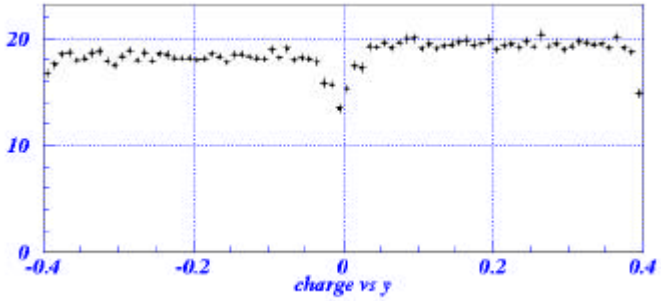
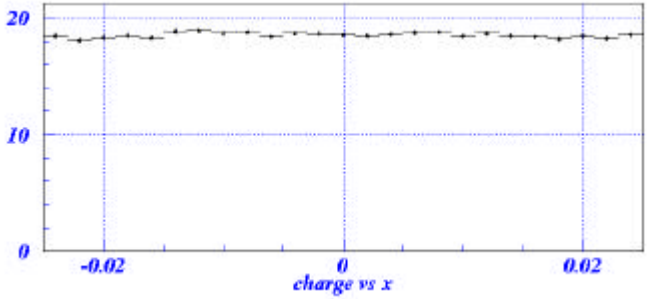


Irradiated oxygenated sensors: measurements

Oxygenated pixel sensors (ATLAS "production" design) have been irradiated at PS up to 10^{15} n/equiv. then tested at SPS H8 beam (those irradiated up to 5.6 10^{14} have been analysed).
Charge collection is good (no losses at pixel boundaries)





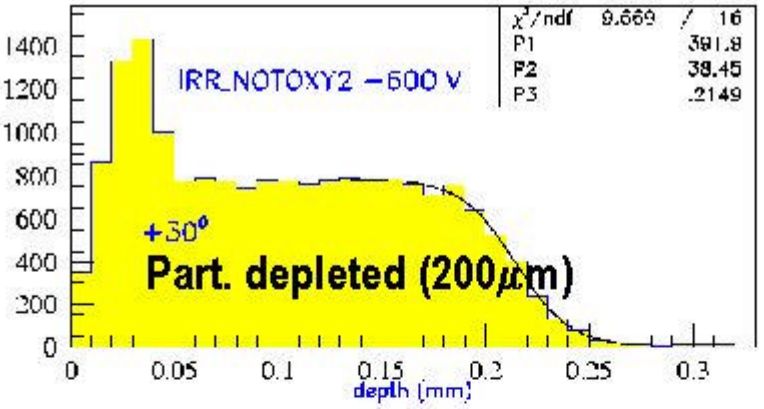


- As expected depletion voltage is lower than non-oxygenated.

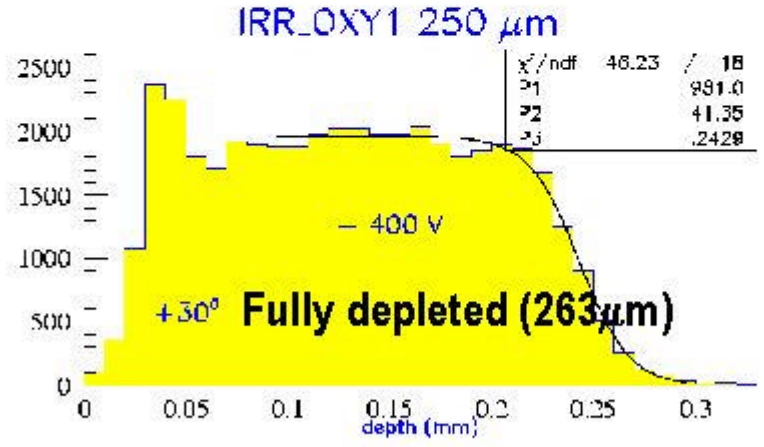
- Overall results are according to expectations, but more tests ongoing (more statistics, full fluence, **p** (not p) irradiation).

- Oxygenated sensors provide safety factor (in fluence) and simplify the access (less problems in warm-up) and the thermal barrier design.

- New spec for Si temperature (<0C) simplifies construction (hot spots).



Not-Oxy

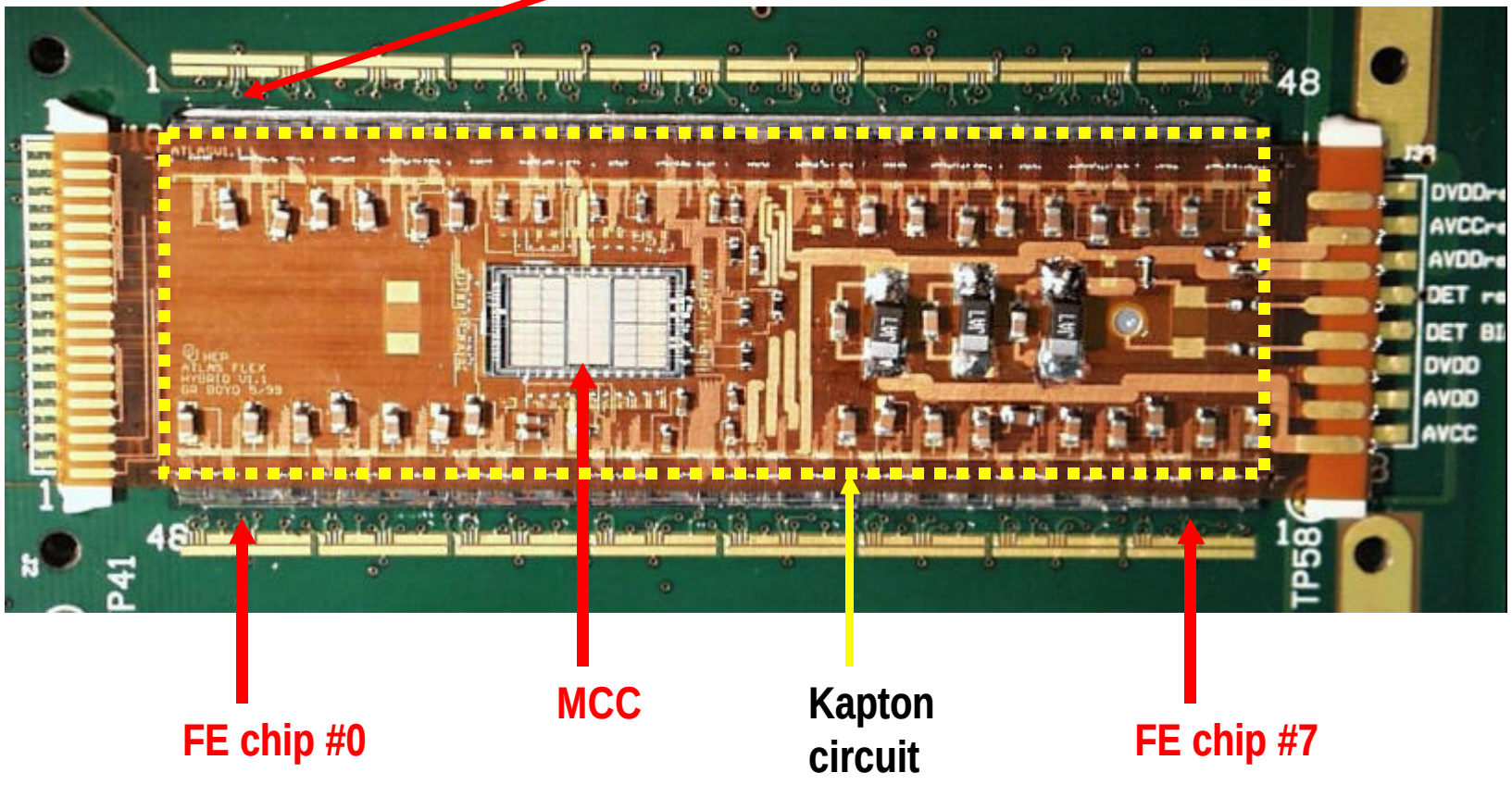


Oxy

Comparison of oxygenated and non-oxygenated after 5.6 10^{14} n/equiv.

Module hybridisation

Module = 1 silicon tile + 16 FE chips + fan-out bussing + control chip (MCC) + data transmission (not shown)



~2 x ~6 cm^2

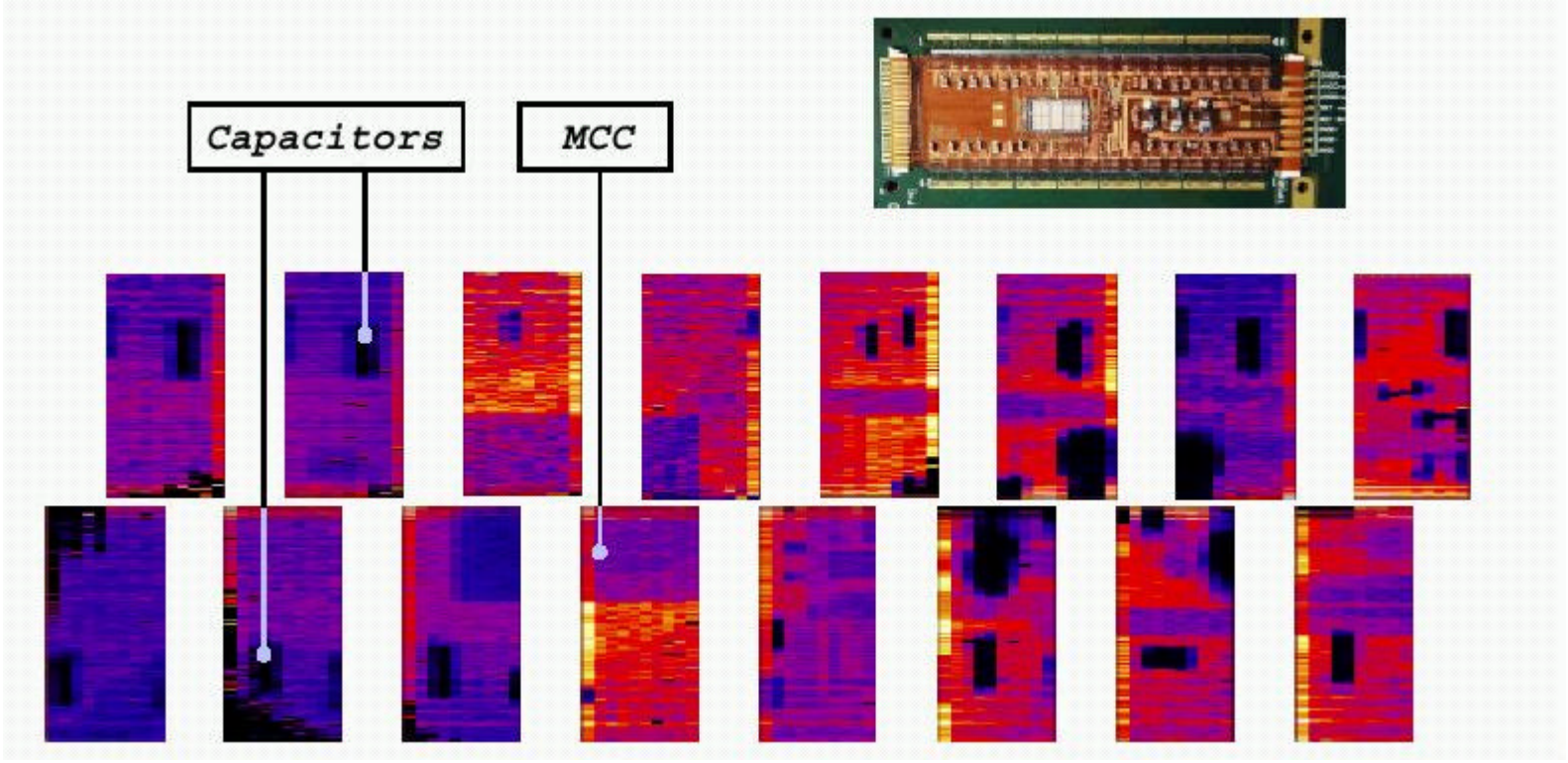
~0.8 W/cm^2

~1 kCHF/cm^2

Chips-to-sensor= bump bonding; chips-to-kapton= wedge bonding, kapton glued to sensor

• 3 modules with thickness 0.7% X0 (i.e. the TDR value, i.e. with 150 mm thick electronics) have been built and operated in lab and beam. They work just fine (thr=3700 e-, D(thr) ~300 e-, noise~200e- over the entire module).

Cd^{109} source run of thin module: shows all 16 FE working and "radiography" of components



• **Bumping/thinning/flipping is established up to 6” wafers. Flex fabrication is ok, but we need more suppliers.**

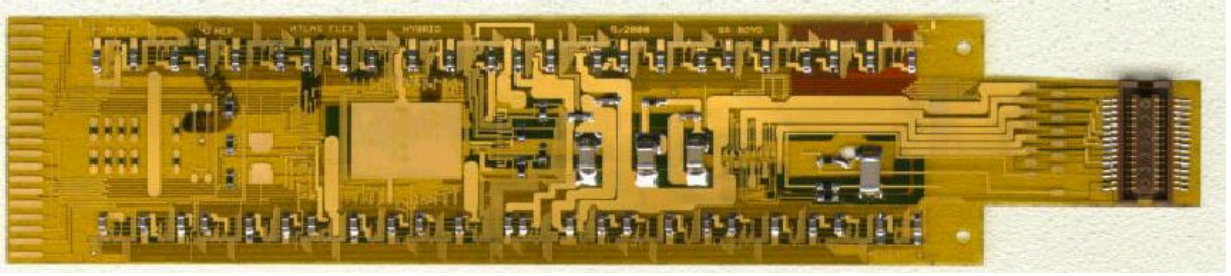
•**Work is also going on to qualify the glue interface between the module and the support structure (thermal and mechanical interface). We have a baseline choice, but we want to optimise the parameters and define a well controlled process for this crucial operation (we need a large number of dummy modules for this study)**

• **We passed (Aug.24) the bare module FDR. Main recommendations were:**

- **produce ~50 modules/supplier (check yield and problems in “production mode”)**
- **consider extension to 8” wafers**
- **continue the study of reworking**
- **define the test policy (KGD) and its cost/benefices**

• **Flex FDR is scheduled on Dec 11.**

Flex2.x



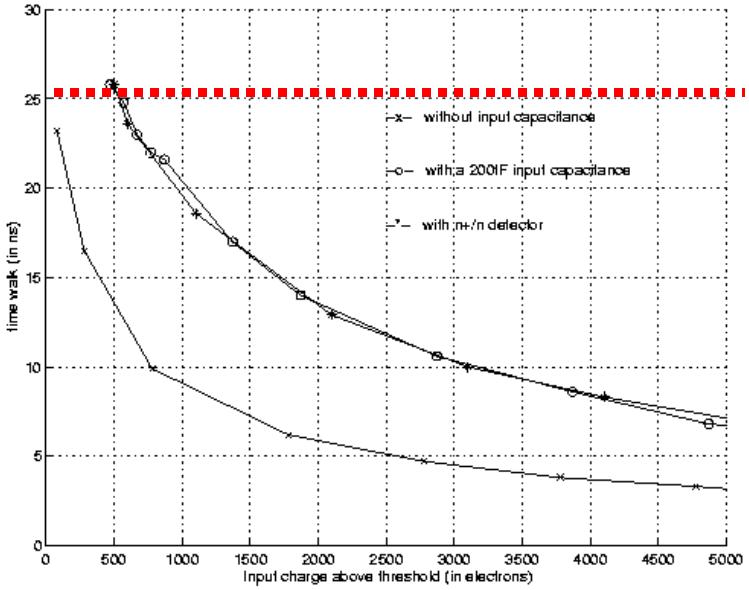
The Front-End electronics

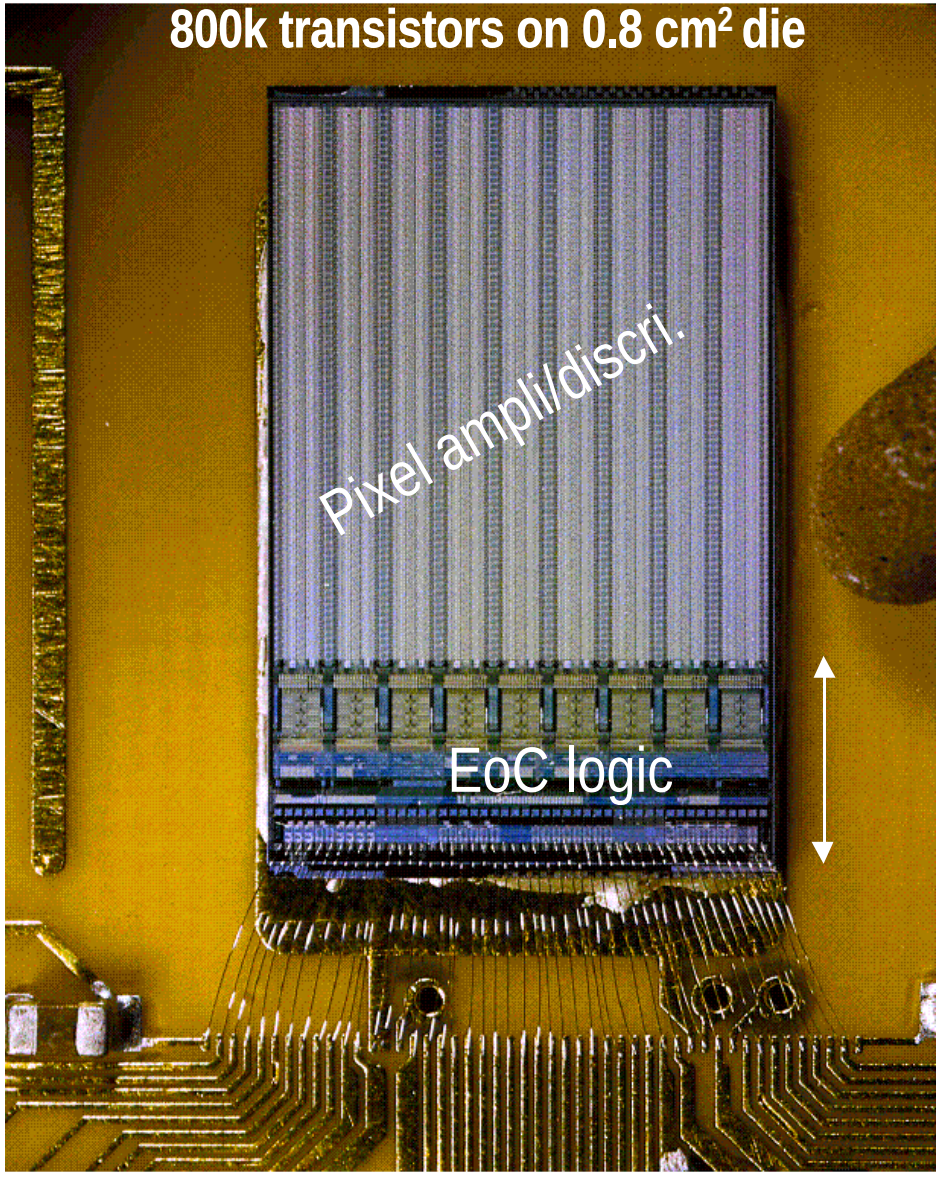
Rad soft electronics was built, bump bonded on sensor and operated on beam (1998-1999).

LHC specs have been met.

Routine operation at 3000 e^- threshold with both s_{noise} and $s_{thr} \sim 150e^-$.

Small timewalk: need ~600e^- above threshold to have signal inside 25ns.





•Rad-soft to rad-hard transition (started in early 1999) considerably more difficult than expected (even if not-final front-end chips (e.g. MAREBO) of comparable complexity and size were already realised in DMILL by our designers).

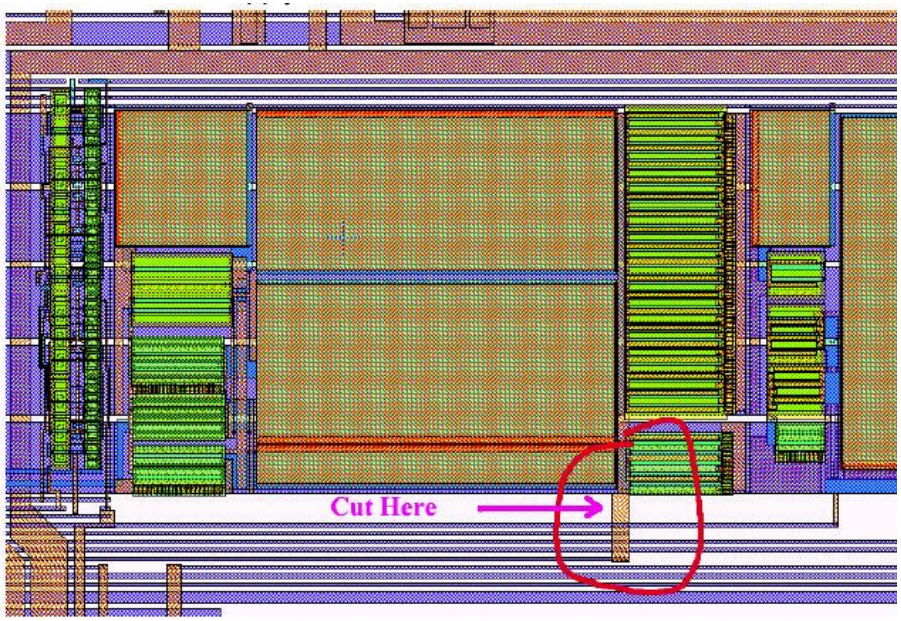
• To minimise risks we decided to have 2 r-h suppliers and to design the same FE chip first in DMILL (more mature, less expensive, but 2-metal layers only) then in HSOI4 (3-metal layers, possible to fit the B layer pixel cell (300 mm long) in).

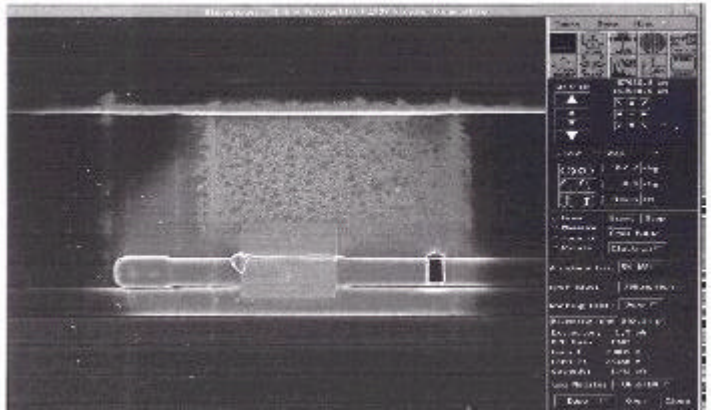
• This policy has also the advantage to bind all designers to a unique design and to emphasise “ownership” versus “competition”.

• FE submitted in August 99 to Temic, back in October. General properties of the chips ~OK, but miserable yield. Some design errors (insufficient driving power of some nodes, short not detected by DRC) made the investigations more difficult and time consuming.

• Focussed Ion Beam (FIB) surgery has been necessary to correct one layout error (cntrl discriminator threshold voltage) and operate the chip.

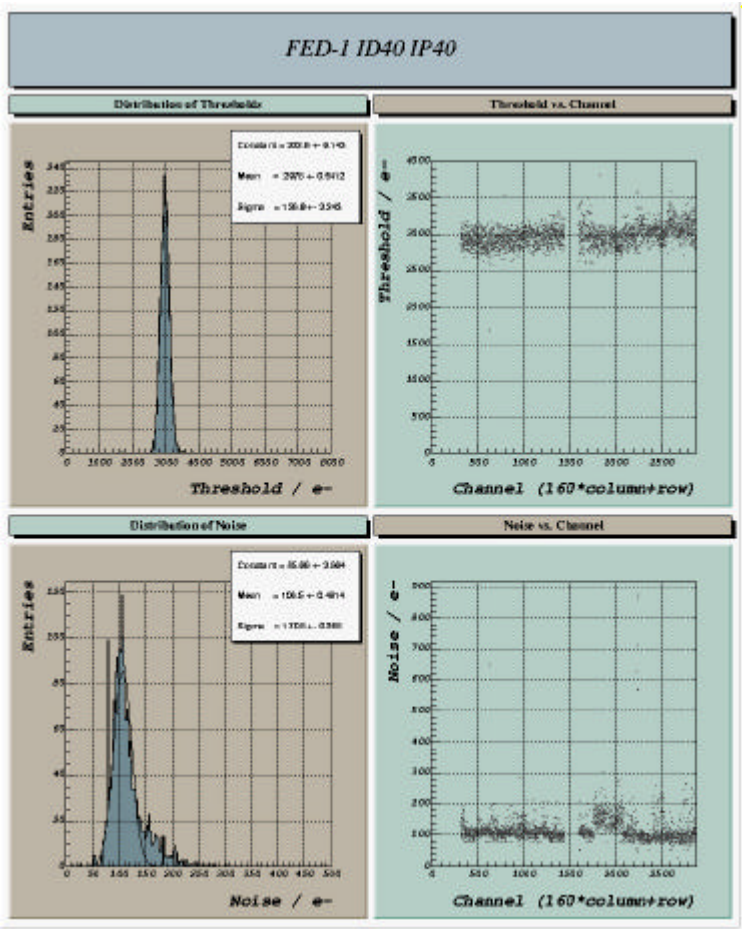
•Possible also to include test pads in some locations and investigate further some critical part of the circuit.

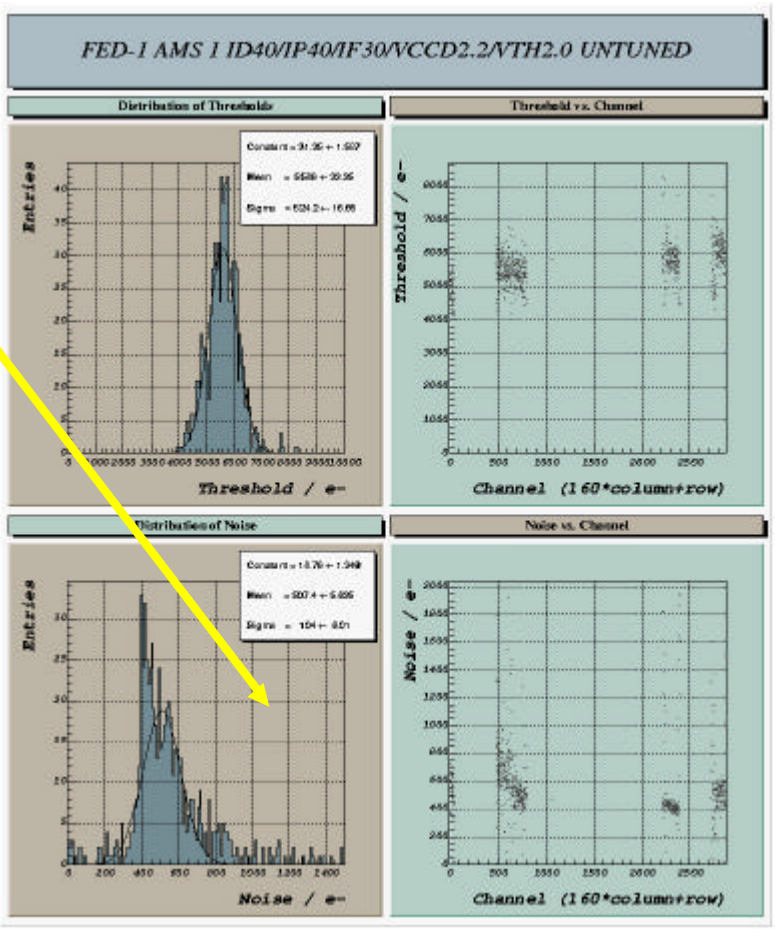




- **Threshold dispersion and noise are ok (125 e- and 110e-)**
- **Some chips integrated with detector even if buffer undersized and yield problems.**

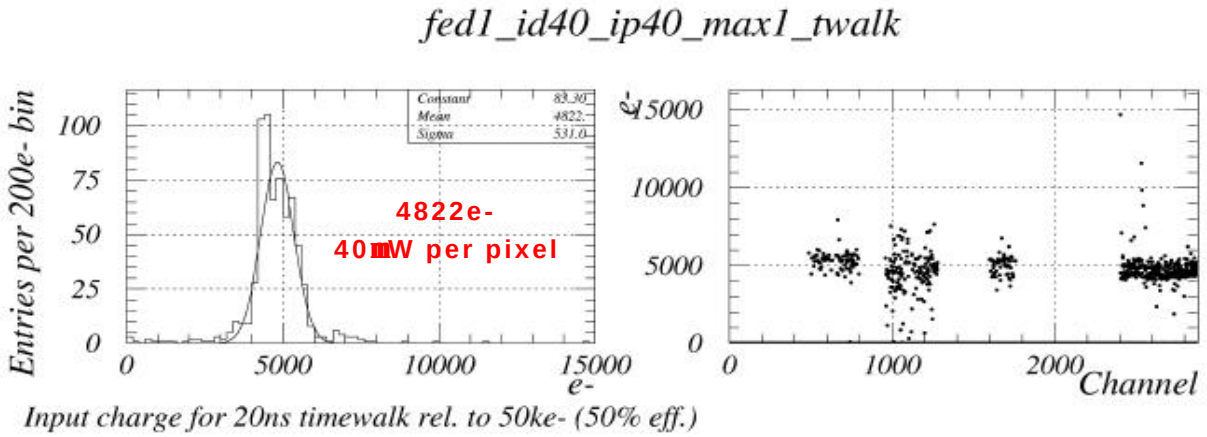
Noise larger than expected (500 e-), cross-talk very low (~2%).





- **Time dispersion within the chip is very good (1.1 ns rms).**

- **Timewalk of bare chip is fair. In-time (i.e. within 20ns) threshold of 4800 e- obtained at 40 mW/pixel power consumption. Once connected to sensor the in-time threshold is slightly above 5000 e-.**



- **Two major sources of low yield:**
  - **bit loss in a 2880 bit long quasi-dynamic control shift register, and**
  - **a defect in a dynamic storage node used in the readout logic which causes it to discharge on a timescale of 100ns (other dynamic nodes work well)**

- **This gives a 19% yield only for the above registers (minimal register tests) and no chips passing all acceptance tests (yield was 90% on rad-soft (HP) FE_B).**

- **Back-up run (same implant at the same time, metalisation steps later, no more need for FIB) done after first investigations. Go ahead in February 00, back at the beginning of April 00.**
  It has sensibly better yield but still one order of magnitude below expectations.

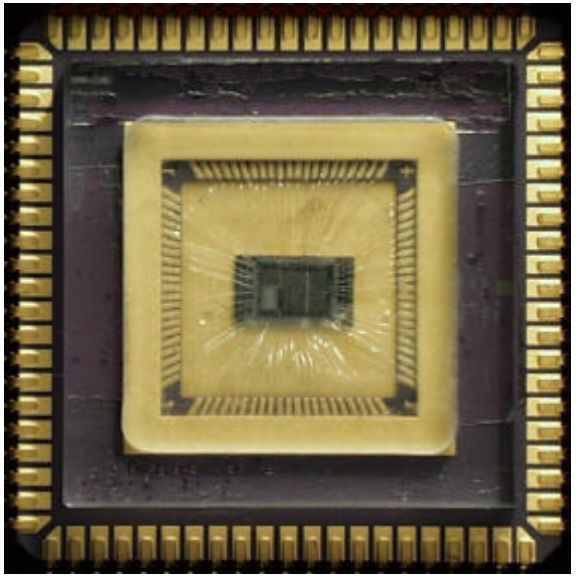
- **Lots of investigations on our side (FIB-ed and individually measured good and bad pixel cells), many discussions with DMILL experts and Temic technical staff .**

• We have then proven that the yield in the critical nodes is due to low drain-source resistance for two different NMOS transistors. This resistive behaviour is only seen in bad pixels (which show up typically in groups of 5 or so).

• Reverse engineering done at Temic did not show any evidence for technology problems, the parameter of the run were at the edge of the acceptance tests (but still in)

• The other relatively large chip (3.5 x 6.1 mm) submitted in the same run (a prototype of the Module Control Chip: MCCD0) did not have yield problems (11/14 worked above design frequency (90 MHz), this yield is as expected considering the chip area).
This chip contains only static logic.

8 MCCs have been irradiated to 30MRad, they all happily survived (SEU study ongoing).



- **Is the problem this run? Or the technology? Or our design in this technology?**

• We then decided (and reviewers (15/6/00) agreed with us) to submit two similar FE_chips in the reticle, i.e.:

- **a chip as the original FED with all bug fixes and all the prescriptions to minimise the yield problems,**
- **a chip where the critical dynamic nodes are made static. This requires more transistors and we decided to leave out the threshold control circuitry (to submit without major redesign).**

• In the same reticle (submitted on July 20, delivery expected Nov 17) also a quasi final version of the MCC + optochips. Technological splits have been made to clarify the origin of the yield problem.

• Decision if DMILL is a valid technology for our F-E chips to be taken not later than Feb 2001 (lab + irradiation tests). If answer is negative, we have to cope with a schedule delay of 8-12 months.

• **Design of the HSOI4 version of the chip was well advanced when we decided to stop it as a consequence of a production cost increase by 2.5 (Aug.00).**

• **Translation of our design in DeepSubMicron(*) started immediately (preparation was going on in the background since few months) with two designer workshops at LBNL (Sept 20-22) and Cern (Sept 29) . June 1st 2001 is the projected submission date.**

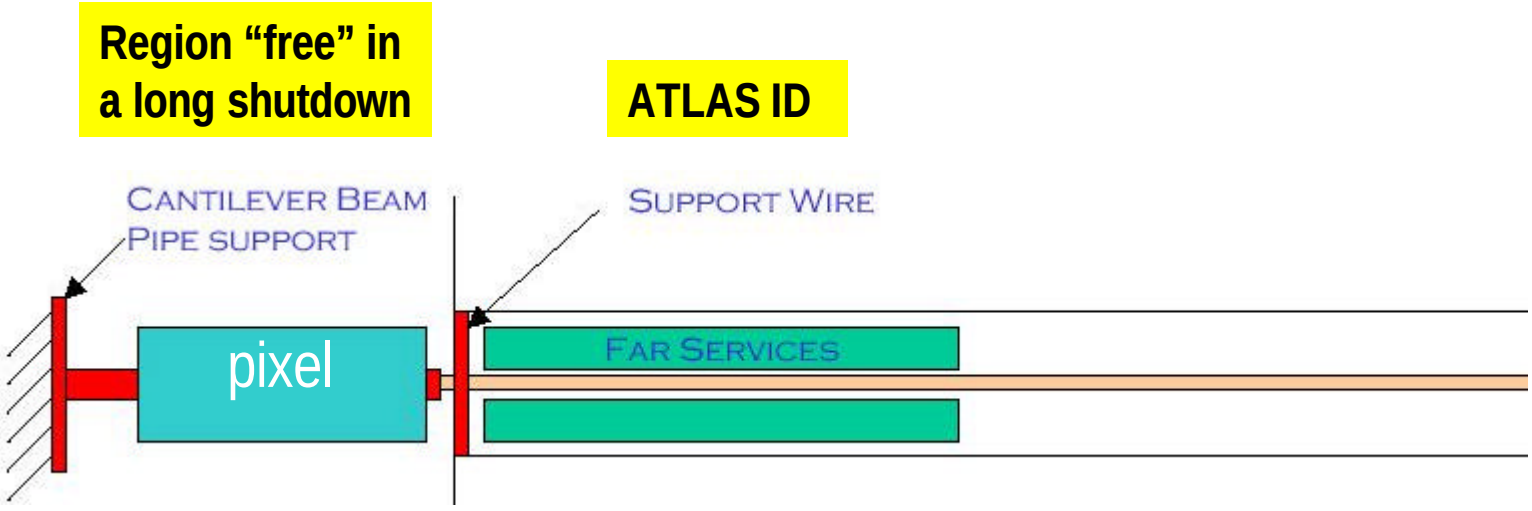
(*) DSM (i.e. 0.25 mm gate length commercial ASICs) was recently proven to be rad-hard once proper design prescriptions are used ("edgless" layouts and use of guard rings). Sources available to HEP are IBM (frame contract with CERN in place) and TSCM.

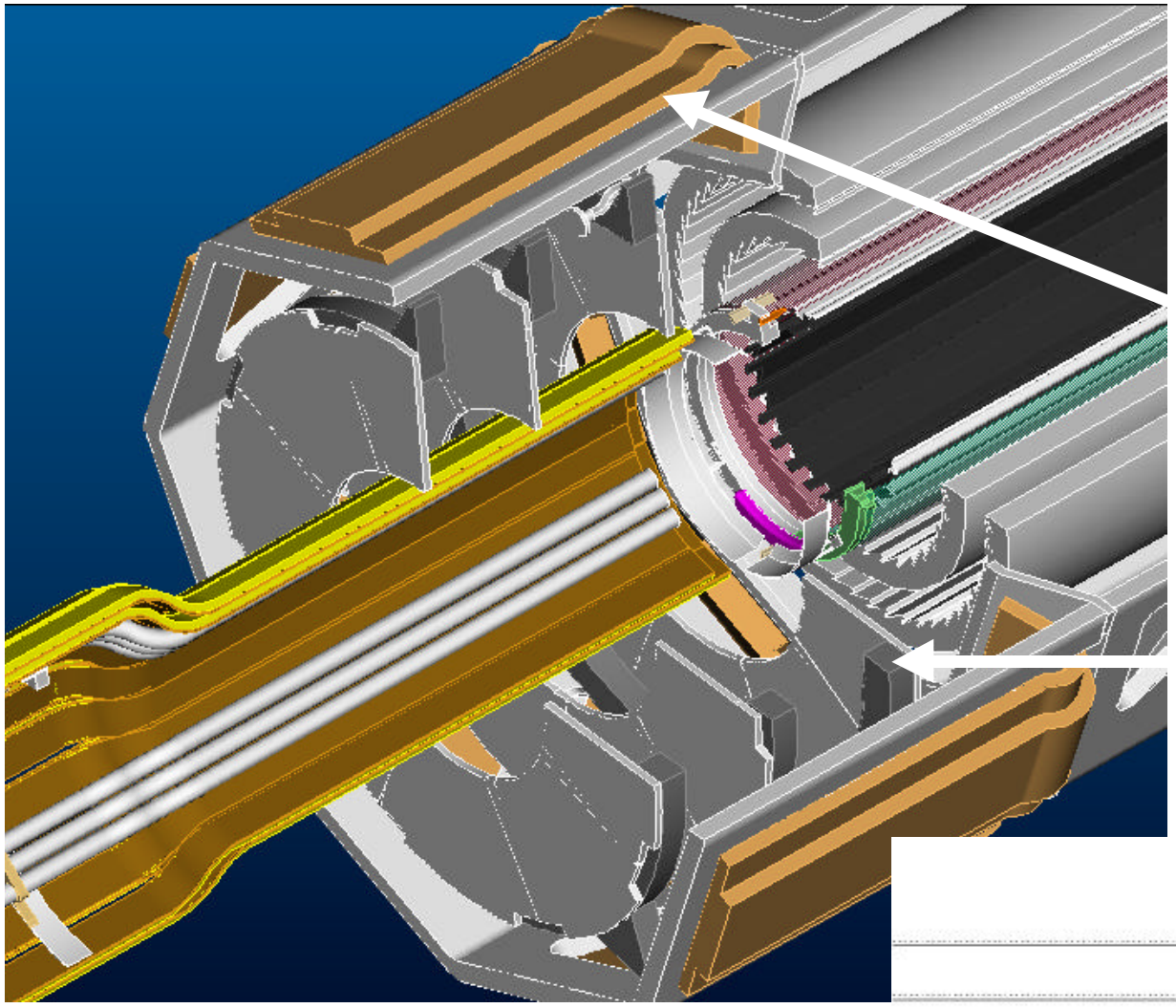
Layout update

• **Assuming TDR layout and present LHC schedule we would need to install 90% of the system (all but the B_layer) on 4/04 (i.e. together with the barrel ID).**

• **To cope with the rad-hard electronics schedule (assume DSM):**
  • **reduction of pixel total surface (i.e. # of modules) and**
  • **installation as much as possible independent from the rest of the ID**

•**This has been proposed, accepted by the IDSG and is currently under optimisation (need SCT forward inner bore change). It preserves the work done to-date (same modules, same staves, same sectors,…) and allows insertion of the full pixel system in a long shutdown scenario (forward calorimeter & forward beam pipe section out).**

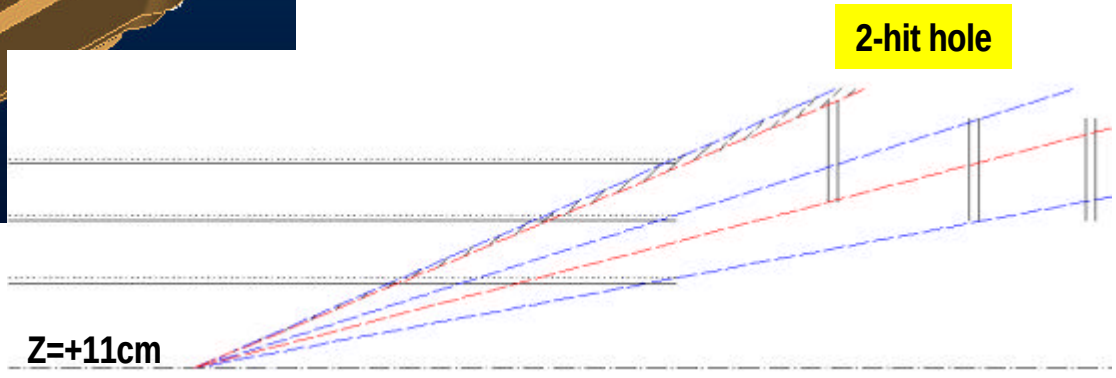




- **Outer pixel envelope must be minimized (to minimize impact of SCT bore change)**

- **Barrel Services need to be reduced in width to fit through and on a narrower panel**

- **9-sector disk for first disk to reduce acceptance losses**



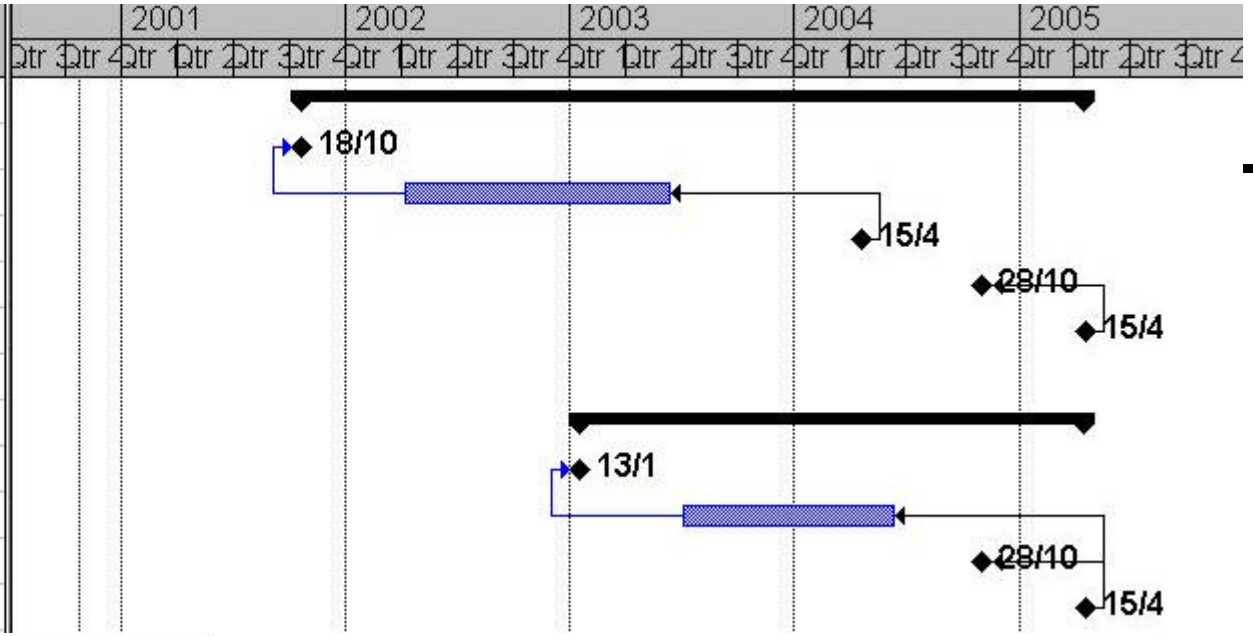
- **# of modules = 1782/2228 = 80% of TDR layout (the smallest possible compatible with 3 hits, acceptance over |h|<2.5 and use of existing parts)**
- **Installation can happen up to Spring 2005 (i.e. 1 year later than TDR). Eventual installation (upgrade) after turn-on doable without major intervention.**

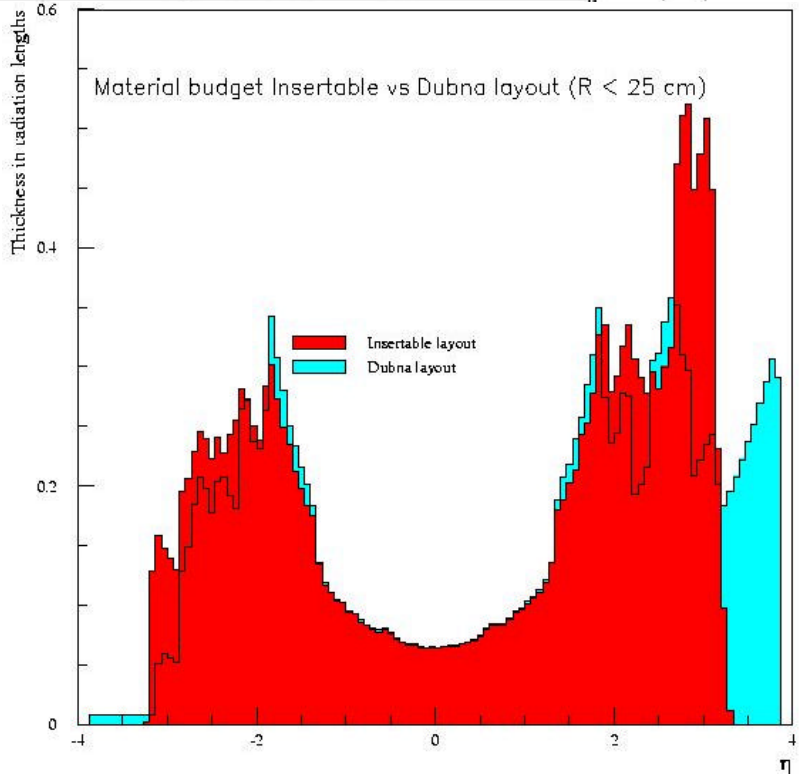
Barrel						Active	Tilt
	Radius(mm)	Staves	Modules	Chips	Channels	Area(m^2)	Angle(^{o})
B-layer	50.5	22	286	4576	1.76E+07	0.28	-19
Layer 1	88.5	38	494	7904	3.04E+07	0.48	-17.5
Layer 2	122.5	54	702	11232	4.31E+07	0.68	-17.5
Subtotal		114	1482	23712	9.11E+07	1.43	
Disks							
	Inner	Outer				Active	
Z(m)	Radius(mm)	Radius(mm)	Modules	Chips	Channels	Area(m^2)	Sectors
495	99.2	160	54	864	2.49E+06	0.05	9
580	88.1	148.9	48	768	2.21E+06	0.04	8
650	88.1	148.9	48	768	2.21E+06	0.04	8
Subtotal(Both Sides)			300	4800	1.38E+07	0.28	50
GRAND TOTALS			1782	28512	1.0E+08	1.71	

- **New baseline double wall Be beam pipe has been recently defined, which makes possible in situ bake-out (use of internal getters). This implies increased B_layer mean radius to 50.5mm (was 43mm in the TDR).**

$$\sigma(d_0) = 11 \oplus \frac{8 \oplus 71 \cdot \frac{r_B}{40.0} \oplus 14 \cdot \sqrt{x} \cdot \frac{r_{bp}}{24.5}}{p_T \sqrt{\sin\theta}} \mu m$$

ID	Task Name
1	**TDR layout**
2	Submit production electronics
3	Fixed module production
4	First installation complete
5	Complete module prod(B-Layer)
6	Complete installation
7	
8	**Insertable layout**
9	Submit production electronics
10	Outer module production
11	Complete module prod(B-Layer)
12	Complete installation





- **Schedule advantage is clear (oversimplified).**
- **Material does not increase much. Some increase around h=2.5, some decrease above (B_layer services go sooner to large radius).**

Mechanics, cooling and services

The pixel detector mechanical structure

Local support structure

Intermediate support structure

Global support structure

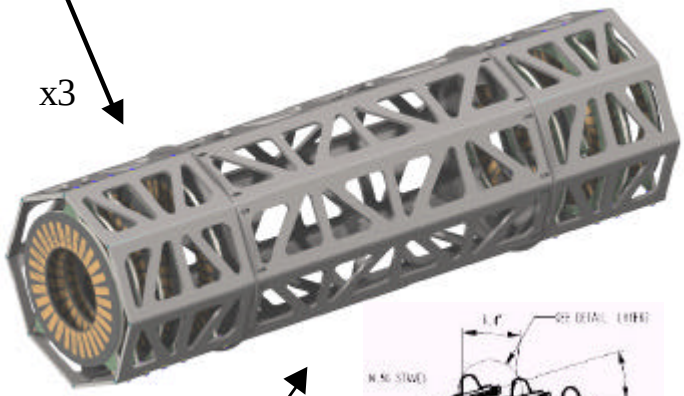
x m (8-9)

x3

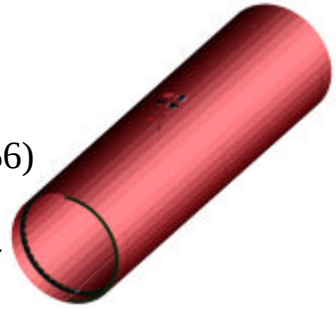
x3

Sector

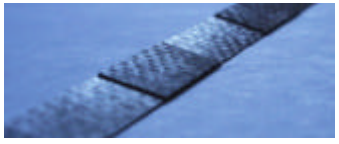
Disc ring

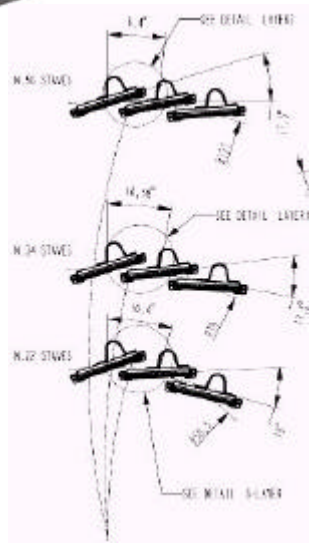


x n (22,40,56)



x3





Stave

Barrel shell

- **Good progress on local supports.**
- **Status and workpackage reviewed at LBNL workshop (April 00)**
- **we passed local support FDR on June 15.**

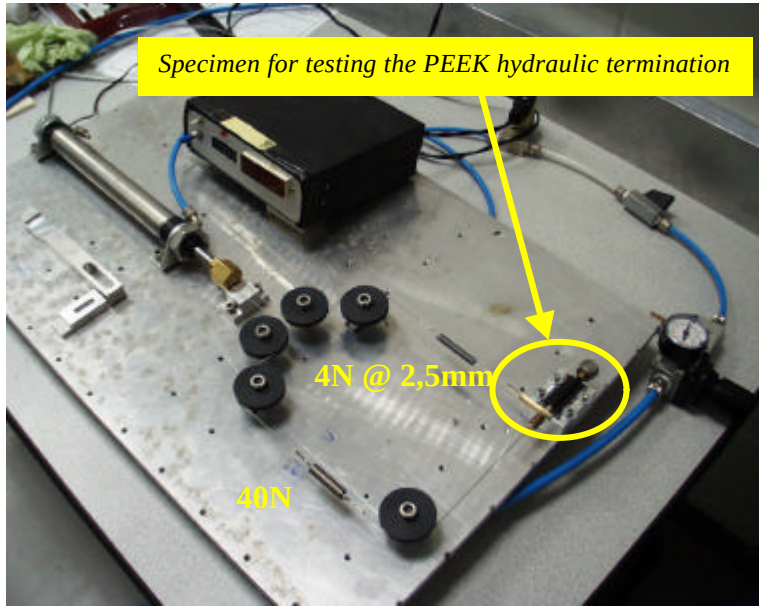
examples of progress in local supports

- **Considerable effort on defining QA for fabrication process and fabricate samples (e.g. 20 Omega stiffeners fabricated and qualified dimensionally and for gas tightness).**

- **Destructive pressure tests for Omega/C-C tubes indicate tolerance at >22 Atm.**

- **Fatigue tests done through pressure cycles (5 10^4 cycles@0-8 Atm) and temperature cycles (+20; -20) both on structures and on glue joints do not show problems.**

- **Details of critical parts (e.g. terminations) defined and stress&fatigue tests done (3 10^3 cycles at 40N and 10Nmm, i.e. x10 the nominal values) also on fully irradiated parts.**



• **Moving from generic design to detail of design and approaching the fabrication criteria.**

• **Comments of FDR referees (Szeless, Catinaccio, Godlewski, Oriunno) were positive and indicated the need of:**

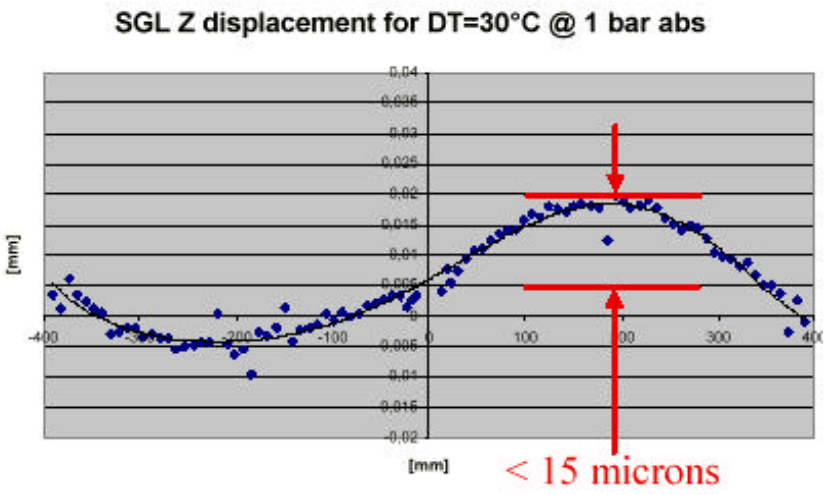
- **more prototypes (O(5%) of final sample) to understand yield and problems in production**
- **use of industrial processes as much as possible.**
- **the choice between use of Al tubes weakly coupled to structures and sealed carbon tubes is left to the collaboration once more pre-production work is done (this is now scheduled in Dec.00)**

• **The local support PRR is scheduled for Feb 01.**

Cooling

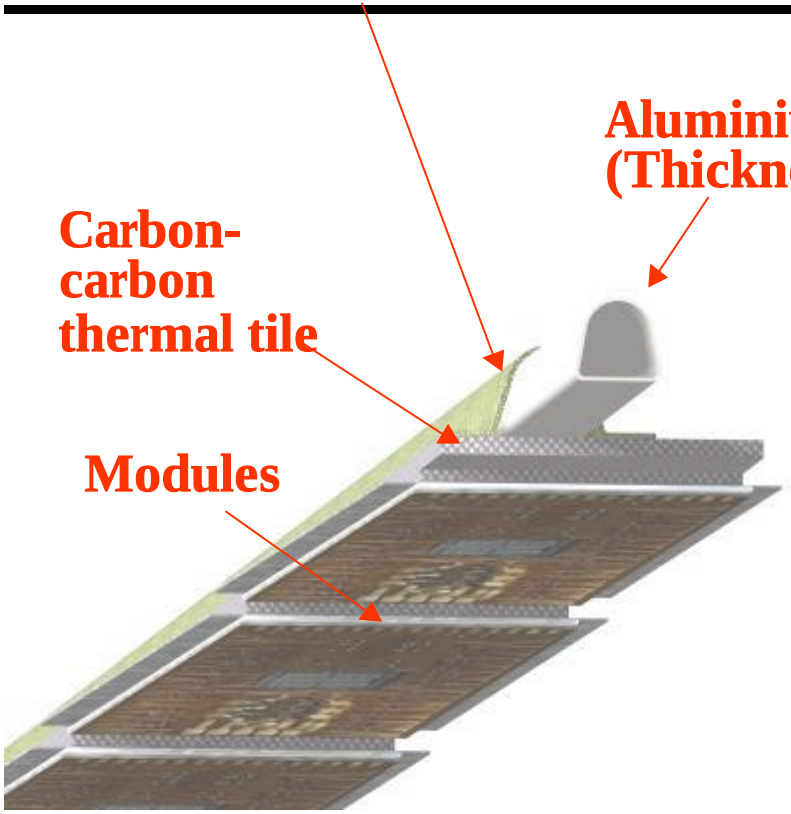
With evaporative C_3F_8, possible to cool two staves in series (simplify services). Stave is the most critical for cooling (more power, asymmetry).

Low stave deformations during cool-down

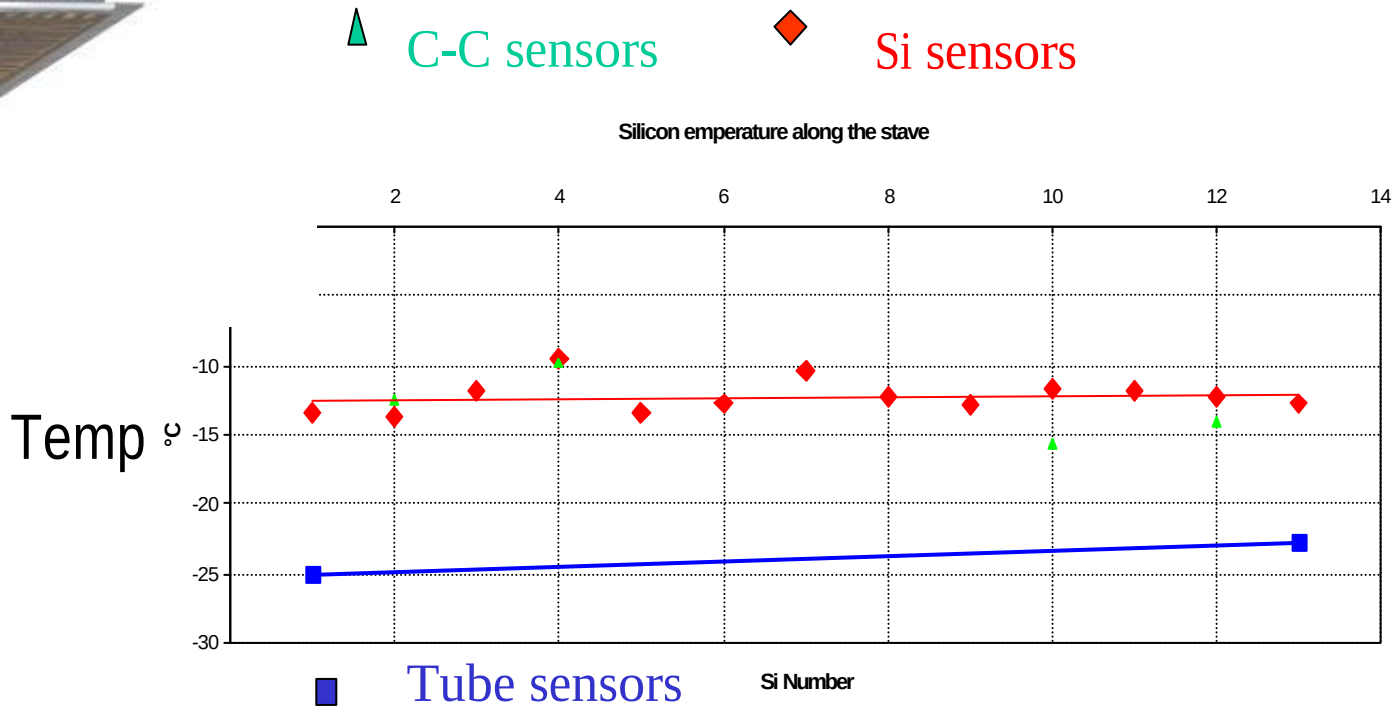


Cooling review (14/6/00) positive for evaporative C_3F_8

Carbon fibres with Cyanate Ester matrix Omega (Thickness 0.3 mm)

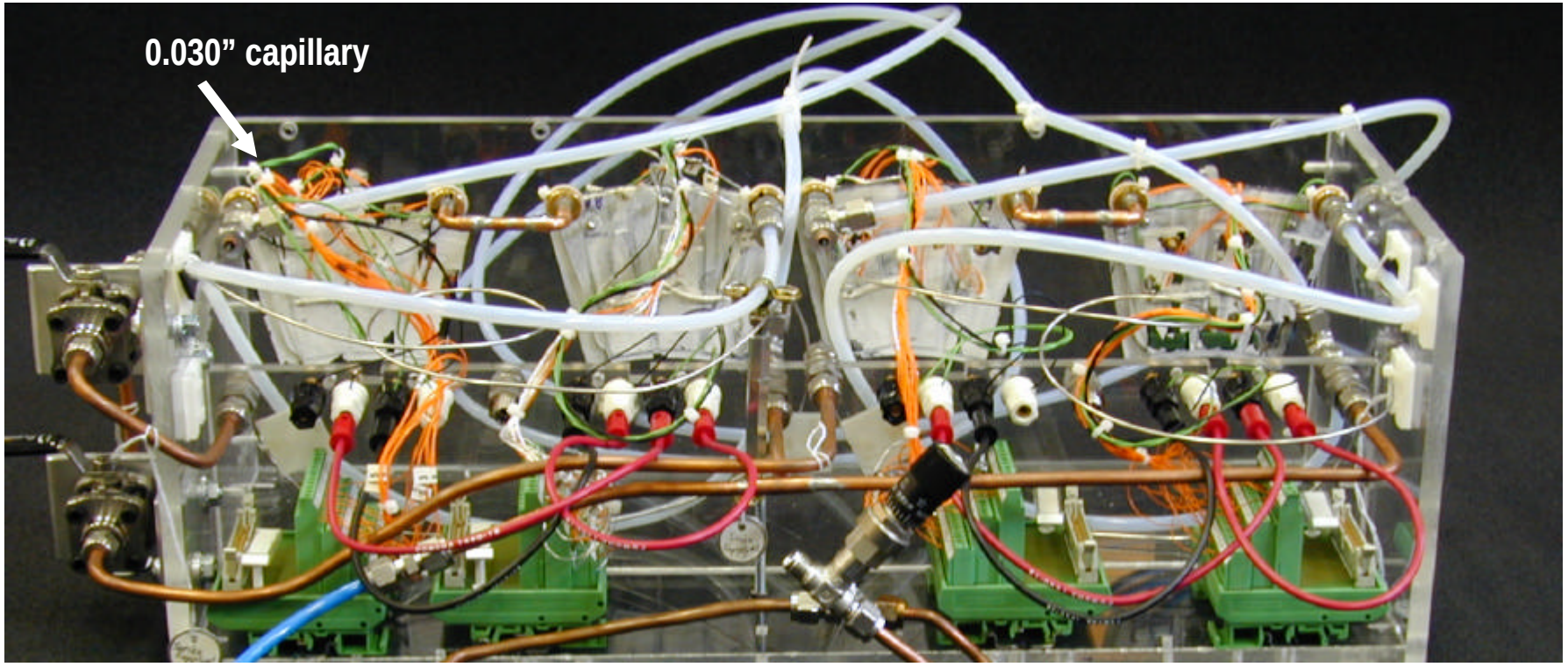


Cooling results satisfactory also for the back-up stave solution

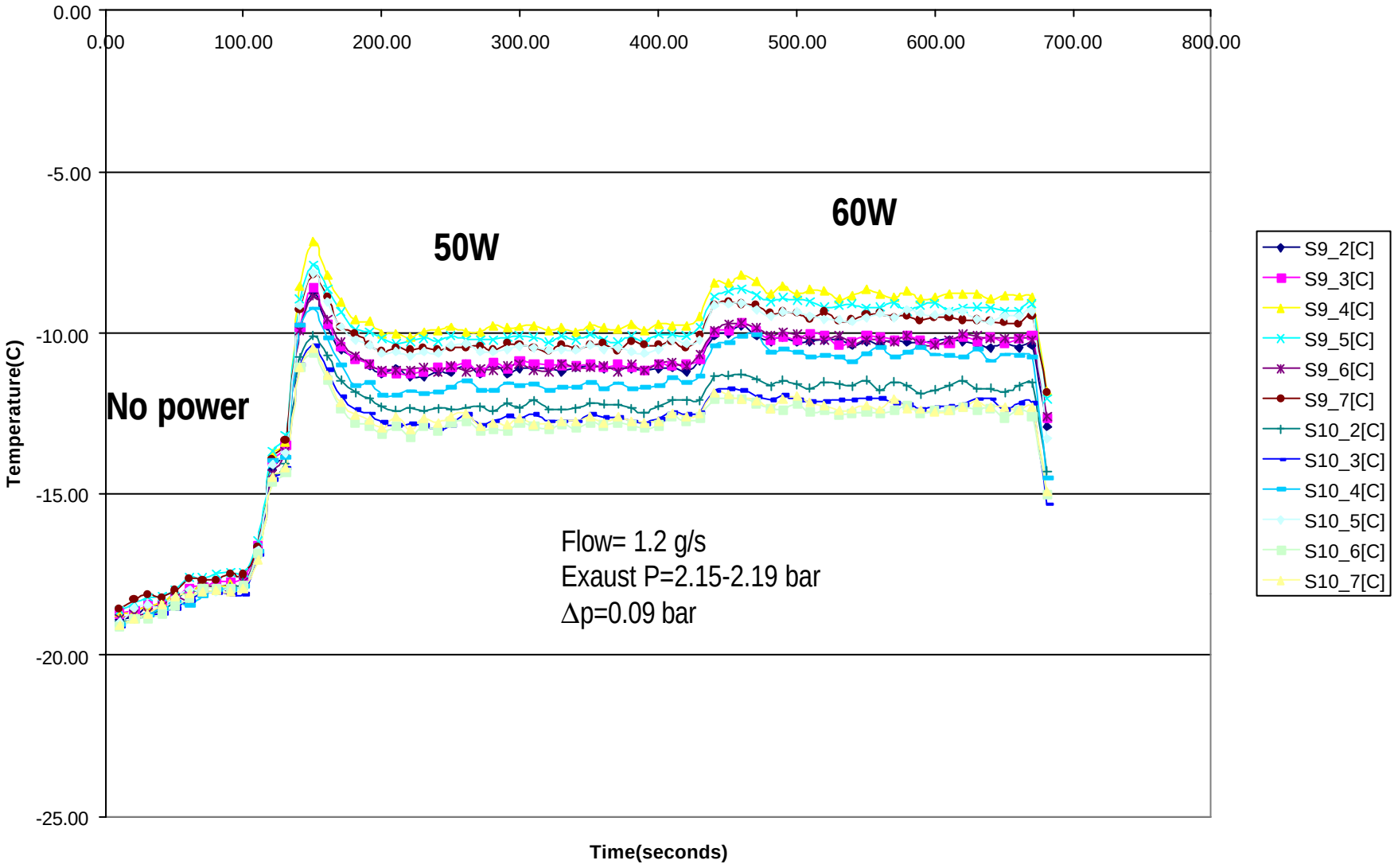


Results with disks also very encouraging

here the layout in the evaporative test set-up at Cern (2 times 2 sectors in parallel)

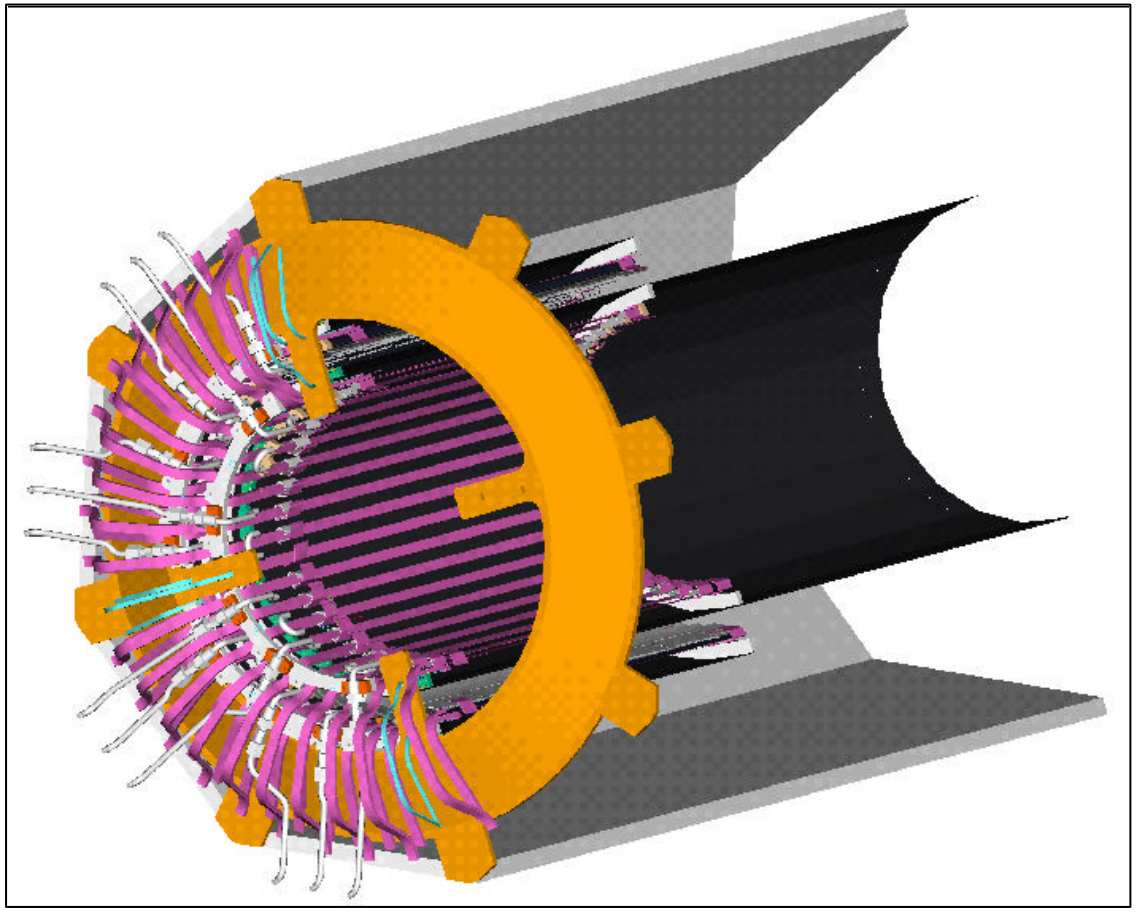


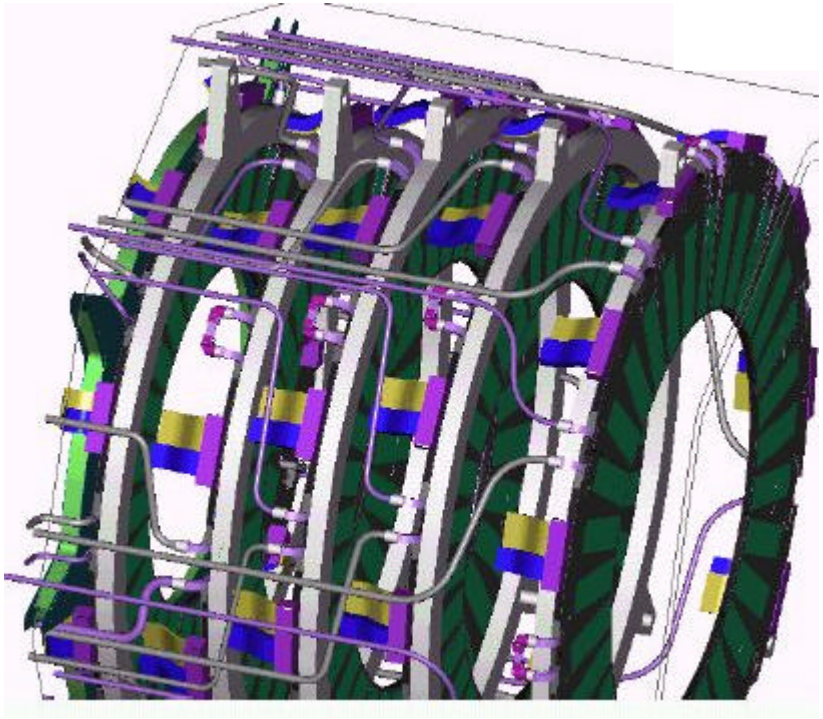
here the results on the Si temperature (2 sectors in parallel, 12 silicon tiles)



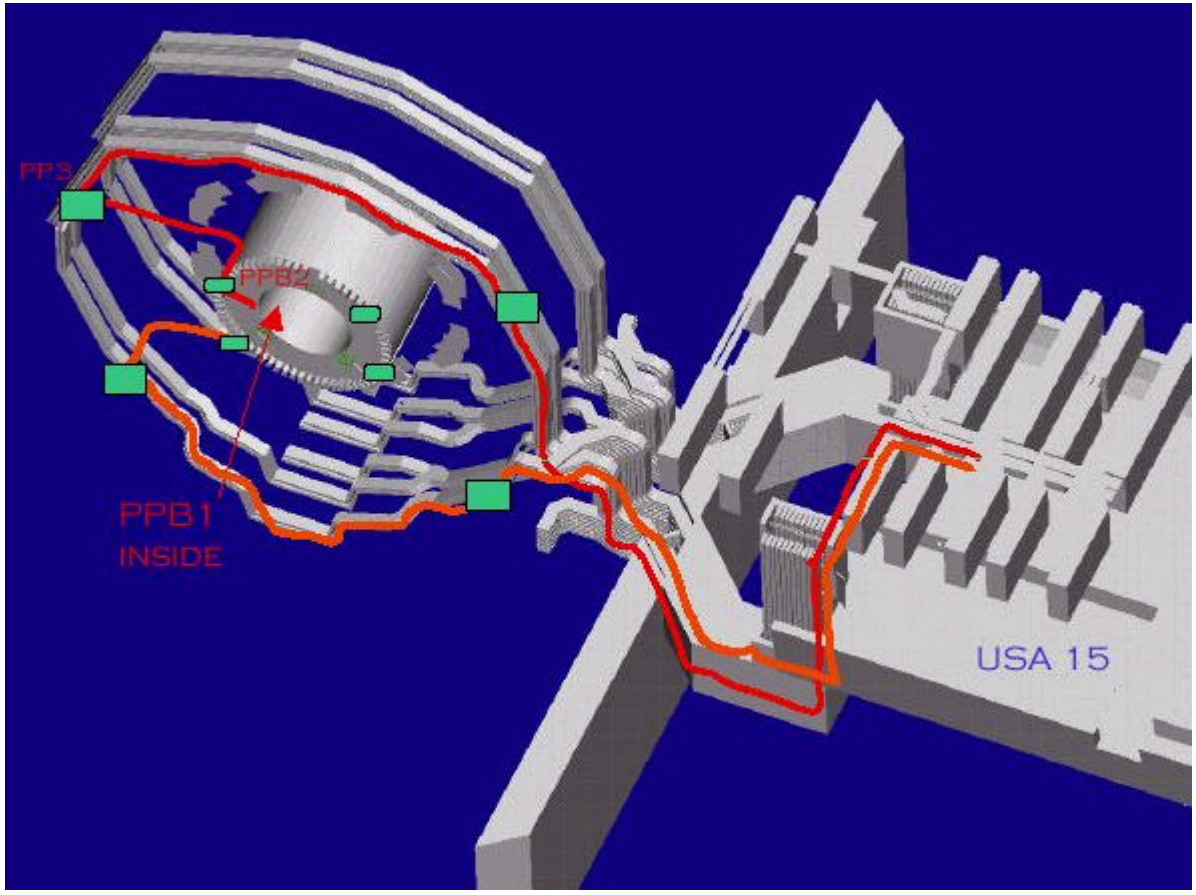
Integration and services

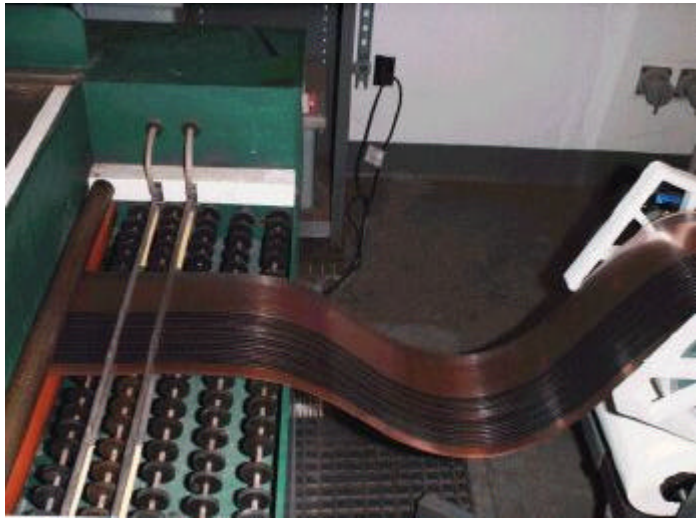
• **Coming closer to the actual construction of the parts, we look more and more in detail to cable and tube paths, installation sequences and related problems**





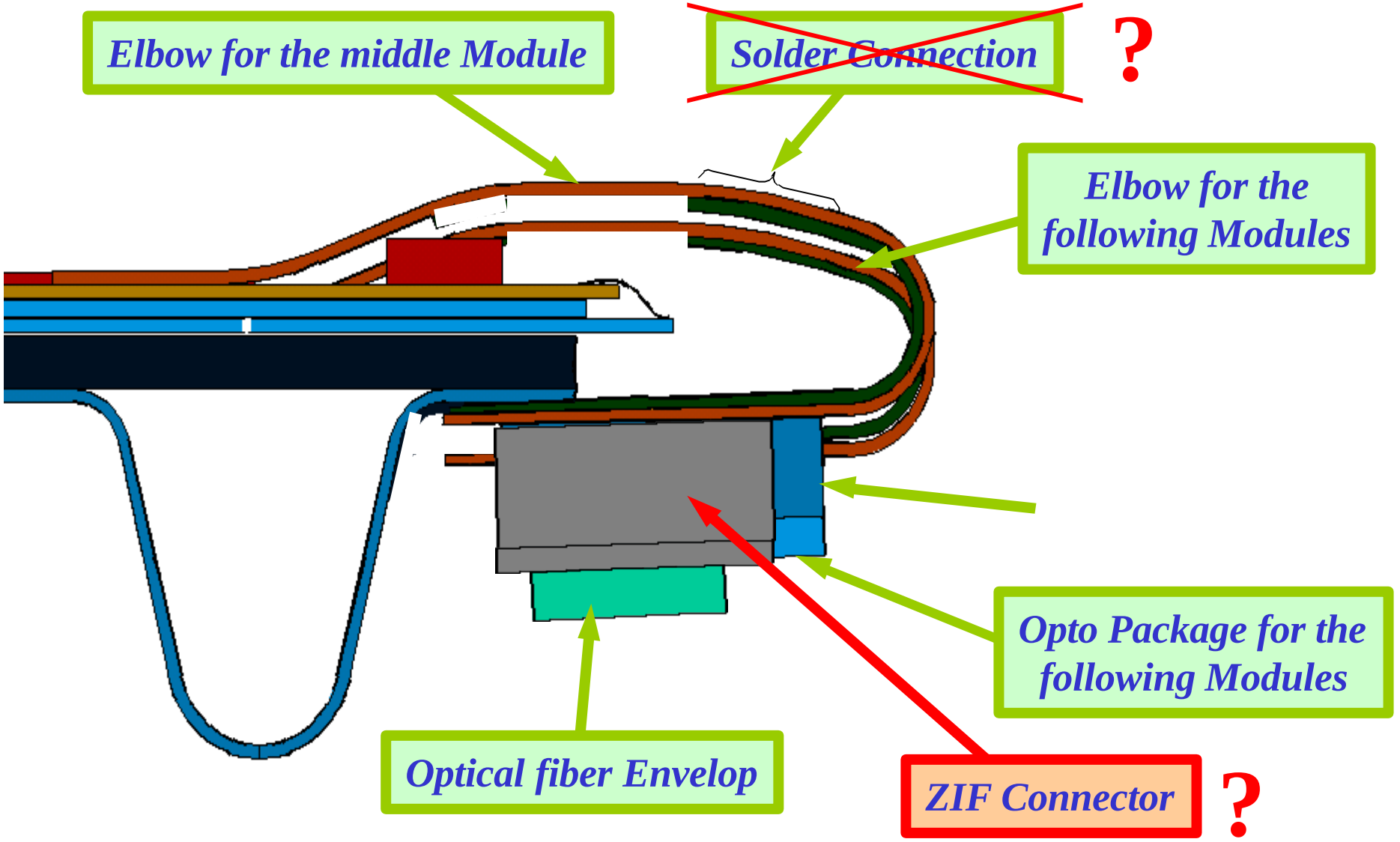
- Detail of the cable path is studied (patch panels, connections, voltage drop).
- Mock-up are built to understand real cross-section and handling
- US15 is also considered as location for (part of) power supplies (shorter cables).





- Low mass cable prototypes are under fabrication at LBNL

• **Also pigtails (stave more difficult) have been prototyped and are under test.**



Conclusions

• Progress on oxygenated sensors allows to build pixel sensors surviving longer or warmer or at smaller radius.

• The pixel project has encountered difficulties in the transition of the front-end chip from rad-soft to rad-hard technology.

• With the exception of the point above, we are progressing according to expectations.

• We are putting maximum priority and large amount of resources onto the rad-hard problem and we did change the layout to minimise its impact on the schedule.