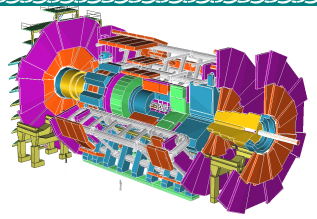


ATLAS PIXEL MODULE TESTING

US ATLAS Pixel Review, LBNL, 2nd November 2000

John Richardson
Lawrence Berkeley National Laboratory

Overview

The 'Demonstrator' PLL Test System (Nov. 1997-date)

- System architecture
- The PLL (Pixel Low Level card)
- The PCC (Pixel Control Card)
- PixelDAQ software
- Wafer probing
- Analogue test procedures & example results

The TurboPLL Test System

- System architecture
- The TurboPLL
- The PICT & TurboPCC
- Production module-testing plans

The Demonstrator Test System

Introduction

Conceived in November '97 and realised for April '98 CERN testbeam, LBL/Wisconsin collaboration. Designed initially to address the needs of (radiation-soft) demonstrator FE-chip (FE-A & B) testing.

The full spectrum of test requirements was provided for by one system e.g.:

- **Probe testing of bare electronics wafers (in order to identify 'known good die' (KGD) prior to dicing).**
- **Performing detailed analogue evaluations (threshold, ENC, timewalk, crosstalk TOT calibration etc.) of bump-bonded assemblies in the laboratory.**
- **Being capable of performing comprehensive tests at intermediate steps in module construction e.g. probing bare modules prior to flex attachment.**
- **Providing the readout system for testing single-chip assemblies and full-size modules in the H8 testbeam at CERN.**

This 'fully integrated' approach in which identical hardware and software is used at all evaluation stages has proven extremely beneficial in terms of understanding what to expect from a particular device in the testbeam e.g., for a given configuration which has been arrived upon through detailed laboratory optimisation.

This system was adopted throughout the whole collaboration and represents *the standard* for all FE electronics & module evaluation work performed therein.

The Demonstrator Test System

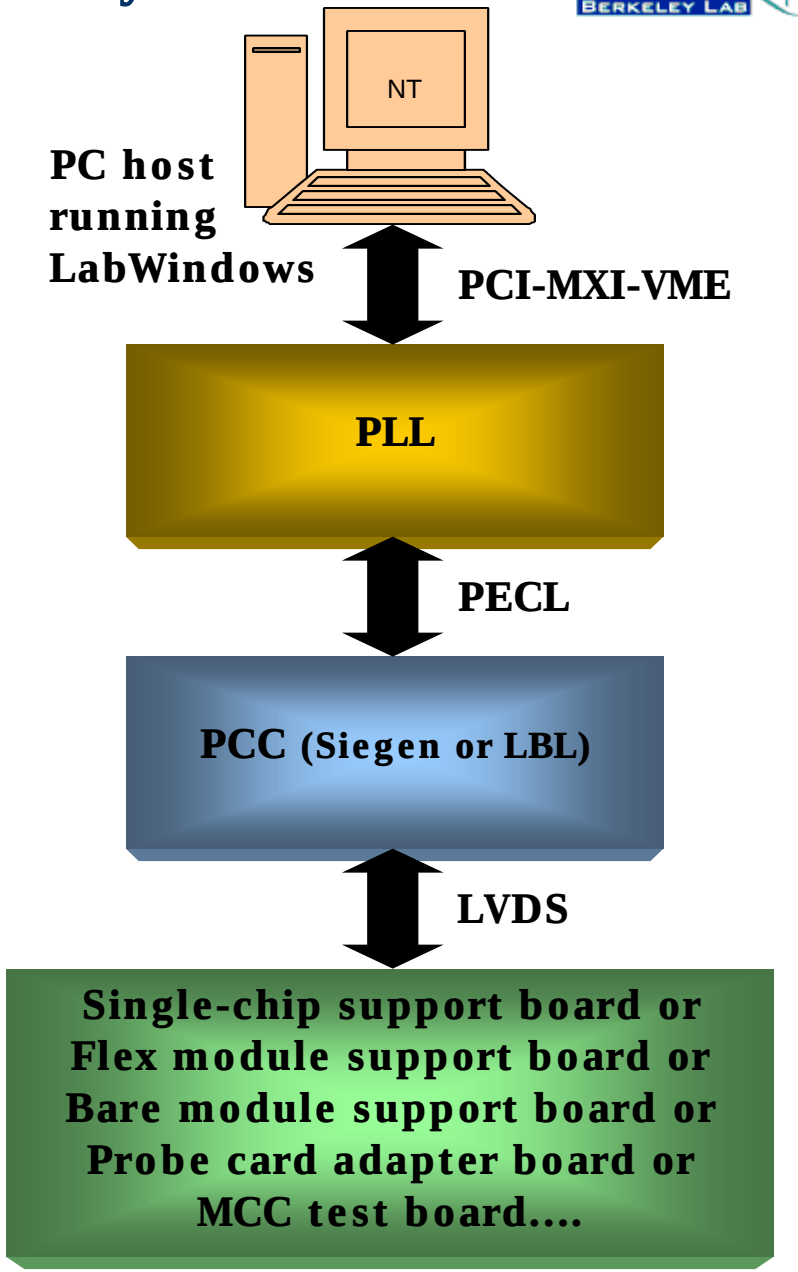
System Architecture

Basis is 6U VME board (the 'PLL') which incorporates a large Orca FPGA and input/output FIFOs for communication with the host PC.

Pixel Control Card (PCC) provides 4 DACs for setting the calibration pulse amplitude (VCAL) along with threshold control for FE-A. Also includes a delay chip for varying the relative timing of the cal strobe and LV1 trigger with 250ps granularity over 64ns.

Data transmission between PCC and the module/single-chip support board is via LVDS on a short flat cable with low –profile (Robinson P50) connectors. Support board is mostly passive, containing local termination/decoupling etc. but has LVDS buffering for digital signals.

The software package is written in ANSI C in the NI LabWindows for NT environment – provides very useful GUI creation tools along with necessary VME libraries.



The Demonstrator Test System

The Pixel Low Level Card (PLL)

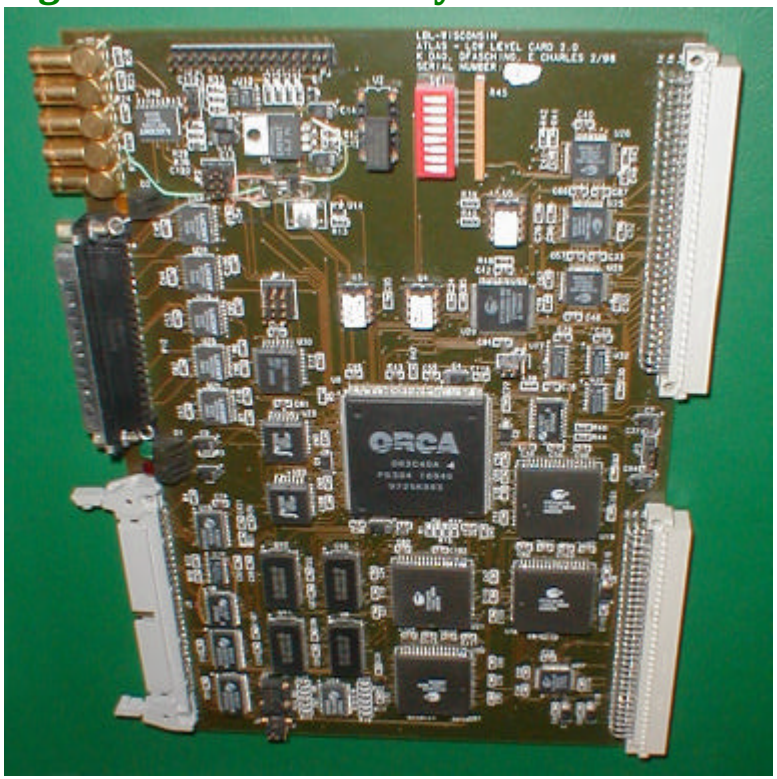
The central feature of the demonstrator test system is the VME resident PLL. This is based upon a 43,200-gate FPGA which is controlled using list processing via a 32-bit 32k-deep FIFO. Data is also returned to the host using such a FIFO.

Purpose is to create the relevant waveforms for the configuration of downstream entities (i.e. PCC, MCC, FE-chips) using a variety of protocols, along with issuing hit-strobes and triggers. Returning data is word-aligned and either sent in raw form to the output FIFO or histogrammed on-board using an available 2Mbytes of SRAM.

Level-1s may either be generated internally (for threshold scanning etc.) or provided externally via a LEMO connection. Also the fast-OR (hitbus) signal from the FEs may be used as the source of LV1 trigger creation (introducing a programmable delay).

Other LEMO connections allow the PLL to be controlled via an external 40MHz clock (for testbeam use etc.) along with providing strobe and hitbus monitoring.

Interface to PCC is via a D-type terminated shielded twisted-pair cable using PECL transmission.



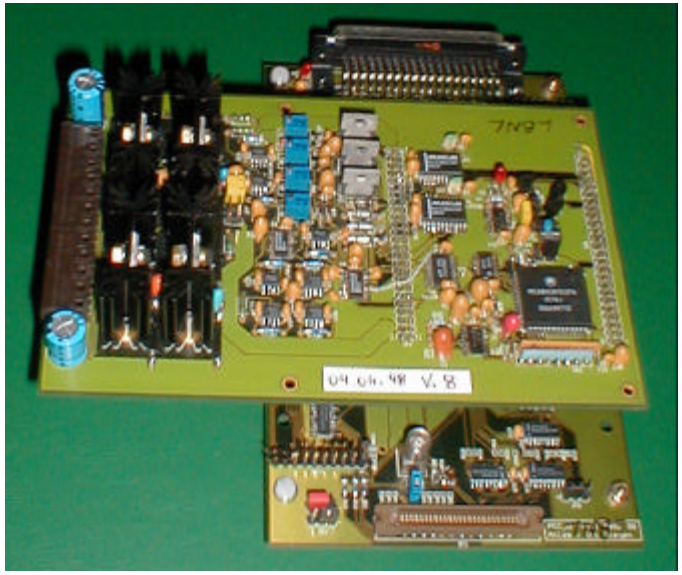
The Demonstrator Test System

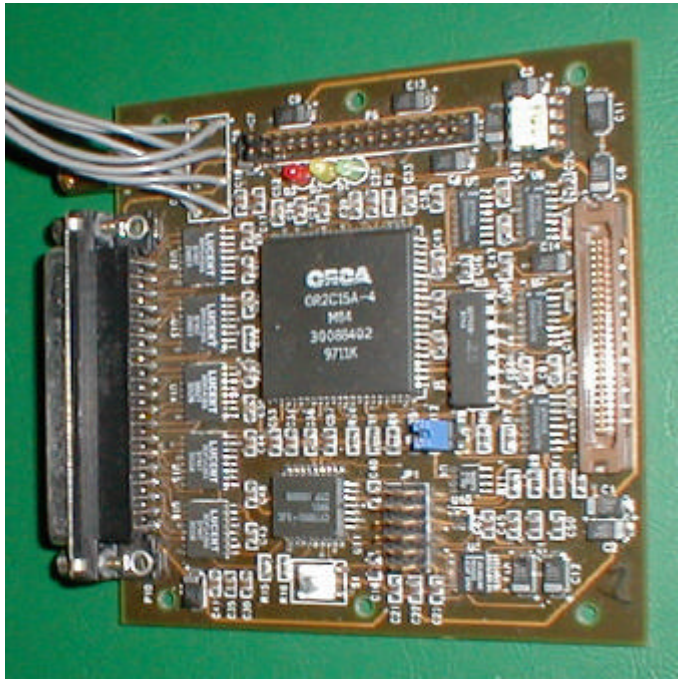
The Pixel Control Card (PCC)

This part of the system was a German contribution. Their version had integrated power supplies for powering the MCC and FE-chips along with current monitoring using on-board ADCs.

Also FPGA based. Has its own serial command protocol for configuring the four 12-bit DACs and delay unit along with reading the ADC data and powering up/down.

A version of the PCC was also produced by LBL & Wisconsin which had reduced functionality (no internal power supplies). This was used mostly at LBL for wafer probing etc. due to its greater portability and reliability.





The Demonstrator Test System

The Demonstrator Software (PixelDAQ)

The LabWindows development environment was chosen for its speed (code is developed in ANSI C) and the convenience of comprehensive, high-level GUI creation tools. Also provided are all of the necessary library routines for talking to instrumentation using a variety of standard protocols, (GPIB support in particular proved invaluable on occasion).

Panel based GUI enables the user to define the overall 'static' configuration for the FE-chips, MCC and the PCC. Also the user may define a 1D or 2D scan using any combination of parameters, (e.g. inner scan strobe-delay, outer scan input charge for timewalk studies).

Direct real-time monitoring is provided in the form of a 2D hitmap along with 4 1D plots which may be histograms (for any pixel) of 'hits vs. scan-parameter', 'hits vs. TOT' or 'mean-TOT versus scan-parameter'.

Static configurations and scan setups are stored as files so the user may dial up particular parameter sets quickly and consistently. Thus a means of standardising test procedures across the various institutes is provided, this will become a very important feature towards full scale production.

Automatic analysis routines are also included for fitting s-curves, calculating optimal trim-DAC settings and determining TOT calibrations etc.

The Demonstrator Test System

Wafer Probing

Each die is put through a range of tests on the probe station prior to bumping & dicing in order to identify KGD before bump deposition, dicing and subsequent flip-chip onto sensors

Current range of tests include:

- **automated dig. & analog power consumption**
- **write/read test of DAC, Global & Pixel reg's**
- **serial test; check for corruption in 40MHz serial output data stream**
- **digital hit injection test; 100 strobes per channel, look for 100% efficiency**
- **analogue hit injection test; make course VCAL scan and estimate threshold and ENC for all 2880 channels, look for 99% efficiency within each col.**
- **check that fast-or (hitbus) is functional and observe analogue test pixel output**

Takes ~1½ minutes per die so ~3 hours per wafer including set-up & wafer alignment

The Demonstrator Test System

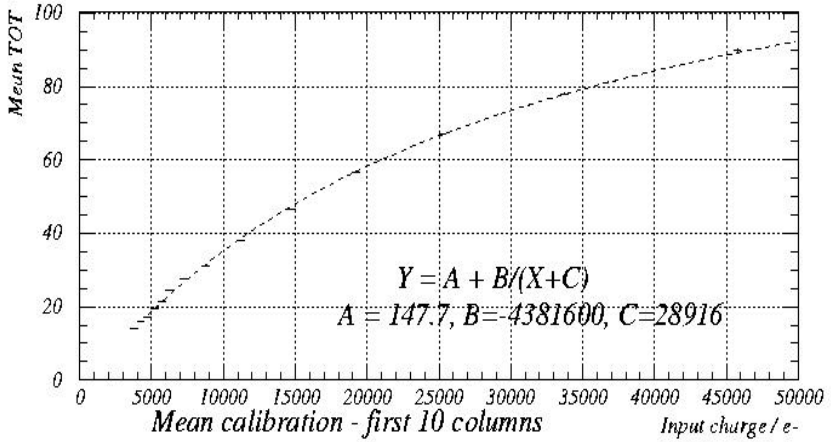
Analogue Test Procedures & Example Results

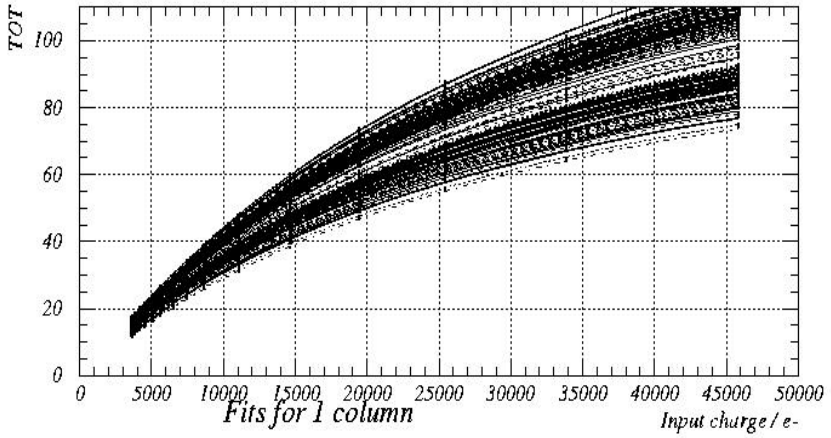
For each 'new' module the initial stage in the analogue configuration process is to tune the feedback current DACs for each FE chip in order to maximise the dynamic range for TOT measurement. Care is taken to match the chips and to ensure that for all channels there is no risk of efficiency loss due to TOT > trigger latency.

Then a 'threshold scan' is performed in which the range of calibration charge is scanned to ~6ke- in fine steps. Histograms of efficiency vs charge are produced for each channel to which an error-function (s-curve) fit yields the threshold and noise values. Takes ~0.5hr to fully process the 650 million hit injections.

The distribution of thresholds is then analysed for each chip and a 3-bit TDAC value is assigned to each channel by virtue of its position within the distribution.

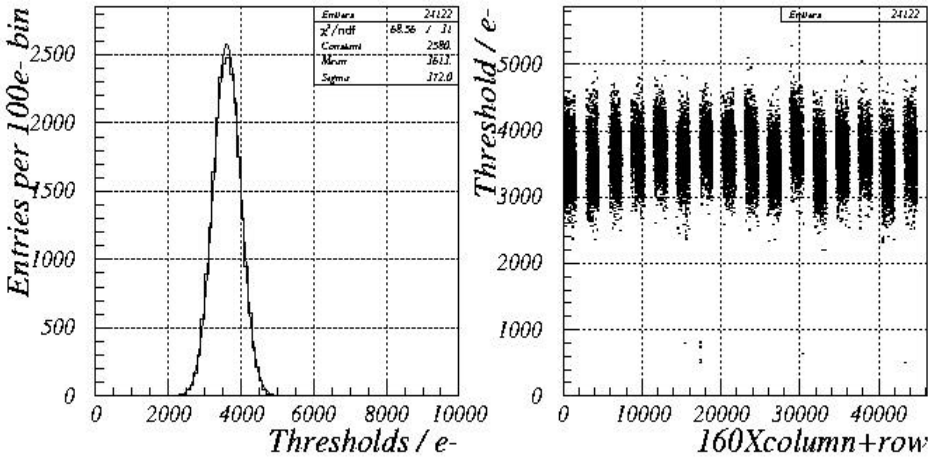
Having loaded the TDAC values another threshold scan is performed. At this stage the overall module threshold dispersion is dominated by chip-to-chip variations rather than intra-chip spreads.

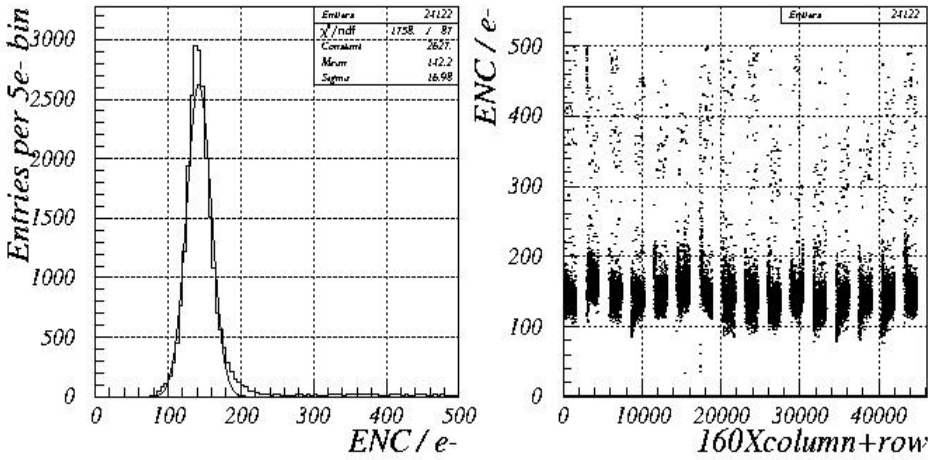


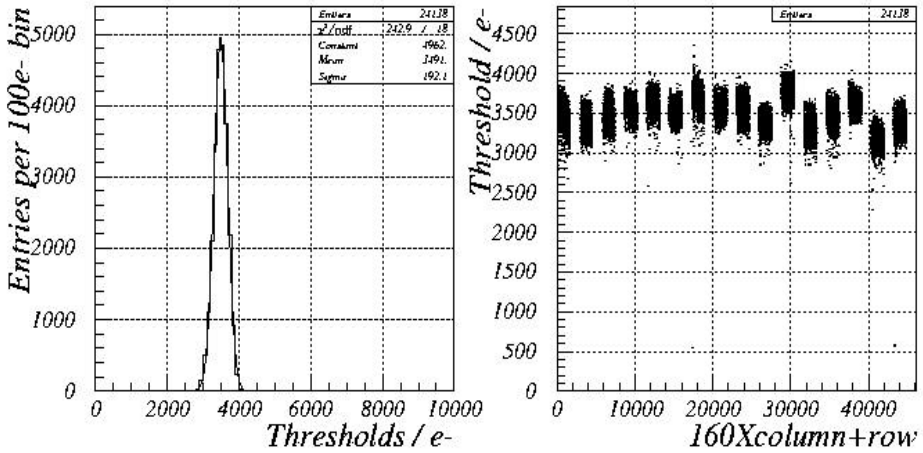


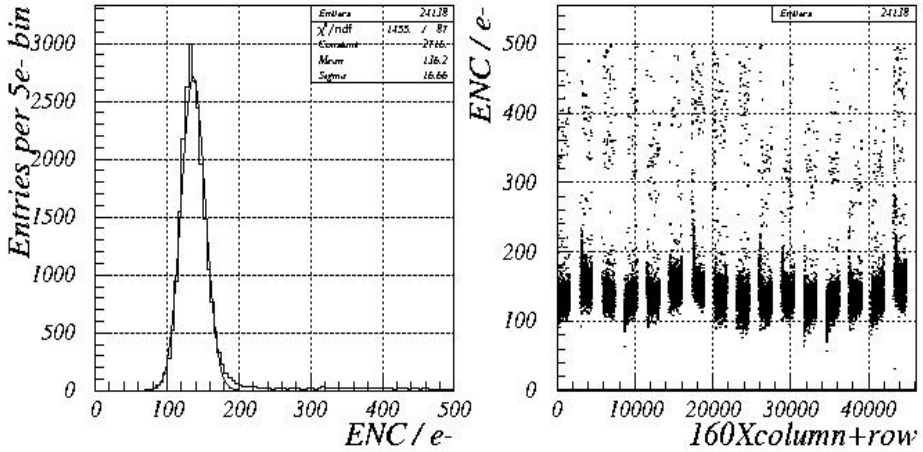
The Demonstrator Test System

Distributions of threshold (upper) and ENC for a module after the feedback current have been matched. The threshold distribution sigma = 372e- at this stage.









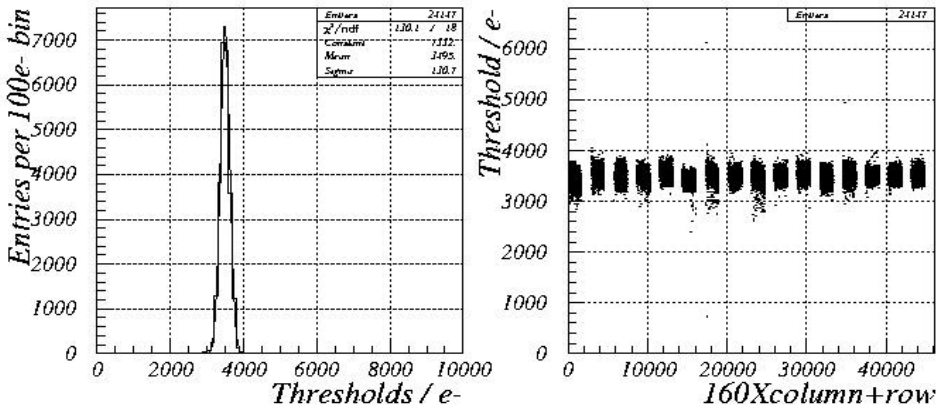
Having tuned the individual 3-bit threshold trim-DACs for each chip, the dispersion is now dominated by chip-to-chip variations, sigma = 192e-. The noise peaks at 146e- for this bare module.

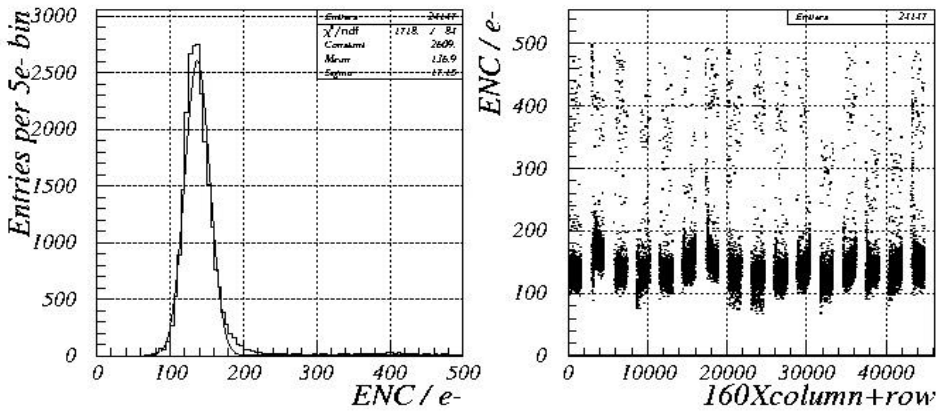
x

The Demonstrator Test System

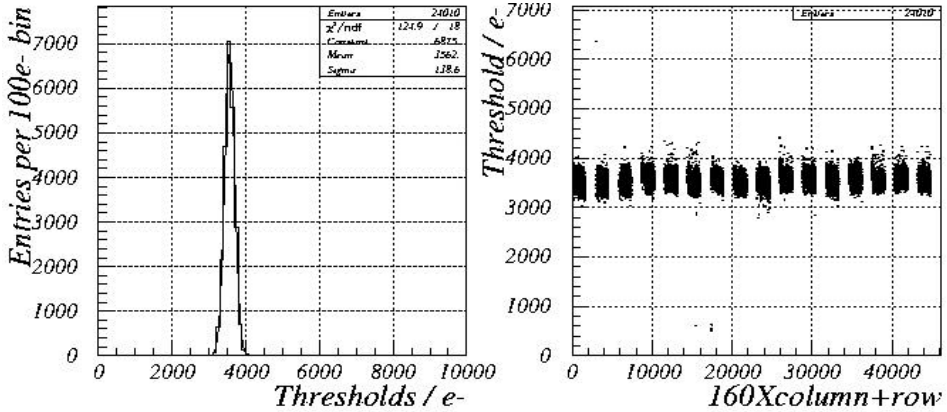
Finally the overall threshold knob for each chip is adjusted in order to minimise the overall dispersion. These examples show how an initial threshold dispersion of 370e- may be reduced to 131e-.

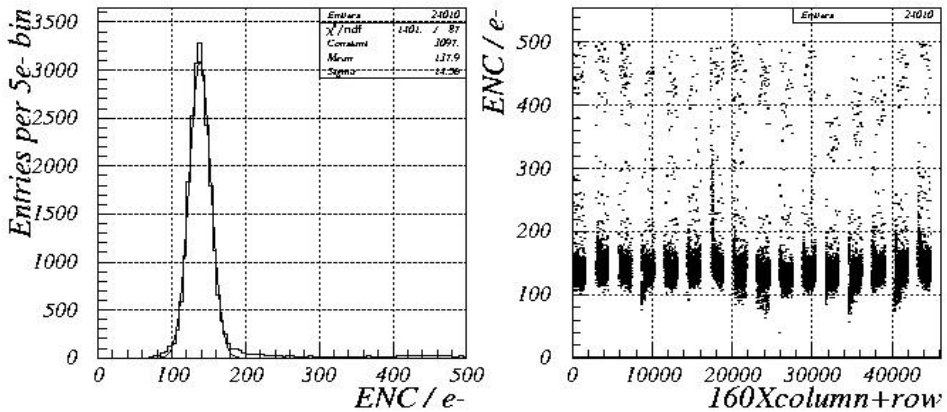
Transparent mode (one FE at a time)





Full MCC mode (concurrent readout)

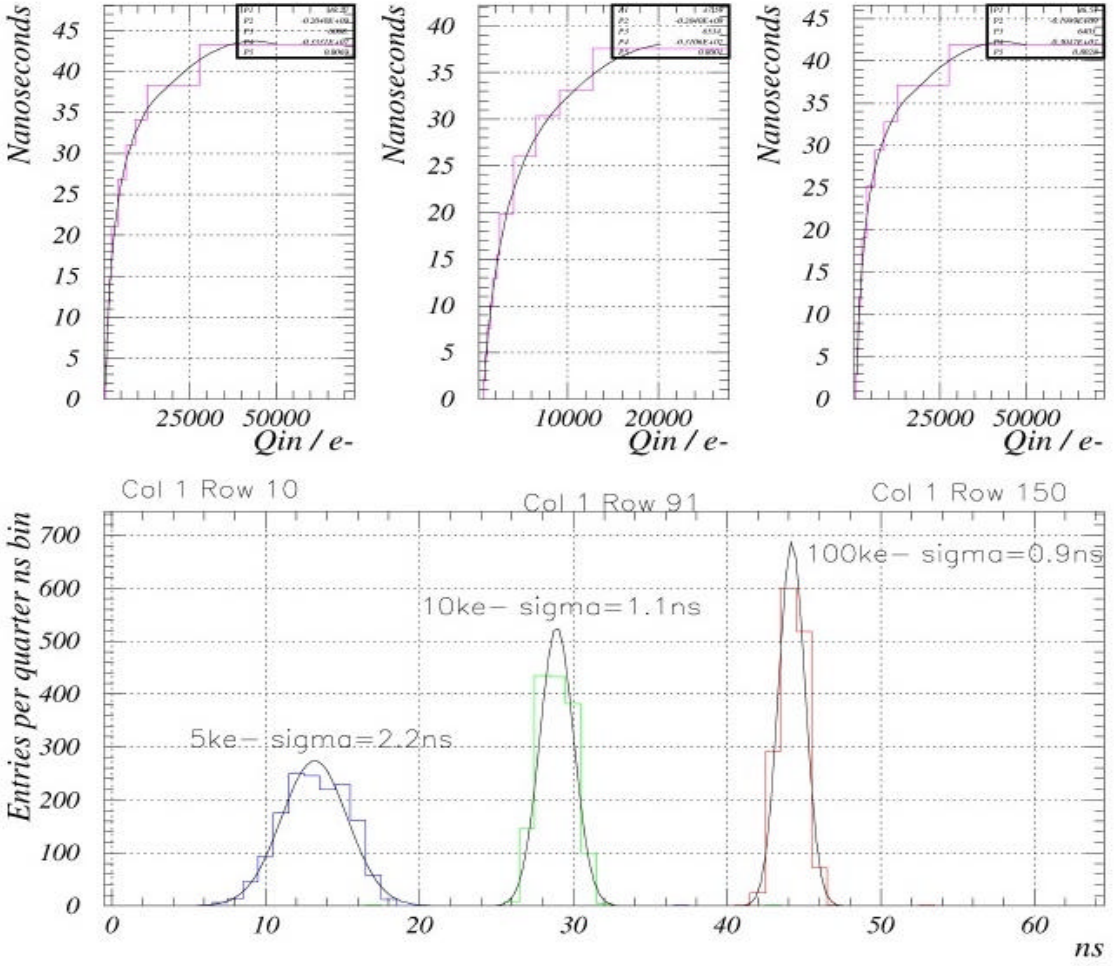




The Demonstrator Test System

The timewalk may be determined by establishing a 2-dimensional scan in which the relative timing of the charge-injection strobe and the level-1 trigger (strobe delay) forms the inner scan. The outer scan is formed by the magnitude of the injection pulse for which a range of 3ke- to 100ke- is used.

This plot illustrates a timewalk study for a single FE-B chip. The upper 3 curves show the discriminator response time versus input charge for 3 channels. In the lower plot there are 3 disributions of response time for 5ke-, 10ke- and 50ke- charge. The time dispersion is very good (~1ns) and the degree of timewalk is illustrated by the relative positions of these distributions on the time axis.



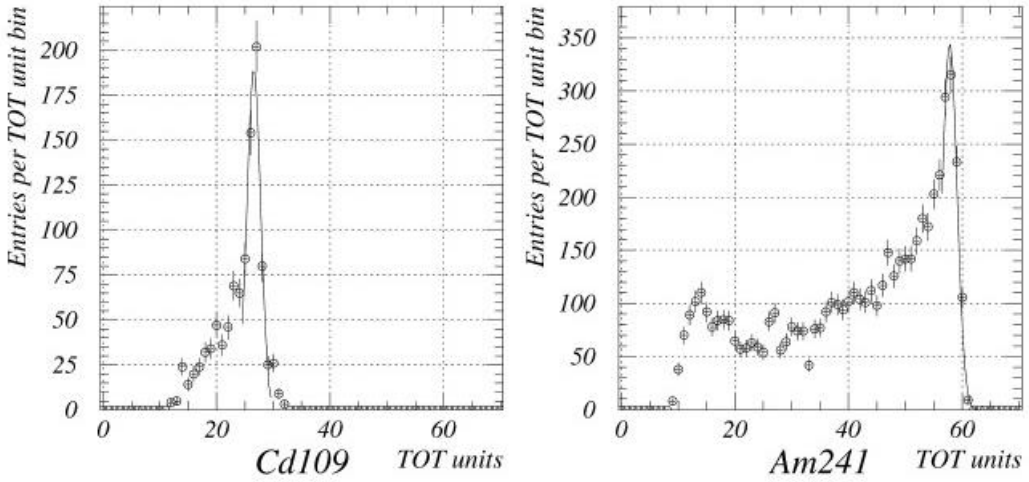
The Demonstrator Test System

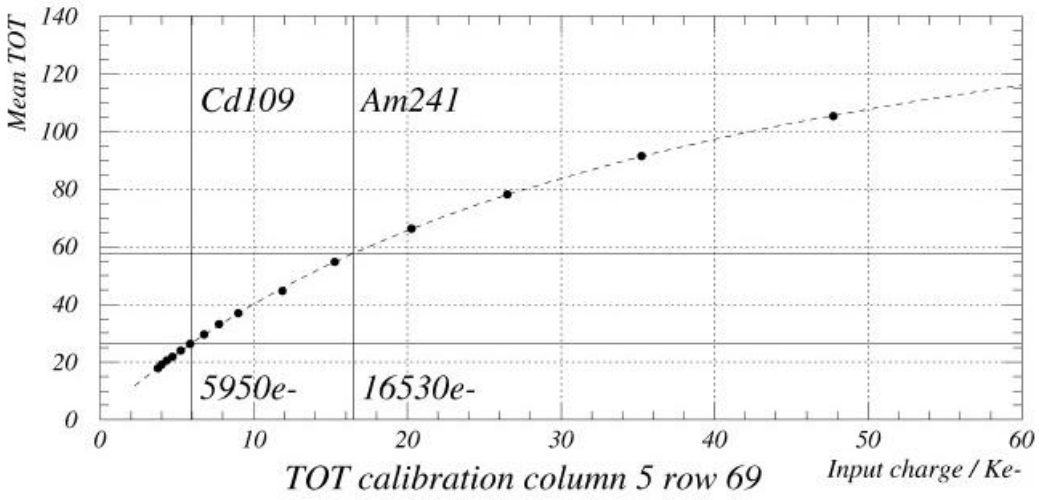
The external-hitbus triggering capability is taken advantage of to determine the absolute calibration, (i.e. the verify the injection capacitance magnitude). Photon sources such as Cd_{109} and Am_{241} are useful since a known discrete amount of energy is usually deposited in the silicon.

However this implies that there is no triggering mechanism available except for the fast-OR circuitry on the readout chips. The PLL receives these hitbus pulses and generates a programmable delay before issuing the requested number of contiguous level-1 triggers.

This plot shows spectra for 2 sources for an individual channel. The lower plot has the derived photopeaks superimposed on the TOT calibration curve for the same pixel showing a typical agreement of 5%.

Using this method the PLL system is capable of processing ~10^7 hits in <1hr whilst displaying the data on the GUI in approximate real time.





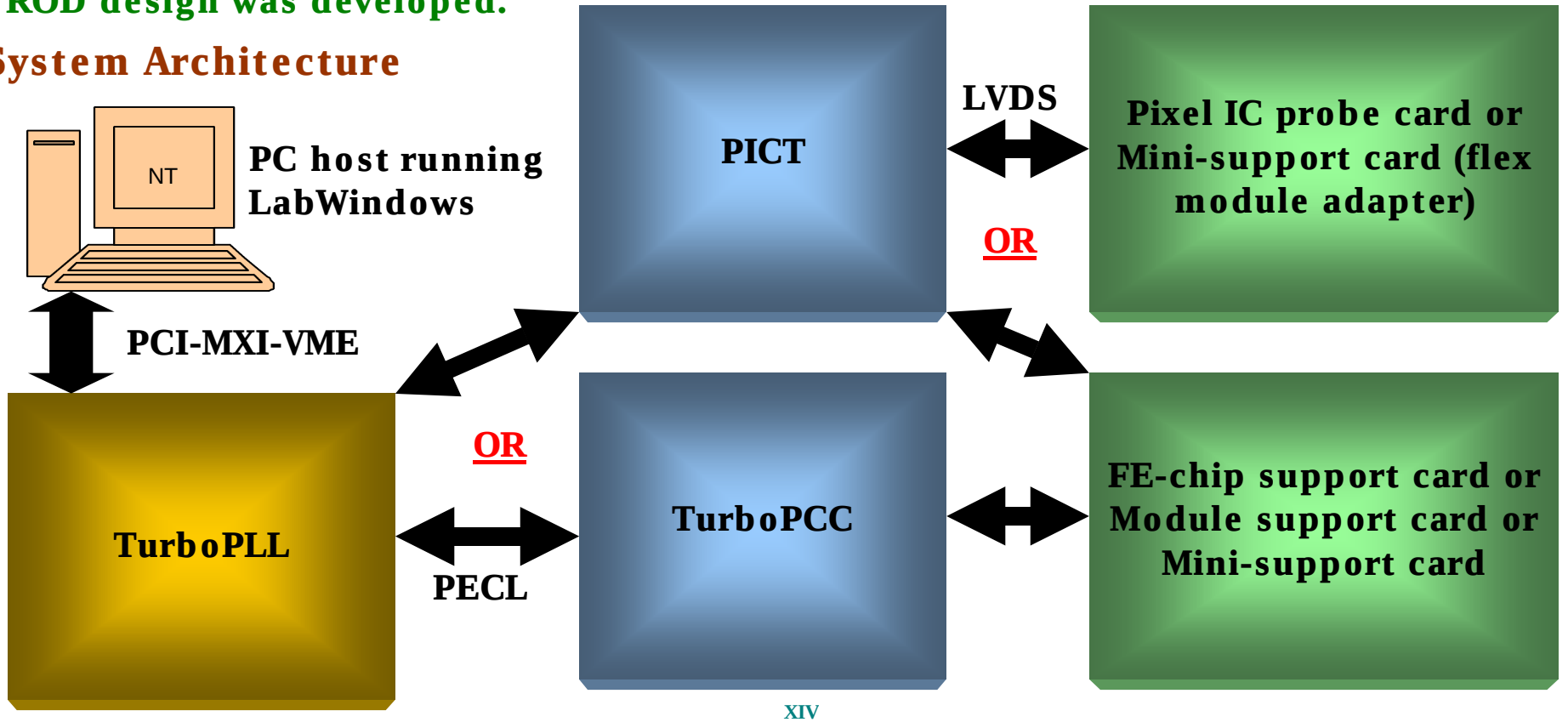
The TurboPLL Test System

Introduction

Progression into the radiation hard electronics realm introduces new requirements for our standard FE & module evaluation procedures. The TurboPLL system (currently being fabricated) was designed to address these requirements (amongst others).

Architecture is directly based upon the original PLL approach, which had proven so ideally tailored to our needs and which represents the model upon which the ATLAS ROD design was developed.

System Architecture



The TurboPLL Test System

The TurboPLL

Expectation that on-detector electronics will tend to slow with irradiation, therefore it is desirable to test die at elevated operation frequencies pre-irradiation in order to determine how likely they are to meet the specifications when they have been exposed to 50Mrads.

Principal upgrade to the PLL part of the test system was the introduction of a programmable clock generator offering a broad range of frequencies up to 100MHz.

This necessitated the implementation of two 512k-deep front-end FIFOs which serve to divorce the signal transmission and reception from the FPGA control clock (which always operates at 40MHz).

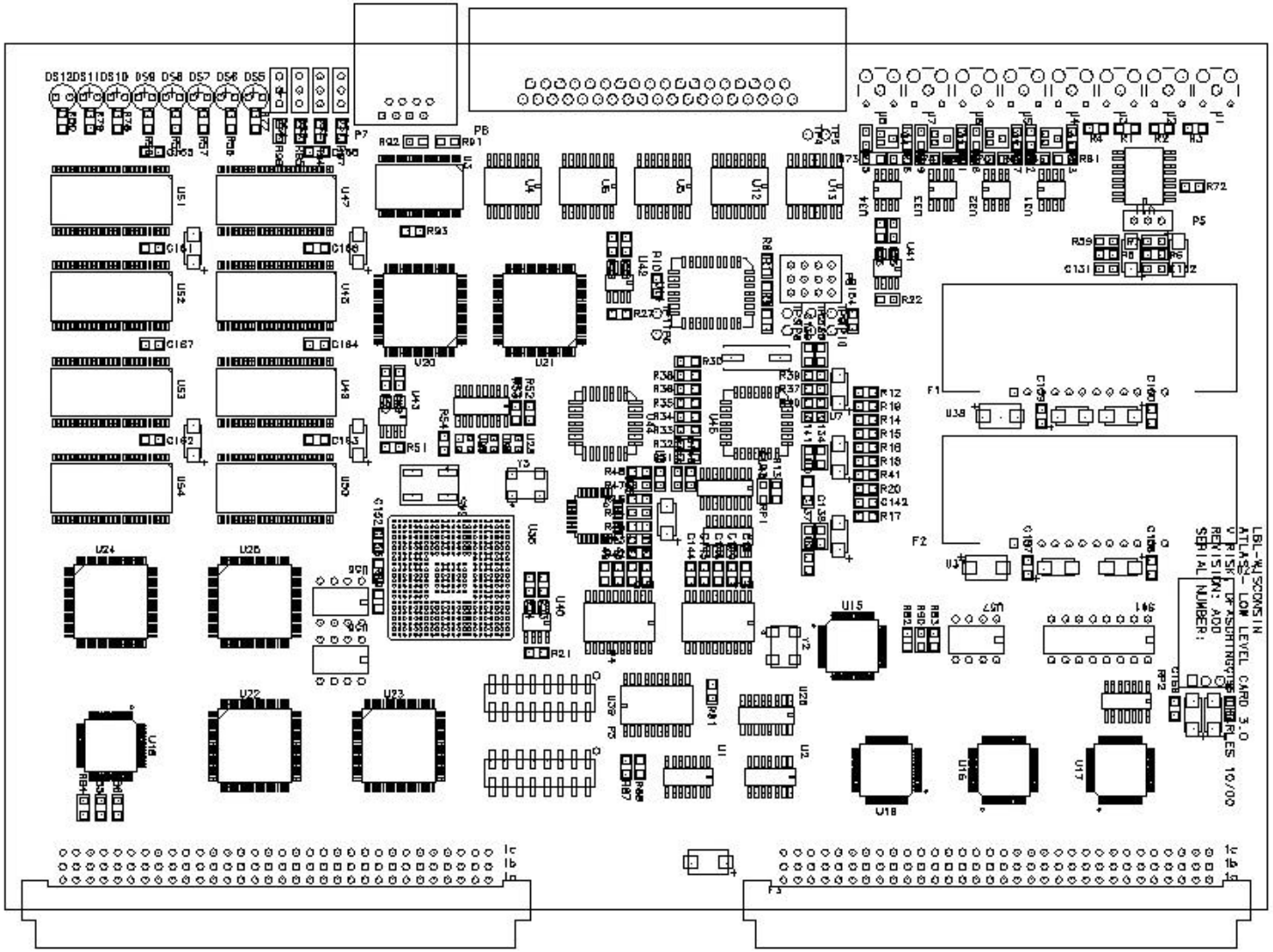
The FPGA itself has been upgraded to a much larger Xilinx part. Also the on-board histogramming capability has been upgraded by a factor 8 in order that data may be stored for an entire module at once. This will lead to a factor 2.7 improvement in analogue characterisation speed for 16-chip modules.

All of the front-end buffering has been upgraded with higher performance parts (with 0.5ns rise-time) to facilitate 100MHz operation.

Many other minor upgrades and improvements e.g. extra NIM inputs and outputs and support for the 2 data link output which is required for B-layer modules (previous incarnation only supported a single data link).

The TurboPLL Test System

TurboPLL Board Layout:



The TurboPLL Test System

The TurboPCC and PICT

The TurboPCC is designed to support the 100MHz maximum operation speed provided by the TurboPLL. As for the TurboPLL this required that all of the receivers/drivers be higher speed parts.

Other upgrades include;

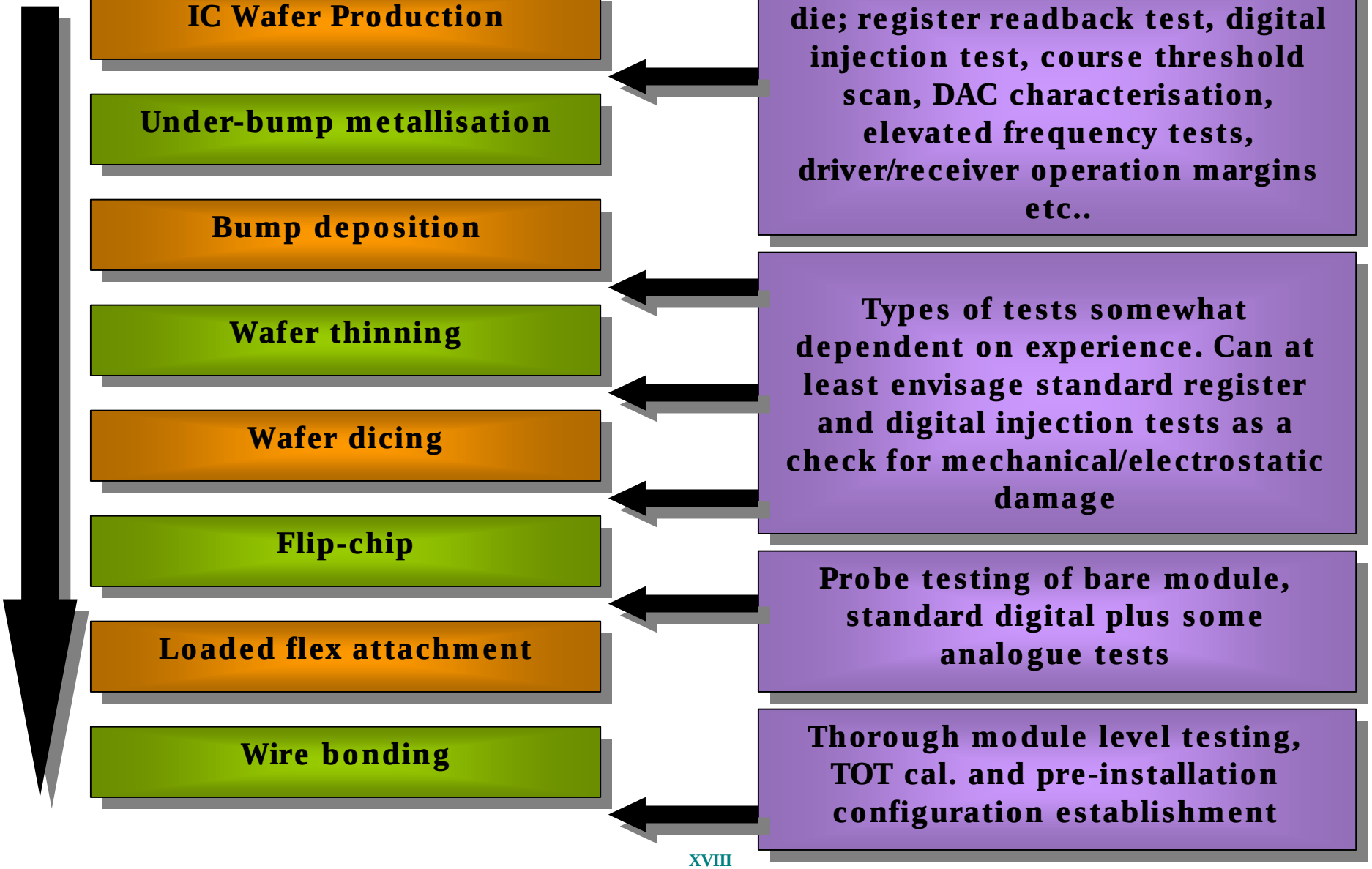
- **Higher performance FPGA controller**
- **Improved strobe delay support (broader range)**
- **Integrated chopper circuit for external charge injection**
- **Higher resolution VCAL DAC (14-bit) for improved granularity during threshold scans**

The PICT (Pixel IC Test card) is aimed towards highly detailed parametric testing of digital signals coming from, and provided to, the FE chips. Principally this capability would be applied at the bare wafer probe-test level to seek die which may be marginal in performance (which would otherwise appear OK with the usual set-up).

Provides the ability to vary several properties of downstream digital signals (timing and amplitudes) using a range of *Analog Devices* transceiver and delay chips (with 14-bit DACs for precise control). Also incorporates window comparitors to check the margins of upstream signals.

A comprehensive set of voltage and current monitoring ADCs is also included to test FE-DACs and automatically log power consumption etc. A temperature monitoring ADC is also installed to sample 10KΩ on-module NTC thermistors.

Production Module-Testing Plans



Conclusions

The original PLL test system has served the collaboration excellently. The concept was a very good match to the various requirements for FE IC testing and full scale module testing, particularly in terms of speed and versatility.

A wealth of experience has now been built up by many groups through the various FE-chip and module development stages and a second system (which is currently being fabricated) has been developed which is based on the original concept but includes many upgrades and improvements.

This new system will also be distributed to all of the collaborating institutes involved in IC/module testing and will form the new official set-up. To this end we plan to deliver 20 TurboPLLs, 5 PICTs and 15 TurboPCCs.

There are open questions relating to how testing should be conducted at the various points during module construction. The answers will become clearer as more experience is gained producing these multi-chip devices. The TurboPLL system is well suited to deal with the many possible requirements.