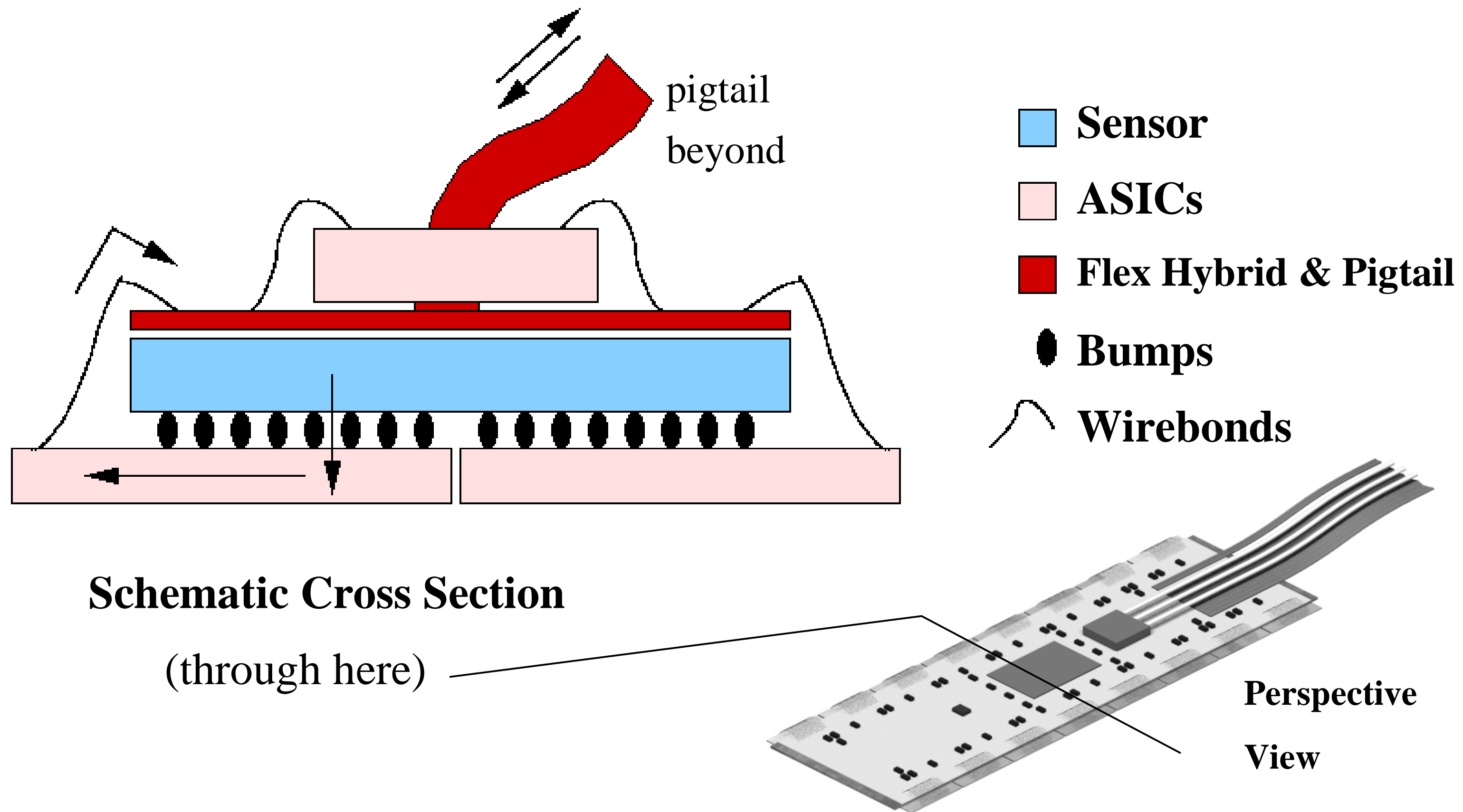
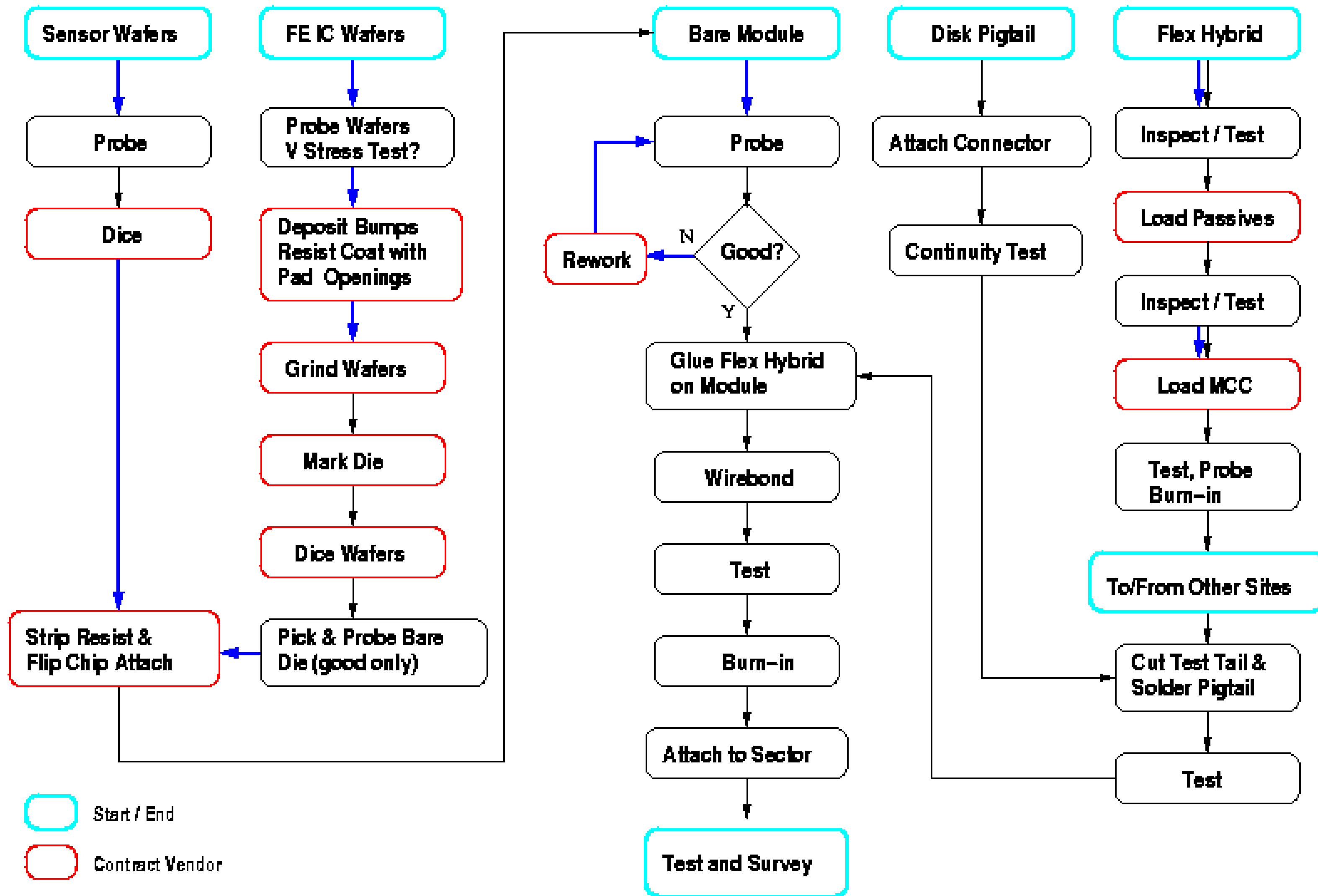
Module Assembly

WBS 1.1.1.5

- Pixel module anatomy
- Assembly Flow
- Individual pieces
- Production Plan and Rates
- Cost and Schedule Summary
- Development plans

The Pixel Module




U.S. Atlas Pixel Module Assembly Flow, Nov. 2, 2000
Sensor Wafers
Probe
Dice
Strip Resist &
Flip Chip Attach
FE IC Wafers
Probe Wafers
V Stress Test?
Deposit Bumps
Resist Coat with
Pad Openings
Grind Wafers
Mark Die
Dice Wafers
Pick & Probe Bare
Die (good only)
Bare Module
Probe
Good?
N
Y
Rework
Glue Flex Hybrid
on Module
Wirebond
Test
Burn-in
Attach to Sector
Test and Survey
Disk Pigtail
Attach Connector
Continuity Test
Flex Hybrid
Inspect / Test
Load Passives
Inspect / Test
Load MCC
Test, Probe
Burn-in
To/From Other Sites
Cut Test Tail &
Solder Pigtail
Test
Start / End
Contract Vendor
Overseas Shipping

FE IC Wafers and Die

- US to **thin** and **probe** wafers
- US to return **Known Good Die** (KGD) to bump vendors

When Do We Probe Wafers/Die?

- During development: after fab, bumping, thinning & dicing.
- After all yields are known can select best stage(s)
- Same setup used at all stages.
- Bumped wafers must be probabed (=> resist openings)
- Use CDF method for single die probing.

Bump Bonding

- Bump Bonding is a non-US responsibility.
- Includes deposition of **bumps**/**under bump metalization** on **FE IC**/ **sensor wafers** as well as flip chip assembly.
- STATUS:
  - **Two vendors** qualified via dummy and active prototypes (small qtty)
  - Both have handled 4" sensor and 6" IC wafers.
  - They have or are acquiring 8" wafer capability.
  - IZM and AMS to produce 2x50 dummy modules in 2001 (mechanically identical to production modules)
  - Active modules to be produced in 2001 as FE IC availability permits.
  - **Third vendor** being considered (only has 6" wafer capability => DMILL FE ICs).

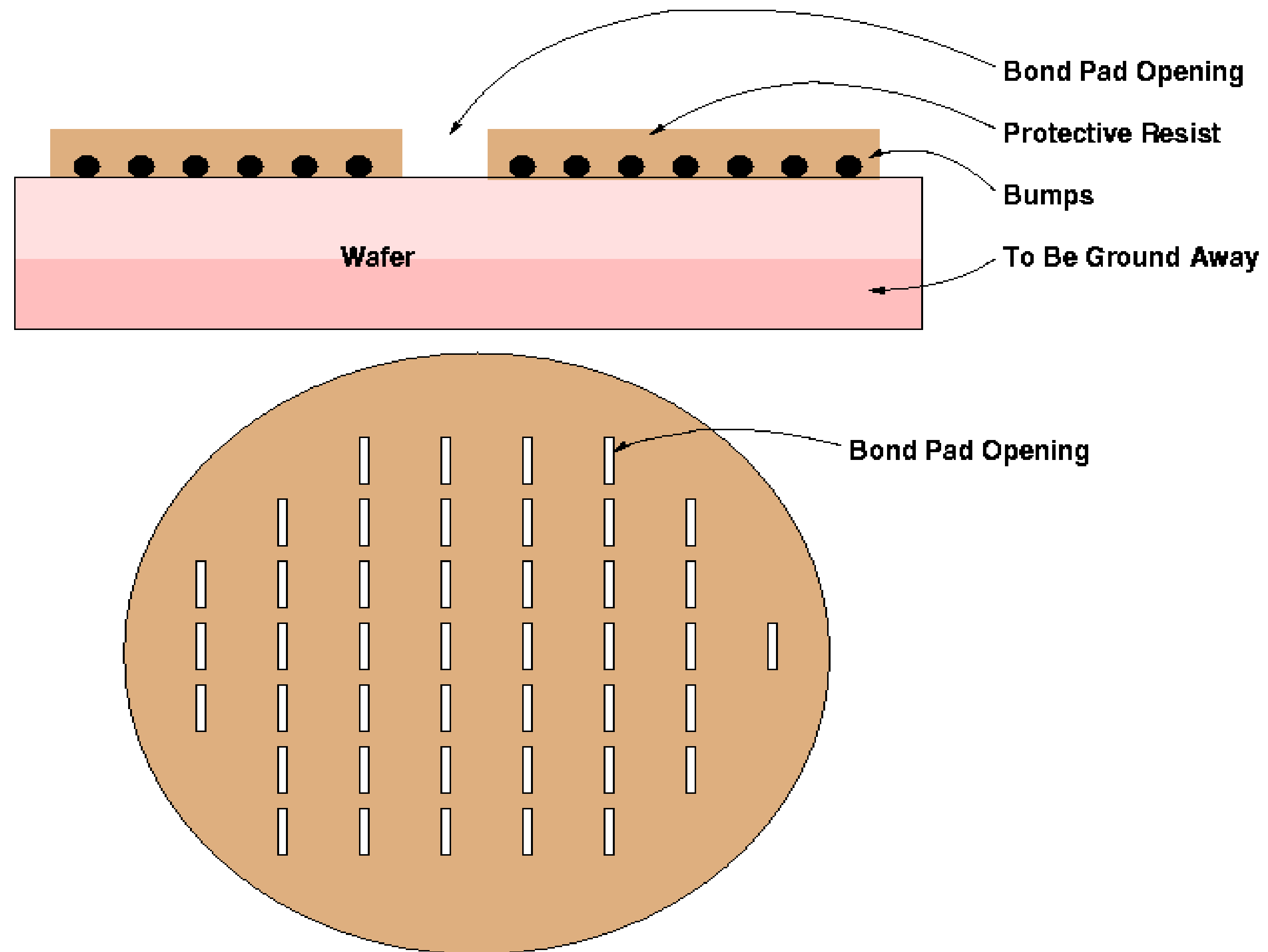
AMS (IT) – evaporative indium

IZM (GER) – solder bumps

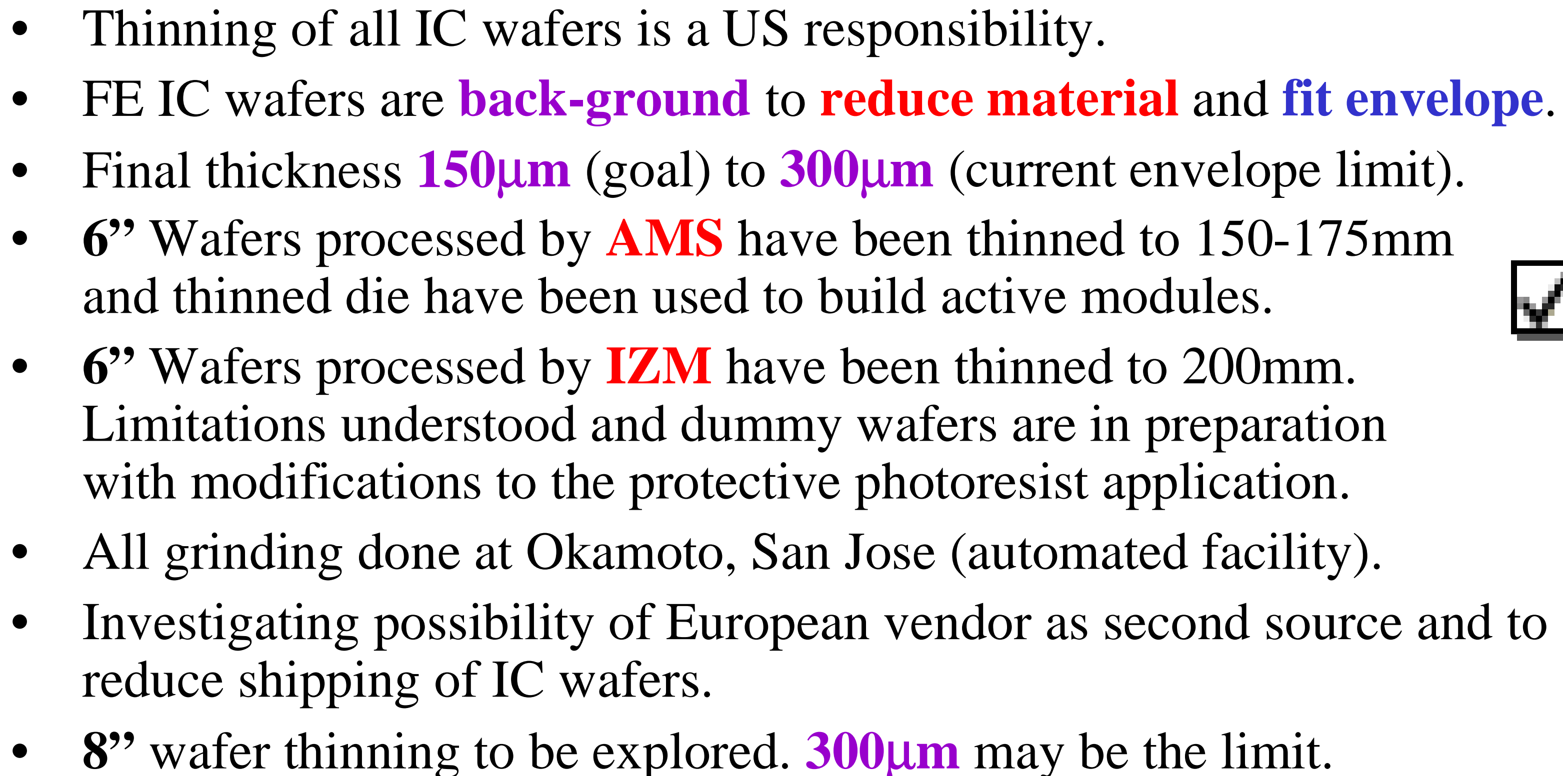
Sofradir – reflowed indium

- Projected production rate **40 modules/wk** (20 IZM + 20 AMS).

FE IC Wafer With Bumps



IC Wafer Thinning

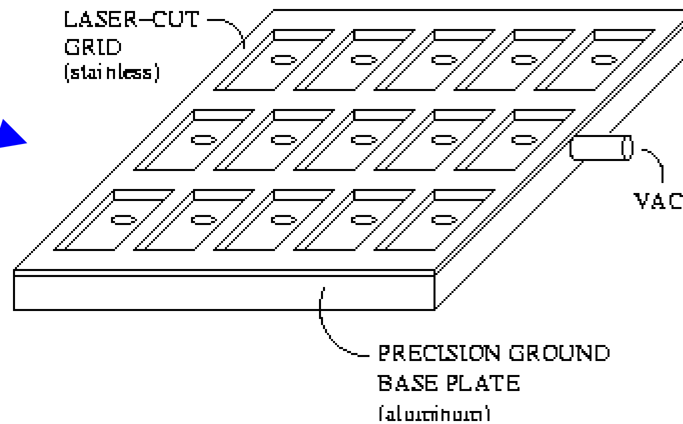


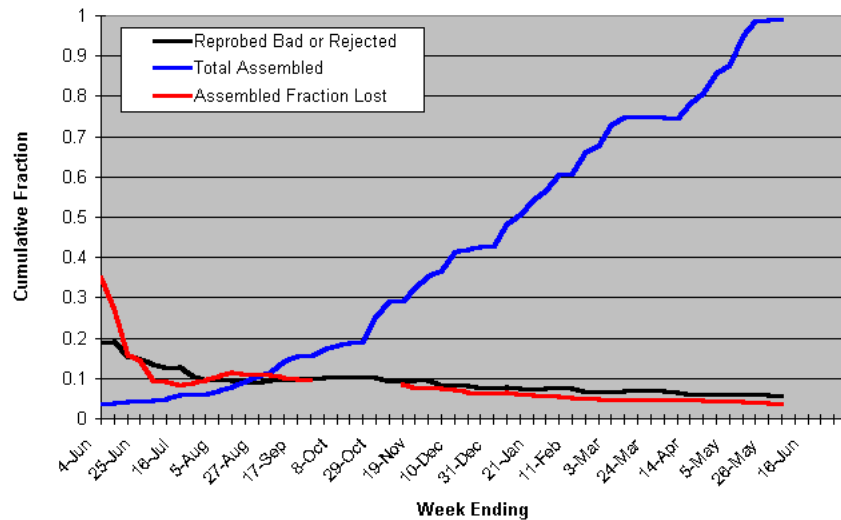
- Thinning of all IC wafers is a US responsibility.
- FE IC wafers are **back-ground** to **reduce material** and **fit envelope**.
- Final thickness **150µm** (goal) to **300µm** (current envelope limit).
- **6”** Wafers processed by **AMS** have been thinned to 150-175mm and thinned die have been used to build active modules.
- **6”** Wafers processed by **IZM** have been thinned to 200mm. Limitations understood and dummy wafers are in preparation with modifications to the protective photoresist application.
- All grinding done at Okamoto, San Jose (automated facility).
- Investigating possibility of European vendor as second source and to reduce shipping of IC wafers.
- **8”** wafer thinning to be explored. **300µm** may be the limit.

Single Die Probing

Fixture used to Probe 8,000

SVX3D chips for CDF



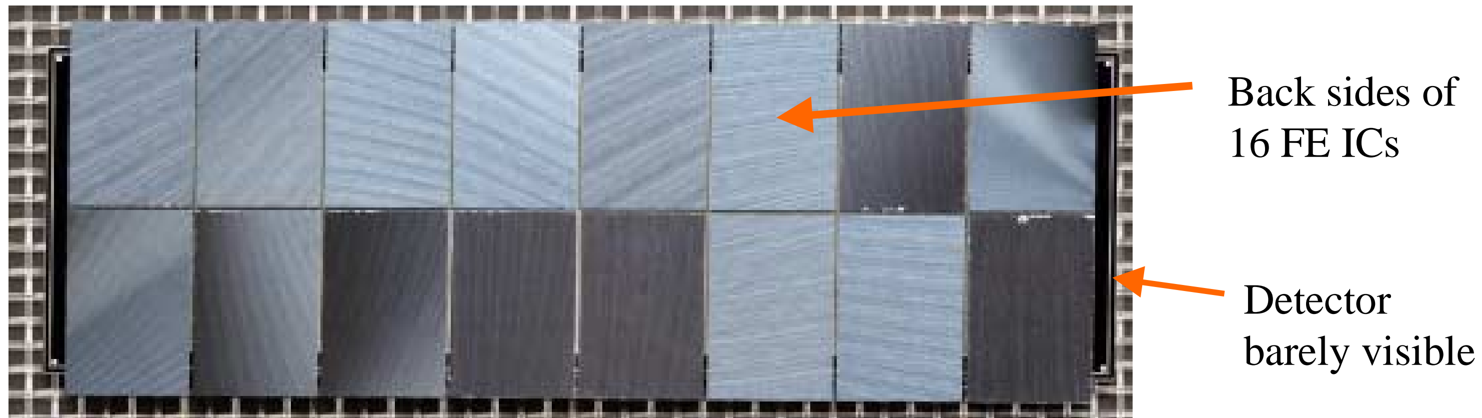


CDF Chip Probing

Results

Bare Modules

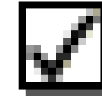
- **US to probe and accept for module assembly.**
- **Prepare to debug modules that fail probe.**
- **Must know identity of each die (marking under study).**
- **Assume returning to bump vendor or elsewhere for die replacement.**

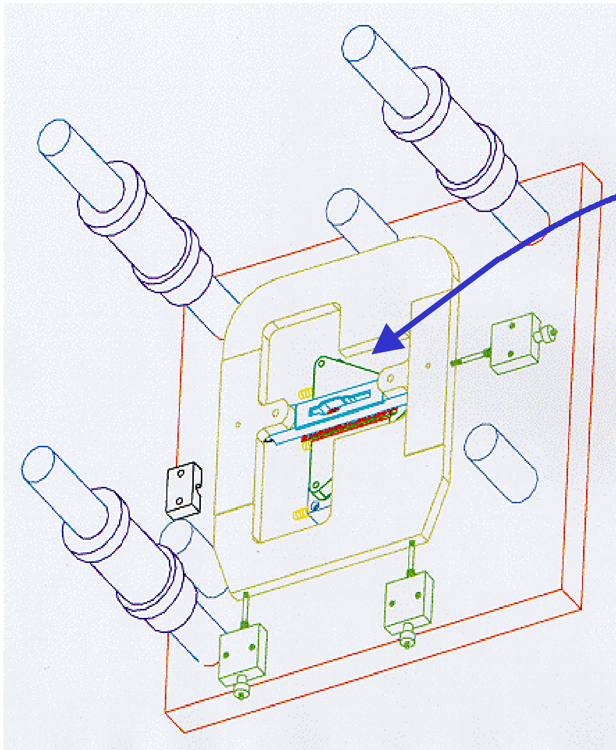


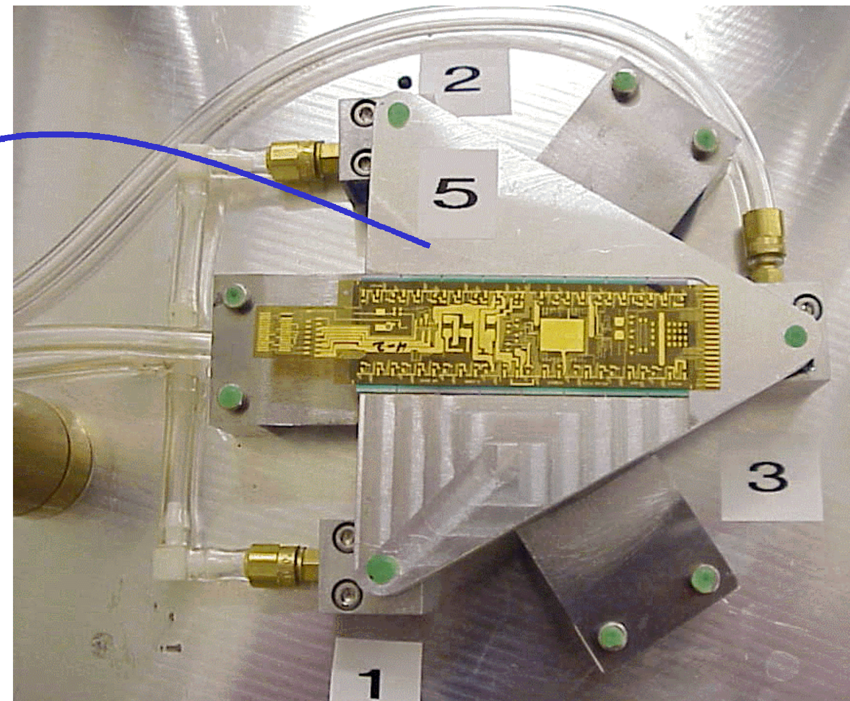
Flex Hybrid and Pigtail
(Covered in separate presentation)

- US to fabricate all flex hybrids and load passives.
- US to share MCC loading and test.
- US to fabricate and test all **disk** pigtails.
- Flex hybrid is **universal** up to module assembly.
- Customized for specific disk by adding pigtail before module assembly.
- Flex with pigtail must be Known Good Part.
  (tested all connections, MCC function, HV paths)

Mechanical Assembly

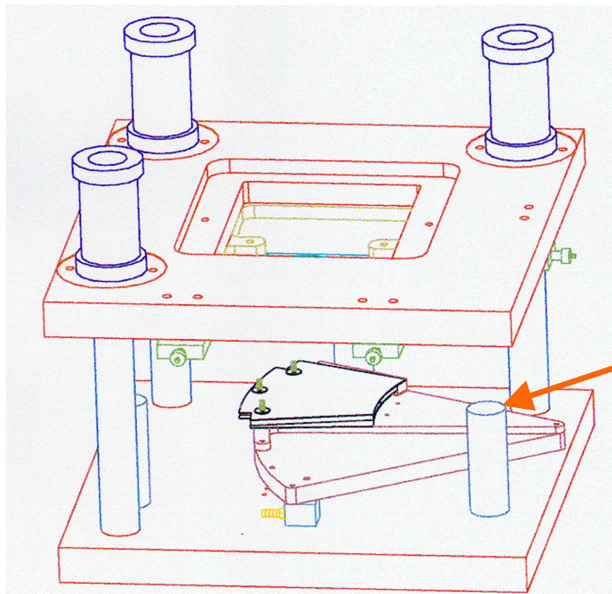
- **Prototype fixtures designed, built and tested** 

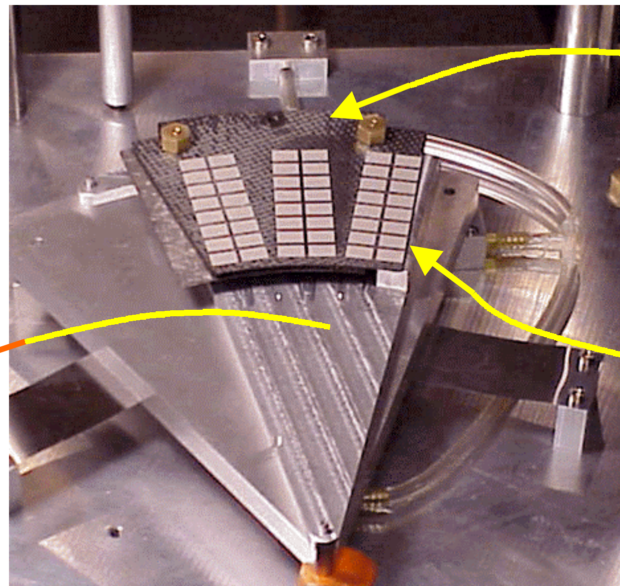




Assembly of Modules onto Sectors

- **Same base assembly as Module fixture.**
- **Prototyping advanced: techniques used to test prototype sectors.**





Carbon sector structure

Thermal compound for FE chips on module

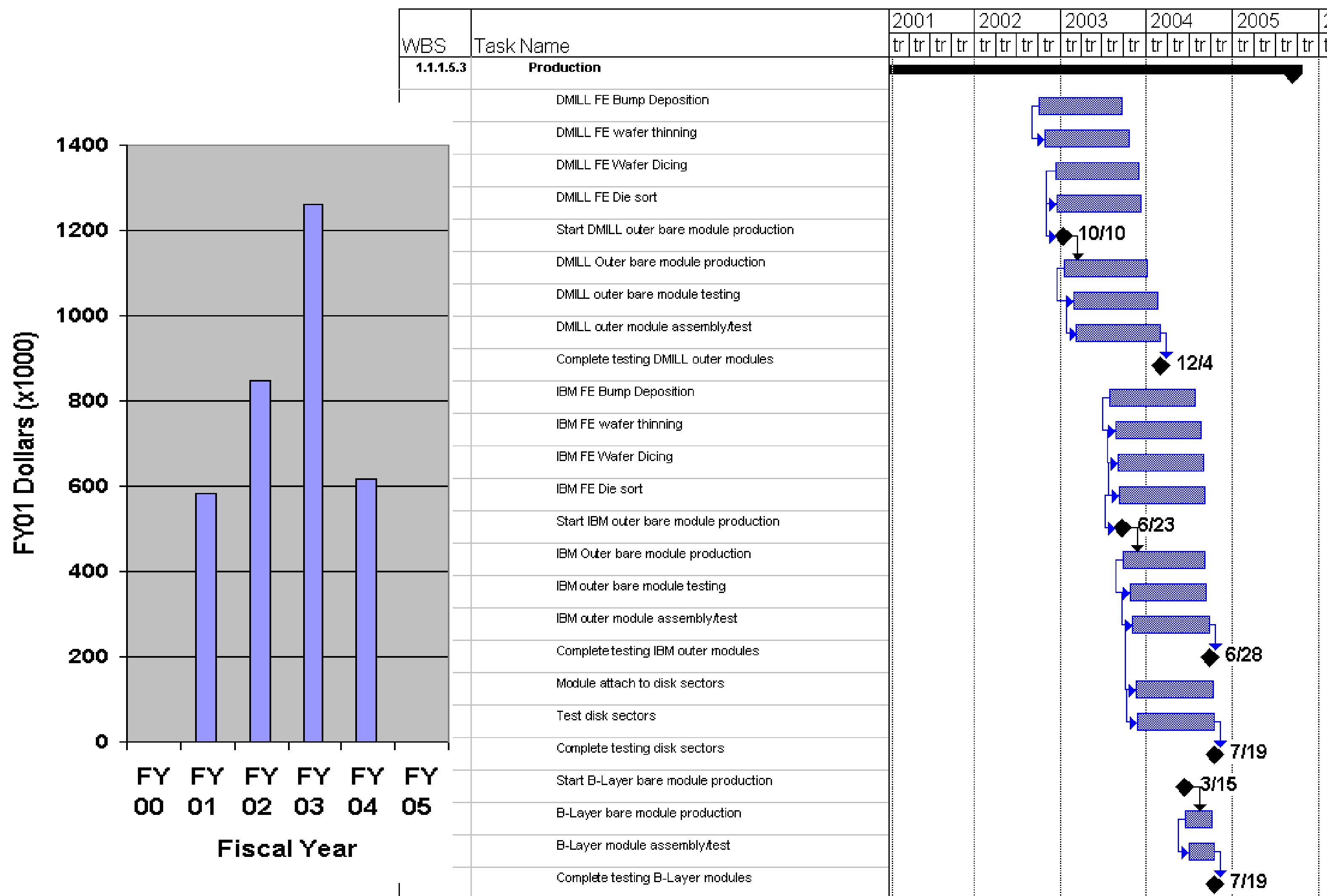
US Production Sites

- **Wafer/Die Probing: LBNL**
- **Wafer thinning**: **Okamoto** (Bay Area)
- **Wafer dicing**: **various qualified vendors** (Bay Area)
- **Die sort and mark**: **LBNL**
- **Bare module probing**: **LBNL**
- **Flex Hybrid Fab: Compunetics-type vendors TBD, CERN.**
- **Flex Hybrid assembly**: **Flex One, SMD, etc., Oklahoma.**
- **Module mechanical assembly(25% of total)**: **LBNL**
- **Module wire bonding**: **LBNL** and **Ohio State**
- **Module testing & Burn-In**: locations TBD, depending on availability of manpower and equipment (eg. wire bonding for repair) **LBNL** , **Ohio State** possible, **Oklahoma, New Mexico** under development.
- **Module attachment to disk sectors and test**: **LBNL**

US Production Rates

- Current scheduled bare module rate is **~6/wk** to **LBNL** (vendor projected capability is 10/wk)
- Planning **2 modules/day** probing & assembly capacity.
- Sector assembly now scheduled at **1/** 4-days but present fixturing capable of **1/** 2-days
- Module and sector assembly rates can be increased with more fixturing
- Plan for test and burn-in capacity to **exceed** assembly rate within cost constraints, because test capacity is not so readily expandable.

WBS 1.1.1.5.3 **Production Schedule**



U.S. ATLAS E.T.C. WBS Profile Estimates

Funding Source: All
Funding Type: Project
10/24/00 2:31:52 PM
Institutions: All

WBS Number	Description	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	FY 05 (k$)	Total (k$)
1.1.1.5	Module Assembly/Test	0	0	194	282	420	206	0	1102
1.1.1.5.1	Design/Engineering	0	0	82	96	14	0	0	191
1.1.1.5.1.1	Prototype Design	0	0	0	0	0	0	0	0
1.1.1.5.1.2	Production Design	0	0	0	0	0	0	0	0
1.1.1.5.1.3	Testing Design	0	0	82	96	14	0	0	191
1.1.1.5.2	Development and Prototypes	0	0	112	122	46	0	0	280
1.1.1.5.2.1	X-ray Inspection	0	0	6	6	6	0	0	17
1.1.1.5.2.2	Wafer Thinning	0	0	0	0	0	0	0	1
1.1.1.5.2.3	Wafer Dicing and Die Sort	0	0	1	3	2	0	0	6
1.1.1.5.2.4	Module Assembly and	0	0	84	83	30	0	0	196
1.1.1.5.2.5	Module Attachment	0	0	22	30	8	0	0	60
1.1.1.5.3	Production	0	0	0	65	360	206	0	631
1.1.1.5.3.1	IC Wafer Thinning	0	0	0	0	2	2	0	3
1.1.1.5.3.2	Dicing of IC Wafers	0	0	0	0	12	12	0	25
1.1.1.5.3.3	IC Die Sort	0	0	0	3	51	4	0	58
1.1.1.5.3.4	Module Assembly	0	0	0	17	108	48	0	173
1.1.1.5.3.5	Module Testing	0	0	0	45	138	63	0	245
1.1.1.5.3.6	Module Attachment	0	0	0	0	12	39	0	51
1.1.1.5.3.7	Sector Electrical Testing	0	0	0	0	25	35	0	60
1.1.1.5.3.8	Production database	0	0	0	0	12	3	0	16

Development Areas

- FE Wafers: Probe bumped, Thin 8", Mark die,
  Stress test (wafer burn-in), Dummy wafers.
- Electrical Probing: Flex hybrid, Bare module.
- Flex Hybrid: Fab. Sources, Wirebonding.
- General: Assembly line issues (Q.C., monitoring, etc.),
  Use dummy modules to address mechanical issues.