WBS 1.1.1.3 Pixel Electronics

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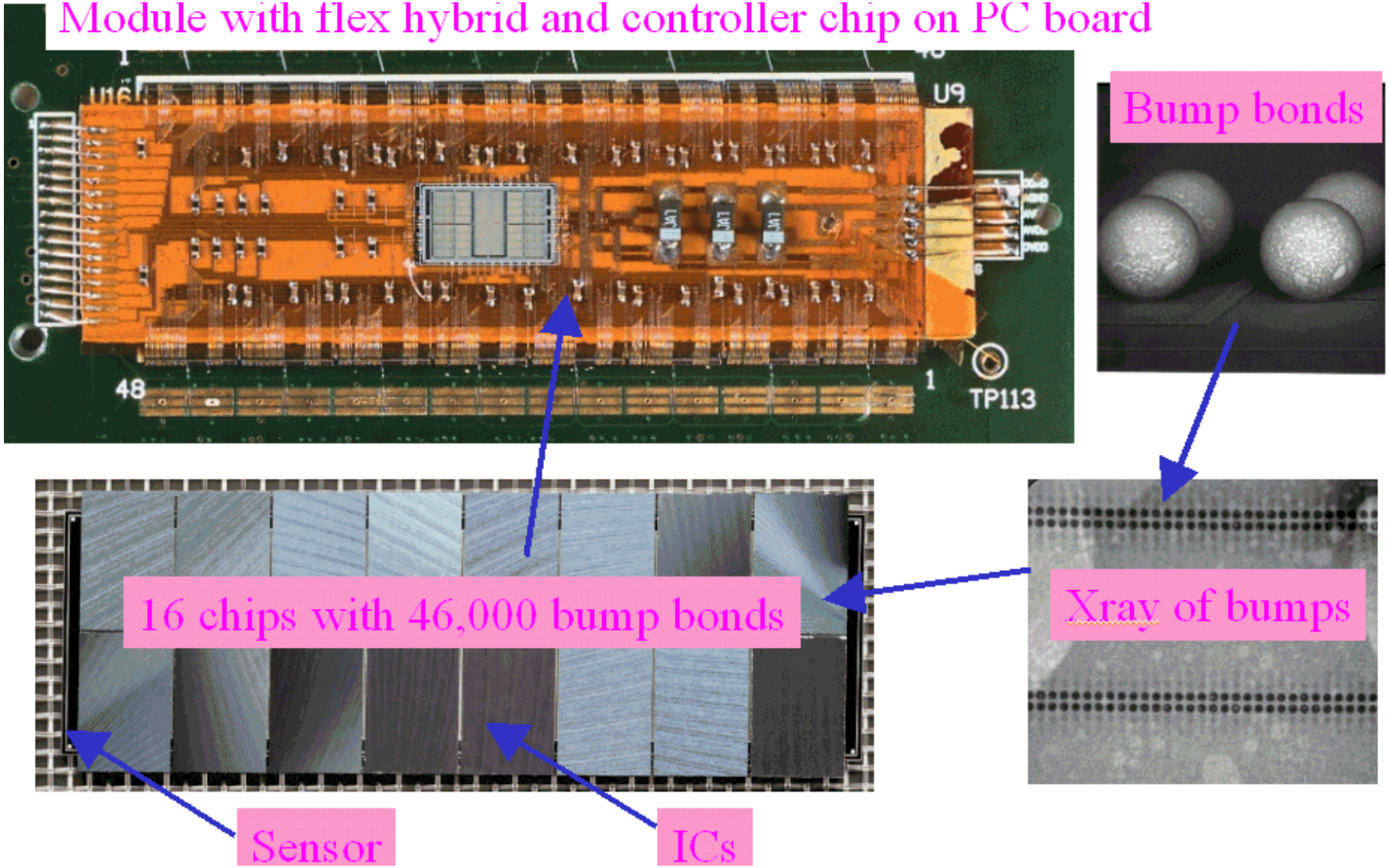
- Overview of Electronics System Design
- Initial Rad-soft Prototypes
- Rad-hard Conversion Program
- Deep Sub-Micron Conversion
- Testing (see also talk of J. Richardson)
- US Roles, Basis of Estimate, Cost and Schedule
- Summary

Overview of On-Detector Electronics

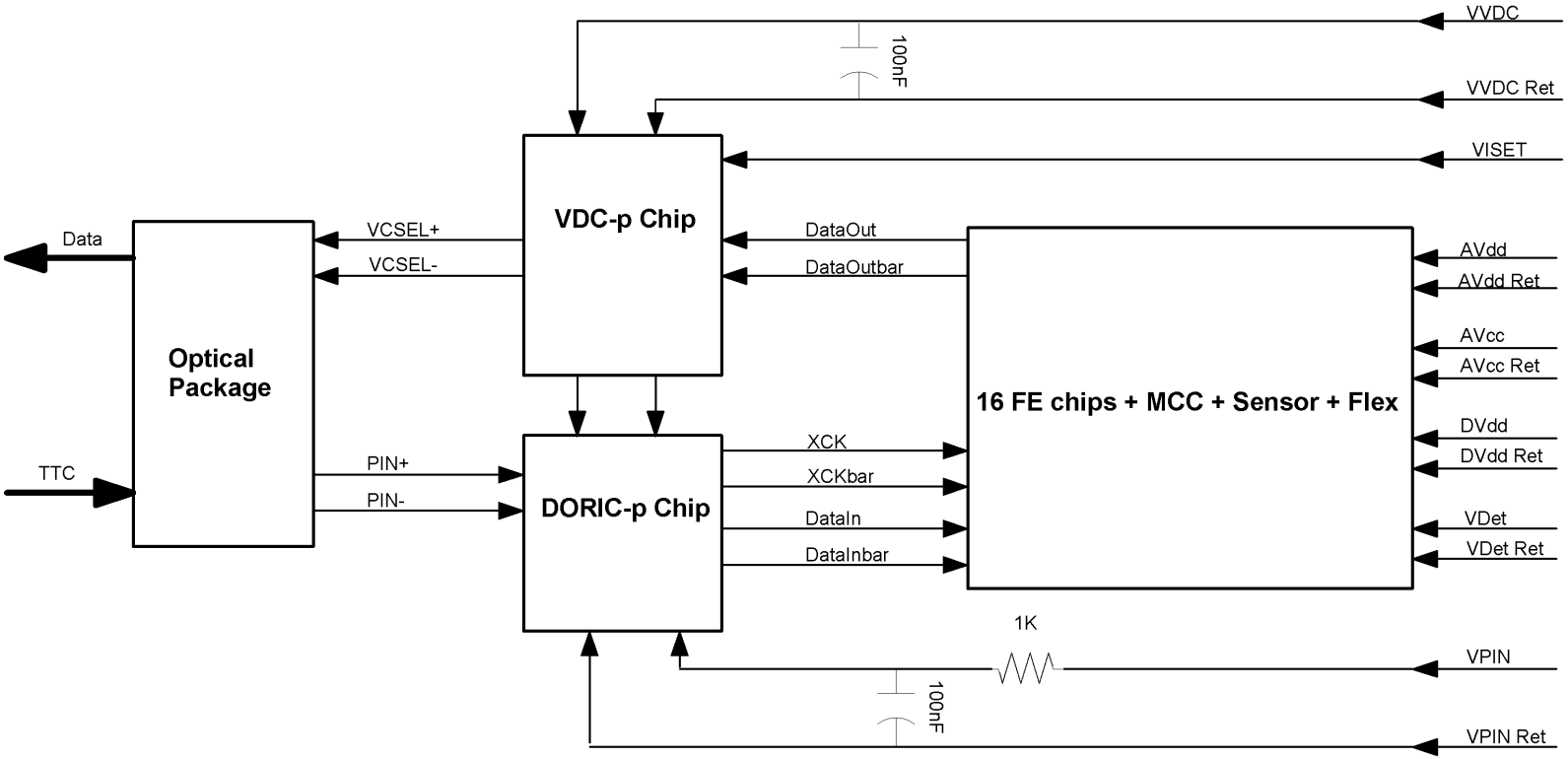
Basic building block is Pixel Module:



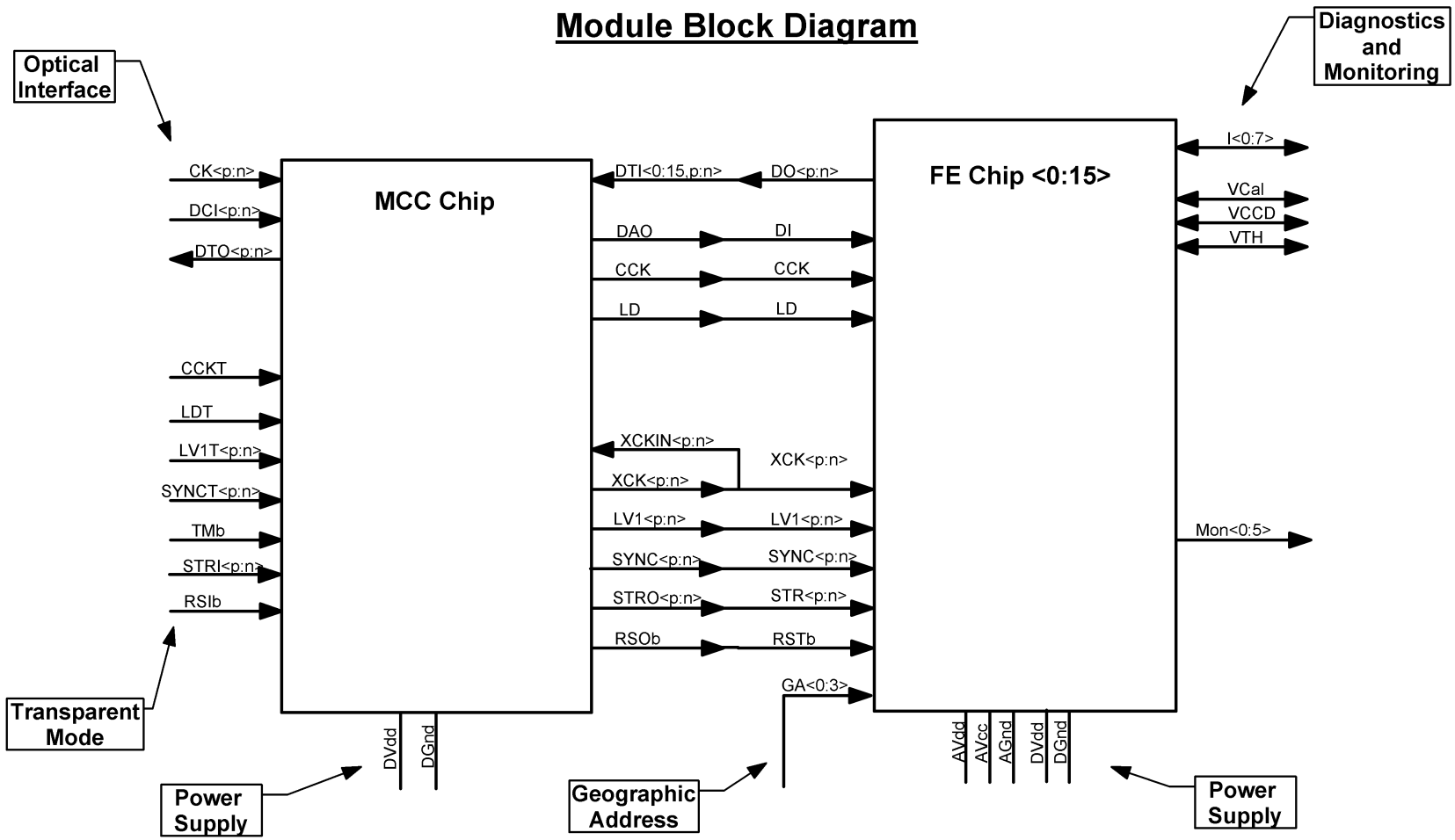
- Active area is 10cm^2, 46K channels, 16 FE on sensor substrate, and MCC chip.

Electronics components of pixel module:

- **Front-end chip:** Sixteen 7.4x11.0mm die per module, each containing 2880 pixels of size 50μ x 400μ, plus control of internal biassing and readout circuitry.
- **Module Controller chip:** assembles data from 16 FE chips into single event, and provides module level control functions and interface to opto-electronics.
- **Opto-electronics:** Driver for VCSELs used to transmit data stream to USA15 (VDC-p) and decoder for clock and command stream from USA15 (DORIC-p).
- **Power Distribution:** Six supplies and one control voltage provided from USA15.



Connections inside of Bare Module (MCC+FE+Sensor only):



- Interface to outside uses serial in, serial out, and 40 MHz clock.
- Only slow control uses CMOS signals. All critical connections use LVDS protocol.
- No analog signals are required between chips. FE chips have internal reference and 8-bit DACs to adjust front-end bias currents and calibration charge.

Overview of Off-Detector Electronics (WBS 1.1.3)

Basic Concepts:

- RODs are detector-specific 9U VME64x modules in USA15 which provide event data on 1.6Gb/s S-links to the ATLAS DAQ (ROB = ReadOut Buffer).
- Common design effort for SCT/Pixels, including LBL, Iowa, and Wisconsin in US, plus Cambridge, Oxford, and UCL in UK. Design is based on strengths of pixel test systems, and closely integrated with on-detector electronics system design.

Components (ROD crate = 16 ROD/BOC plus TIM and RCC):

- **ROD (ReadOut Driver):** Receives data from up to 32 pixel modules (limited by output S-link bandwidth), and builds this into ATLAS event fragments. Provides clock and control support for pixel modules, with extensive list processing capability. Supports local calibration (including fitting) and data monitoring (with possible synchronization or re-initialization on the fly) using fast DSPs.
- **TIM (Timing and Interface Module):** Accepts timing and control information from ATLAS TTC system and distributes it over ROD Crate Backplane. Accumulates BUSY status from RODs and generates crate-level BUSY.
- **BOC (Back of Crate Card):** Includes opto-electronics for interfacing to pixel modules, including all timing adjustments, and S-link for transmission to DAQ.
- **RCC (ROD Crate Controller):** Crate processor for all DAQ/DCS needs.

On-Detector Electronics Ingredients

- **Pixel Array (Bonn/CPPM/LBL):** FE chip of 7.4 x 11.0mm die size with 7.2 x 8.0mm active area. The chip includes a serial command decoder, Clock, LVL1, and Sync timing inputs, and serial 40 Mbit/s data output. The set of hits associated with a particular crossing is "requested" by sending a LVL1 signal with correct latency. FE chip then transmits corresponding digital hits autonomously.
- **Module Controller (Genova):** Collects data from 16 FE chips and implements a silicon event builder. Performs basic integrity checks and formats data, also implements robust module level command/control. FE chips on module connect to MCC in star topology to eliminate bottlenecks and increase fault tolerance. Output is configurable from one 40 Mb/s up to two 80 Mb/s streams.
- **Opto-link (OSU/Siegen/Wuppertal):** Multiplexed clock/control sent over 40 Mbit/s link to module, data is returned on one or two 80 Mbit/s data links. Transmitters are VCSELs, receivers are epitaxial Si PIN diodes. Basic link is 5x5x1.5mm package, connected to VDC-p and DORIC-p optolink chips which have LVDS interfaces. The fibers are rad-hard silica core multi-mode fiber from Fujikura.
- **Power Distribution:** Significant ceramic decoupling on module. Flex pigtail used to reach patchpanels on end of detector (PP0). Then Cu Flex (HV + signals) plus twisted round Al (LV power) to endcap wall (2.5m, PP1) and gap region (3m, PP2). Followed by conventional cables to muons (PP3) and USA15 cavern. Additional filtering/protection components are placed on some patchpanels.

Status of Opto-electronics and Opto-links:

- OSU converted SCT design from AMS bipolar to DMILL CMOS, and simulated at schematic level. Siegen did layout, further simulations. Chips included in FE-D1 submission, and extensively tested. Several errors found in DORIC-p preamp and DLL which prevent useful operation. All known problems fixed in FE-D2 run.

Irradiation issues for opto-links:

- Collaborative effort of SCT and pixels (Wuppertal from pixels) have performed systematic irradiation studies of optical fibers and opto-elements (PINs and VCSELs) up to pixel fluences. Results show no significant risks, provided PIN is operated with adequate bias voltage (up to about 7V), and provided VCSELs are operated with sufficient bias current (up to about 20mA).
- Only major issue is single event upsets caused by interactions in the very thin epitaxial layer of the PIN diode. Irradiations at PSI this Spring clarified the magnitude of this effect, and it is quite serious. Spec for link pre-rad has BER of 10^{-12}, and during full-fluence BER of as high as 10^{-8} for B-layer is seen. SEU errors modeled, and cause single command bit errors and localized clock jitter.
- Have significantly upgraded the MCC command set to be highly fault tolerant. Commands are successfully decoded under any single bit error. Critical LVL1 command is lost with double error, mis-interpreted with triple error.
- FE-D1 version of VDC-p irradiated up to 50 MRad and works (with bias changes).

Power Distribution:

- ATLAS ID has chosen to operate detectors by placing all power supplies in USA15 (or US15) to allow use of standard commercial components.
- Major disadvantage is very long (up to 140m) cable runs required. Careful attention to engineering/prototyping of the power distribution system needed!

Concepts include:

- Single point grounding inside tracking volume with floating power supplies.
- Treatment of supply/return for supplies as low-impedance transmission lines (broad-side coupled pairs on Flex cables, twisted pair in conventional cables).
- Filtering (common-mode chokes and large capacitors) at PP3 to isolate detector from pickup going from USA15 to detector. Transient protection and more filtering at PP1 to isolate modules from voltage surges that could kill electronics.
- Global (entrance level) decoupling with 1206 high density ceramics, and local (chip level) decoupling with 0402 high density ceramics on Flex hybrid. All digital and analog supplies are filtered. Material and envelope requirements are strict.
- Flex components selected. First radiation tests done this Spring at PS, with good results. Not yet clear whether design is adequate (noise/grounding/stability, etc.)
- Major issue is full system-level prototyping to validate concepts and performance. This requires working modules, cable prototypes, and noisy environments.

Electronics Challenges in FE Chips and Requirements

- Operate properly after total dose of 50 MRad (nominal ATLAS 10 year dose). Also cope with expected leakage currents from sensors of up to 50nA per pixel.
- Operate with low noise occupancy (below 10^{-6} hits/pixel/crossing) at thresholds of 3Ke with low timewalk to have "in-time" threshold (hit appears within 20ns) of about 4Ke . Requires low threshold dispersion (< 200e) and low noise (< 300e).
- Associate hits with 25ns beam crossing, including effects of timewalk in front-end, digital timing on FE chip, clock distribution on module, and timing of modules.
- Meet these specifications with a nominal analog power budget of about 40μW/ channel and a nominal total power for the complete FE chip of about 200mW.

Features of final design:

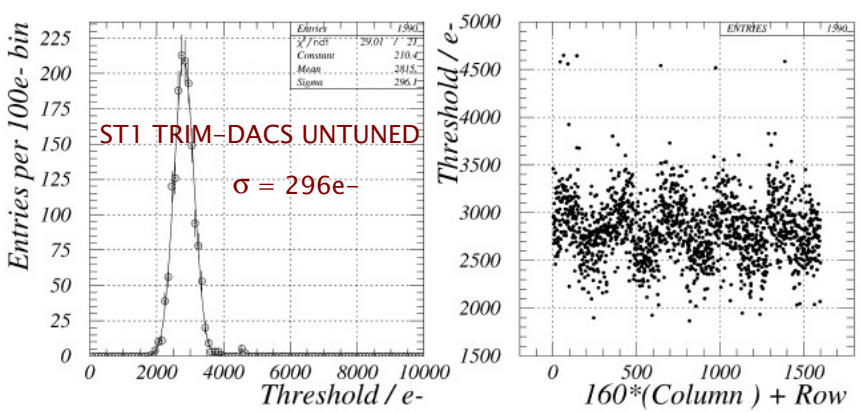
- Preamplifier provides excellent leakage current tolerance and relatively linear time-over-threshold (TOT) behavior via feedback bias adjustment.
- Discriminator is AC-coupled, and includes 3-bit trim DAC for threshold vernier.
- Readout architecture uses distributed 7-bit timestamp bus, and leading-edge plus trailing-edge latches in each pixel to define times of LE and TE.
- Asynchronous data push architecture used to get data into buffers at the bottom of the chip, where they are stored for the L1 latency, after which they are flagged for readout or deleted. Chip transmits Trigger/Row/Column/TOT for each hit.

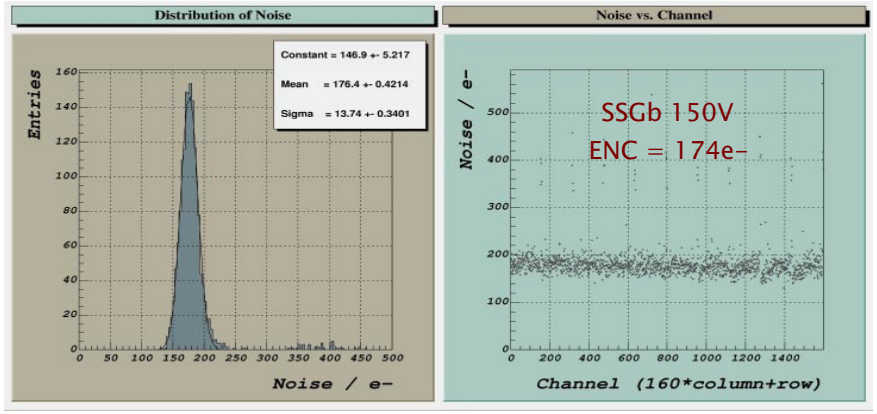
Rad-soft Demonstrator Program

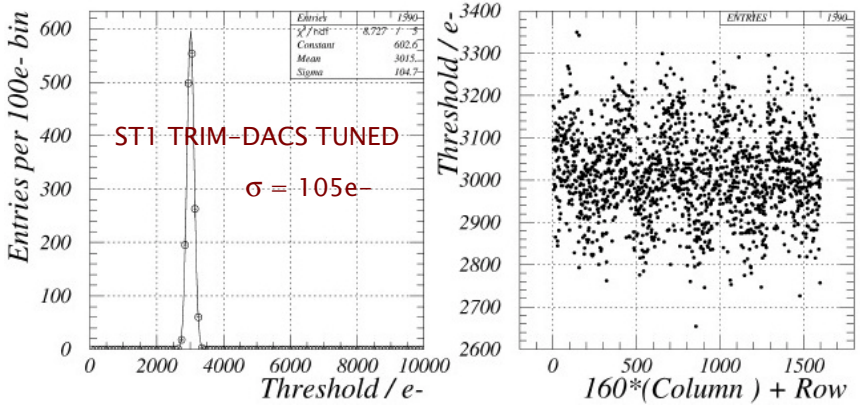
- In 1997, we agreed on overall design specifications for the FE and MCC chips necessary to implement this module design in a prototype form. We decided to pursue two prototypes for the FE chip. This was based partly on history and partly on the goal of submitting designs to two different rad-hard vendors.
- One was called FE-A, and was designed for submission to AMS 0.8μ BiCMOS. This process was viewed as a prototype vehicle for DMILL. The chip was submitted in Oct. 97, and testing began in Jan. 98. A second, purely CMOS version, FE-C, was submitted in May 98. This chip has 880K transistors.
- The second was referred to as FE-B, and was designed for submission to HP 0.8μ CMOS. This process was viewed as a prototype vehicle for Honeywell. This chip was submitted in Feb. 98, and testing began in Apr. 98. This chip has about 850K transistors. Almost all results to date are based on 20 wafers of FE-B, which had an average yield of about 92% after thorough digital/analog testing.
- A DMILL prototype matrix (no EOC, simple readout) called MAREBO was also submitted in Jul 97 and tested in Jan 98, to verify the FE design in DMILL.
- The MCC was submitted in May 98, along with FE-C, returned in late summer.
- All of these chips contain minor errors, but in all cases their functionality was quite close to the submission goals. Extensive lab testing and testbeam studies have been carried out on all chips. Excellent performance has been achieved.

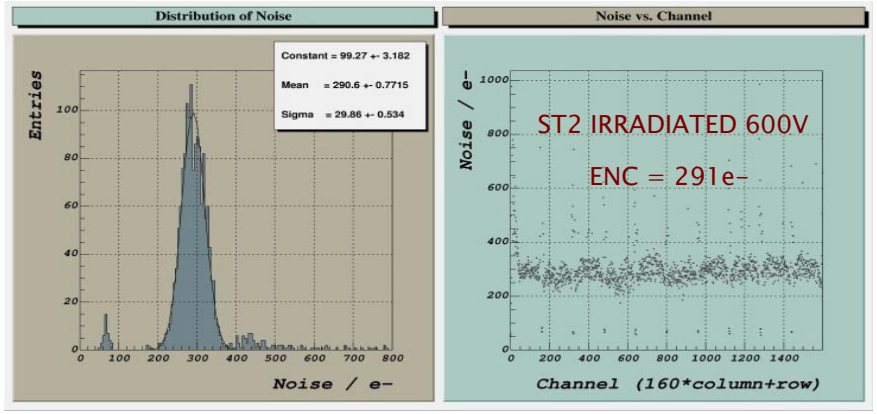
Lab Measurements

Examples of threshold and noise behavior in single chips:



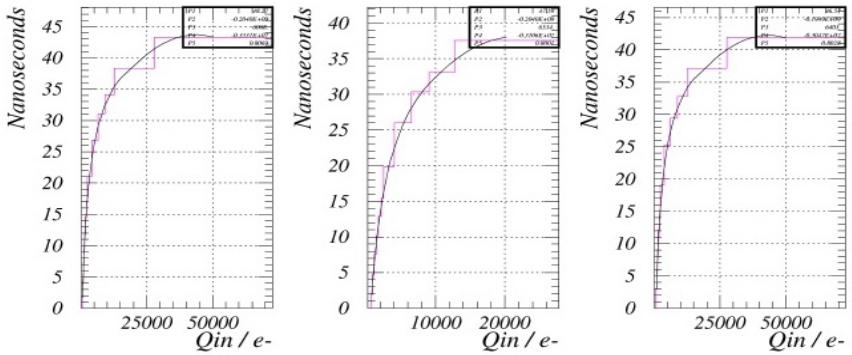


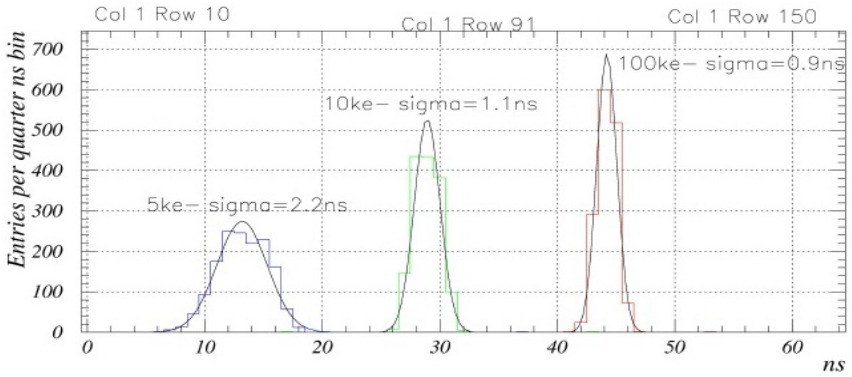




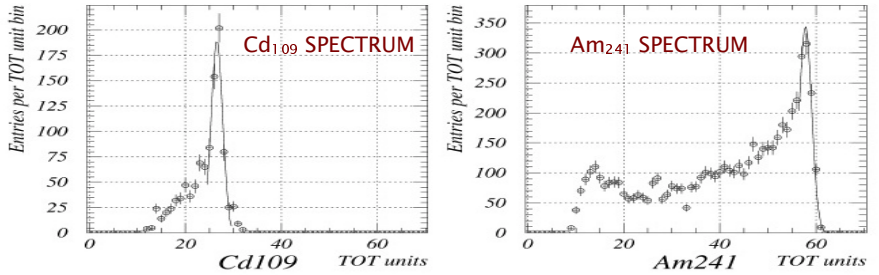
- Using individual Trim DACs, manage to achieve excellent dispersions.
- Measured noise is quite good, even for small-gap design pre-rad, and noise still remains acceptable after irradiation (reduced shaping time and parallel noise from leakage current itself both increase noise).

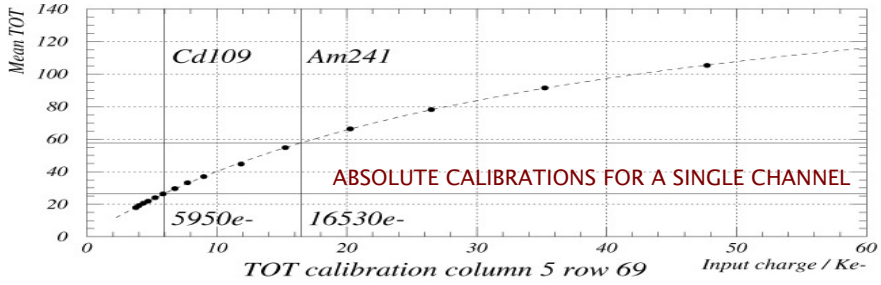
Examples of timing and charge measurements:

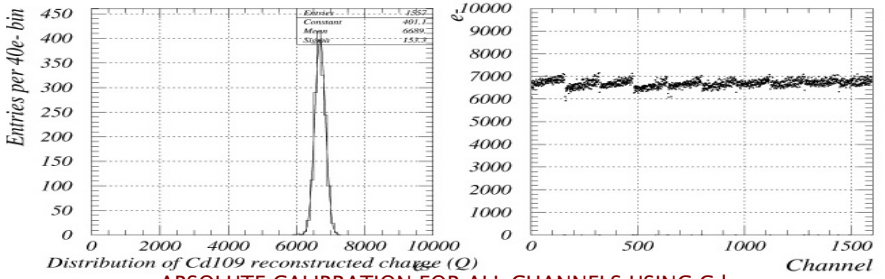




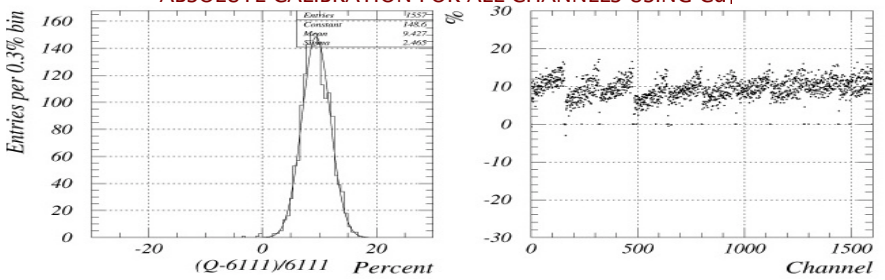
- Timing performance at large charge is excellent, and timewalk is acceptable.
- Charge measurement is high quality, but requires individual calibrations. Uniformity of internal calibration is good.





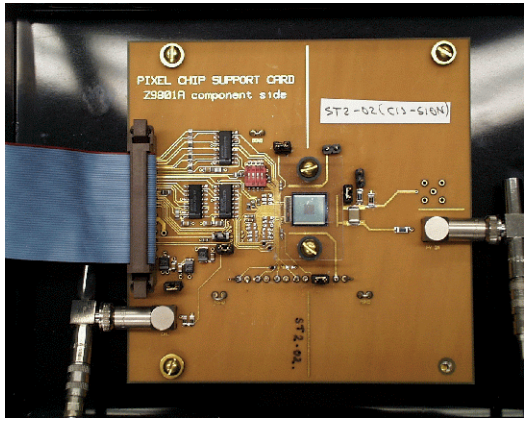


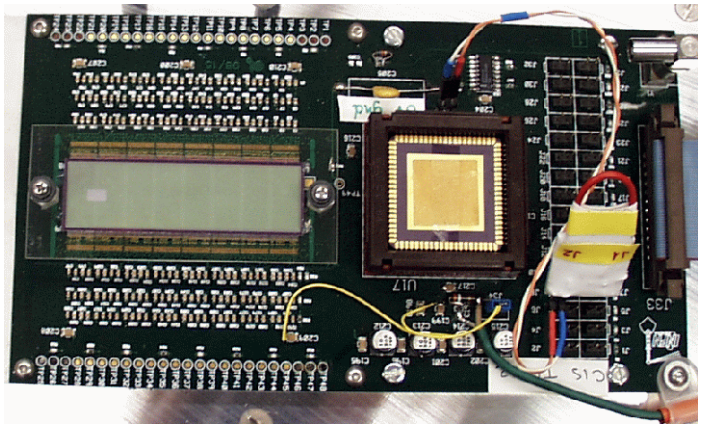
ABSOLUTE CALIBRATION FOR ALL CHANNELS USING Cd_1

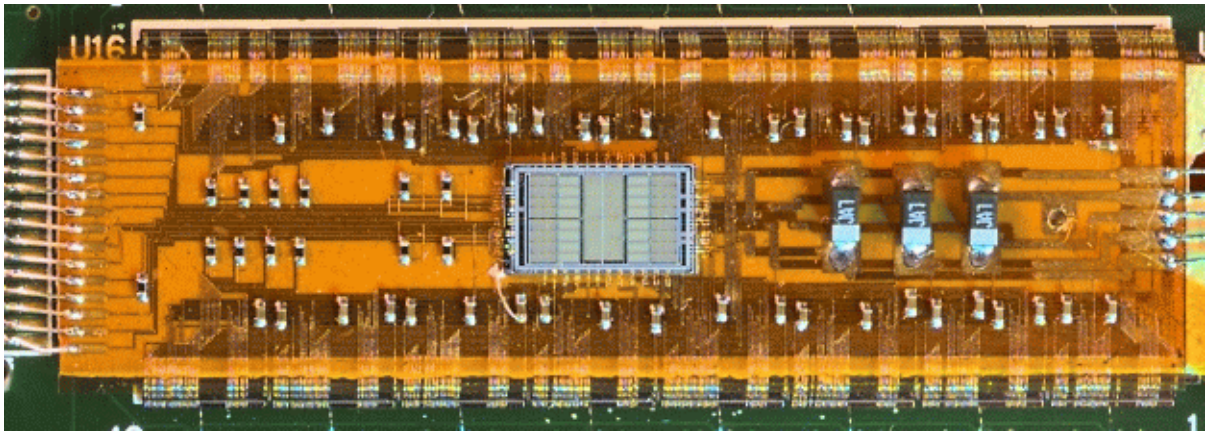


Module Prototyping:

- Built many “single chip” devices using smaller sensors for small-scale studies. Some studies were done with irradiated sensors and rad-soft electronics.
- Built about 20 modules, roughly half with IZM solder bumps and the other half with AMS Indium bumps. Several assembled as “bare” modules with interconnections on PC board, most as “Flex” modules, and a few as “MCM-D” modules. Some, but not all, of these modules work very well.

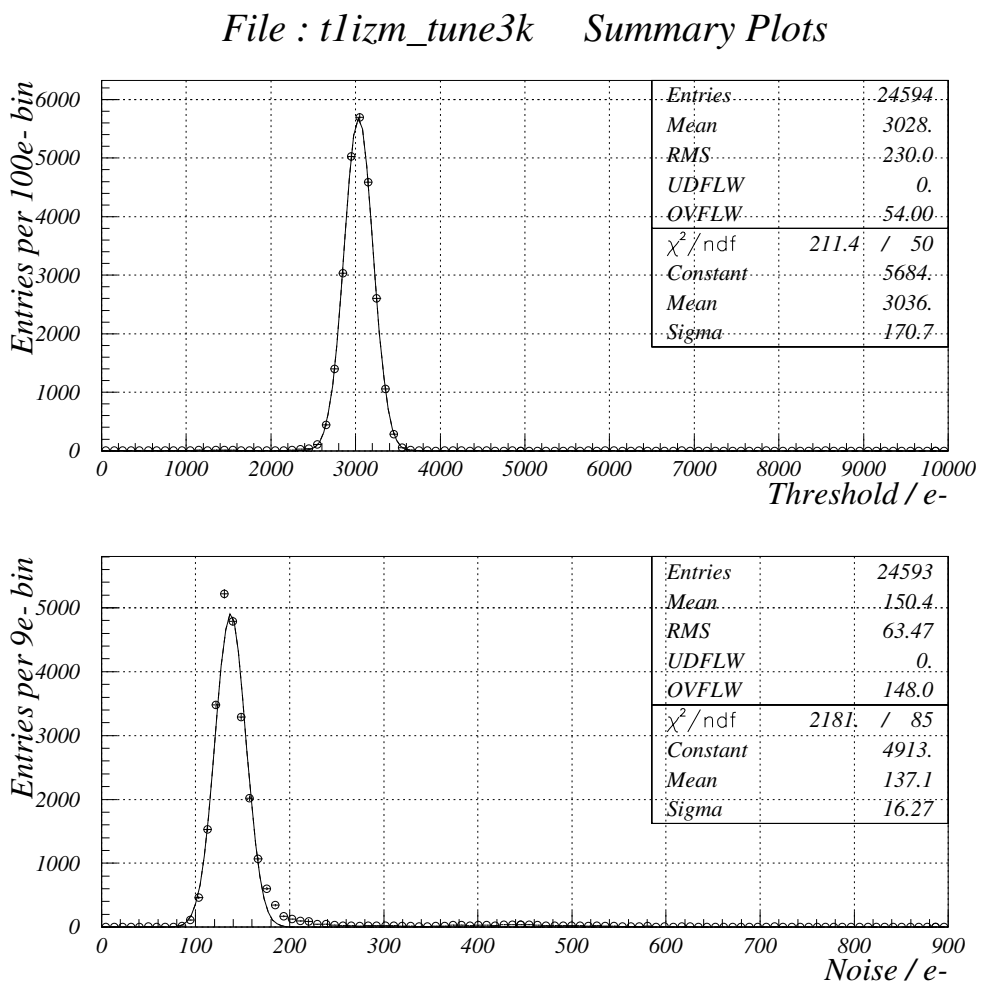






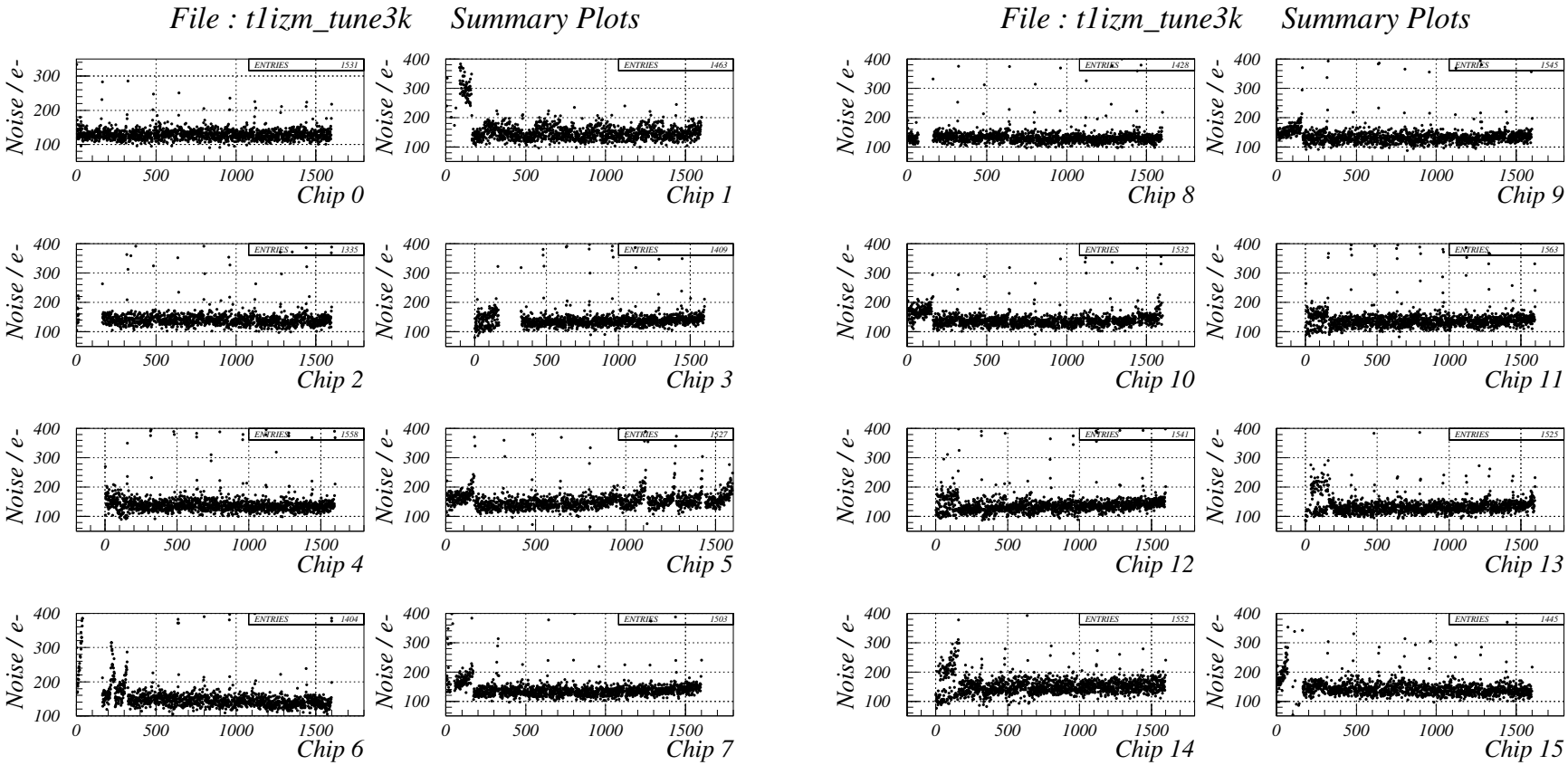
Examples of Module Results:

Bare Module (FE chips wire-bonded to PC board):



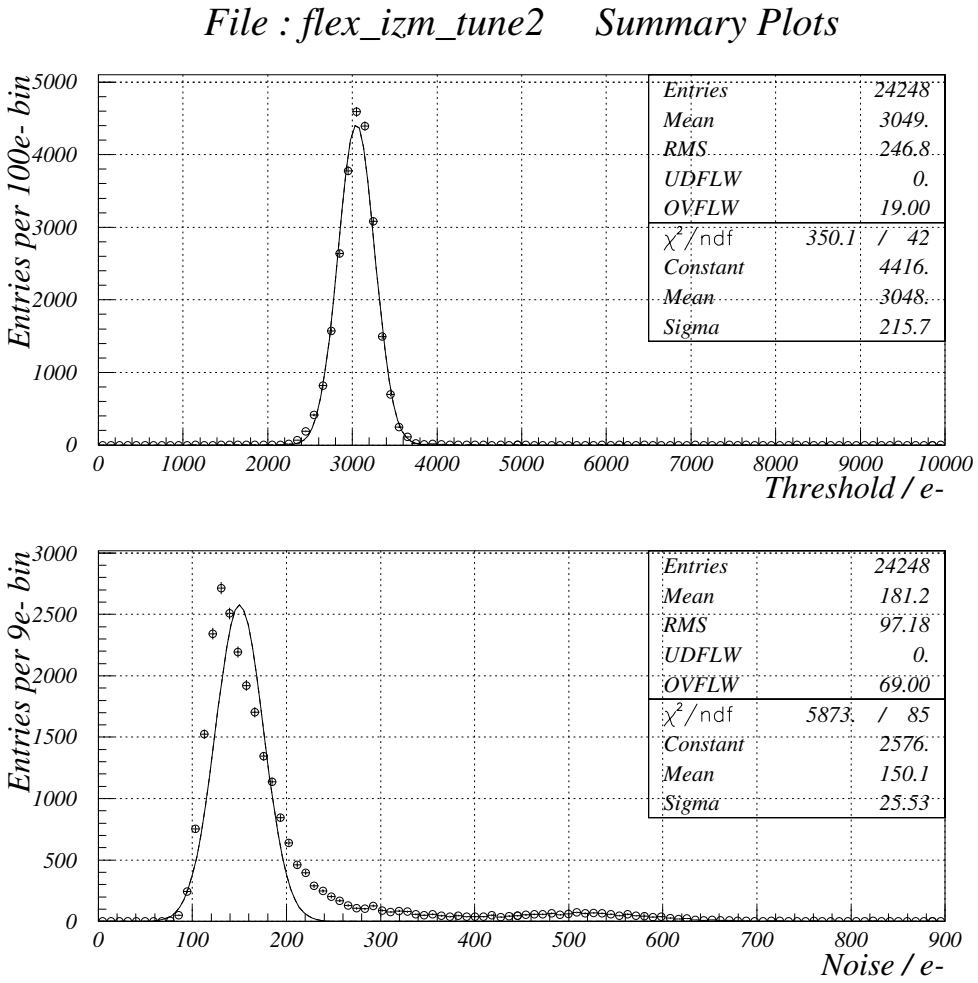
- Module has excellent threshold and noise behavior. For FE-B module should be only 16x1600 = 25600 good channels. Dead channels here are apparently all from bump-bonding problems (shorts).
- Threshold dispersion (230e) and noise (150e) for whole module are about same as for single chips.
- Module was operated in self-trigger mode at 70 KHz with excellent performance.

Plots of noise in each chip versus pixel number:



- Column 0 has longer pixels, plus most bumping defects (handling problem).
- This particular prototype comes close to meeting real ATLAS requirements for a module, although it is a rad-soft version.

Performance of best Flex module is not as good:



- Threshold dispersion is the same as for bare module.
- Noise distribution has a long tail. The origin of these noisy channels in this module is not clear.
- These results are from Spring 99, and have not been improved due to subsequent bumping problems with IZM which are still under study.

- Many impressive results from first prototype modules, but much larger statistics needed to check whether high quality modules can be built in a reproducible manner. Lab and testbeam characterization ability is now well-developed.

Initial Radiation Hard Strategy for FE Chips

Pursue essentially identical designs with two vendors:

- **ATMEL/DMILL:** Began first work on FE-D in Summer of 98. Chip was submitted to ATMEL on Aug 10 99. Design contains some "simplifications" in digital readout from FE-B design to fit into DMILL constraints, as well as some improvements. Performance targeted at outer layers, with 400μ pixel and 24 EOC buffers per column pair. Readout performance should be adequate for operation at 10^{34}.
- Comments: CMOS density relatively low, especially for NMOS, and only two metal process. This forced design to make compromises. Have made minimal, but significant use of bipolars in FE-D. Barely succeeded in fitting necessary circuitry into available footprints. Concerns about radiation hardness for pixels.
- **Honeywell/SOI:** Began serious work on FE-H in Fall 99. At this time, only LBL and CERN had TAA agreements in place to do design. In addition, Honeywell was in process of revising Layout Rules, which caused significant delays. A number of minor improvements relative to FE-D, taking advantage of better device density and third metal layer. Design should be more robust, and performance is targeted at B-layer as well (32 EOC buffers).
- Comments: Density and routing both good, and can eliminate many design compromises. Radiation hardness of individual devices seems excellent. Cost is higher, so yield must also be higher to be affordable.

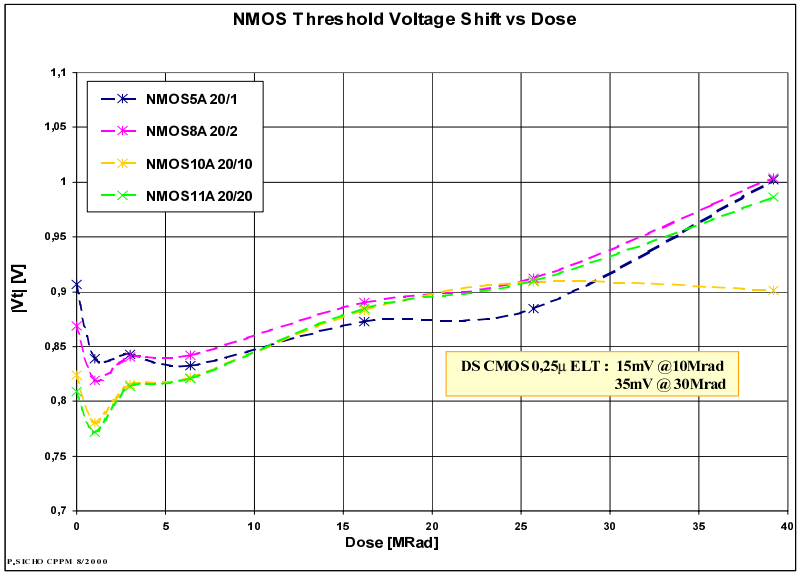
Summary of FE-D Program

FE-D1 reticle included many die (10 in total):

- Two pixel FE chips (FE-D). For the FE-D1 run, they were identical. For the FE-D1b run, they were very slightly different (changes in M1 and M2 masks).
- Prototype MCC chip. A prototype of several key elements of final MCC, about 20mm^2 core size. Includes FIFO block for final chip, plus large synthesized command decoder block. Presently have tested 14 die, of which 11 work. Appear to be no problems with this design, including operation at XCK = 80-90MHz.
- Prototype CMOS opto-link chips (one DORIC-p and three VDC-p). VDC-p seems to work well up to about 150MHz. DORIC-p has several problems which are now understood, and largely related to validation of design without parasitics.
- Additional test chips: LVDS buffer for rad-hard test board, PM bar with W/L arrays and special pixel transistors, Analog Test chip with all critical FE-D analog elements. All work well, and transistor parameter measurements suggest run is slightly faster than typical. Many detailed characterizations of Analog Test Chip.
- Have irradiated several Analog Test chips, and several PM bars in April PS run. Single devices are OK to 50MRad, but Test chips no longer work. Irradiated several VDC chips to relevant doses in May in PS, and they operate properly. Currently irradiating MCC-D0 in PS, and results look good up to 30MRad doses.

Irradiation Results on DMILL

Device level results marginally OK (but NMOS not biased):



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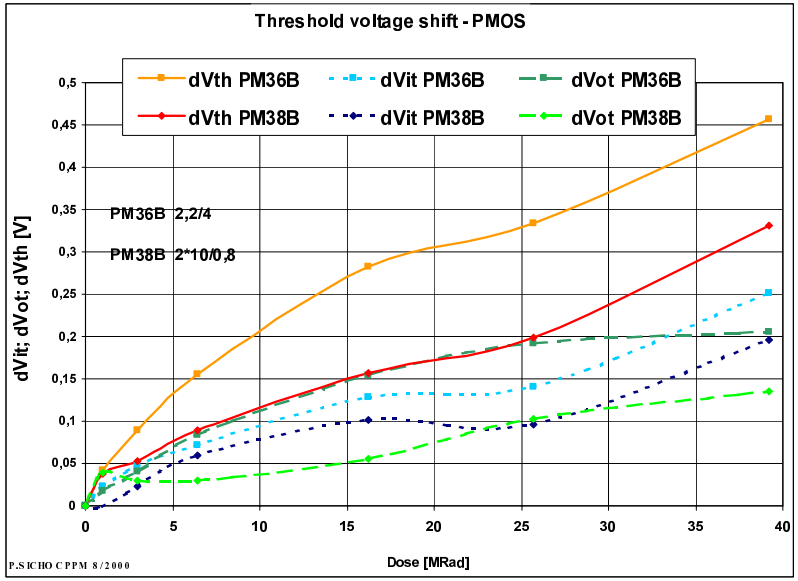

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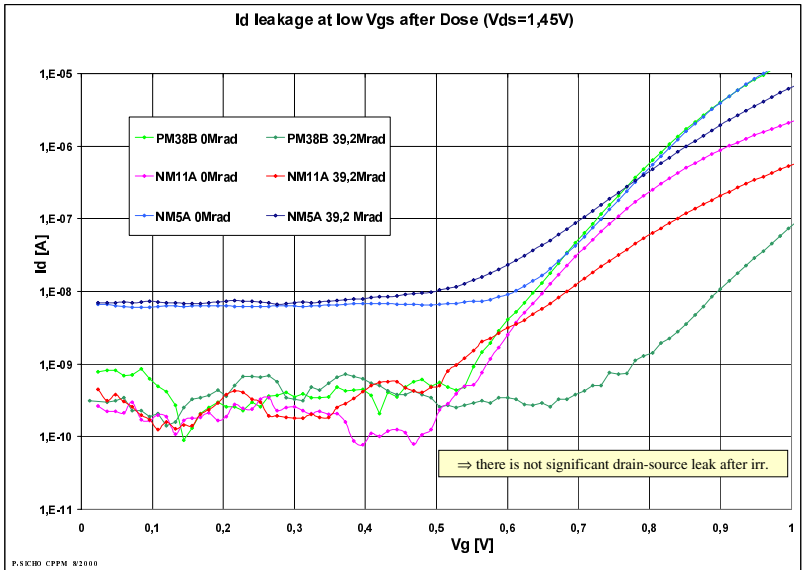
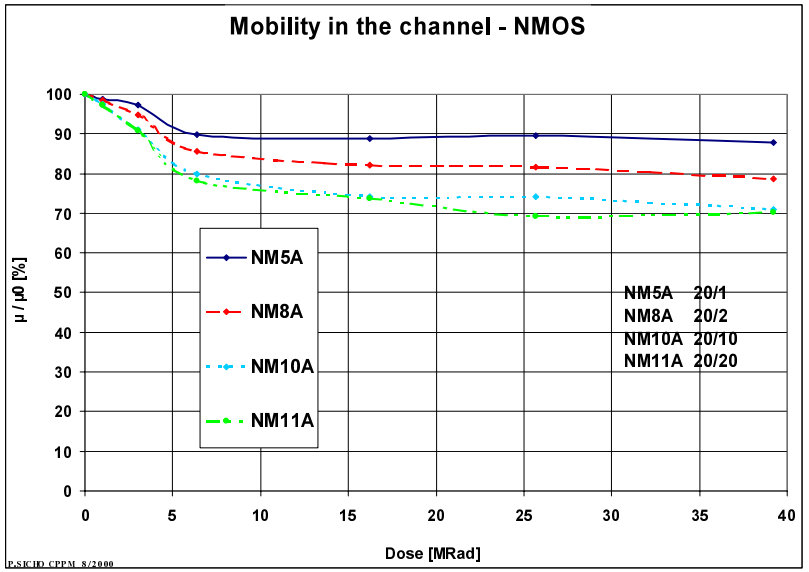




Summary of FE-D1 Results:

Front-end chips:

- Several design errors found, including capacitor short missed by faulty DRC, and several missing or under-sized buffers in control and readout portions of chip.
- Very poor yield observed (no acceptable quality chips on these wafers). This arises mainly from two circuit blocks, and seems to be a technology problem.
- The first circuit is the 2880-bit shift register used to control the configuration of each pixel (calibration and readout masks, plus TDAC values). The yield in the FE-D1 run for this circuit alone was about 25% (circuit is a few percent of die), but improved to 80-90% in FE-D1B backup run (nominally identical processing).
- The second circuit is part of the readout logic inside of each pixel. One observes malfunctioning pixels, which disturb the readout of a column-pair (320 pixels). The behavior is consistent with one NMOS used to reset a dynamic node having a low off-resistance. Subsequent studies confirmed this theory in detail.

Module Controller chips:

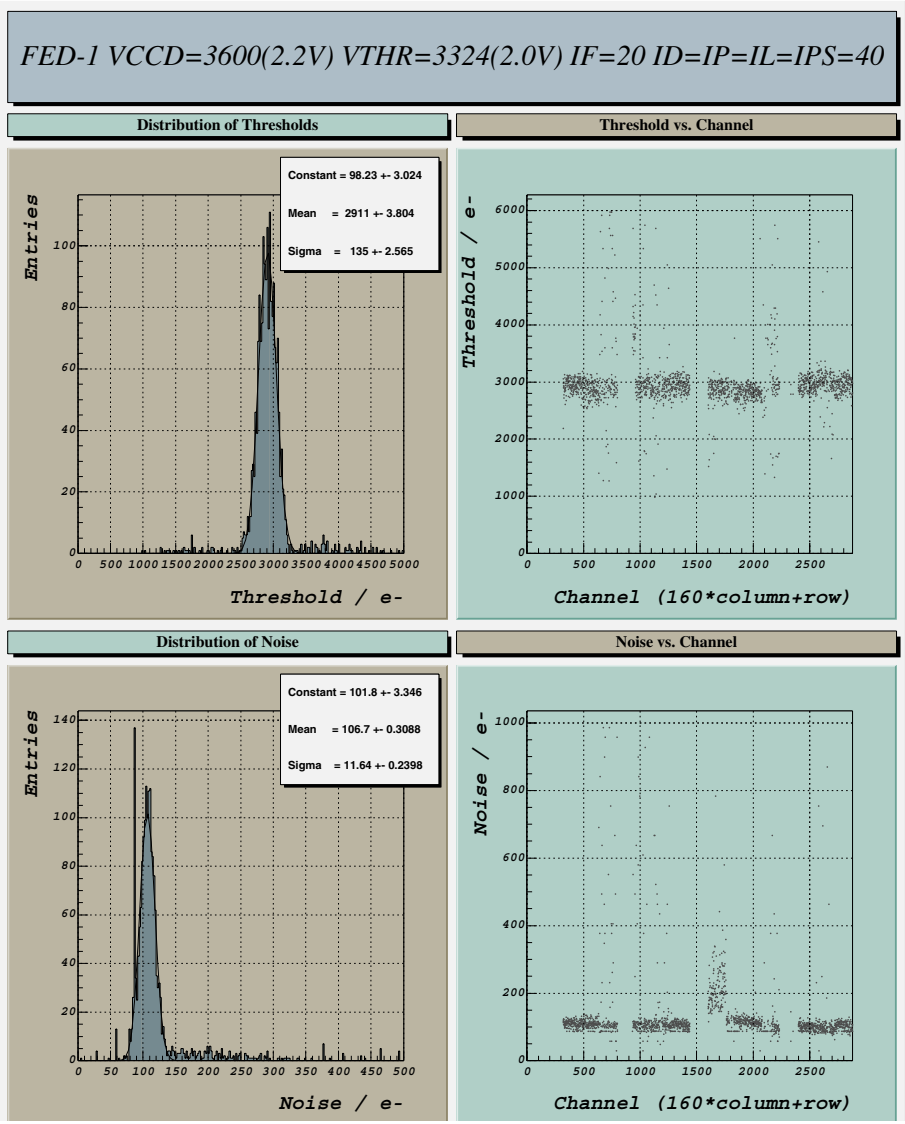
- Performance was as expected, and chips tested successfully to 80-90 MHz. Yield, based on a small number of packaged parts, was about 80%.

Opto-electronics chips:

- VDC-p worked well. DORIC-p doesn't operate properly due to polarity error and parasitic loading of several critical nodes. Behavior reproduced in simulation.

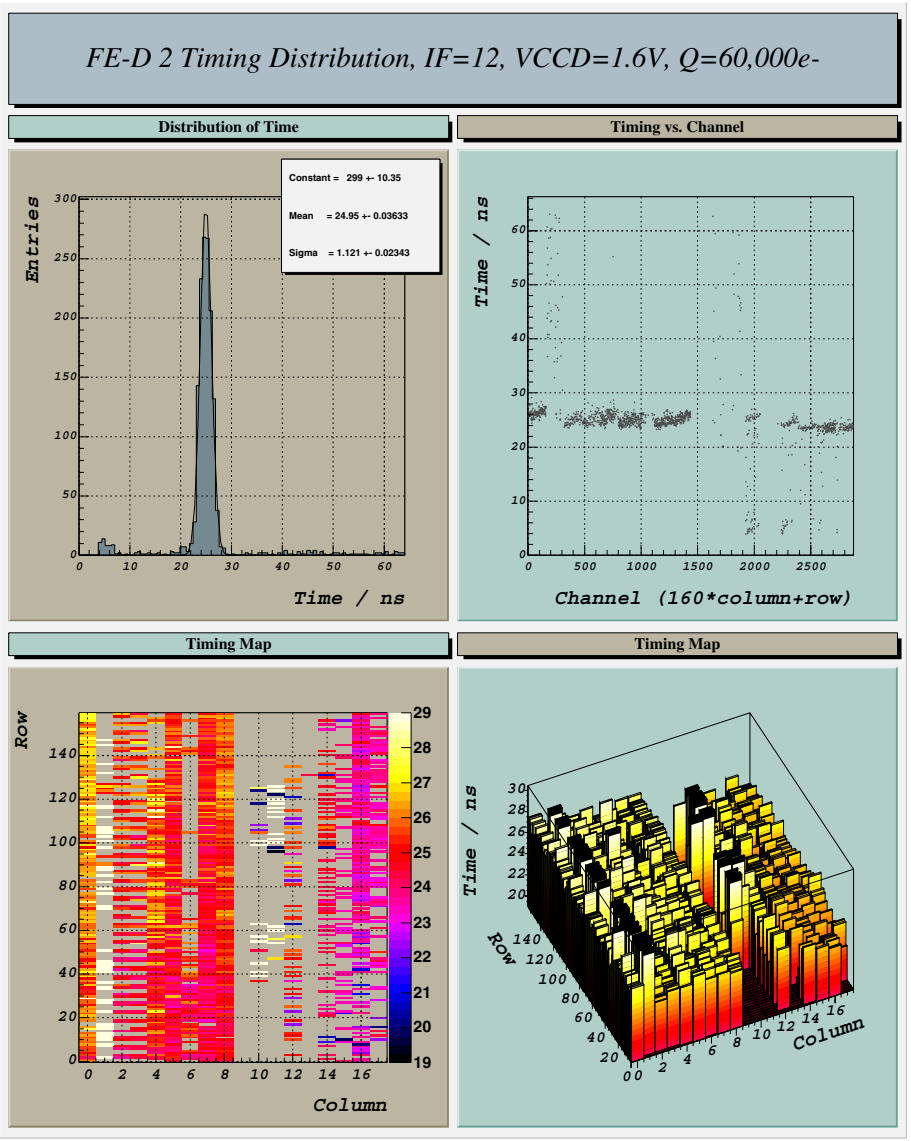
Measurement Highlights:

- Typical threshold scan of good FE-D chip. After tuning, see expected improvement in threshold dispersion (this is a bare chip):



- After tuning, the dispersion is reduced to about 135e.
- The noise is a bit higher than expected, and this is worse still for chips attached to detectors (observe 400-500e noise instead of expected 200e). This is not presently understood.
- Note many missing groups of pixels in channel map.

- Have performed timing studies by injecting a large charge (60Ke) and scanning the delay to find when the hit moves from one crossing to the next:

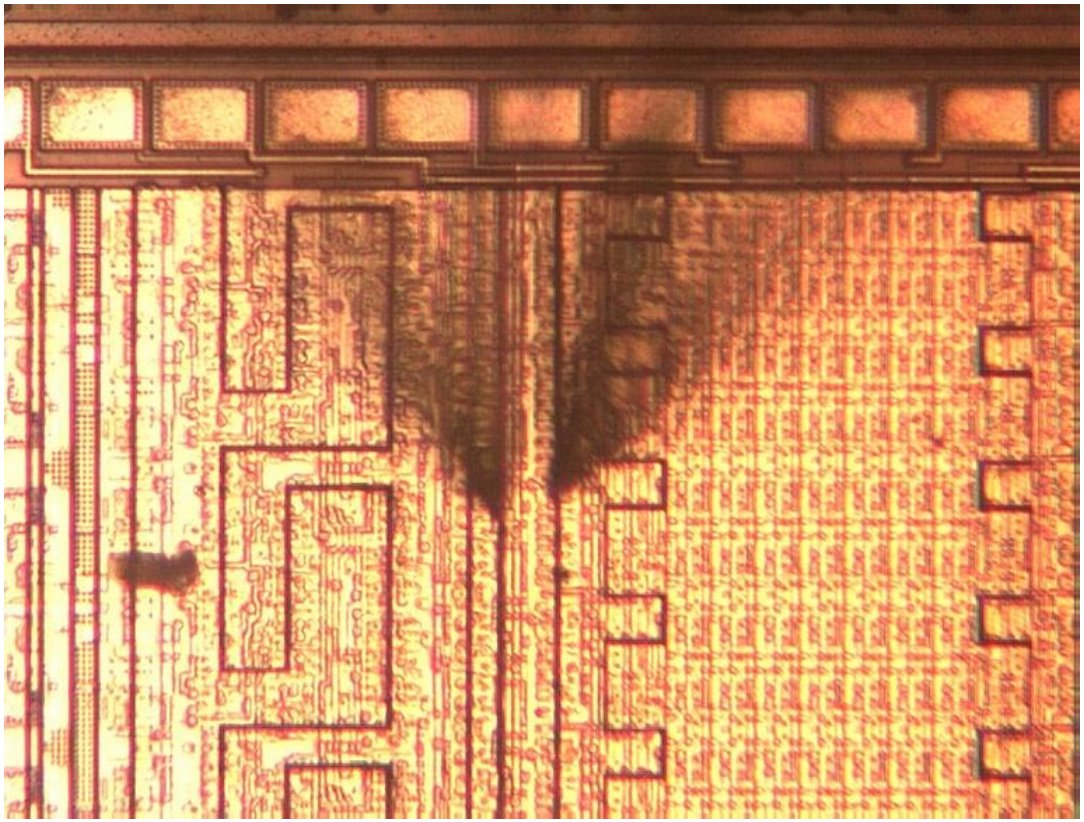


- Some indications of systematic effects, but chip had many bad/ dead channels, so hard to tell.
- Taking an RMS over the channels gives 1.1ns, similar to the results obtained from FE-B in the past.

- Many additional measurements made, including:
- TOT charge measurements with acceptable performance.
- Cross-talk measurements with very good performance (2-3%).
- Timewalk measurements with poorer performance than expected, marginally acceptable.

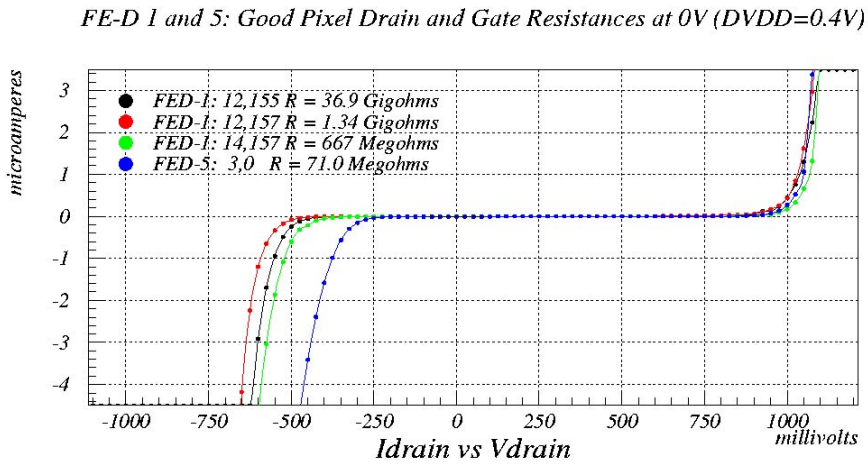
Example of Defect Analysis in Yield Studies

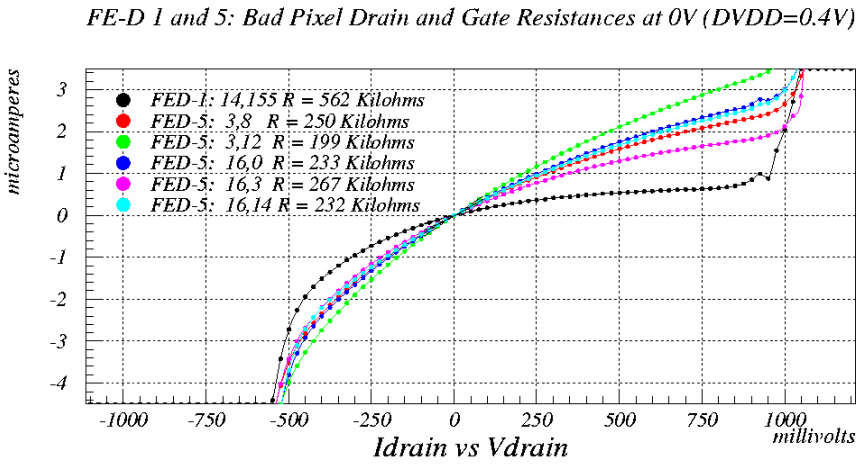
- Two chips which had been characterized in the lab had series of 20 small (8μx8μ) pads deposited by FIB surgery to allow probing of suspect “leaky NMOS”.
- Measurements were made of DC performance of the suspect device (somewhat complex to interpret since they are done in situ), as well as the dynamic performance (using an FET Picoprobe) of waveforms during operation.

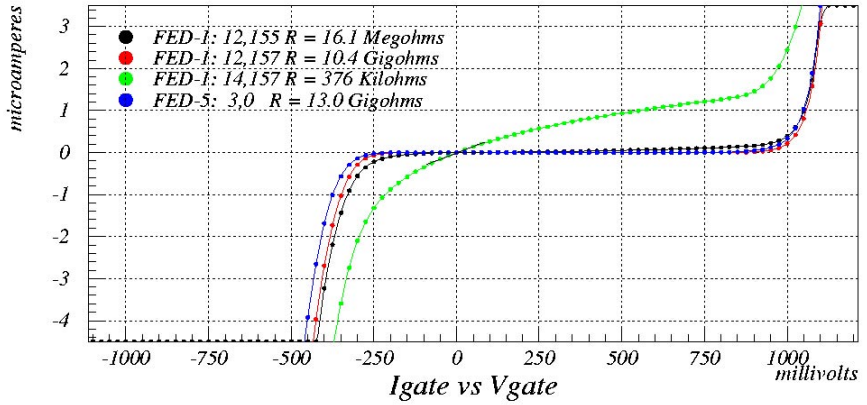


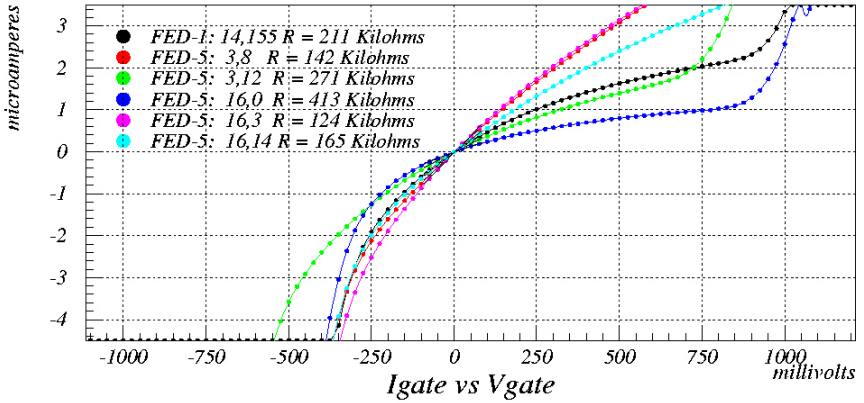
- Two 10μ probe needles place on pads. One pad was on the drain, the second on the gate of the suspect NMOS.

DC curves for pixels previously classified good/bad:



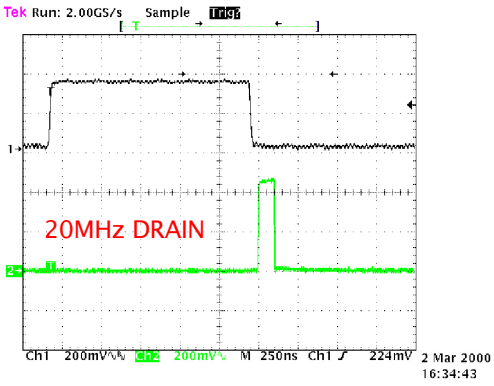


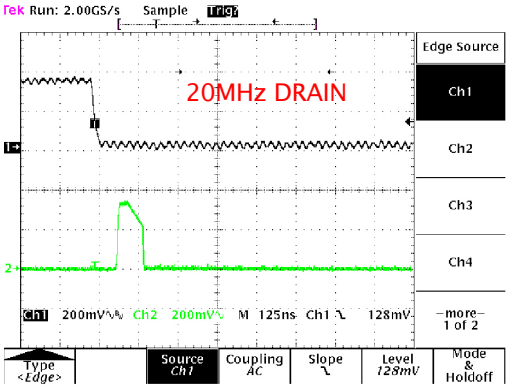


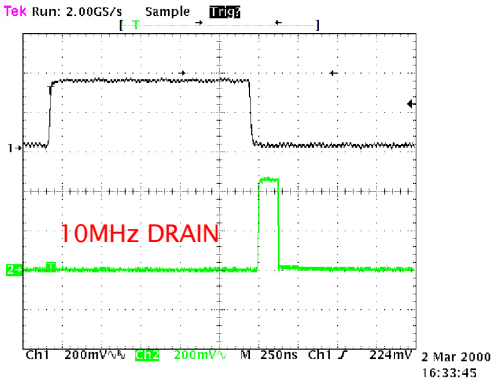


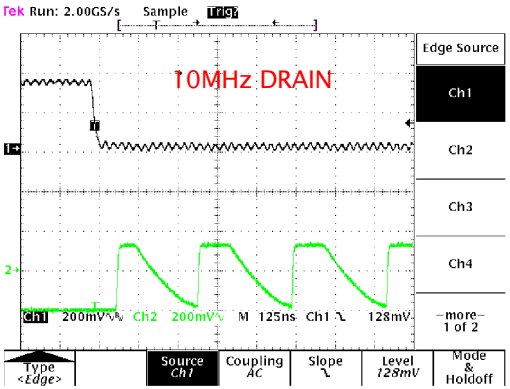
- Bad pixels consistently show apparent drain-source resistance in off state of a few 100's of KOhms. Good pixels show resistance of many orders of magnitude larger, with actual value most likely limited by Tungsten residue after FIB pad deposition.

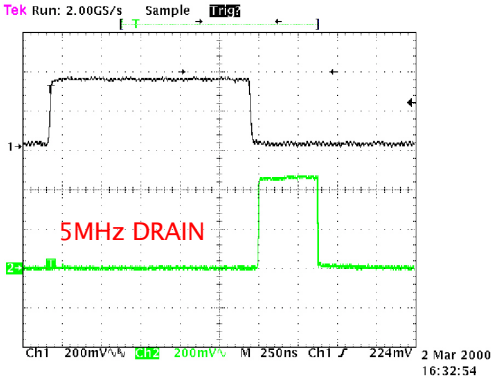
Dynamic measurements of a good and a bad pixel:

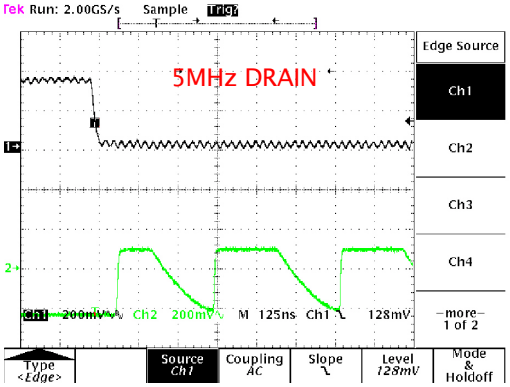












- Measurements of the state of the dynamic node (green trace) were made directly using FET probe (20fF load capacitance).
- Good pixels show stable logic high value over relevant timescale.
- Exponential slope for bad pixel corresponds to dynamic phase when logic value is “leaking” away.
- Depending on clock frequency for column readout, it is possible to produce a “digital oscillation”

Summary of Steps Taken

- Discussion with ATMEL in Jan. 00 meeting in Nantes on how to resolve yield problems. ATMEL performed analysis of defective pixels on two devices, and found no traces of contamination or etch problems that could explain the observed leakage behavior of bad NMOS. Have also analyzed SIMOX wafers looking for defects, and nothing was found (but hard to see).
- ATMEL completed processing on backup wafers from original FE-D1 run, providing us with six additional wafers (FE-D1b). These wafers were processed up to the poly etch at the same time as the original FE-D1 wafers, but processing for many critical steps done later. Compared to FE-D1, they had higher (but still not great) yield on pixel shift register, and similar yield on the readout circuitry.
- Extensive studies of our measurements as well as our layout performed by LETI/CEA (R. Truche, one of process developers), with some resulting suggestions.
- Assistance also from E. Delagne (Saclay, ATLAS LArg). Similar problems were observed in a recent SCA submission. A possible model was proposed, involving problems with poor etching of dense polysilicon traces or contacts located on top of trenches. Recall trenches are a unique feature of DMILL process, and are not completely planar, causing potential problems in processing.
- Such structures are present whenever we have low yield in sub-circuits, and are not present when we have acceptable yield, but detailed predictions did not agree perfectly with measurements.

Second DMILL submission (FE-D2)

Design modifications made:

- Prepare a version of FE-D in which all known design errors are fixed, but the basic design is the same, known as FE-D2D (dynamic).
- Prepare a second version of FE-D in which, in addition, a static version of the pixel register and the readout logic is used. This required additional space, and so the three TDAC bits were dropped from each pixel. This is FE-D2S (static).
- Prepare modified VDC-p and DORIC-p chips. All known problems uncovered during the testing of the first chips were fixed, and validated in simulation.
- Prepare the full second-generation MCC chip.

ATMEL proposal for FE-D2 (expected wafers-out Nov. 15):

- Process a standard 8-wafer engineering run with these designs, but with additional inspection steps for the critical processing of trenches and poly.
- Process an additional full lot (an internal ATMEL run) with significant processing variations in three areas: Leff (critical mask dimension for gate poly patterning), poly etching, and poly contact formation, producing 9 split wafer groups.
- The additional wafers would be made available for us to test to quantify the yield as a function of the process changes. In addition, we have designed special process monitor structures to look for poly processing problems near trenches.

Honeywell HSOI4 submission (FE-H)

- Began work on submission to Honeywell SOI in Fall 99, but most engineering resources were still dedicated to issues related to DMILL.
- This process has significantly higher density than DMILL due to its smaller devices and 3-metal support, allowing us to make a more robust design. Also, the radiation hardness as characterized for single devices appears to be better.
- This design work was nearing completion in Aug, when we discovered a large price increase (factor 2.5: 20K$/wafer in large quantities). As part of this design, we have developed a good technology file and a complete standard cell library.
- We improved the DMILL design in a number of ways, making it more robust. The critical dynamic elements were all eliminated, which forced us to retain a 50µ x 400µ pixel size to provide space.
- We reformulated the design for the digital logic blocks which do not require full-custom layout, defining them using synthesizable Verilog. This investment improves the rigor of the design, and will ease conversion to a 0.25µ version.
- We would have been ready to submit an engineering run containing two FE chips, the VDC and DORIC, and associated test chips, by early October this year. All of this work is now shelved indefinitely (and recent acquisition of Honeywell by GE makes the future even more uncertain).

Deep Sub-Micron Approach:

- One of dominant effects of irradiation of CMOS devices is creation of trapped charge in the critical gate oxide layers. Below about 10nm oxide thickness, the charge trapping largely vanishes due to quantum tunneling effects. Modern 0.25µ processes are the first to operate fully in this regime (they have 5nm oxides).
- The RD-49 collaboration has studied details, confirming that if one controls leakage paths using layout, then a commercial 0.25µ process can be very rad-hard (circuits tested to 30MRad). Many technical concerns addressed (no latch-up observed due to epi substrate, high SEU thresholds, small V_T and g_m shifts), but little experience with full-scale devices, so still unknowns in this path. Concerns remain about lifetime under irradiation, and susceptibility of thin oxides to rupture or failure due to voltage transients on long power cables.
- Growing experience with analog designs, and quality of SPICE models is high, but achieving optimal performance would probably require at least one iteration.
- CERN has negotiated a frame contract for LHC with IBM for their CMOS6 process. The price is significantly lower than the traditional rad-hard vendors.
- This places us into a commercial mainstream, where we can be assured of low prices and availability in the future, and could hope for yield closer to FE-B.
- In wake of continuing problems with achieving acceptable yield with FE-D and acceptable cost with FE-H, have begun conversion of designs with high priority.

Proceeding towards 0.25μ versions of Pixel Chips

Background:

- We now have at most one traditional vendor for our rad-hard designs in pixels.
- We have found that our designs must be more aggressive to fit within the restrictions imposed by DMILL (use of dynamic logic and storage, little SEU tolerance, operation over very large parameter variations, very large die size, etc.). This requires extra engineering and testing, and there is extra risk.
- This makes it imperative to develop 0.25μ versions of our pixel chips (FE, MCC, VDC, DORIC), or we risk having nothing with which to construct ATLAS.

Vendor issues (Note 0.25μ processes use 200mm wafers):

- Default path is to rely on the CERN-negotiated frame contract for access to IBM 0.25μ process. This provides advantage of fixed prices and guaranteed access through 2004. There is only limited MPW access and limited technical contact.
- A second path is to use MOSIS to access the TSMC 0.25μ process. The processes are very similar (minor differences in via sizing and spacing rules, plus only 5-metal instead of 6-metal). Costs are slightly (10%) higher. Fermilab (BTeV) has already performed irradiations, and finds excellent results (only ^{60}Co so far).
- We have begun development of common design environment and standard cell library, in collaboration with Fermilab and RAL, and this looks very promising.

Major Issues for FE-I Conversion:

- Basic idea is to develop conservative chip, like FE-H, based on 400μ pixel, about 32 EOC buffers, and overall with the same basic design. Goals is to retain identical current budget to that of FE-D/FE-H (services are critical factor).
- Need significant changes in present front-end design for feedback and threshold control, which rely on small W/L NMOS devices which cannot be built in 0.25μ with annular layouts. This most likely leads to active leakage compensation and a two-stage preamp design. A differential preamp to reduce common mode is also under consideration. A major goal is further improvement in timewalk.
- Have significant concerns about SEU tolerance of designs, and several solutions are planned for this. Will use error correcting registers for Global configuration and SEU-tolerant registers for local configuration, combined with more robust state machine designs to minimize non-transient effects of SEU.
- For digital readout, propose to move towards a fully static readout design, to minimize impact of SEU and leakage. Will use differential data transfer from pixel to EOC to improve speed and reduce pickup. Plan to use more top-down design for critical logic blocks, largely synthesized from state diagrams, leading to more synchronous and robust behavior.
- Also a new idea to include digital timewalk correction in CEU based on TOT values. This could give us more flexibility in achieving timewalk specs, which have proved marginal and difficult to improve in our present complete chips.

Planning and Status for FE-I

Bonn (Fischer, Comes, Ivan):

- Responsibility to update cell layout for library to include TSMC compatibility, separate substrate connection, additional pixel-specific cells.
- Conversion of analog blocks from FE-D, including DACs, chopper, and threshold control. Design of Hamming-code correcting registers.
- Responsibility to integrate and submit Analog Test Chip like that included in FE-D submissions. This would be a MPW run with TSMC, targeted for Jan/Feb, 2001.

CPPM (Blanquart), in process of transfering to LBL:

- Responsibility to develop and lay out new analog front end design. Will be on a fast track for TSMC submission, and is presently the critical path.
- Responsibility for design of biassing and threshold control, current reference, analog buffer, and LVDS I/O (if we choose to update the existing standard cells).

LBL (Mandelli, Marchesini, Meddeler, KFE):

- Overall responsibility for design environment and common TSMC/IBM rules.
- Responsibility for updated column pair readout (pixel hit logic, pixel memories, CEU, and sense amps) plus pixel control block, updated EOC buffer design, and integration into complete column pair.

- Responsibility for all digital logic at bottom of chip, which will be almost entirely synthesized and mainly placed and routed with automatic tools.
- Responsibility for overall integration of all blocks into final submission to IBM.

Current Activity on FE-I:

- Proceeding on FE-I as rapidly as possible, with significant progress in all areas. Full team listed above is working with high priority.
- Have a first version of common design environment (tech files), and work is starting to adapt the CERN/RAL standard cell library. Studying corner models: IBM corners seem to cover all post-rad effects as well, and circuits change speed by about a factor of 2 faster/slower at 2.0V (TSMC corners are only +/-50%).
- Have first versions of designs for new pixel hit storage circuitry, bottom-of-column logic (CEU+sense amps), and EOC buffer logic. Many Verilog simulations running already. Working to convert FE-H synthesizable Verilog from Synergy to Synopsis for all digital blocks in the bottom of the chip.
- Major issue is how best to create new front-end design. Can either proceed via rapid MPW prototype, followed by engineering run (early delivery of design, but with measurements before full run) or via careful, well-simulated design with no prototype measurements. This requires further evaluation.
- Constraints placed by need to fully characterize and qualify a new design with a new vendor during 2001 suggest an engineering run is required by Jun 1 2001.

Current plans for other conversions:

- Discussed conversion issues for MCC-D2. Since the design is driven by high-level (Verilog) description, with limited use of full-custom blocks, conversion should be relatively easy. Have done first synthesis of one block. Given need for evaluation of MCC-D0 and MCC-D2 on rapid schedule, expect to begin real work in Jan 2001, with goal of submitting a complete prototype when FE-I is ready.
- Discussed conversion issues for VDC and DORIC. Present groups have begun conversion, and would expect to produce new designs either for an MPW run in early 2001, or for the FE-I engineering run.
- There is potentially a large conflict between resources needed for the work above, and resources needed to develop pre-production quality DMILL versions of the chips in the FE-D2 run (FE-D3). We will re-discuss all of these issues in Dec pixel week, based on first results from characterizing chips from FE-D2 run.

Yield assumptions:

- For identical die size in HP 0.8μ process (FE-B), achieved 92% yield.
- One large scale chip already in existence in IBM 0.25μ is CMS APV25. The die area is 60mm^2, and a yield of 84% was observed for about 500 tested chips.
- To be conservative, have assumed a yield of 50% for FE-I in cost estimate.
- Will try to follow IBM “R” rules for better yield. High yield and low wafer count will be a major factor in accelerating the module assembly schedule.

Other implications of 0.25μ choice:

- Bump-bonding with 200mm wafers has been discussed with IZM and AMS. IZM has capability now (major upgrade of all machines in bumping line over the last year), but no experience. AMS plans to develop capability soon (critical issue is Indium evaporator system). Initiating a “dummy module” program using 200mm wafers to qualify vendors.
- Material budget will likely grow, since can only thin 200mm wafer to about 300μ, instead of the 150μ value achieved for 150mm wafers.
- Testing of 200mm wafers requires new probe stations. Presently LBL and Bonn are planning to acquire new semi-automatic probe stations for this purpose (LBL machine is in project budget).
- Testing of chips at voltages in the range of 1.6V - 2.5V is being included into production test systems, and is not difficult. Production probing/testing system based on pin drivers which are programmable, plus some 74LVC bus drivers.
- Power distribution is more challenging. Will attempt to keep the present current budgets in order to prevent low voltage power services from growing further. Power cable concept is based on goal of 2V voltage drop, but there are concerns about voltage transients induced by changes in current consumption. Transient protection below 5V is difficult (varistors, zeners, and avalanche diodes all develop soft clamping curves in this region). Exploring new technology (EPD-based devices from Semtech), but not known yet whether they will be rad-hard.

Radiation Hardness Qualification and Testing:

- **Characterization of processes using single devices and test structures:** This work has been carried out already for both DMILL and HSOI. The DMILL work was done when the process was still under development with LETI.
- **Irradiate complete circuit blocks from present designs:** An example is the analog test chip created for the FE-D run. It allows full studies of the front-end, including adding capacitive loads and leakage current, in a small simple chip.
- **Irradiate FE chips while they are operating:** Have already built “rad-hard test board” for this purpose. Constructing an optimized “parametric” tester to characterize chips in detail (essentially use commercial ATE chips to build a custom IC tester). This allows changing clock frequencies, scanning phasing/ timing, and scanning I/O thresholds/voltages to evaluate how much margin a given die has for achieving its operational specifications. This electronics is being developed at LBL, to be ready by early next year (see talk of J. Richardson).
- **General Testing:** plan to use parametric testing for selecting “known good die” during production. These die should remain good (with high confidence level) after irradiation. The production cuts would have to be “tuned” by characterizing many chips both before and after irradiation. Wafer probe criteria would be optimized to provide acceptable yield before irradiation, as well as good confidence level of continued operation after irradiation. This is a more difficult problem for DMILL than for a 0.25μ design where post-rad effects are much smaller.

US Roles:

- **Overall Electronics coordination:** since 1998.
- **FE-D design effort:** Our contributions were the digital readout design. The design team was two full-time designers. We also play a major role in all chip testing, including frequent trips to our FIB vendor.
- **FE-H design effort:** We developed a front-end design (prototyped in Nov. 98), and characterized the process pre-rad and post-rad. Our design team consisted of three designers. Our roles were digital readout and overall integration.
- **FE-I design effort:** The present team is three designers, one of whom will leave by the end of the year. We have recently hired the lead analog designer from CPPM (who was otherwise about to leave HEP). The Bonn role includes design and layout of some analog and digital blocks, and LBL will do the rest.
- **DORIC-p/VDC-p design effort:** OSU has one engineer and one postdoc part-time, plus part of a senior physicist. They are working on design and testing.
- **Testing systems:** LBL (initially in collaboration with Wisconsin) developed first generation test system (VME-based PLL module, PCC board, and single-chip support boards). LBL designing second generation test system. All test systems are provided by LBL, and will also develop “burn-in” board to allow continuous operation of many modules with periodic sampling of their performance.
- **Production Testing:** LBL will probe 50% of FE wafers, OSU will probe 50% of opto wafers. Additional roles in bare module and assembled module testing.

Basis of Cost Estimate and Schedule

Baseline Scope:

- Two hit system built entirely using 0.25μ technology chips, with possible exception of opto-link chips (higher voltage requirements for VDC-p).

Goals:

- Three hit system, with third layer (barrel plus two disks) provided using DMILL technology. Given the nominal ATLAS schedule, this is the only way to advance the module construction schedule sufficiently to complete a three hit system.

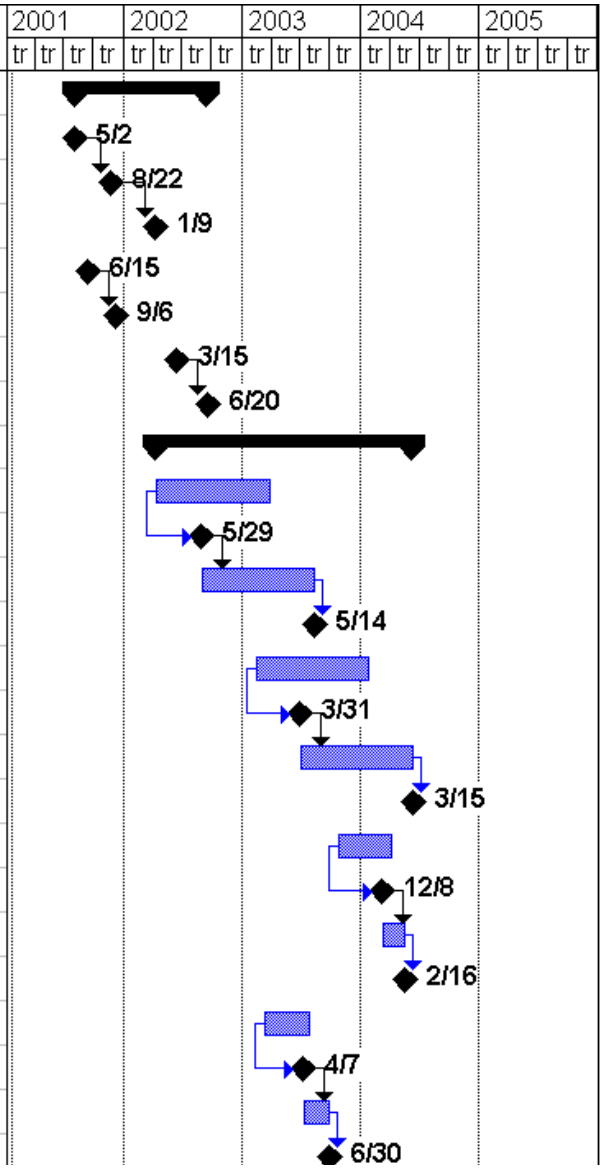
Major Steps:

- Third generation of DMILL chips (FE-D3): Assuming that FE-D2 has acceptable yield, noise performance, and radiation hardness, this would be a pre-production version. We assume that it does not require significant engineering resources.
- First generation of 0.25μ chips (FE-I1): First prototype 6-wafer engineering run, including all chips (FE, MCC, VDC, DORIC). Evaluation would occur during 01.
- Second generation of 0.25μ chips (FE-I2): This is assumed to be a 48-wafer run (smallest production run available under IBM frame contract). This would be a pre-production run for outer layers, and would be evaluated in 02.
- First generation of 0.25μ chips optimized for B-layer (FE-IB): This would probably be on FE-I2 run, and aggressively optimized for high occupancy and total dose.

Schedule

Major milestones in Electronics Schedule:

WBS	Task Name
1.1.1.3.2	**Development/Prototypes**
	FE-D3 submitted
	FE-D3 wafers arrive
	FE-D3 wafer tests complete
	1st 0.25 micron prototype submitted
	1st 0.25 micron prototype delivered
	2nd 0.25 micron prototype submitted
	2nd protoype 0.25 micron wafers delivered
1.1.1.3.3	**Production**
	DMILL wafer fab
	1st DMILL wafers arrive
	Test DMILL wafers
	DMILL Fe testing complete
	Outer FE IBM Production
	1st outer IBM wafers arrive
	Test outer FE IBM wafers
	Outer IBM FE Testing complete
	B-Layer FE Production
	1st B-Layer wafers arrive
	Test B-layer wafers
	B-Layer testing complete
	Optical IC production
	1st Production Optical ICs
	Test optical Ics
	Optical IC testing complete



- Assume priority given to IBM in near-term.
- Assume modifications to FE-D2 are minimal, and it works as expected.
- Assume IBM work for outer layers is larger complete before B-layer work is started.
- Assume B-layer prototype is on same run as second 0.25μ outer layer prototype.

Funding Profile

U.S. ATLAS E.T.C.

WBS Profile Estimates

Funding Source: All **Funding Type:** Project10/24/00 2:14:12 PM

Institutions: All

WBS Number	Description	FY 96 (k$)	FY 97 (k$)	FY 98 (k$)	FY 99 (k$)	FY 00 (k$)	FY 01 (k$)	FY 02 (k$)	FY 03 (k$)	FY 04 (k$)	Total (k$)
1.1.1.3	Electronics	0	0	0	0	0	756	579	470	26	1830
1.1.1.3.1	Design/Engineering	0	0	0	0	0	381	400	161	0	942
1.1.1.3.1.1	IC design	0	0	0	0	0	189	269	11	0	469
1.1.1.3.1.2	Test design	0	0	0	0	0	140	29	0	0	169
1.1.1.3.1.3	Systems Engineering	0	0	0	0	0	52	101	151	0	304
1.1.1.3.2	Development and Prototypes	0	0	0	0	0	374	137	0	0	512
1.1.1.3.2.1	Atmel/DMILL prototypes	0	0	0	0	0	160	0	0	0	160
1.1.1.3.2.2	Honeywell	0	0	0	0	0	10	0	0	0	10
1.1.1.3.2.3	0.25 Micron	0	0	0	0	0	31	54	0	0	84
1.1.1.3.2.4	Test	0	0	0	0	0	173	83	0	0	257
1.1.1.3.3	Production	0	0	0	0	0	0	42	308	26	376
1.1.1.3.3.1	Front-end ICs	0	0	0	0	0	0	19	229	26	274
1.1.1.3.3.2	Optoelectronics	0	0	0	0	0	0	23	79	0	102

Summary and Conclusions

- System design largely exists for both on-detector and off-detector electronics.
- Prototypes of major chips (FE, MCC) built using rad-soft electronics have been extensively tested in lab and testbeam. Present designs basically meet all ATLAS requirements.
- Design of first rad-hard prototypes in DMILL appears sound, but yield is unacceptably low. Working with vendor to understand problems. Second generation of design, including vendor corner runs, is now in fabrication. Delivery of FE-D2 wafers expected in mid-Nov.
- Expect that go/no-go decision on whether to continue with DMILL design could be made by Feb. 2001. If all goes well, anticipate pre-production submission in May.
- Work on Honeywell version has been cancelled shortly before submission due to unacceptable cost increases, losing more than 6 months of design time.
- Work on 0.25µ versions of all chips has priority, and is proceeding rapidly. Complete set of prototypes (FE, MCC, VDC, DORIC) expected by Sept. 2001. Although some questions remain, this approach appears ready to lead to a high-quality pixel tracker for ATLAS.
- With the new fully-insertable mechanics design, believe that we have a credible schedule to deliver the baseline scope (2 hit system) for nominal ATLAS turn-on.
- It is now appropriate to convert this effort into an official US construction project !