Microelectronic-enabled Detectors

Who we are

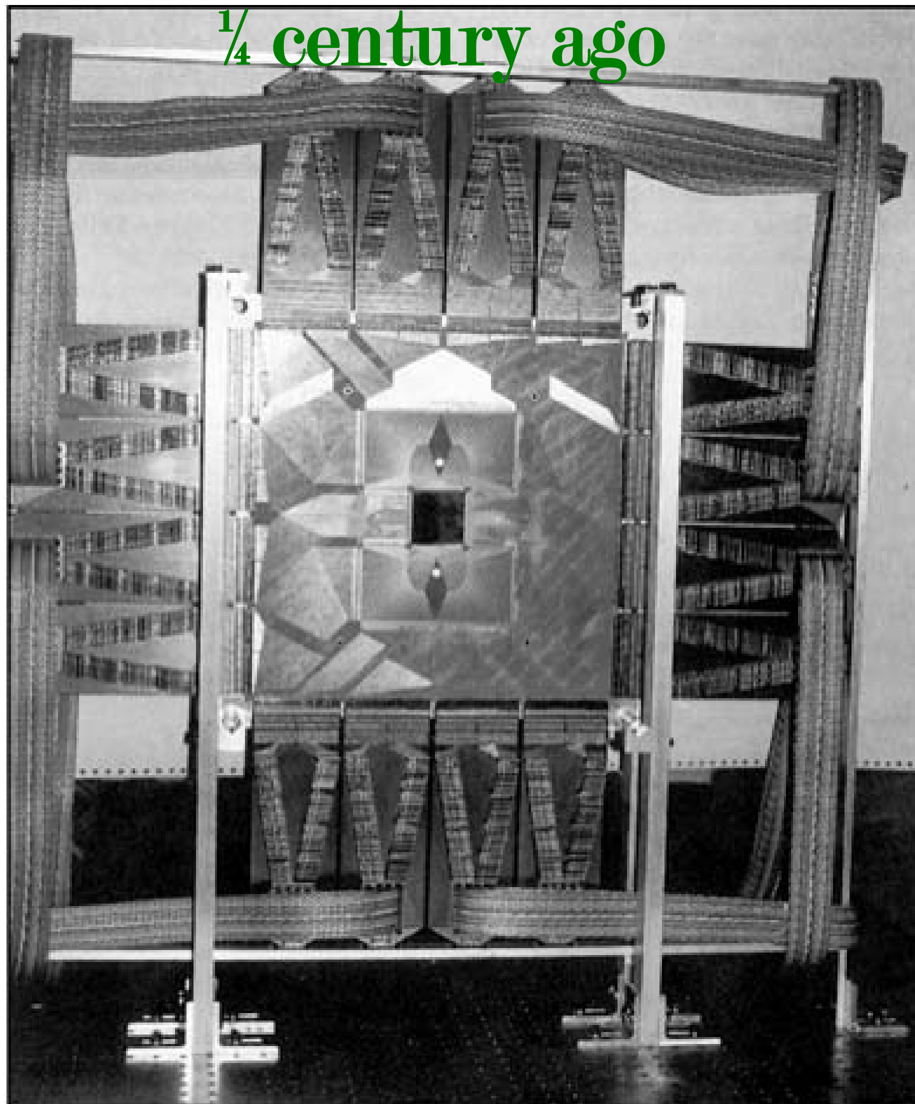
What we're doing

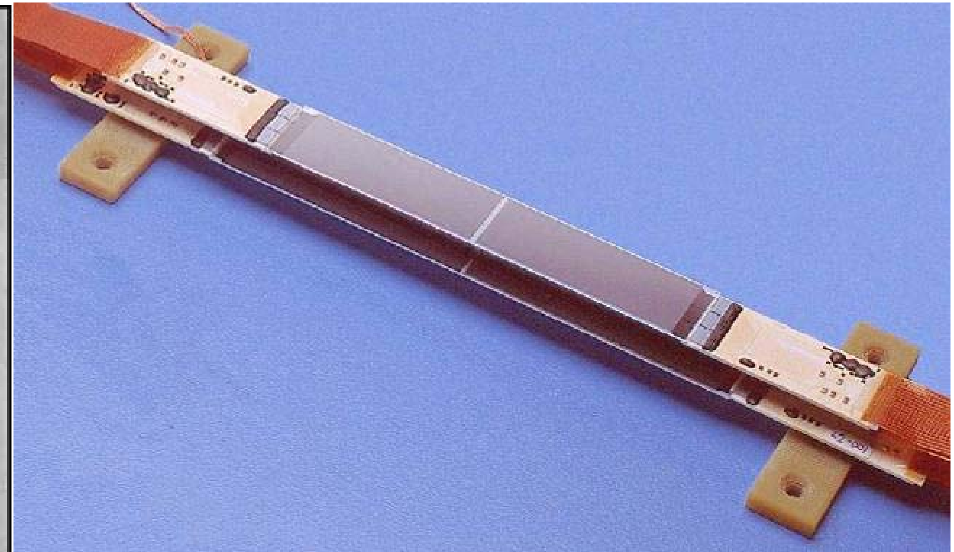
Interconnections

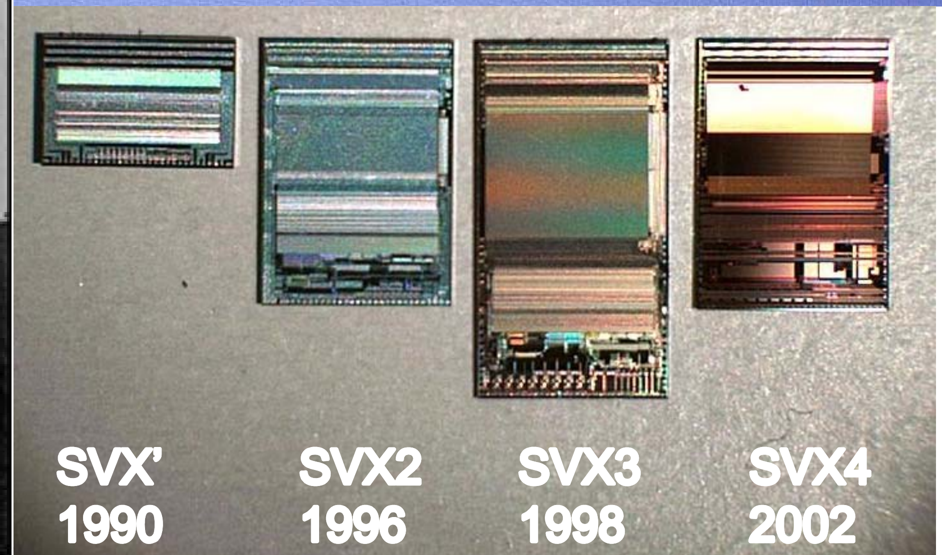
How we work

Peter Denes
Engineering Division, Director (acting)
IC Design Group Leader
Advanced Light Source, Deputy Director for Engineering

Microelectronics ↔ Detectors







LBNL Engineering Division

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TECHNOLOGY TRANSFER
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Department Head

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R. ALVAREZ
RESEARCH AND INSTITUTIONAL INTEGRITY OFFICE
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PHOTON SCIENCES
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Associate Laboratory Director

ADVANCED LIGHT SOURCE
R.W. FALCONE
Division Director

300 staff
60% Mechanical
40% Electrical, Software, …

Electronics for Detectors

ELECTRONICS, SOFTWARE & INSTRUMENTATION ENGINEERING

Henrik von der Lippe, Deputy Director
Joan M. Wolter, Administrative Support
Marilyn Wong, Timekeeper/ Back-up Support

Accelerator Electronics — Alessandro Ratti
- Accelerator EE Engineering: Lawrence R. Doolittle, Marco T. Monroy, Carlos Serrano
- NSD-88 Inch Cyclotron: Alessandro Ratti; Michel Kireeff Covo, Gudrun H. Kiesl
- Engineering Applications - UXO: James B. Greer (G)
- Laser Optics: Russell B. Wilcox
- Pulsed Power, HIFAR-EE / LIGHTING: William L. Waldron; James E. Galvin, Louis L. Reginato (Ret)

ALS-EE — Walter C. Barry
- Accelerator & Beamline Technology Section: Barry J. Bailey; Moises O. Balagot, Patrick W. Casey, Helen K. Chen, Jonathan Elkins, Paul Molinari, Robert S. Mueller, Massimiliano (Max) Vinco, Kenneth D. Woolfe
- Accelerator Physics: Gregory J. Portman
- Instrument Section: Michael J. Chin; Jonah M. Weber, Michael P. Fahmie (Ret)
- RF Section: Slawomir Kwiatkowski; Kenneth M. Baptiste, James J. Julian

ALS-SE — Alan Biocca
- Edward E. Domning, Hanjing Huang, Susanna R. Jacobson, Yunian Lou, Brian V. Smith, William F. Steele, Christopher A. Timossi, Michael E. Urashka, Eric C. Williams

CENTER FOR SYSTEMS BIOLOGY ENGINEERING — Jian Jin
- Rosanna Cambie, Robert A. Nordmeyer (Ret), Rafael Gomez-Sjoberg

ELECTRONIC SYSTEMS — Sergio Zimmermann
- Dionisio Doering, Bryan C. Holmes, Jimmie K. Johnson, John M. Joseph, Donald A. Landis (Ret), Pier F. Manfredi (G), Thomas L. Merrick (Ret), Thorsten Stezelberger, Judy J. Strikkinen (T), Bojan T. Turko (Ret), Chinh Q. Vu, Harold Yaver
- Peter Denes: Richard C. Jared (Ret), George Zizka (Ret)

ELECTRONICS TECHNOLOGY — Robert M. Candelario
- MATRIX AREAS: Michael J. Bell
- ALS Fabrication: Randolph M. Candelario, Robert W. Gassaway, Ronald L. Gervasoni
- Electronic Maint/Fab: William R. Kellus
- Ion Beam Technology: Thomas A. McVeigh
- NSD-88 Inch Cyclotron: Doyle F. Byford
- Pulsed Power, Accelerator Electronics: Craig F. Rogers
- SuperCon: Peter (Chip) C. Kozy
- RF and Instrumentation: Mark Regis
- ALS MAINTENANCE: Timothy L. Kuneli
- ALS Electronics: Ronny A. Colston, Larry G. Holzer, Sergio Rogoff, Edgardo J. Romero II, Peter J. Rosado, Michael T. Sawada, Ronald B. Slater
- MATRIX AREAS: Robert M. Candelario
- EH&S Electrical Safety: Steven L. Chow
- Electronics Maintenance: Eric G. Henson
- Electronics Services: Bradley S. Bingham
- Fabrication: Cheryl S. Weldon
- L'OASIS: Nathan M. Ybarrolaza
- LSD-Human Geno[...]
- JGI-Walnut Creek: Greg D. Mannino
- NSD-88 Inch Cycl[...]: Charles P. Reiter
- Physics/Electronic[...]: Jacqueline C. Wy[...]
- Physics Microsyst[...]: Co Tran
- RF and Instrument[...]: Marek E. Szajbler

INTEGRATED CIRCUITS — Peter Denes
- Robert Abiad (G), Julien L. Fleury (G), Dario Gnani, Armin Karcher, Bradley N. Krieger, Abderrezak Mekkaoui, Jean-Pierre Walder; Bob Yi Zheng, Anita Whichard

SEMICONDUCTOR DETECTORS — Paul Luke
- Mark Amman, Stephen E. Holland; Guobin Wang, Julie S. Lee, Nicholas P. Palaio, Richard H. Pehl (G), Craig S. Tindall

SOFTWARE ENGINEERING — H. von der Lippe (T/A)
- Bio-Instrumentation: Earl W. Cornell, Lee Lisheng Yang
- CXRO: Robert F. Gunion
- GRETINA: Carl A. Lionberger
- JGI/PGF Instrumentation: Paul J. Barale, David E. Humphries, Christine L. Naca, Steven E. Wilson, Karen Zakaria

Abbreviations
Cnt = Contract
CS = Consultant
G = Guest
L = Leave
M = Matrix
Ret = Retired Retiree
S = Student
T = Telecommute
T/A = Temporary/Acting

Key
Dark Red = Deputy Director
Red = Group Leader
Blue = Supervisor

ESIE Org Chart MARCH 2009

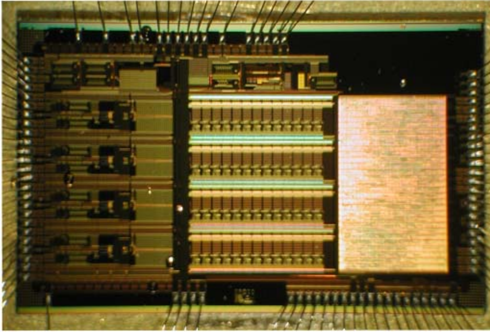
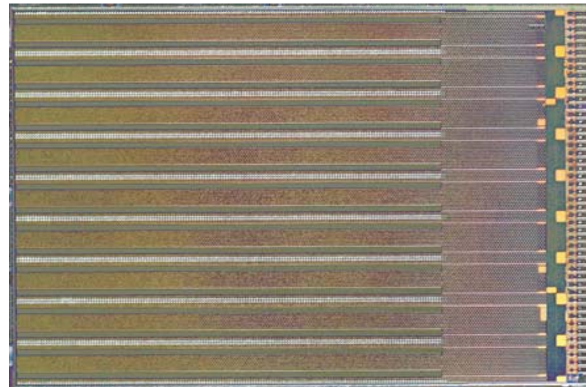
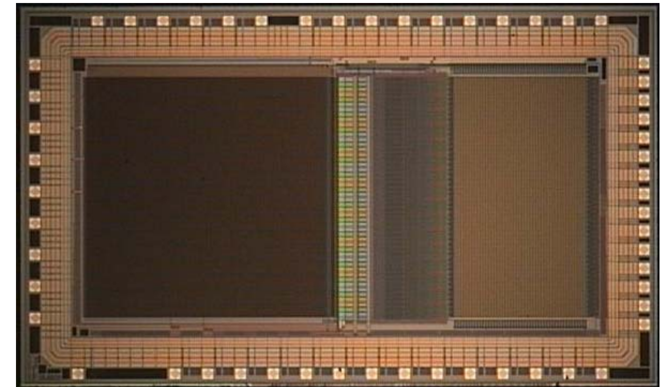
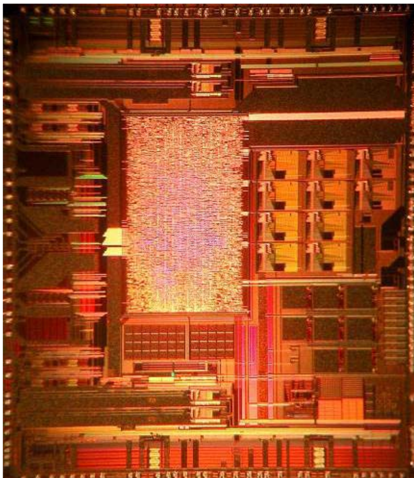
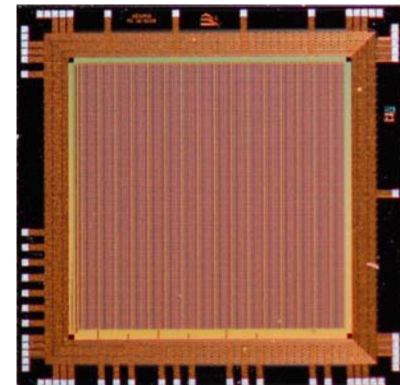
Portfolio

- **Integrated circuit *design***
  - **Pure analog (almost none)**
  - **Mixed mode – some digital (majority)**
  - **Mixed mode – a lot of digital (some)**
  - **Pure digital (none to date)**
  - — **Commercial fabrication**
- **Solid state detector *design***
  - — **In-house and commercial fabrication**

Steve's talk

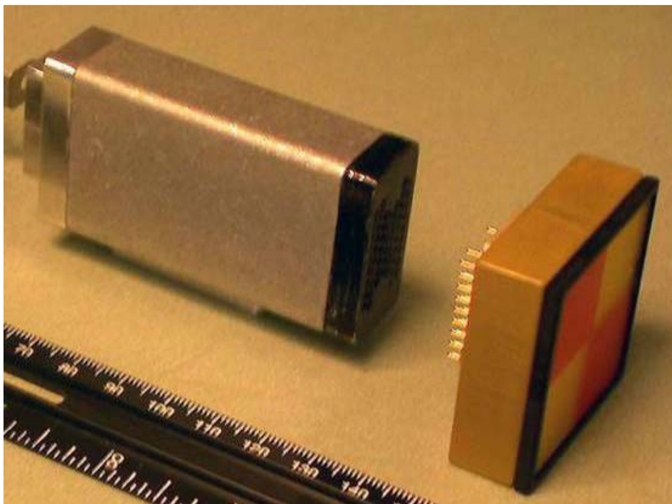
- **Discrete electronics**
  - **Pure analog (front-ends)**
  - **Mixed mode – some/lots digital (majority)**
  - **Pure digital (back-end readout / trigger)**
- **Hybrids, complex assemblies, etc.**

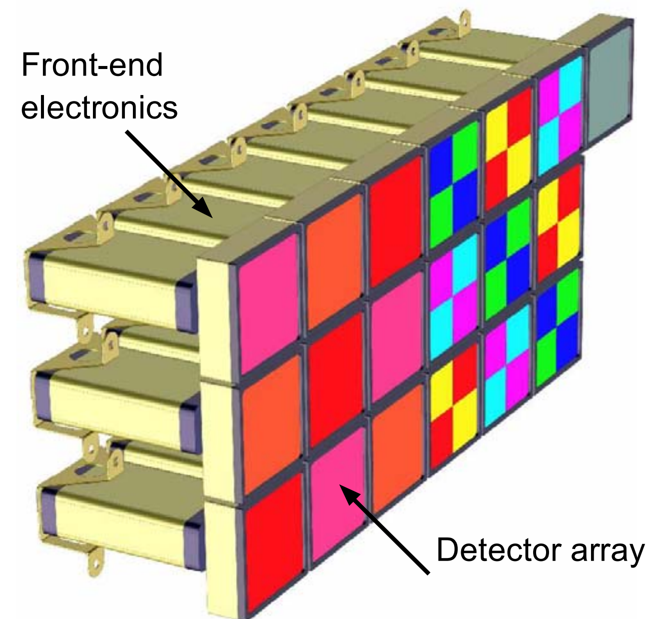
Current HEP IC Activities

ICs for CCDs	ICs for Next Generation Hadron Collider Pixels	ICs for Next Generation Lepton Collider Pixels
		
		

CCDs

- Photons → bits
- Cold, low power operation
- Suitable for space



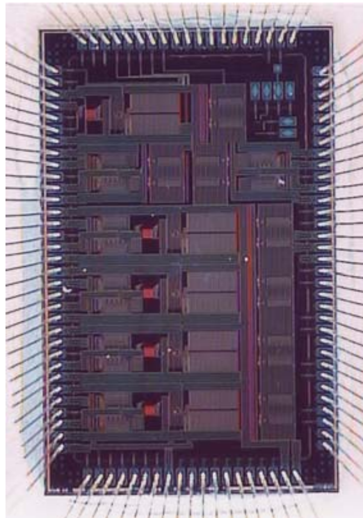


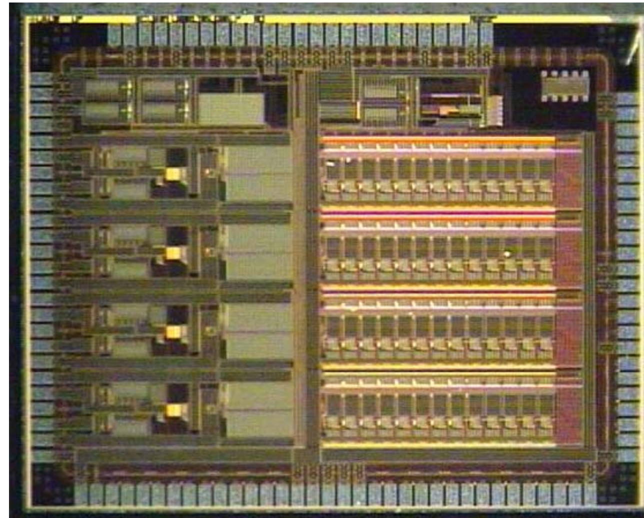
Design Challenges

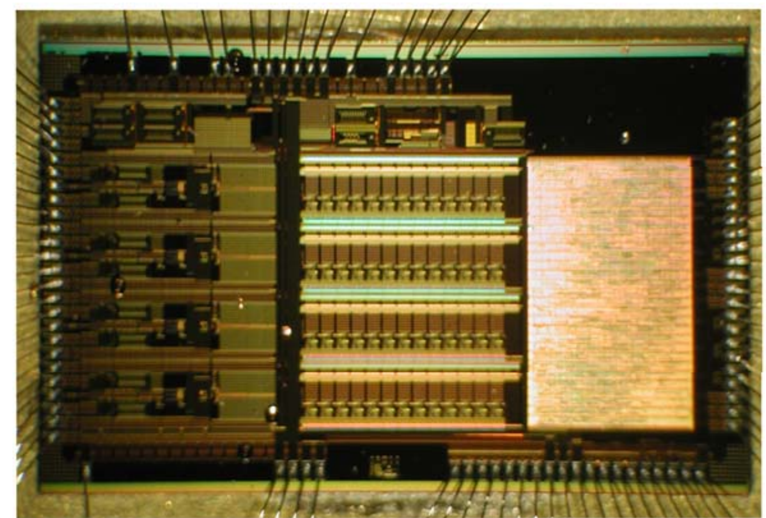
- **Excellent S/N**
  - — **Long integration time → low temperature operation to minimize dark current**
    - **Electronics has to operate at 140K, *and* at room temperature for testing and characterization**
  - — **Low noise: 2 e^- from CCD ⊕ 2 e^- from readout**
  - — **16 bit dynamic range**
- **For use in space**
  - — **Low power**
  - — **Suitably radiation hard**
- **Minimize I/O**

Readout IC (CRIC)

- Architecture study
  - Floating-point (multi-slope) integrator with built-in CDS
- Pipelined ADC
- Autonomous (digital control, correction and calibration; clock generation [programmable]; test functions)







CRIC

Conv
Timing generator
Vin
Ref gen
CRIC 3
Comp
14 stage pipeline ADC
Digital delay
Digital calibration
Digital correction
ADC value
ADC calibration engine
Configuration interface
SDO CK DI DO

CRIC 1
CRIC 2
CRIC 3

- **Systematic design + extensive simulation**
- **Increasing complexity with each iteration**
- **Each iteration performed as expected**

CCD Clock and Bias

- Thick, fully-depleted LBNL CCD requires high (>5 V) voltage clocks (+ and −) and supplies
- Parallel CCD clocks are high capacitance loads
- To maintain 2 e^{-} noise from CCD requires low noise supply voltages
- Initial goal – 1 voltage and 1 clock in
  - — Ultimate compromise, a few voltages and 1 clock

Clock IC (CLIC)

Parallel Clock Driver a

Vog Generators

Serial Clock Driver SW RG pos

Digital Logic

6 bit DACs

Serial Clock Driver Ha Hb

CRIC 3.3V Generators

Vr Generator (M15V)
VDD Generator (M25V)

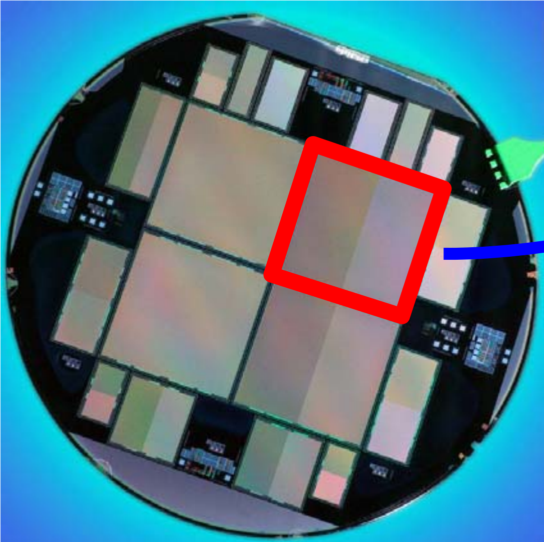
Serial Clock Driver SW RG neg

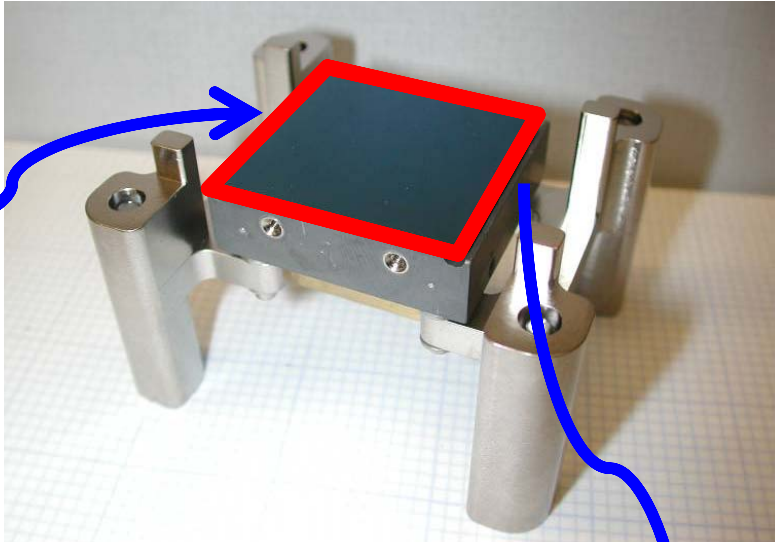
VSub

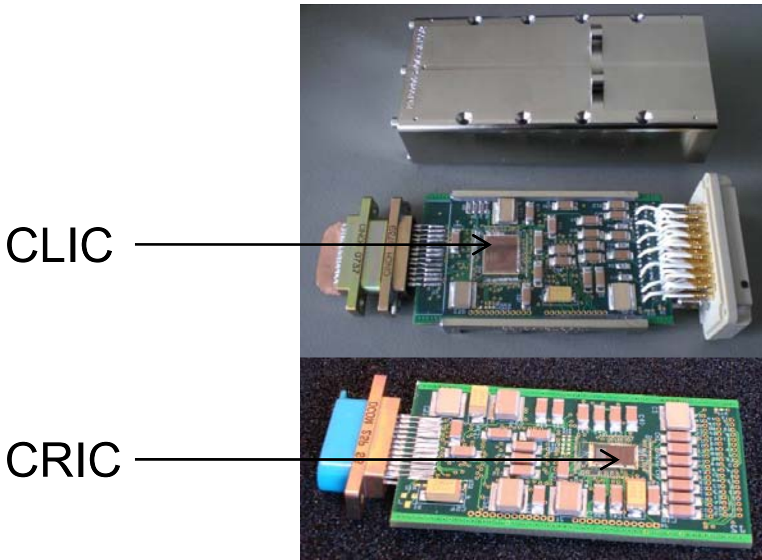
Vog Generators

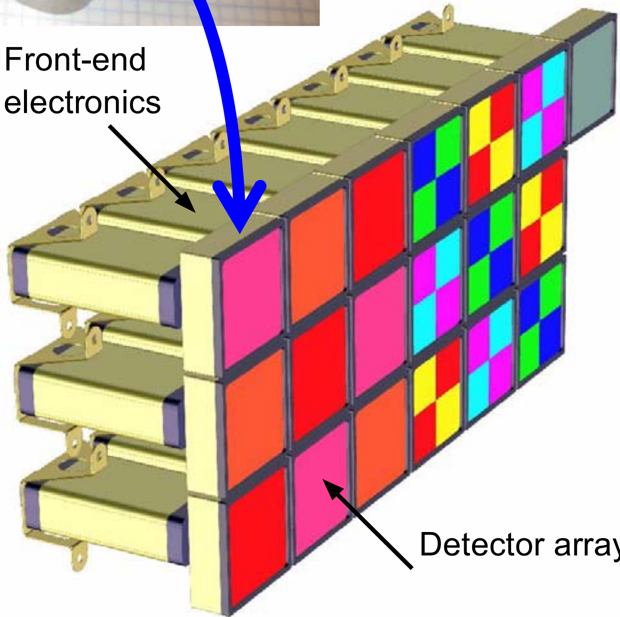
Parallel Clock Driver b

Put it all together









Future CCD Electronics R&D

FY10.

- Add additional circuitry and internal switching to the CRIC input stage so that it supports both p-channel and n-channel CCD types.
- With enhanced funding, we want to start study and design of larger channel count CRICs to support the current LBNL effort (and by others) for CCDs with many output ports.

FY11.

- Analog design work to extend CLIC to p-channel and n-channel CCDs – may require two flavors of ASIC.
- With enhanced funds, submit n/p-channel CRIC.

FY12.

- VHDL design of more flexible and capable CLIC clock pattern generator.
- Fabricate n-channel CLIC
- With enhanced funding, we want to extend the dynamic range of the CRIC to support multi-object spectrographs.

Future Hadron Collider Tracking Detector R&D

- Advances are needed to enable the next generation of detector for HEP experiments

- <u>Lower cost for same performance</u>
  - Impossible to build much larger detectors without this
- <u>Lower mass and power</u>
  - Detector mass limits the physics reach
  - This area includes more efficient power distribution as well as higher performance cooling
- <u>Greater rate capability and radiation dose tolerance</u>
  - Essential to take advantage of higher intensity accelerators.
- <u>New functionality</u>
  - The more information acquired the greater the physics reach
  - Includes "detector intelligence" eg. for momentum triggering.

- The LBNL R&D program consists of specific items always with these goals in mind

Integrated Circuit Design

- IC design is central to the LBNL R&D program.
- IC technology touches on all roadmap goals: cost, power, rate, radiation, and new functionality.
- Therefore, IC developments drive or enable other R&D areas.
- LBNL started exploring the 130nm technology node for pixel readout as soon as the present ATLAS pixel chip was done (at LBNL).
- Launched the design of a next generation pixel chip in FY07.
- This work evolved into the FE-I4 design collaboration (LBNL, Bonn, for ATLAS upgrades CPPM, Genova, NIKHEF)
- NOTE: New ideas and exploratory IC design work are generic, but a full size pixel readout chip (the only way to really prove new developments) can only be produced as part of a project.
- We are now starting to explore technologies beyond 130nm for further advances in pixel readout.

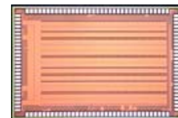
FE-I4

- FE-I4 will be the largest HEP IC to date
- This will significantly reduce the cost of future pixel detectors
- (Bump bonding flip-chip cost is per chip, not area)
- In addition, FE-I4 represents a x3 increase in rate and radiation hardness.

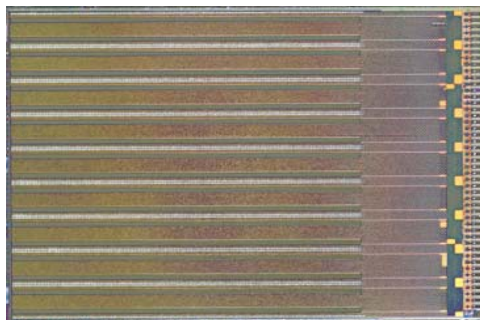
(all images to same scale)

130nm Demonstrator test chips

FY07



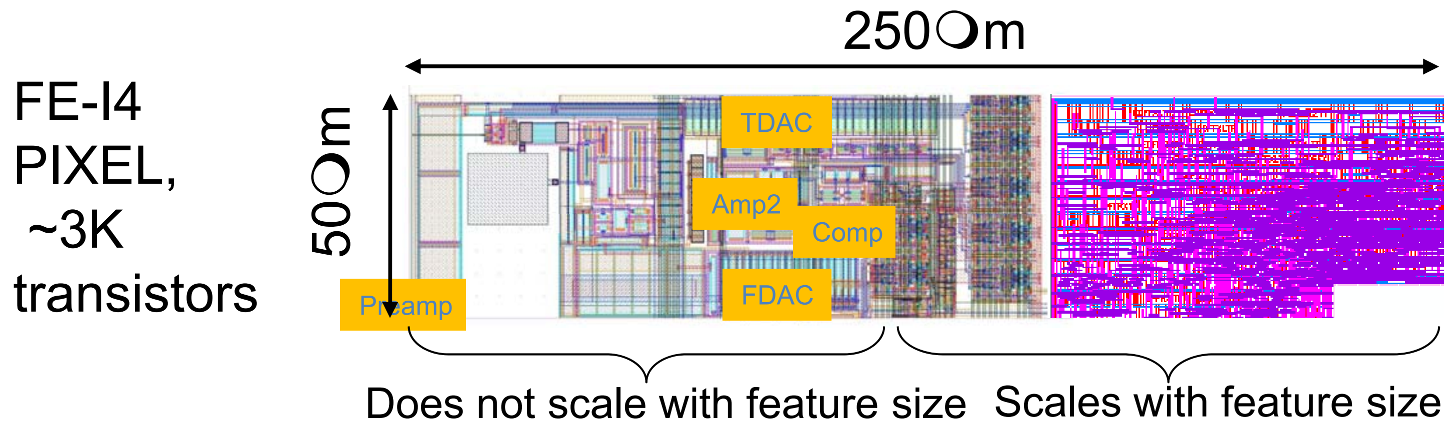
FY08



FE-I3 (in use in ATLAS)

FE-I4 to be fabricated in FY10

Future Pixel ICs



Design saturated with analog part.
Need to INCREASE digital functionality
at higher rate (more memory)

Target size for ATLAS Phase II

- Higher rate demands smaller IC pixels to avoid "pileup" inefficiency
  - Also sensors want smaller pixels will tolerate higher radiation dose
- These smaller pixels must pack more digital memory and processing (due to the higher rate)
- Two options to explore
  - "Conventional" smaller feature size (follow Moore's law)
  - 3-D electronics

Smaller Feature Size

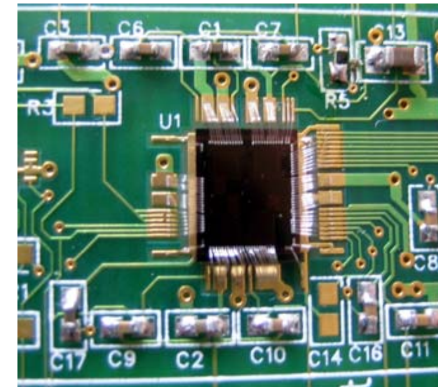
- This is the more conservative option because it relies on mature industrial technology.
- Has the problem that analog circuits do not scale down with feature size beyond 130nm.
- The proposed solution is to reduce the analog performance and compensate with added digital processing.
- FY10: submit technology exploration test chip in 90nm or 65nm (TBD). Test and refine analog designs in FY11, 12
- FY11-12: submit technology exploration test chip in 45nm. Evaluate radiation hardness of high K dielectric + metal gate

3-D Electronics

- Industry is increasingly adopting 3-D integration of ICs for certain applications, but technology is not yet mature.
- Two directions: 3D SOI (see below) and 3-D multi-project submission organized by FNAL, launched in May 09.
- Over half of the test chips in the FNAL run are based on variations of the FE-I4 analog pixel (3 France/LBNL chips and 1 FNAL chip).
  - Visitor from France spending the year at LBNL to work on 3D
- FY10: test first 3-D prototypes and continue collaboration with French labs for further iteration, including new amplifier design for smaller pixels.
- FY11-12: Further iteration probably needed. Compare merits of 3-D with small feature size as the better option for the next generation of pixels. Possible connections to new functionality.

DC-DC Conversion

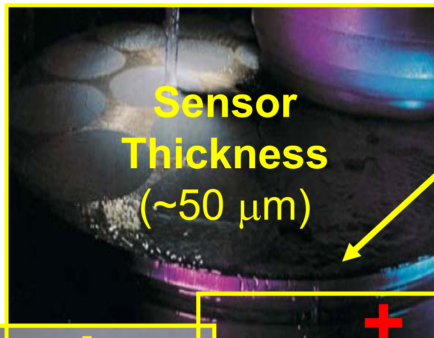
- As detectors grow larger, power distribution inefficiency brings an important mass penalty
- LBNL led the development of low mass, rad hard DC-DC converters, starting in FY06 with switched capacitor devices.
- FY07 x4 prototypes were provided to ATLAS and CMS groups for testing, and published in IEEE TNS.

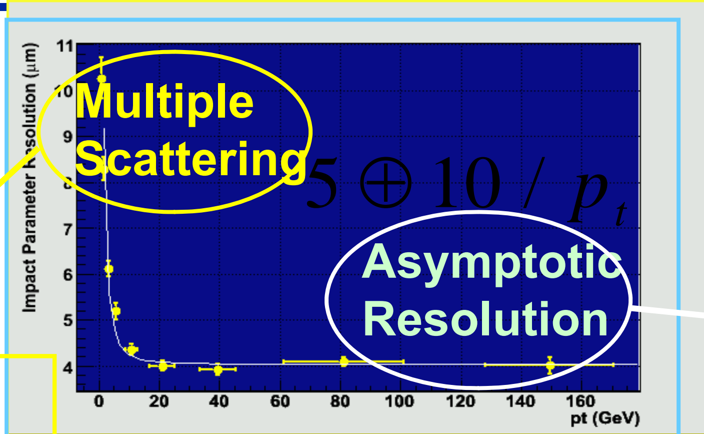


x4 DC-DC
0.5A, 15mm x 15mm

- Following this work, turned to first development of x2 internal converter for HEP chips.
- FE-I4 will be the first HEP chip to include an internal DC-DC converter.
  - This concept has now been adopted by other ATLAS and CMS groups for their future chips (pixels and strips)
- FY10: Test internal converter in FE-I4 vs. radiation dose
- FY11-12: Explore standardization of internal DC-DC conversion for smaller feature size technologies.

Future Lepton Collider Tracking Detector R&D



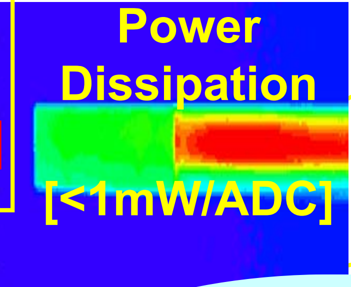


Pixel Size (10-20 μm)

S/N + Cluster Size

\+ Ladder Support

\+ Services Cooling [80 mW/cm²]

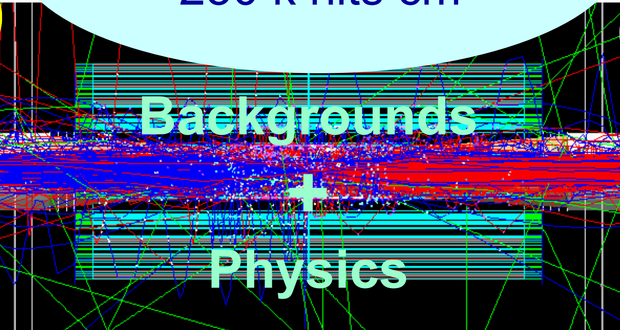


ADC Resolution [~5 bits]

Readout Speed [25-50 MHz]

Airflow removes
70-100mW/cm²
< 0.5 mW/ADC

5 hits/BX
X 9 (20 μm pixels)/hit
= 250 k hits cm^{-2}

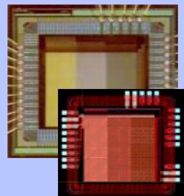


25 MHz r/o
25 μs/512 pixel col
O(1 %) occupancy

(demonstrated)
[R&D in progress]

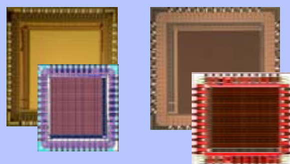
Monolithic Pixel Work for Last 3 Years

Thin CMOS

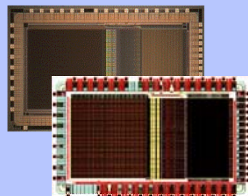


AMS 0.35μm-OPTO

• **LDRD-1** (2005)
10, 20, 40μm 3T pixels



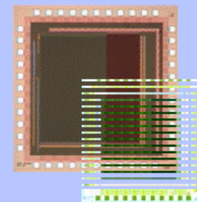
• **LDRD-2** (2006)
(+ LDRD-2RH(2007))
20μm pixels,in-pixel CDS
(+ RadHard pixels)



• **LDRD-3** (2007)
20μm pixels, in-pixel CDS
on-chip 5-bit ADCs

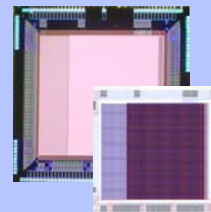
SOI

OKI 0.15μm FD-SOI

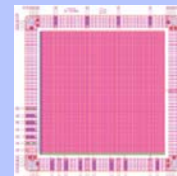


• **LDRD-SOI-1** (2007)
10μm pixels,
analog & binary pixels

OKI 0.20μm FD-SOI



• **LDRD-SOI-2** (2008)
20μm pixels, in pixel CDS
fast binary pixels

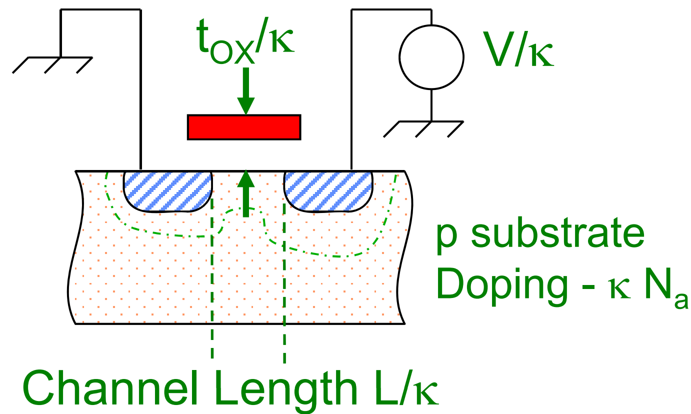


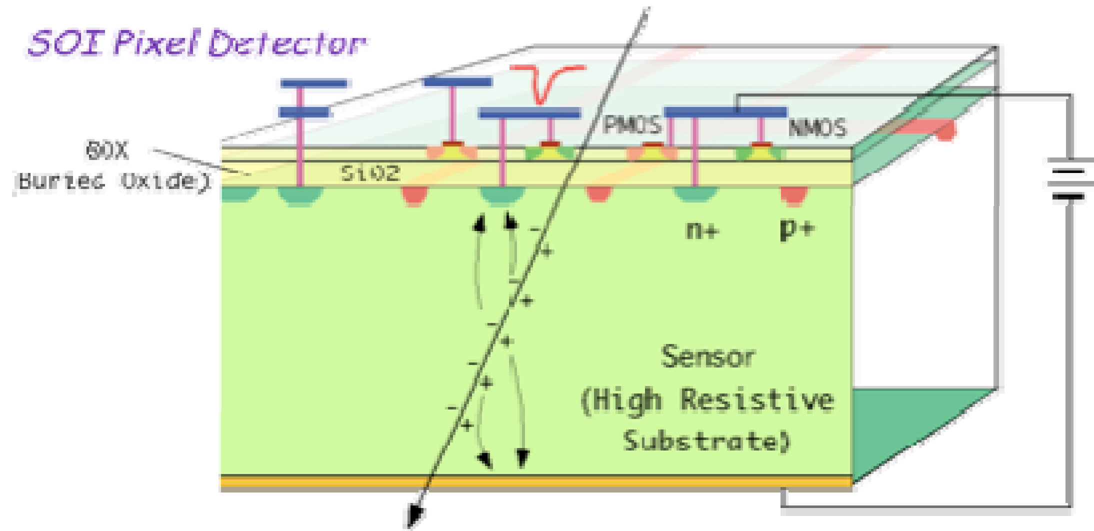
• **SOImager** (2009)
~13μm pixels, 4x4 mm^2
imager w/ fast readout

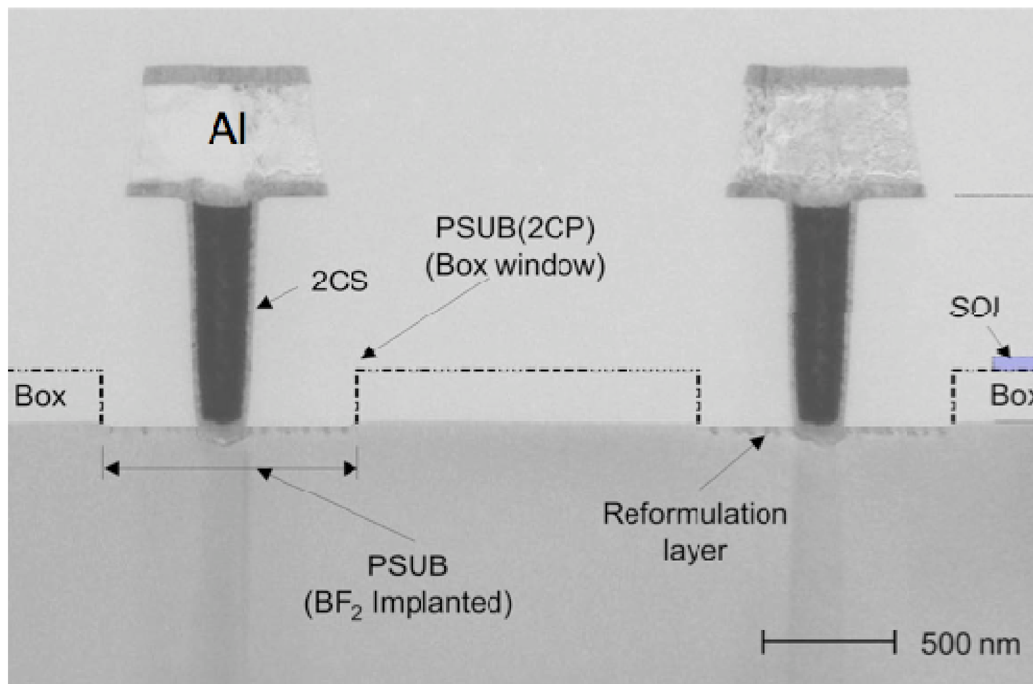
Approach and Accomplishments

- Push bulk CMOS APS to logical limits
  - — Demonstrate speed and performance
  - — Demonstrate integration (on-chip, per-column 50 MHz ADCs)
  - — Work halted due to termination of funding
- New approach: SOI (see next page)
  - — Demonstrate speed and performance
    - Including “zero power” digital pixel
  - — 3D integration (as a detector) with high-ρ Si
  - — Successful collaboration with KEK
    - Partially supported by US/Japan funds

Silicon-On-Insuator







Via KEK – Oki FD-SOI process

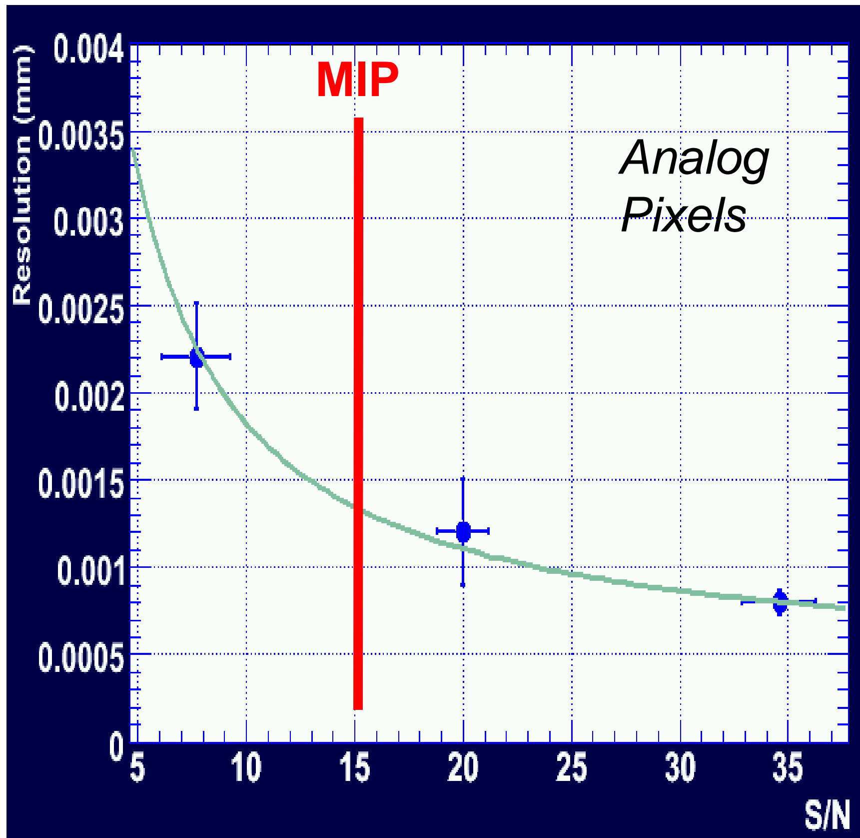
Contact to substrate
Other, subsequent, R&D

☺Low capacitance (excellent S/N)
☺Compact and simple

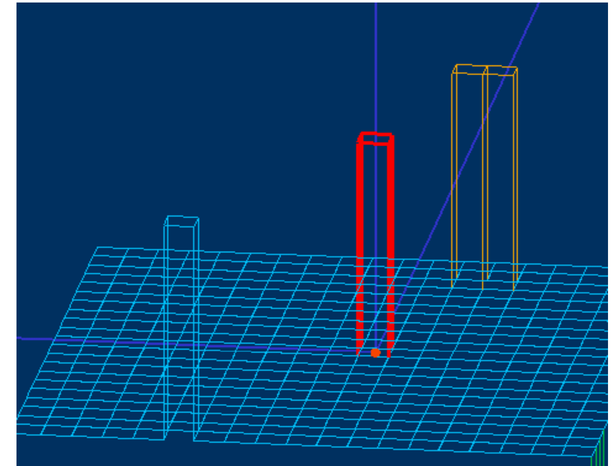
☹Sole source

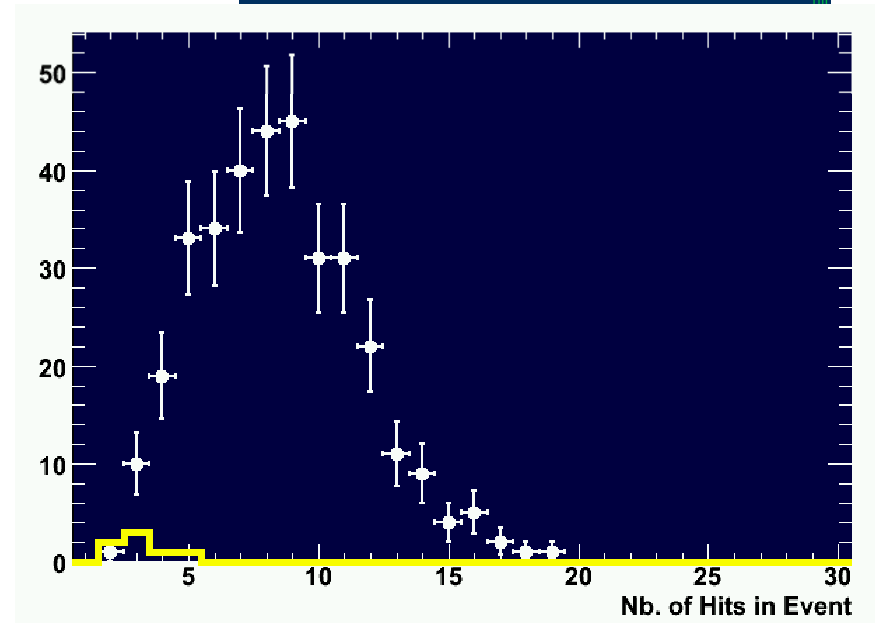
☹Back-gating
☹Radiation hardness

SOI Demonstrates 1 μm Position Resolution / Digital Pixels



Digital Pixels at ALS BTF





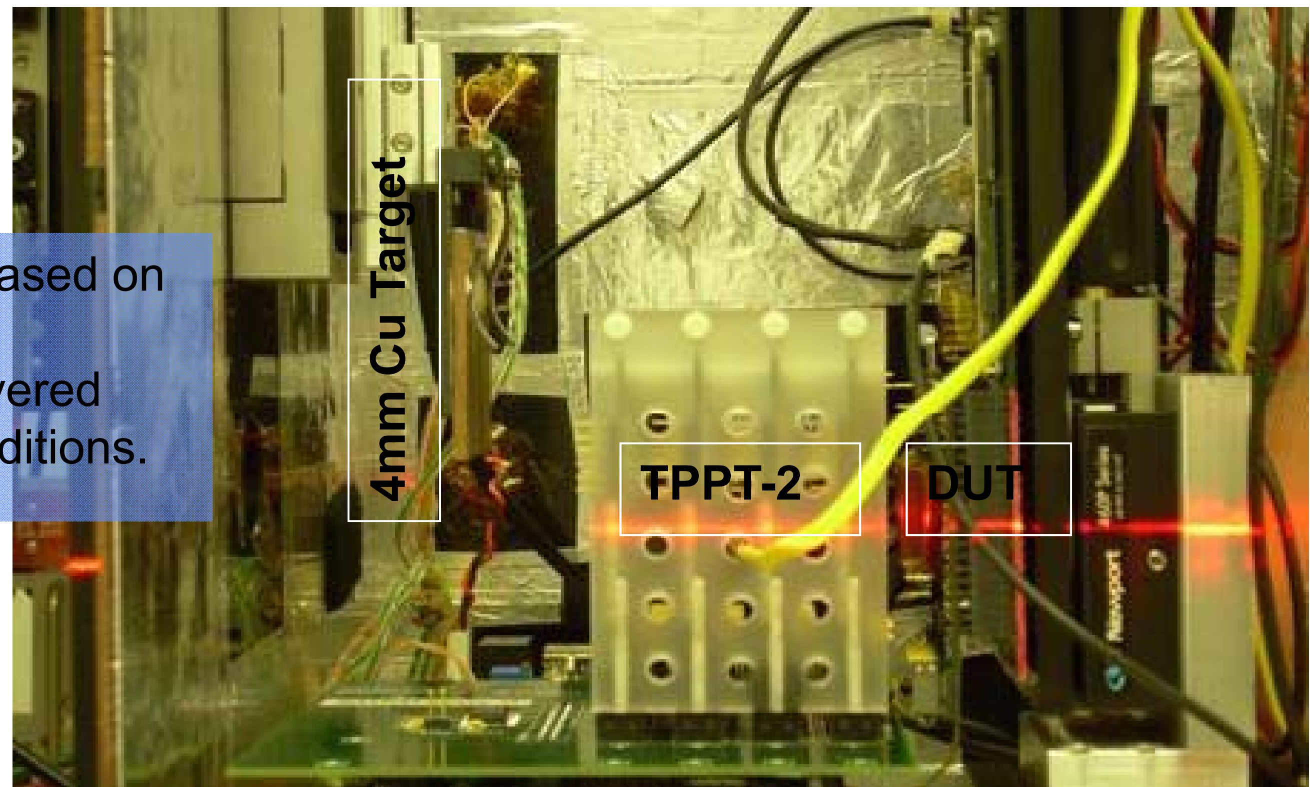
Scan with laser
vary power to simulate different S/N
cross-check with e^- beam

Thin Pixel Pilot Telescope

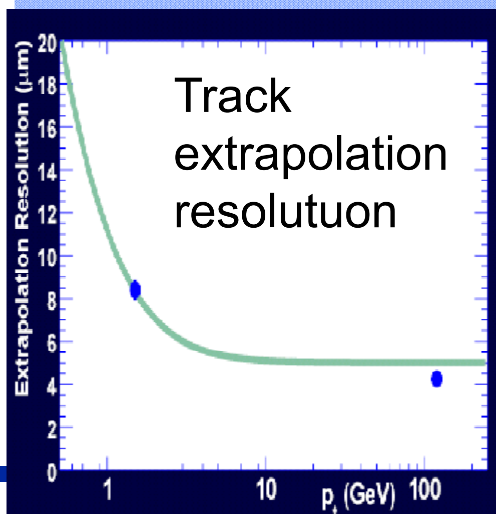
Develop Thin Pixel Tracker prototype to study operation and alignment, tracking capabilities in dense environment, vertex reconstruction accuracy with thin target, test new sensors;

Layout: 4 layers of 50 μm thin MIMOSA 5 sensors (17μm pixels) + reference detector;
Sensor spacing 1.5 cm

- First beam telescope based on thin pixel sensors;
- System test of multi-layered detector in realistic conditions.

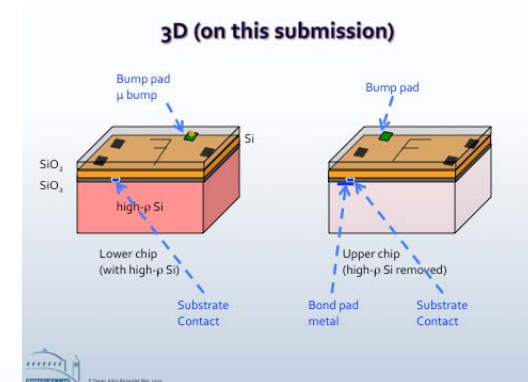


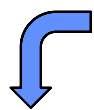
Beam: 1.0-1.5 GeV e⁻ from LBNL ALS booster at BTS
120. GeV p at MTest, FNAL



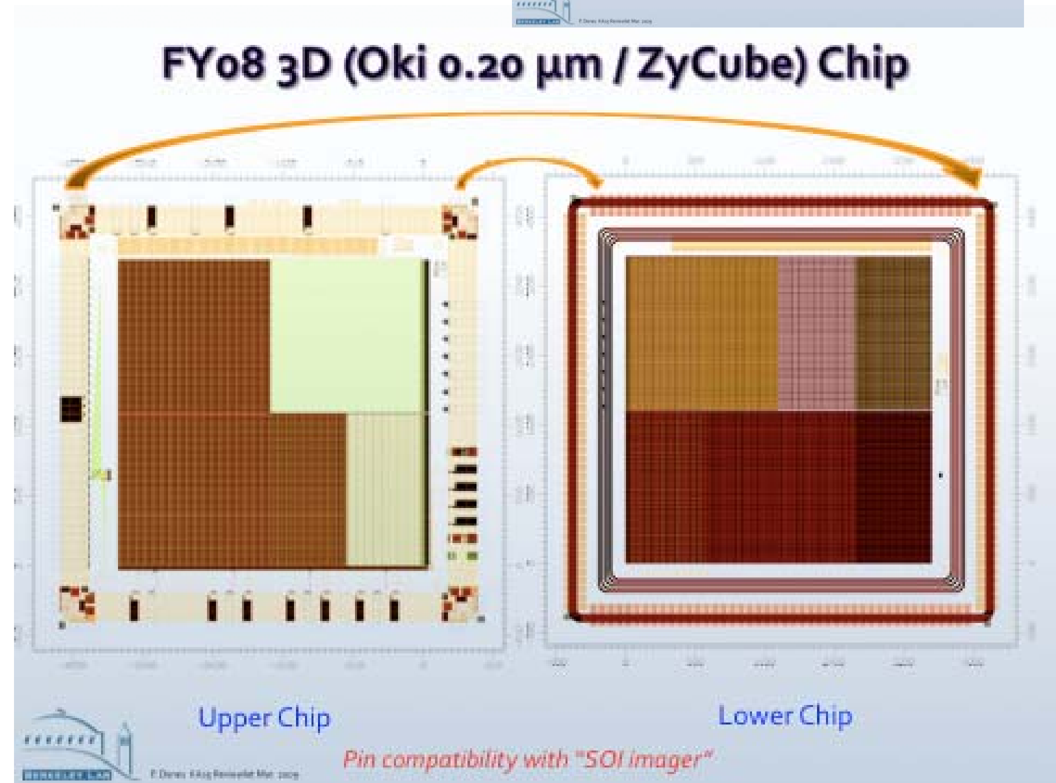
3D Silicon-on-Insulator

- **Use 3D technology to interconnect a "sensor" layer with an "electronics" layer**

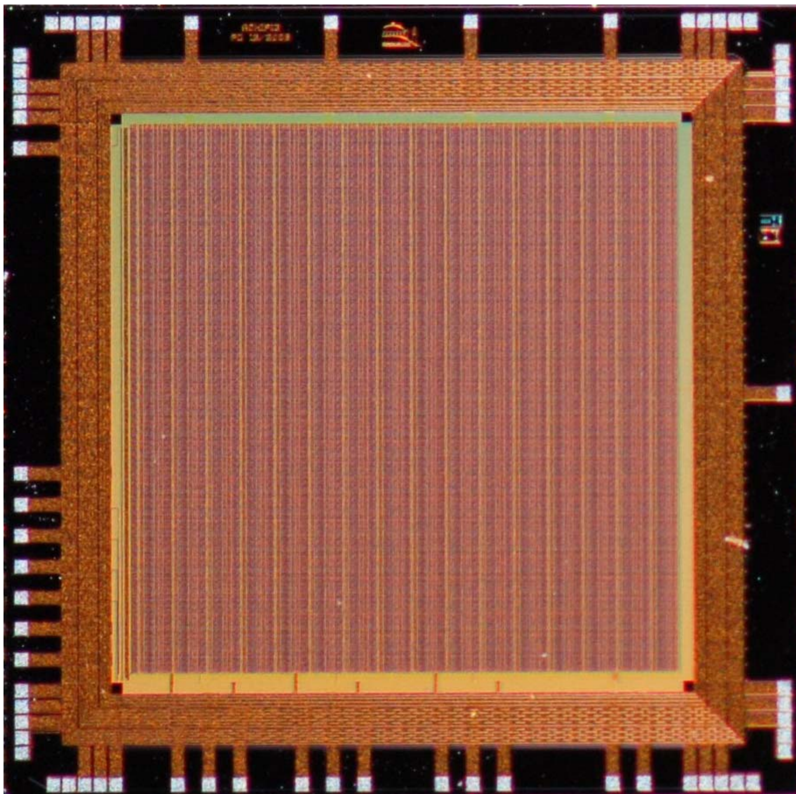




- **Chips back soon**
- **Several years of SOI R&D helps with conventional 3D challenges**



In addition to 3D Chip

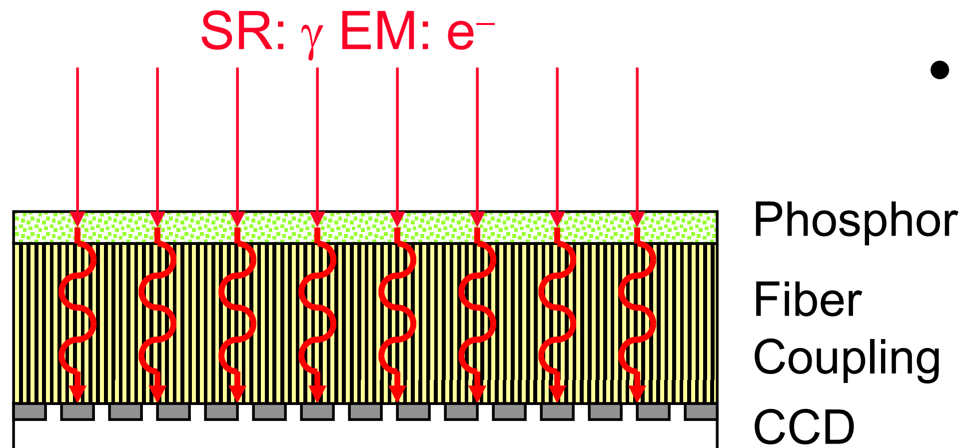


- 3D chip is on the same run as this medium size SOI APS (based on previous designs)
- Will be used to construct an SOI pixel telescope

Connections

- This collected expertise is also used to address detector challenges elsewhere in the Office of Science:
  - BES national user facilities at LBNL
  - Advanced detectors for NP (not so much IC, but other electronics, Ge detectors, …)
  - BER (ICs for PET)
- As well as other agencies and national/international WFO
- 2 examples from ALS and NCEM

Fast CCDs for Synchrotron Radiation Research



- **Original idea: “fast” CRIC**
- **LBNL CCD → direct detection**

- **Most common SR detector is a phosphor, fiber-coupled to a CCD**
  - **Also the standard EM detector**
- **Biggest impact: just make this faster!**
  - **$ spent to improve brightness lost in readout time**

Development of (almost) Column Parallel CCD

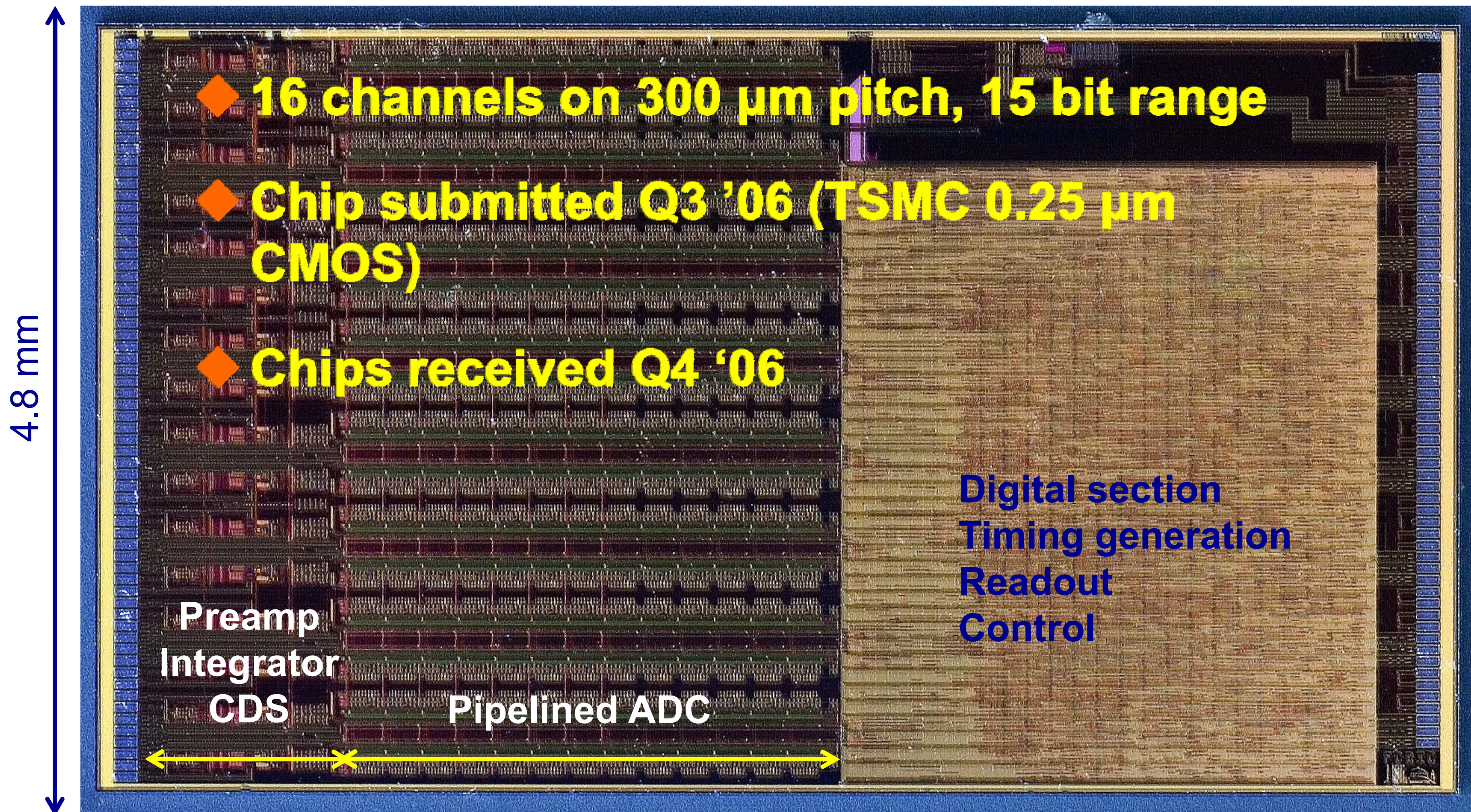
Constant
Area
Taper
Mini-shift reg.

Output stage

Mini-SR with taper
Metal strapping

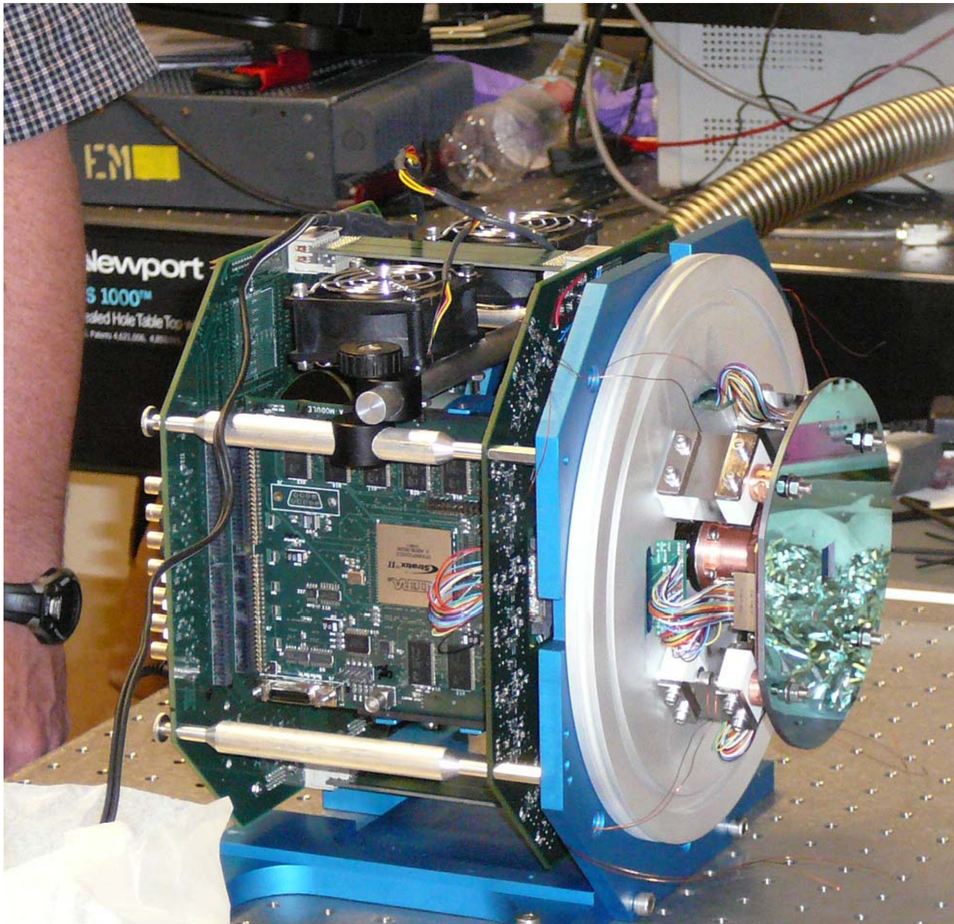
~300 µm pitch
bond pads
(wire-bondable)

fCRIC



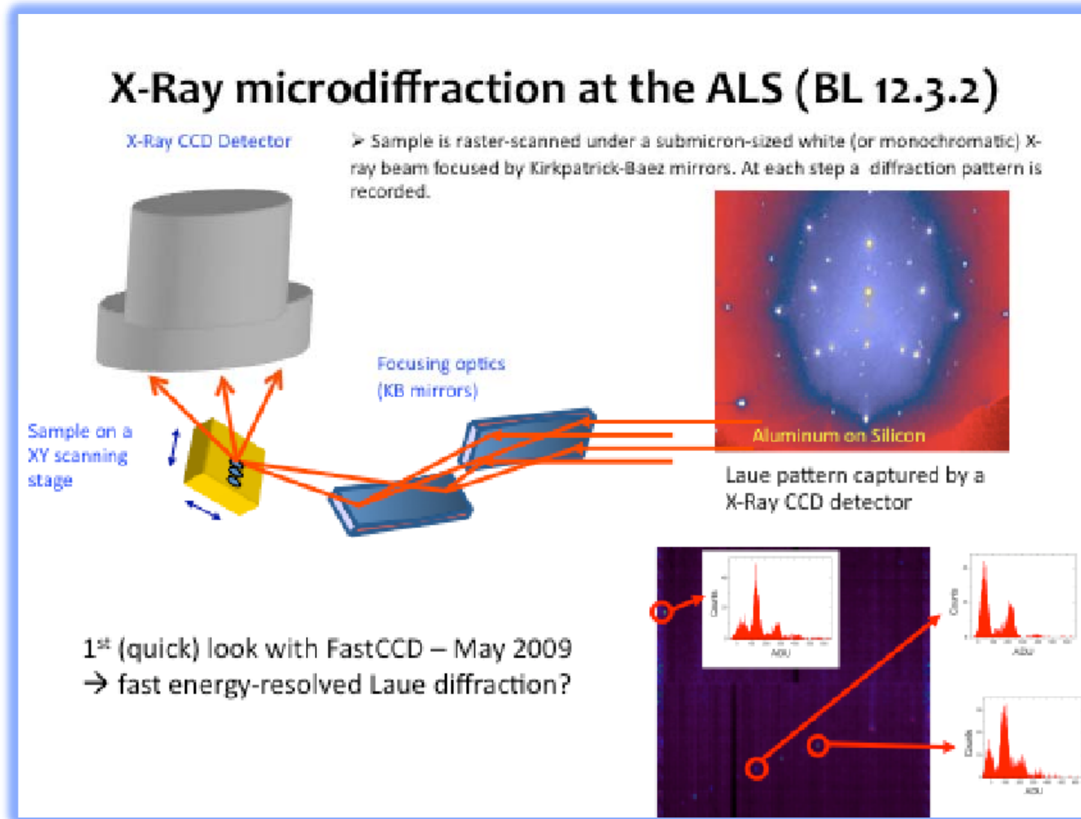
Developed at same time as CRIC3 – good synergy: at one point all of us were working on CRIC / fCRIC

Collaboration with APS



- **LBNL: CCD, fCRIC, “substrate”**
- **ANL: DAQ, software**
- **Systems for LCLS at SLAC**
- **BES ARRA funds for producing systems for ALS**

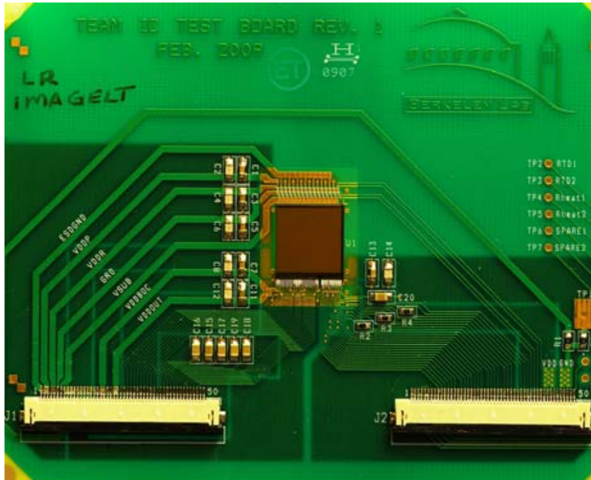
Faster *and* Better



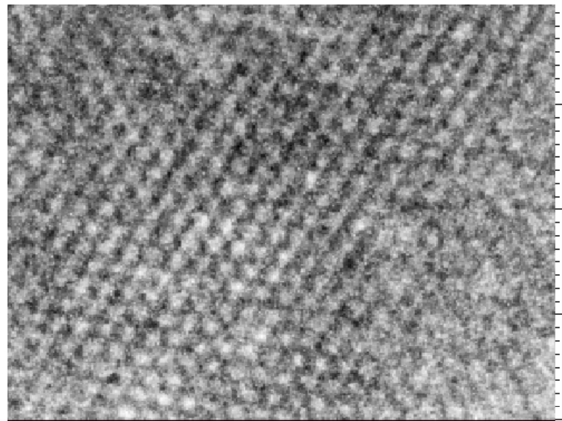
- 1st look in microdiffraction beamline
  - direct detection → energy resolution
- Next use at ALS = STXM
- Next use at APS = XPCS

BES Detector R&D proposal now funded

Detectors for EM



TEAM 1K on carrier



Atomic resolution image of Pb in Al matrix

- Developed for *TEAM* project
  - 1 Mpix in use now
  - 2 Mpix in fabrication (our 1st reticle scale chip – ATLAS next)
- Requires exceptional radiation hardness
- Feeds back into design for future lepton colliders
- HHMI funding for next generation

FTEs Drawing Transistors

9
8
7
6
5
4
3
2
1
0

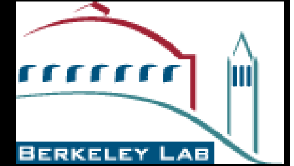
FY01 FY02 FY03 FY04 FY05 FY06 FY07 FY08 FY09

WFO
LDRD
NSF
BER
BES
HEP

Conclusions

- Long history of integrated circuit innovation at LBNL
- Critical capability for HEP experiments
- Substantial progress has been made on monolithic pixels and ICs for CCD readout over last three years – but there are many R&D challenges ahead.
- Ramp up R&D on ICs at ultra-high rate/high radiation.
- IC group has been typically 6-9 people. Strength in numbers (~everyone contributes to every project). HEP = 1.5 (min) – 5.5 (max) FTEs this decade
- Strong connections to other fields benefit HEP

Backup



Infrastructure

In addition to IC Designers and EEs

- Associates (board layout, coordination …)
- Technicians
- CAD tool / computing support

Laboratory investments

- *Significant* GPE investments in equipment for MSL (as well as bonders, probers, …)
- G&A pays for software and computing hardware
- Recharge pays for computing support

IC Design Software

- We use Cadence and Mentor (and MSL uses L-Edit)
- All of the cost is borne by G&A
  - Not KA15
- We are part of collaborations, and have to be software compatible

- We support a variety of CAD tools, with a wide range of costs