Electronics Production Status

K. Einsweiler, LBNL

Status of FE-I3 Wafer Probing:

- Probing results from first production run wafers.
- Next delivery under PO for remainder of production order

Summary of Off-Detector Electronics:

- Summarize ROD Rev E status
- Summarize BOC status
- Other Off-detector Electronics

Power Supply Status:

- Proposed schedule is PS FDR in June, PS PRR in Sept/Oct.

Status of FE-I3 Wafer Probing

FE-I3 Engineering run:

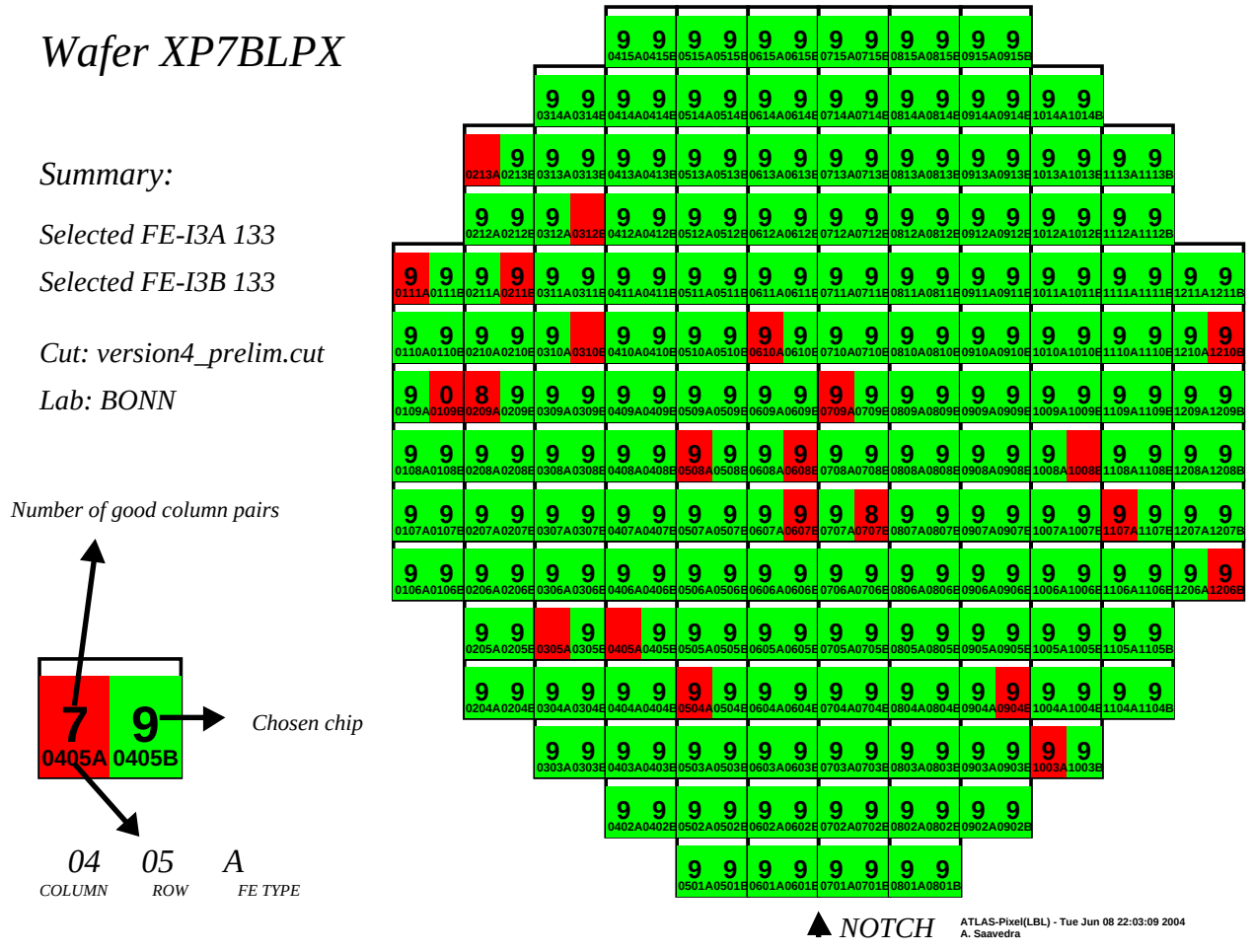
- This set of 3+3 wafers were probed with an early probing software chain, and therefore did not have the full range of cuts applied. Cuts were primarily digital.
- Additional cuts now applied include complete digital columnpair testing (TOT processor, all error bits), auto-tune threshold followed by complete analog scans testing TOT, plus FDAC, GDAC and TDAC performance. In addition, now do cubic fitting to VCal DAC, and real-time extraction of VCal and Capmeas corrections to generate calibrated thresholds for wafer analysis.
- In first batches of bare modules made with “A” series of chips (wafers from engineering run), do see defects that would now be eliminated. In particular, have seen several chips with column pairs with readout corruption (pass digital inject scans, but fail TOT scans), as well as a chip with a poor GDAC range.

FE-I3 Production runs:

- Software has evolved and stabilized over last two months. Have now reached a mature state, with well-defined cuts. There are presently about 90 cuts applied, covering every aspect of FE performance. Chips that get through this chain should really be good. Major improvement in LBL reliability was use of multiple needle touch-downs before beginning testing - this made probing much more reliable. Prior to this, we would make a second pass on each wafer, re-probing bad chips.
- First production run of 24+24 wafers is now almost completely probed. Bonn has probed all 24 wafers. LBL has probed 23 wafers, with number 24 running now. Bonn takes about 30 hours per wafer to probe, and LBL is a bit longer (use of commercial GPIB instruments instead of a custom probe card).
- Both groups can achieve a sustained probing rate of a wafer every two days. They have not been pushing this all of the time, because it did not seem to be the critical path. Note that with present yields in the range of 70-80%, a good wafer almost always has more than 200 good chips, or about 12 modules worth. Therefore, a wafer every two days implies about 40 modules/week per probing site.
- Have now received next production delivery of 48 wafers from IBM, almost 6 weeks ahead of schedule. On the original plan, there had been delays from mid-May to early July, due to long foundry turn-times (we were told to assume contractual maximum of 20 weeks). These delays were then reversed. We do not know yet whether the next delivery of 48 wafers will follow in July, or in late August. With present yields, either would be fine.

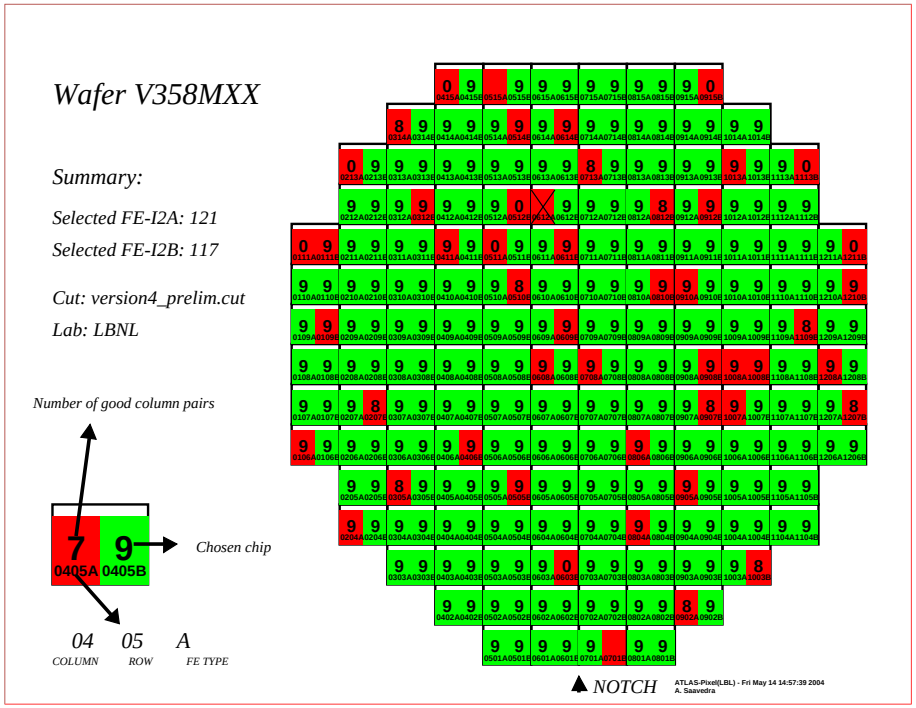
Results for first wafer from second production run:

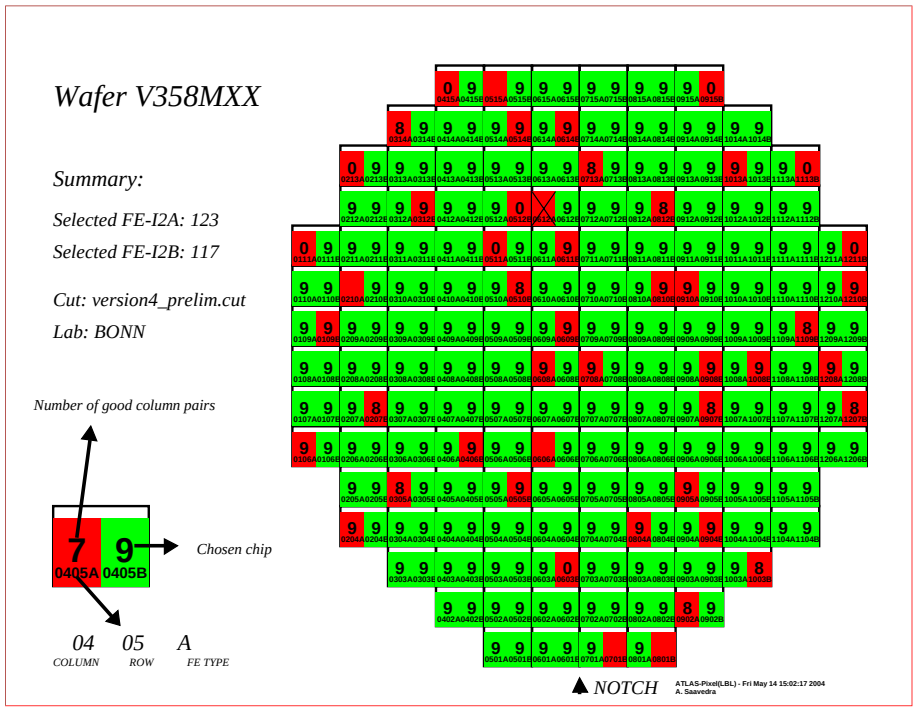
- Bonn has already completed probing their first wafer from the second production batch. LBL should start later this week.
- First results from Bonn are excellent, with an astonishing yield of about 92%:



FE-I3 Probing cross-check:

- Have recently taken one wafer probed at LBL, and sent it to Bonn for probing as well. Have carried out a detailed analysis of differences:





- Wafer map on left is original LBL probing (single pass), wafer map on the right is Bonn probing. LBL finds 238 good chips, Bonn finds 240 good chips (83% yield).
- If we take the union of these maps (chips found good by at least one site), we get 244 good chips, with LBL having 6 “false rejects” and Bonn having 4 “false rejects”.
- Differences in failed chips are minor and somewhat random. Typically they are currents just outside windows or number of good channels just outside windows.

- Have also systematically compared measured distributions for all variables for good chips. Found only three systematic differences. These include somewhat higher MonLeak DAC RMS for Bonn (not important) and somewhat higher threshold scan noise for Bonn (not important).
- The one significant difference found was in the external injection threshold. The present cut is wide enough to be insensitive, but the difference was large. As we would like to use the internal-external threshold difference as a measure of the true threshold of a chip, this is an important measurement. The problem was traced to the use of an old TPCC in Bonn which did not have the VCal buffer gain modification (change made in Summer 2002 by adding four resistors to board).
- This has now been fixed in the Bonn wafer probing setup, but all wafers probed up to now will have the wrong estimate for the external-internal offset. However, this difference has been found to lie around 1200 electrons in LBL (and now is apparently about 1000e in Bonn), so we will continue with our nominal threshold target of 4Ke internal, assuming that this really means 3Ke actual threshold. We may not ever use a value per chip for this offset, depending on how the offset varies during the production.
- A second wafer, originally probed in Bonn and then sent to LBL has also been checked. This wafer had a lower yield (about 70%), mainly due to Pixel Register defects. The agreement between the two data sets is quite good, but not perfect. This comparison is ongoing, but the agreement looks good enough for us to certify the production wafer probing.

- A Yellow selection to allow a few defects in the Pixel Register has been defined. In this case, chips passing all other cuts are selected, but the number of good column pairs must be less than 9. Several failing pixels are allowed, but all pixels are required to have the three critical control latchs (Mask, Kill, and Hitbus) always working to ensure there are no global impacts of bad pixels. For normal wafers, this gives about 3-5 additional chips (about a 1-2% yield increase). However, for one wafer with many bad pixel registers, 17 additional chips passes the yellow cuts, corresponding to an increase of 10% in the yield. For now, we do not plan to use any such chips in production.

Storage of results in PDB:

- Have now stabilized the data to go into the PDB (test status = R/Y/G, plus calibrations = 2 Capmeas, 4 VCal params, 1 offset param), and request has been submitted to Polina several weeks ago. For now, Aldo produces a table of these values for each wafer, for consumption by bare module probing sites.

Off-Detector Electronics Status

ROD Production:

- Have produced 25 “pre-production” RODs using Rev E design. Of these, 24 are presently working, and the final one needs a BGA part change for repair (maybe).
- The nominal allocation for pixels is 9 of these RODs. Seven have been distributed to the pixel collboration (Bonn, CERN, CPPM, Genova, Iowa, LBL, Wuppertal). The remaining two will be used for multi-ROD readout.
- All major orders for production quantities of parts (for both SCT and pixels) are out. Note that for the “big ticket” items (DSPs, FPGAs, memories), pixels is only allowed to order a quantity of RODs appropriate for a 2-hit system (86 RODs in operation, plus appropriate spares quantities).
- Have placed the PC board fabrication on hold pending resolution of two final sets of issues. This is a 100K$ order, and we cannot afford to make any mistakes. The first issue is a recurring VME problems seen by SCT in Cambridge with heavily loaded crates, which is proving difficult to reproduce and isolate. The second is an occasional problem seen when using the optimized assembly histogramming code, that is most likely software, but until it is proven to have disappeared, it could still be hardware related. Expect to release the board order for production fairly soon (few weeks at most).

BOC Production:

- Initial order for 10 pre-production (BOC Rev C) boards placed by Wuppertal. Component orders significantly delayed by decision of Wuppertal to go through CERN for parts orders. No estimate for delivery of loaded boards yet.
- Have borrowed one SCT BOC (Rev B) from Cambridge for the CTB operation for this year. Cambridge seems willing to help us by loading two boards for us through their production vendor. This would give us limited opto-link capability in our system tests in Genova and LBL, and is quite important.
- Wuppertal needs to complete development on “personality card” which will map data links correctly for different pixel configurations. Peter Gerlach has been working on this, but do not know the schedule.
- Orders for boards and parts for full 2-hit system need to go ahead soon (by June at the latest ?). Particular urgency should be given to orders for PLDs that are almost obsolete.

Readout Link Production:

- ATLAS is expecting the pixel community to pay approximately 50 KCHF for their share of the readout links (recall this is a standard CERN item now, whose cost is shared between TDAQ and sub-systems).
- They need a pledge letter fairly soon, but understand that money will be borrowed from CERN and paid back after 2007. Pledge letter is just a committment to pay back...

TIM Production:

- Final model of TIM is working in UCL (TIM3B). The PRR is now scheduled at CERN during the June SCT week (when no-one from pixels is available to attend...)
- Will discuss availability of one such TIM for final evaluation. In the mean time, expect that only the one old TIM1 is needed for the CTB until the TIM3B is in production. The TIM1 has been delivered to Genova already.
- UK will deliver tested production boards to pixels towards the end of this year or early next year. Price still to be negotiated.

VME crates:

- Eight production VME crates ordered for use in USA15 for pixel DAQ. Delivery presently scheduled for July at CERN. Propose to store them in the pixel lab. There will be a common spare crate for pixels/SCT, and two common spare power supplies.

Backplane Production:

- Final model of backplane has been developed, but is still under evaluation.
- Have one earlier prototype, and hope to get a second one that should serve pixels until the production versions are available.
- Expect production late this year. Consider these as part of production crate.

Power Supply Status

Components:

- **Module LV supplies:** presently most promising candidate appears to be Wiener PL6021 crate system, which includes 12 channels of 12V 11.5A power supply in a CANbus controlled 3U crate. Wuppertal and LBL are each waiting delivery of complete crate in early June. Evaluation to be done by Wuppertal and Milano.
- **Module HV supplies:** presently most promising candidate is ISEG 16-channel system. This has recently been upgraded for pixels to include a current limit mode as well as the standard current trip mode. First two prototypes have just recently been delivered to CERN. There is a competing offer from CAEN, and a first prototype module, operating in an SY1527 mainframe, has been delivered to Genova. Evaluation for both ISEG and CAEN prototypes is proceeding in Genova.
- **Opto-link supplies:** SC-Olink design is essentially complete at Wuppertal. They have provided first DCS/ELMB controllable prototypes in April. The spec is presently being revised so that I(VVDC) = 0.8A, V(VVDC) = 10V, I(VISET) = 20mA, V(VISET) = 5V. These are the specs for the SC-Olink supply from Wuppertal, and they have been agreed to by the opto-link community, and Danilo has recently updated the services documentation.

- **PP2 Regulator system:** Milano has developed two generations of regulator boards. They have delivered several copies of a first version of the PP2 crate and controller board for system testing.
- Initial testing of new regulator board indicated acceptable performance in single-module mode.
- Controller board is being upgraded from present “dumb” version with parallel port interface to more intelligent version with FPGA and ELMB/CANbus interface. First prototypes should be tested in late June in Wuppertal by Milano developers.
- Major issue at the moment is instability observed in PS irradiation. More information and testing on this issue is urgently needed. Attempting to reproduce this result in the lab in LBL using system test setup.
- Design and specifications for the production version of this system are presently under revision, with promise of first release of schematics this month. This is becoming quite urgent.

Review Schedule:

- Prensently, PS FDR is scheduled for June 22 at CERN, and expect to have PS PRR in Sept/Oct.
- Prepared a “to-do” list recently for the FDR review, and Milano, Wuppertal, and LBL should all be working on their documents. Do not anticipate any major issues for this, except for the recent developments with the second generation regulator boards.
- Preparation for PRR is more complex, as we need to have complete system tests in place using pre-production components. The plan for this is that Wuppertal is the primary test site, and LBL is a second “back-up” test site. Preparations in both sites are well underway, but will not have complete systems until late June. It will be very difficult on the current schedule to have “pre-production” regulator boards and controllers integrated on this timescale.
- Note that this schedule means that production power supplies will only be available (at best) at the end of 2004.