delayed relative to plans for the preprototype ROD but will be on schedule relative to plans for the production ROD. The delay in the implementation model for the preprototype will result in a delay for the first preprototype articles by approximately two months. Because the baseline schedule contained a corresponding amount of float with respect to first use of the preprototypes, the final preprototype units should be on schedule.

complete.

UC Irvine

In addition to evaluation of hybrid implementation models, work at UCI in October included continued studies of a ROD implementation model using DSPs for decoding. A software upgrade for the decoder section of the ROD was completed. This software provides a good idea of the performance possible in a real DSP-based decoder in the absence of errors. Performance was acceptable. The ROD decoder software, as well as the DSP Direct Memory Access (DMA) as it is utilized in the ROD, were documented. Issues concerning ROD control were explored, *i.e.* functions that the host DSP in the ROD may need to implement. Cost and power estimates were revised to include the latest changes. The proposed SCT/Pixel ROD slot pinout was updated.

The simulation of input data used in studies of decoder performance was modified to simulate jet events. At this stage, for technical reasons in the simulation, the maximum occupancy for a simulated jet event is 3%. The decoder proves resilient to these 3% occupancy events, even at high rates (10% of events).

Data bus and DMA controller performance of the TMS320C62x DSP chip were studied using test programs, evaluation module, and oscilloscope. Some undocumented device behavior was discovered that must be considered during ROD design. Transfer rates between the TMS320C62x evaluation module and the host PC were studied. Rates may be sufficient to allow the PC to participate in emulation of the ROD. For example, the PC could simulate the host DSP in the ROD.

Pixel ROD numerology was studied. It was found that in most scenarios the number of pixel modules that can be serviced by one ROD is limited by Readout Link bandwidth. Mapping of SCT and Pixel input links into RODs was investigated for both 72 and 96 input link scenarios. Both scenarios contain some complex mapping, and neither scenario was favored over the other.

University of Wisconsin

VHDL coding has been progressing. This effort was centered on the decoder and FIFO. In parallel the behavioral model was written in C. One thousand events were run through both the VHDL and C models. The result of the two model are in agreement this give great confidence that they will performed as expected.

Design of the gatherer was done and VHDL coding was started. There is little doubt that the gathering function can be done in VHDL at this time.
Architecture for a hybrid design was completed this uses DSPs for the histogramming of calibration data and control of the ROD. The model is well founded and looks doable

1.1.3.3.7 Preprototype ROD

UC Irvine and University of Wisconsin
The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed above under WBS 1.1.3.2.3. The joint implementation model is

*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

1.1.3.1.1 Strip Test Beam Support

UC Irvine

Hardware and software support for laboratory and beam tests of SCT electronics and modules continued. New programmable logic (GALs) for the Silicon Low-Level Card (SLL) to be used with detector modules instrumented with ABC/D chips, as well as new system software for the DSP modules, were distributed to the SCT community, including users at LBNL, Freiburg, CERN, Melbourne, and Valencia. The new GALs and system software contain fixes for the subtle timing problem that was diagnosed with ABC/D modules last month. Timing Control Cards (TCCs) were sent to users upon request.

1.1.3.1.2 Pixel Test Beam Support

Fabrication of 8 PLL cards are under way. The parts and printed circuit cards have been ordered. These cards will be used for laboratory tests of the pixel electronics. This should be the last fabrication of testing hardware for the pixel electronics. There will still be software support needed in the future.

1.1.3.2.1 ROD Requirements

UC Irvine and University of Wisconsin

ROD requirements are largely complete. A review of the requirements for all components of the off-detector electronics is planned for November. Telephone meetings with UK collaborators working on other components were held in order to establish the requirements for those components.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No significant refinements of the essential model were made during October.

1.1.3.2.3 ROD Implementation Model

Development of the implementation model continues to be the focus of ROD design effort. Effort continued to focus on a hybrid approach in order to combine the best features of the FPGA-based and DSP-based approaches studied previously. The detailed assignment of tasks between FPGAs and DSPs was not complete at month's end, although the technology choice can be considered

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

Design of a new calibration plate continued with the idea of using precision dicing to eliminate the use of the calibration bar. Discussions were held with a photo-mask vendor concerning the production of this plate.

Results on module metrology at the Rutherford Lab were received and studied. Transverse precision was similar to ours but module thickness variation was outside specifications. We need to learn how to evaluate this parameter on our metrology system.

Assembly was completed on a single sided module using working detectors. This has been successfully connected to a partially loaded Cafe-M/ABC hybrid and bonded. The module can be read out. Noise measurements are in progress.

A summary report describing the results of precision dicing experiments was sent to the vendors under evaluation. Preliminary feedback was received.

1.1.2.3.3 Production

No activity.

1.1.3 Readout Drivers (A. Lankford/R. Jared)

Milestones	Baseline	Current	Status
*Select PreROD implementation	30-Oct-98	4-Nov-98	Delayed
*Requirements review	30-Nov-98	18-Nov-98	On schedule
*Compl. System design	28-Dec-98	28-Dec-98	On schedule
*System design review	11-Jan-99	11-Jan-99	On schedule
*Compl. PreROD design	29-Jan-99	31-Mar-99	Delayed
*Compl. PreROD layout	15-Feb-99	15-Apr-99	Delayed
*Compl. PreROD procure	1-Mar-99	30-Apr-99	Delayed
*Compl. PreROD PCB fab	16-Mar-99	16-May-99	Delayed
*Compl. PreROD 1st assemble	30-Mar-99	31-May-99	Delayed
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	15-Jul-99	Delayed
*PreRODs complete	20-Aug-99	20-Aug-99	On schedule
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule

Most of the redesign needed for the second prototype hybrid was completed this month. The full redesign however awaits the final layout of the new versions of the front end readout chips. Discussions were held with the vendor who will fabricate theses hybrids and a modified set of inks were chosen and the process was changed in order to reduce the observed mechanical bowing in these hybrids. A new ceramic substrate design was completed and sent to the ceramics vendor for fabrication.

1.1.2.2.2 Development and prototype fab

A number of ABCD chips were mounted upon hybrids and tested.

The Nusil, R2186-2 encapsulant was irradiated. It has not been evaluated after irradiation. Further tests on the Thermoset ME-730 suggest it may be however too viscous for our application.

An attempt was made to mount the kapton hybrid on a ceramic substrate. It was however damaged in the lamination process. A new, more gentle process, was suggested and will be tested in November.

Samples of the new suggested gold conductors for the next batch of hybrids were received and evaluated. Wire bonding appears satisfactory on these samples.

Ceramic substrates for the second prototype were received from the vendor.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98	Complete
Prototype tooling complete	1-Apr-99	1-Apr-99	On schedule
*Compl. Design of proto assy/test	14-Jun-99	14-Jun-99	On schedule
*Compl. Fab of tooling for proto	14-Jun-99	14-Jun-99	On schedule

This design review depends upon parallel progress in a number of institutes which are following the same process. Not all are up to the same level.

LBNL
1.1.2.3.1 Design of Assembly and Test

is believed that this metalization along with grounding the backside on the hybrid minimizes the effects of capacitive coupling of the circuits to the isolated substrate underneath. The ABCDs were found to show basic functionality after 10 MRad of protons. More detailed studies are continuing to test for any speed limits or other marginal performance after irradiation.

1.1.2.1.3 Production

Activity is continuing on establishing a Frame Contract between CERN and Honeywell and Temic. This would primarily be for our future production orders although even engineering and pre-production runs could benefit from volume pricing discounts depending upon what is finally negotiated. The initial Market Survey was sent out in August and replies were received in late September from both Honeywell and Temic as well as a few other vendors. We are finalizing the Technical Specification and the wording of the Invitation to Tender with the goal of getting that out in early November. The main issue in the Technical Specification with which we have been struggling for several months is a Quality Assurance clause. We have had preliminary discussions with the vendors but no consensus has been reached and it is also not clear if ATLAS and CMS (both parties to this Frame Contract) can agree upon what to negotiate. We have agreed now to issue the Invitation to Tender without any QA clause in the Technical Specification. This is to keep to the time tables dictated by CERN tendering rules. We will attempt to negotiate QA requirements during the negotiating phase of the tender process.

1.1.2.2 Silicon Strip Hybrids(C. Haber)

Milestones	Baseline	Current	Status
Preliminary design review	3-Aug-98	10-Jan-98	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	1-Jan-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Jun-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Jun-99	Delayed
*Compl. 2nd proto assembly	17-May-99	1-Jul-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	10-Jul-99	Delayed

The delay in obtaining working integrated circuits and in the design of the new set of chips will cause a delay in the Preliminary Design Review and in the 2nd prototype hybrids. This is because the hybrids need a stable chip layout to complete the design.

LBNL

1.1.2.2.1 Design

larger total doses. We put the CAFE-P submission on hold until we could better understand this problem. The data at this time indicates that the resistors change by up to 50% after 10 MRad of Co irradiation compared to less than 30% after 10 MRad of proton irradiation. It appears that this is not a dose rate effect but rather a difference between the Co gammas and the 55 MeV protons at the cyclotron. The CAFE-Ms are still operational after these large resistor changes. One with an exposure to 19 MRad of combined protons and gammas is still operational with only moderate increases to the shaping time. Simulations of the new CAFE-P also show the same robustness. Our plan now is to make a decision by mid-November on whether to slightly shorten the initial target shaping time to anticipate these larger changes or not and then to submit the CAFE-P for fabrication. The studies of gammas vs. protons will continue.

The ABC design has made progress but slower than expected. The problem of a stuck bit in one counter of the present design has finally been tracked down to a mask error. We are working with Honeywell to understand how that occurred in processing and how to prevent it in the future. The DCL speed problem now has a new design fix which is being reviewed and the front-end receivers and the command decoder have all been modified. RAL is starting to assemble the chip. One missing sub-circuit is the final layout of the improved DACs. The other fixes are being implemented in the full chip layout as it is being assembled. Another design review is scheduled for 17-Nov during ATLAS Week but it is not obvious that this will be the Final Design Review. Certainly the verification steps will not be complete by then and so another review will be needed later.

The re-design of the ABCD is making good progress now that the new DMILL Design Kit was received in September. Two new front-end designs are nearly complete and the back-end is complete with the exception of the modified command decoder coming from LBNL. A review of ABCD is also planned for ATLAS Week with the final review to be in December after all the verifications are complete.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

A lot of time was spent to understand the Maxim resistor changes under gamma irradiation as explained in the design section above. With the stuck bit (or "bit 6 problem") finally resolved to be a mask error, the testing of ABC functionality has been completed. Some more work was done at LBNL and UCSC to understand the operation of multiple CAFE-Ms and ABCs in modules. We have two modules working, one with CAFE-Ms and ABCs and the other with CAFE-Ms and the older CDPs, at and below nominal thresholds. We are now looking at subtle hybrid and IC interactions in an attempt to optimize the overall performance.

Four ABCDs were tested and irradiated at the LBNL cyclotron. These are from the second batch of fabricated ABCDs. Also, these parts had the backside of the wafers metalized before dicing in an attempt to see if that improved the stability issues seen on earlier tests. The tests did show much better operation with the backside metalization. It

Additional assembled hybrids were successfully mounted to a bare 16-chip module mounted on a support cared. At LBNL this was done with film adhesive that cures quickly at 60^{o}C. At Oklahoma this was done with double-sided tape. Wire bonding from the flex hybrid to the 16 front end chips was completed successfully. Preliminary tests indicate full digital functionality of most to all of the chips and tests at Oklahoma and CERN are underway(the module assembled at LBNL was transported to CERN to continue testing during the pixel week and ATLAS week meetings). These are the first functional ATLAS pixel modules. Additional test results are covered under 1.1.1.2.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	15-Dec-98	Delayed
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	15-Dec-98	Delayed
*Issue call for tender	9-Nov-98	9-Nov-98	On Schedule
*Submit 2nd ABC	16-Nov-98	31-Dec-98	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-98	Delayed
*Closing date for tender	21-Dec-98	22-Jan-99	Delayed
*Submit 2nd ABCD	27-Jan-99	31-Dec-98	On Schedule
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	On Schedule
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	7-May-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	21-May-99	Delayed
*Test systems complete	26-Apr-99	26-Apr-99	On Schedule
*1st ICs avail. For 2nd proto hybrid	18-May-99	26-May-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	21-May-99	On Schedule

1.1.2.1.1 Design/Engineering

LBNL & UCSC

At the beginning of October, some CAFE-M parts were removed from our ^{60}Co source where they had been placed to receive very low dose rates of gammas. We were surprised to find that the resistors had changed by an amount larger than we had seen for much

with passive components and the Module Control Chip(MCC) and attached to 16-chip FE-B modules flip-chip assembled some months ago by Boeing. This is a major achievement and represents the first successful prototype module fabrication by the pixel collaboration. The first full prototype modules with flex hybrids were assembled first at Oklahoma and then shortly thereafter at LBNL(and CERN after transport to the November ATLAS week).

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd,K. Einsweiler, M. Gilchriese)

Milestones	Baseline	Current	Status
*Compl. 1st proto. Design	29-Oct-98	30-Jan-99	Delayed
*1st proto. Design review	18-Feb-99	18-Feb-99	On Schedule
*Compl. Tests of 1st protos.	18-Mar-99	18-Mar-99	On schedule
*Select module type	18-Mar-99	18-Mar-99	On schedule
*2nd proto. Design review	17-Sep-99	17-Sep-99	On schedule

LBNL and Oklahoma

1.1.1.5.1 Design/Engineering.

We have put on hold the further design of fixtures for assembling flex hybrids, mounting flex hybrids to bare modules and for wire bonding and testing until experience is obtained with the first assembled module. The number of 16 chip bare modules is very small - only two are available and one of these has been sent to Oklahoma for their use. Thus the assembly of the first module will be done by hand without the use of fixtures. We do not expect a delay in completing the required tooling in time for a review in February 1999. Some fixtures are complete and the remaining fixtures are not expected to be complicated to produce.

1.1.1.5.2 Development and Prototypes

Flex hybrids were loaded with passive components at Oklahoma and LBNL. At Oklahoma this was done using conductive epoxy to mount the passive components. At LBNL it was done by soldering. At LBNL a stiffening piece of 5 mil Kapton was attached with film adhesive to the flex hybrid to make a more rigid structure for the very first attempts. At Oklahoma the hybrid was mounted on a thin aluminum plate. Module clock and control chips(MCC) from Genoa were wire bonded successfully to the hybrid, although this is a difficult operation. The space on the hybrid is marginal and the aluminum bond pads on the MCC chip are of poor quality. Some bonds had to be repaired with conductive epoxy.

An assembled hybrid was first attached to four FE-B chips at the corners of the hybrid, placed on a module support card and read out by the pixel DAQ system. The basic functionality of the hybrid was demonstrated in this way at both Oklahoma and LBNL.

now appears to address all of our needs to at least the 50 Mrad dose that is required for ATLAS pixels. Recent work by the Aachen group in CMS also indicates that it has acceptable (and superior to DMILL) noise performance after irradiation as well.

In addition, we have finally tested some process monitor structures from DMILL for their BiCMOS process, and have now carried out irradiations similar to those done for Honeywell Bulk and SOI. The DMILL structures only contain a small number of transistors, not adequate for extracting full SPICE models. They will be used to test the existing models from the vendor and insure their correctness. In particular, we have observed that the present DMILL post-rad models, which are worst-case only, predict very poor behavior, particular for 3V operation. These models suggest that we would need to design in a factor of more than two in speed margin to meet specifications after irradiation, and this is probably not possible. This situation needs to be clarified. Furthermore, the models from the vendor are intended only for use with the ELDO SPICE simulator, and do not provide identical results when used with other commercial simulators such as HSPICE, and this needs to be further understood. These evaluations will form the basis for detailed design work in these processes in the coming year. We are also attempting to get more complete DMILL test structures from the vendor that would allow us to extract our own SPICE models. However, characterizing small numbers of test structures does not give us any "corner model" information on best and worst case performance - only the vendor can supply this information.

1.1.1.3.3 Production
No activity.

1.1.1.4 Pixel Hybrids (M. Gilchriese)

Milestones	Baseline	Current	Status
*Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98	Complete
*1st prototype design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	15-Apr-99	15-Apr-99	On schedule
*Select hybrid type	15-Apr-99	1-Mar-99	Ahead
*2nd proto design review	28-Apr-99	28-Apr-99	On schedule
*Compl. 2nd proto design	25-May-99	25-May-99	On schedule

Oklahoma
1.1.1.4.1 Design
Rusty Boyd continued work to analyze the results of the fabrication and test of the first flex hybrids.

1.1.1.4.2 Development
The first flex hybrids designed at UOK and fabricated at CERN were tested successfully for the first time at UOK and then at LBNL. These hybrids were used to fabricate first 4 FE-B chip test modules to validate the hybrid design. Hybrids were successfully loaded

performance expected of the drive transistors in the DMILL pixel cell, and to try to achieve a factor of 2 speed-up in the readout speed of the architecture (hit readout should occur at 20 Mhz within a column pair instead of at 10 Mhz as in the present FE-B chips in order to keep the deadtime down on the B-layer readout). A first pass layout for all of the circuitry has been completed. Significant simulation work has begun, based on using SPICE to characterize the basic building blocks, and then to annotate these delays and loads into a higher level Verilog simulation. Complete large-scale SPICE simulations are also beginning. Over the next month, we should be performing the simulations to verify and optimize the performance. We expect to deliver a first complete version of this large block in mid-November, complete with fairly good quality verification and optimization. This is somewhat behind our original schedule, but is still consistent with the goal of a submission in about Mar. 99 of the complete FE-D chip.

We have initiated scheduling of the official ATLAS Design Review process for the FE-D chip, and hope to have the first review in mid-January. At this time, the major blocks should be in pretty final form, with all major simulations complete. Top level simulations should be just beginning, and it will be a useful moment moment for a review. A followup review, prior to submission, should occur in late Feb. The final review team should be chosen over the next few weeks in collaboration with the ATLAS Overall FE Electronics Coordinator.

We have completed the layout of the pixel front-end and control section (about 1/2 of the pixel circuitry) in the Honeywell SOI process. This layout is extremely compact, and looks capable of leading us to a 300μ pixel size in a radhard chip. The layout work on the bias cells at the bottom of the analog column and the current-mode DACs that control the biassing is now also complete. The digital peripheral logic needed to complete an analog test chip (not a complete pixel array) is now also completed, along with all design rule checks. The designs have recently been sent to Honeywell for what we hope is the final time. Honeywell intends to initiate fabrication of this run when the second customer is ready, before the end of Novemeber in the current schedule. This chip is the next critical step towards preparing a complete Honeywell SOI version of the front-end chip (so-called “FE-H”) for ATLAS in 1999. In recent discussions within the ATLAS steering group, a strong recommendation was made to elevate the priority for the FE-D submission, and postpone additional work on Honeywell preparations. This will significantly delay the FE-H submission, perhaps until Sept. 99. This will make the evaluation of this chip on a comparable timescale with the FE-D chip rather difficult, and poses potentially serious problems for the two vendor radhard approach. Despite these concerns, the majority insisted that it was necessary to have at least one radhard FE chip as soon as possible.

We have received PM (process monitor) bars from a recent combined CMS/ATLAS run in the enhanced Honeywell SOI process (which should be rad-hard to about 50 Mrad), as well as some test structures designed by the CMS Aachen group, and some additional transistors relevant to our designs which Honeywell allowed us to add to their standard PM bar. We have now characterized these structures up to 50 Mrad, and verified the significant improvement in radiation hardness of the “enhanced” SOI process. This process

To further assist us in debugging the modules, we have set up a probing system with several active fast Picoprobes on micro-positioners and a microscope so that we can examine the signals in detail directly on the bond pads, and also diagnose faults more directly. In the present two modules, each of which previously had one bad chip, were debugged, and after wire-bond repair, the bad chips were working properly.
This system also allows us to see small imperfections in the distribution of the signals around the support card or flex hybrid.

We have continued our work on developing our new VME based test system and the corresponding LabWindows software. A significant new release of the PLL and the PC software is now complete. We have delivered all eight working readout cards to our collaborators. Boards have been received for the production of the second set of eight PLL. The first board was loaded at LBL and works. The remaining boards have been sent out to a commercial vendor for loading. These boards should satisfy the present requests within the pixel community for test system capability. We have been working with the Genova group on developing and testing the new MCC support software for both LabWindows and the PLL. In this process, the PC software has been substantially restructured to improve the modularity, and provide many new features. This work is now complete, and all modes of the MCC are working. The updated firmware and software have been made available to our collaborators on the Web, and several sets of PROMs were hand-delivered to speed up the process.

Finally, an additional improvement has been made to the test system by providing a fast chopping capability for external charge injection. The internal charge injection circuit in FE-B does not work properly (it suffers from some slight instability which makes measurements of ENC from the threshold scan fits almost impossible). We have up to now used an external GPIB-controlled pulser for our characterization work. This was acceptable for single-chip studies, but is unacceptably slow for module studies. The second generation chopper board has been received, using a new video switcher with much lower transients. The performance of the new board is not perfect, but when cross-calibrated with our present electronics using a high quality GPIB pulser, the results are consistent within a few percent. This now allows us to perform a complete threshold scan of a single chip in under 3 minutes, or a complete module scan in under one hour (generating 100 MB of output histograms along the way). This was roughly the original design speed forseen for the PLL test system, and it has been a major contributor towards improved module characterization.

1.1.1.3.2 Development and Prototypes

We have been working on the layout of the digital readout circuitry for the so-called “FE-D” (the DMILL version of the front-end chips we have designed and tested over the last year). This is our major responsibility for the DMILL common design effort. The work has been progressing reasonably well, and we now have a fairly mature layout for the in-pixel circuitry, as well as the bottom-of-column circuitry which receives the data form the pixels. The latter circuitry has been considerably upgraded to deal with the poorer

1.1.1.3 Pixel Electronics (K. Einsweiler)

Milestones	Baseline	Current	Status
Submit 1st Honeywell SoI test die	15-Nov-98	16-Nov-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99	15-Jan-99	Under Discussion
*FDR DMILL 1st prototype	25-Jan-99	25-Jan-99	Being Organized
*Compl. Design DMILL 1st proto.	26-Feb-99	26-Feb-99	On Schedule
*FDR Honeywell SoI 1st prototype	5-Mar-99	1-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	10-Aug-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	23-Jul-99	On Schedule
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	10-Jan-00	Delayed

LBNL

1.1.1.3.1 Design

We have continued to work with our two modules mounted on PC board supports. Many tests have been tried to isolate why the noise level is high, and also to attempt to eliminate the "high-current" mode of operation that the modules entered on occasion. Studies were done with single chip structures to try to make them noisier. Even removing all normal decoupling did not produce any significant effect. Studies were done by essentially disabling the analog or digital activity on 15 of the 16 chips on the module, and measuring the response of the one normal chip. This did not significantly reduce the noise problems observed in the module, although it did appear to eliminate the high-current mode. A final attempt was made to improve the decoupling on the module (on LV supplies only), and this seemed to significantly improve the stability, but not the noise behavior of the modules.

In parallel, first prototypes were made with the Flex hybrid circuit for module assembly, designed by Oklahoma and fabricated by CERN. A first test was made using 4 bare front-end die attached to the Flex with an MCC chip. This worked well, but did show higher than expected noise on most of the chips. We then proceeded to assemble a complete module which includes 150μ thick electronics die that had been previously ground after bump-bonding. This module, the third Boeing-bumped module we have tested, worked perfectly digitally. This means that all 48 of the FE chips we have used to build modules have survived the bumping and assembly steps, at least for digital testing. This module does not suffer from high currents. This suggests that the conductive backside contact used in this module (in contrast to the insulating contact made in the previous two modules) may play a role. It has noise behavior which varies from chip to chip, but is not too bad for the best chips on the module (about 200e). This module is by far the closest to a real module prototype that has been made so far in the pixel project. The next steps include investigating its performance with improved decoupling, and probing to understand why one chip fails under analog charge injection.

The program of characterizing adhesives for mechanical, thermal, and electrical properties continues. These tests will allow the selection of adhesives for silicon module to sector attachment and also for core to sector facing attachment. Adhesive are being tested before and after irradiation.

Irradiation of aluminum tube sector 3 began at the LBNL cobalt 60 source. The sector will be retested for thermal and mechanical properties after irradiation to 25 MRads.

1.1.1.1.3 Disk Production
No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Current	Status
*Start market survey	2-Nov-98	20-Nov-98	Delayed
*2nd prototype PDR	1-Dec-98	1-Dec-98	On schedule
*Complete market survey	5-Mar-99	5-Mar-99	On schedule
*2nd prototype FDR	29-Mar-99	29-Mar-99	On schedule
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99	On schedule
*Compl. 2nd prototype design	27-Apr-99	27-Apr-99	On schedule
*Compl. Fab of 2nd prototypes	21-Sep-99	21-Sep-99	On schedule

The delayed completion of the “Start market survey” milestone is not expected to affect other milestones as the market survey completion date has been moved to 31 January with CERN Purchasing approval.

New Mexico
1.1.1.2.1 Design

1.1.1.2.2 Development and Prototypes

Analysis of test beam data was initiated. Static electrical measurements were made on a variety of irradiated and unirradiated but bumped test structures of both p- and n-types. Three Structure 6 (First Prototype) test structures were irradiated at LBNL as input to the finalized capacitance measurements. The HSPICE interpixel capacitance calculation was finalized; it produced results consistent with measurements. A two-dimensional IES electrostatic field solver for PC simulations was begun. DAQ electronic assemblies were received from LBNL and Siegen, and assembly of the test stand was begun.

1.1.1.2.3 Production

Drawings for the cleanroom were reviewed. A drawing for the backside wafer probing chuck and a design for the new probestation dark box were submitted to the machine shop for manufacture.

*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	15-Dec-98	Delayed
Complete fab 1st prototype ring	1-Apr-99	1-Apr-99	On Schedule
Complete fab 1st prototype disk	1-July-99	1-July-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule

There will be a delay in the selection of the concept for the 1st prototype ring and the subsequent design. In part these comes from TV holography test results from the sectors that indicate greater stiffness in the overall system may be needed and part from contractual difficulties between ESLI and Hytec under the SBIR Phase II to ESLI.

LBNL

1.1.1.1.1 Design

A Finite Element Analysis of test mockups of aluminum tube sector prototype 4 was done at Hytec, Inc. to compare with TV Holography measurements of the tests mockups. Analysis revealed that the excessive distortions of the mockups, and also the distortions of aluminum tube sector prototype 4, were most probably due to a facing to core adhesive with too low a shear modulus. The analysis also revealed that a stiffer core material may aid the rigidity of the mockups and the aluminum tube sector. Design work on the disk support ring continues at Hytec, Inc.

An Inner Detector engineering review was completed for the pixel disk system at CERN on October 20.

1.1.1.1.2 Development and Prototypes

TV Holography studies of Aluminum tube sector 4 were completed at Hytec, Inc. This prototype sector revealed excessive distortion as its temperature was changed from room temperature to operating temperature. Test mockups of aluminum tube sector 4 were fabricated at LBNL and sent to Hytec for TV Holography tests and FEA analysis to investigate the causes of this distortion. Based on the analysis reported above, additional mockups with stiffer adhesives and stiffer cores will be fabricated and tested. Aluminum tube sector 4 will be rebuilt based on the results of these tests.

Sector 8 from ESLI (Energy Science Laboratories, Inc.) was fitted with dummy silicon modules and tested for thermal performance with infrared imaging at LBNL. This sector is the first of the 5 disk design from ESLI. From the infrared observations the body of the sector was at a temperature 9 degrees C higher than the inlet coolant with 36 Watts of power was applied to the sector. This was as expected. However the corners at the inner radius of the sector were as much as 16 degrees C above the input coolant temperature. This is excessive and needs to be fixed in successive 5 disk prototypes. This sector was sent to Hytec, Inc. where TV Holography tests were begun.

designed at Oklahoma and fabricated at CERN appears to work as designed and detailed measurements of these modules are underway.

Significant progress in the design of the rad-hard DMILL IC(FE-D) was made and this effort appears to be close to on schedule. Test structures were submitted to Honeywell for fabrication in a standard SoI multi-project run expected to begin fabrication by the end of November. However, progress on the design of the Honeywell prototype(FE-H) has been slow and very significant delays are projected, if one maintains the FE-D schedule. Manpower is insufficient, the Honeywell design capability is not yet approved by the US government for the European institutions and organizational improvements are needed to improve the trans-Atlantic collaboration.

The pixel mechanics design is continuing well and the first prototype disk sector corresponding to the baseline layout was received from Energy Sciences Laboratory, Inc and tested at LBNL. The TV holography capability at Hytec is nearly fully operational and is in use to evaluate the mechanical stability of prototype sectors and test samples.

1.1.2 Silicon Strip System

The submission of the 2nd CAFÉ was temporarily put on hold to evaluate recent irradiation results. It appears there are significant differences in the response to Cobalt and protons and considerable data were obtained to try to shed light on these differences. The sensitivity to Cobalt gamma irradiation appears to be greater and the mechanism is not understood. However, simulation and test results even with the greater damage from Cobalt indicate that the 2nd CAFÉ should be functional but a 1-2 month delay in submission will result. Progress on the ABC redesign has been slower than hoped but another major design review is scheduled for mid-November at CERN. The ABCD redesign appears to be on schedule, and will also be reviewed in mid-November at CERN. The design of the 2nd prototype hybrids is progressing but cannot be completed until the CAFÉ and ABC layouts are complete.

1.1.3 ReadOut Drivers

We have completed requirements and preliminary interface specifications, as well as a conceptual model incorporating all the essential functionality. Development of an implementation model is now well advanced. Work in collaboration with U.K. groups on requirements of the other components of the SCT and Pixel off-detector electronics started. Support is ongoing for Pixel and SCT tests in the laboratory and in beams.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (D. Bintinger)

Milestones	Baseline	Current	Status

November 29, 1998

Silicon Subsystem Report

October 1998

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are included for the first time in this month's report. These milestones are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are within allocated amounts. The initial FY99 budget allocations are about 75% of the baseline plan, in part because of significant delays now expected in the delivery of the first rad-hard ICs and to explore the possibility of obtaining non-project funding for some items. Significant delays are now projected for the submission of the first Honeywell rad-hard ICs, as a result of lack of IC design manpower and in part as the result of underestimating the magnitude of the design and organizational tasks. There will be an extensive IC designer meetings at CERN in November to attempt to maintain the schedule, but it will not be possible to maintain both the DMILL and Honeywell SoI baseline schedules.

1.1.2 Silicon Strip System

Costs are within allocated limits. The submission of the 2nd prototype CAFÉ and ABC are delayed by 1-2 months. This has caused delays also in the completion of the design of the 2nd prototype hybrids(the final chip layout must be complete before completing the hybrid design).

1.1.3 ReadOut Driver System

Costs are within allocated limits. A small delay is projected in the selection of a baseline concept for the preprototype ROD. More significant delays of up to two months are now projected for completion of the first preprototype RODs.

Summary of Detailed Reports

1.1.1 Pixel System

A significant achievement was the first assembly and successful operation by Oklahoma and slightly later LBNL for the entire pixel collaboration of the first prototype pixel modules. Sixteen chip modules with flex hybrids and Module Control Chips were successfully fabricated and initial tests completed(by early November). The flex hybrid