December 21, 1998

Silicon Subsystem Report

November 1998

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are currently within allocated amounts. However, there are substantial uncertainties in the costs of prototypes of the mechanical support structure - the outer frame and related items. This uncertainty will not be resolved until March 1999 when vendor quotes have been evaluated. Completion of the design of the front-end, rad-hard electronics continues to be delayed. We have introduced additional milestones corresponding to a first review of the DMILL and Honeywell ICs some weeks before the corresponding FDRs. These reviews have been necessary in the case of the SCT ICs. There are minor delays still present in the mechanics (selection of the concept for the prototype disk ring support), in the completion of the design of the 2nd prototype sensors and in the first prototype module design. No additional delays relative to last month are evident.

1.1.2 Silicon Strip System

Costs are within allocated limits. The submission of the 2nd prototype CAFÉ and ABC are delayed about two months and both have slipped by a few weeks since the last report. However, there are no longer any unresolved design issues for either chip and only final layout, simulation and verification remains to be completed. This has caused delays also in the completion of the design of the 2nd prototype hybrids (the final chip layout must be complete before completing the hybrid design).

1.1.3 ReadOut Driver System

Costs are within allocated limits. Delays of up to two months continue to be projected for completion of the first preprototype RODs but no additional delays since last month's report are expected.

Summary of Detailed Reports

1.1.1 Pixel System

Preliminary tests of the stiffness of the first all-carbon sector from Energy Sciences Laboratory, Inc. corresponding to the current disk layout have been completed successfully.

Detailed measurements of the existing rad-soft ICs continue to guide the design of the first rad-hard generation of ICs. Work is progressing well on the DMILL prototype and it appears that the required circuitry can fit within 400-micron pixel length as required. Fabrication will begin in December at Honeywell of the SoI test die designed to allow detailed analog and digital evaluation of this process. The first single-chip assemblies done using MCM-D techniques have been received at LBNL and are under test in preparation for a decision between this approach and the flex hybrid approach in February 1999.

The success of the first flex hybrid prototypes has led to the decision to complete a revised design (version 1.5) in time for submission for fabrication at CERN by the end of January 1999.

1.1.2 Silicon Strip System

Additional irradiations with 55 MeV protons were completed on CAFÉ-M ICs and verified that the change in resistors previously seen under proton irradiation is 20-30%. Cobalt irradiations were completed although there is uncertainty in the relative dose of these results and the proton results. In any case, the change in resistor values seen after Cobalt irradiation appears to saturate at about 50%. We do not understand the difference between the Cobalt and (low energy) proton results. Irradiation of CAFÉ-Ms with pions at PSI is planned for December. Since the CAFÉ-P performance is adequate even with 50% resistor changes, we have decided to proceed with the submission by the end of the 1998, before the pion irradiation results are known.

A design review for the ABC was held in November but this was not considered a Final Design Review - too many items left outstanding. A final design review is expected in January 1999. To better focus the engineering, the LBNL engineer working full time on the ABC moved to Rutherford Lab to work with the engineers there.

The work on the ABCD redesign is on schedule and a partial design review was held in November. A Final Design Review is scheduled for December 15. Tests with ABCD2s(backside metallized ABCDs from 2nd fabrication by Temic) are continuing on hybrids and with detectors at LBNL and CERN. Stable operation on a hybrid has been demonstrated but not yet with detectors attached and this remains to be understood.

1.1.3 ReadOut Drivers

Requirements and preliminary interface specifications, as well as a conceptual model incorporating all the essential functionality has been completed. Development of an implementation model is now well advanced. The design work is presently focused on combining the advantages of both FPGAs and DSPs in the design. Work in collaboration with U.K. groups on requirements of the other components of the SCT and Pixel off-detector electronics continues. Support is ongoing for Pixel and SCT tests in the laboratory and in beams. A review of the SCT and Pixel RODs was held at CERN in November and presentations made at the first ATLAS-wide ROD workshop also in November.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (D. Bintinger)

Milestones	Baseline	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	1-Feb-99	Delayed
Complete fab 1st prototype ring	1-Apr-99	1-Apr-99	On Schedule
Complete fab 1st prototype disk	1-July-99	1-July-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule

LBNL
1.1.1.1.1 Design
Design work on the disk support ring concept has been delayed until the completion of distortion testing of ESLI sector 8. This testing, as reported below, has now provided enough information on the stiffness of our primary sector design to begin disk support ring design.

Calculations were done of construction tolerances, post construction measurement tolerances and tolerances for distortion due to temperature change for the pixel barrel stave system. These calculations will be refined and extended to the disk system and to the entire pixel system.

1.1.1.1.2 Development and Prototypes
Rebuilt test mockups of aluminum tube sector 4 were sent to Hytec, Inc. for TV Holography tests and FEA analysis to investigate the causes of the excessive distortion with respect to temperature change of aluminum tube sector 4. The test mockups were rebuilt with a stiffer core-to-facing adhesive and with a vitreous carbon foam core of twice the density (0.1 g/cc). Aluminum tube sector 4 will be rebuilt based on the results of these tests.

Sector 8 from ESLI (Energy Science Laboratories, Inc.) was sent to Hytec, Inc. for TV Holography tests. Preliminary results indicate that ESLI sector 8 has out-of-plane distortion of approximately 0.5 microns per degree C of temperature change. For a cooldown from room temperature to -15 degrees C this would imply a 20-micron out-of-plane distortion at point of maximum excursion. The power on/power off distortions were approximately 3 microns. These preliminary results indicate that ESLI sector 8 is stiff enough to meet distortion criteria. Future test will include vibration mode analysis.

Two silicon module adhesive samples in test fixtures were sent to the LLNL Cobalt 60 source for irradiation to 25 MRads. These two samples were tested before and after irradiation for their thermal conductivity, bulk resistivity, and dielectric strength. The silicone-less thermal grease sample did not harden under irradiation. Previous irradiation of a silicone thermal grease showed hardening after irradiation. Also tests of adhesive shear moduli were made as a function of temperature. A low adhesive shear modulus (<50 psi) is necessary to decouple the silicon module from the sector structure due to CTE differences.

Irradiation of aluminum tube sector 3 continued at the LBNL cobalt 60 source. At the end of November the sector had been exposed to approximately 15 Mrads. The sector will be retested for thermal and mechanical properties after irradiation to 25 MRads.

1.1.1.1.3 Disk Production
No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Current	Status
*Start market survey	2-Nov-98	20-Nov-98	completed
*2nd prototype PDR	1-Dec-98	7-Dec-98	delayed
*Complete market survey	5-Mar-99		on schedule
*2nd prototype FDR	29-Mar-99		on schedule
*Compl. Test 1st prototypes	13-Apr-99		on schedule
*Compl. 2nd prototype design	27-Apr-99		on schedule
*Compl. Fab of 2nd prototypes	21-Sep-99		on schedule

1.1.1.2.1 Design

The 2nd prototype preliminary design review is in its final stages at CERN and is expected to be concluded within the week of December 7. The accelerated timing of the Market Survey (reported in October) means that the failure by approximately 1 week to meet this milestone is not expected to impact the date on which the order is placed.

1.1.1.2.2 Development and Prototypes

Several irradiated single-chip devices were measured for leakage current versus voltage and for interpixel capacitance and then placed in a constant-temperature chamber for controlled annealing. DAQ test stand hardware was installed and software downloaded. A test stand PC and LabVIEW software upgrade were required. Debugging of the hardware/software interface is in progress. Two- and three-dimensional geometrical simulations of interpixel capacitance were completed and found to agree with measurements. The first low temperature measurements of irradiated pixel sensors were performed using a probe station installed in a freezer. I-V measurements of Prototype 1.5 wafers were initiated.

1.1.1.2.3 Production

Clean room drawings were approved. Shipment of clean room components is expected in December. A wafer probing chuck was fabricated.

1.1.1.3 Pixel Electronics (K. Einsweiler)

Milestones	Baseline	Current	Status
Submit 1st Honeywell SoI test die	15-Nov-98	15-Nov-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known
1st design review of DMILL proto	25-Jan-99	25-Jan-99	On schedule
*FDR DMILL 1st prototype	25-Jan-99	15-Mar-99	Delayed
*Compl. Design DMILL 1st proto.	26-Feb-99	7-Apr-99	Delayed
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Sep-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	7-Sep-99	Delayed
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	7-Jan-00	Delayed

Additional milestones for the 1st design reviews of the rad-hard ICs have been added this month. The experience with the review process for the SCT ICs has demonstrated the need for reviews in multiple steps. The date for submission of a 2nd set of test die to Honeywell is not know at this time. We continue to negotiate with Honeywell for a date for a next multi-project wafer run. Submission of the rad-hard prototypes continues to be delayed but no major additional slippage has occurred in the last month.

LBNL

1.1.1.3.1 Design

We have been working on the layout of the digital readout circuitry for the so-called “FE-D” (the DMILL version of the front-end chips we have designed and tested over the last year). This is our major responsibility for the DMILL common design effort. The work has been progressing well. The lead designer recently spent one week in Bonn where the complete CAD database for the chip is being assembled. A first version of the layout was delivered, and small additional work is continuing to complete the layout. A significant optimization was performed to meet the very tight space requirements of the DMILL design, and it now looks as though all of the required circuitry will fit into the allowed 400μ space. The complete Verilog simulation of this block is also progressing well. We expect to have completed all of the basic simulations in time for a first design review at the end of Jan. 99

We have completed the layout of the pixel front-end and control section circuitry and all peripheral logic for the test chips we planned to submit to Honeywell for fabrication in their SOI process. Three complete designs (GDS files) have been sent to Honeywell, and

have passed all relevant ERC and DRC. Fabrication of these designs should have begun within the last week, and we hope for delivery in April 99. These test chips should allow us to perform detailed evaluations of the digital and analog performance of Honeywell SOI. Up to now, all of our work has been done at the level of individual transistors, and we have yet to confirm the expected analog performance of the process (although others in the HEP community have done so, and claim that the performance is very good).

These chips are the next critical step towards preparing a complete Honeywell SOI version of the front-end chip (so-called "FE-H") for ATLAS in 1999. In recent discussions within the ATLAS steering group, a strong recommendation was made to elevate the priority for the FE-D submission, and postpone additional work on Honeywell preparations. This will significantly delay the FE-H submission, perhaps until Sept. 99. This will make the evaluation of this complete Honeywell chip on a comparable timescale with the FE-D chip rather difficult, and poses potentially serious problems for the two vendor radhard approach. Despite these concerns, the majority insisted that it was necessary to have at least one radhard FE chip as soon as possible.

We are continuing our characterization work of Honeywell SOI transistors, and have fit another set of devices irradiated to 50 Mrad doses. The results again look very encouraging, with very minimal parameter shifts. It has been verified that when using these post-rad models, the recently submitted preamp and discriminator designs do continue to operate correctly. Thus, we have every expectation that the FE-H chip will meet ATLAS requirements.

In addition, we have finally tested some process monitor structures from DMILL for their BiCMOS process, and have now carried out irradiations similar to those done for Honeywell Bulk and SOI. The DMILL structures only contain a small number of transistors, not adequate for extracting full SPICE models. They will be used to test the existing models from the vendor and insure their correctness. We have received a new set of post-rad models,including all "corner" parameter variations, and we are evaluating the implications of these models for our design, as well as comparing their predictions to some actual test transistors.

1.1.1.3.2 Development and Prototypes

We have continued to work on single-chip prototypes, including carrying out much more complete measurements of crosstalk and timewalk performance of the complete single-chip with detector. These measurements indicate that the crosstalk performance is very good (typically a signal of 50-100 time threshold is required to fire neighboring pixels). Even in the region at the top of the chip where two pixels are ganged together to cover the dead region on the module between chips, the crosstalk never exceeds 3-4%, which is quite acceptable. The comparable Bonn/CPPM chip indicates significantly worse crosstalk performance, and with the present performance, the ganged region of the array is not very useful (20% crosstalk effects observed).

For the timewalk measurements, we have performed complete charge-time 2D scans, where for each of 18 different charges, a timing scan is done in 0.25ns steps. This allows a careful measurement of the timewalk of each pixel as a function of the input charge. These timing measurements are individually corrected for the actual pixel threshold to compute the "overdrive" (charge above threshold) to get a particular timewalk. These results are all of very high quality, but they demonstrate that the expected performance, in which all hits which are above the high threshold in our dual threshold design would have less than 25 ns timewalk compared to a very large charge value, is not achieved. This represents somewhat of a disagreement with testchip results, and so further study is needed. However, we had already realized that the FE-B timewalk performance was somewhat marginal, and design modifications were performed that should significantly improve the timewalk performance with only modest degradation of the present excellent crosstalk performance.

We have also received single-chip devices that were assembled using the MCM-D (deposition of bus structures directly on the surface of the silicon detector prior to bump-bonding and flip-chipping of the detector and electronics) technique. This technique is a high-tech alternative to the Flex hybrid technique for making module interconnections. On the chip devices, the major feature is all of the vias that pass signals from the silicon detector through to the electronics are all present (there is one 4-layer copper via for each of the 2880 pixels in the single chip). These vias have the potential to introduce extra capacitive loading (meaning noise) and extra capacitive coupling (meaning crosstalk). We have bonded two single chip assemblies to test boards, and they work. We will now begin to make a series of noise, crosstalk, etc. measurements on them to further assess the use of MCM-D technology for module interconnection. The pixel collaboration has agreed to decide between the Flex and MCM-D approaches in Feb. 99, and it is critical to accumulate measurements on various prototypes to guide this choice.

We have continued our work on developing our VME based test system and the corresponding LabWindows software. A significant new release of the PLL and the PC software is now complete.

Further measurements have been performed on our analog test chip to assess the impact of noise on the power supplies on the overall performance of the pixel chips. Noise of varying amplitude and frequency has been injected on the chip power lines, and the increase in noise on the pixel output discriminator (as measured by a threshold scan) has been measured. These measurements are critical to the proper design of the power supply decoupling network on the module. These measurements indicate essentially no sensitivity to power supply noise below about 100 kHz, but quite significant sensitivity in the few MHz region where the preamp gain is maximal. The presence of only a few mV RMS noise in the peak sensitivity region is enough to degrade the noise performance of the pixel front-end chip, and both of the to analog supplies appear to be equally sensitive. This suggests that high quality decoupling of these two supplies, close to each FE chip, may well be needed on the module. Further studies at the module level will also be carried out on this subject.

1.1.1.3.3 Production
No activity.

1.1.1.4 Pixel Hybrids (P. Skubic/R. Boyd)

Milestones	Baseline	Current	Status
*Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98	Complete
*1st prototype design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	15-Apr-99	15-Apr-99	On schedule
*Select hybrid type	15-Apr-99	1-Mar-99	Ahead
*2nd proto design review	28-Apr-99	28-Apr-99	On schedule
*Compl. 2nd proto design	25-May-99	25-May-99	On schedule

Oklahoma
1.1.1.4.1 Design
A review of the flex and MCM-D options for module interconnections was held in November before the ATLAS week. No decision was reached at this review but it was agreed to reach a decision by the February 1999 ATLAS week. A detailed work plan leading to the decision was developed.

It was decided by LBNL, INFN (Genova) and UOK to begin design on a version-1.5 flex hybrid prototype to address some of the issues raised in the assembly of the first prototypes. Traces will now be routed outside the area of the guard ring, while keeping the bond pads inside, so that adhesive need not be applied over the guard ring area. This increased routing area should allow more room between the MCC bond pads and the edge of the MCC, larger power traces to decrease the voltage drop and inclusion of three test input busses that were excluded from the original design because of lack of space. It is also hoped that the decoupling capacitor pad size can be increased from 0402 to 0603 to allow for larger values. Other mechanical improvements are also planned. A "floor plan" will be made available for review by early January. The design is scheduled to be complete and submitted to CERN in hopes that fabrication can be completed by end January 1999.

1.1.1.4.2 Development
The activity has focused on understanding the first flex modules and is reported in 1.1.1.5.

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, M. Gilchriese)

Milestones	Baseline	Current	Status
*Compl. 1st proto. Design	29-Oct-98	30-Jan-99	Delayed
*1st proto. Design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	18-Mar-99	18-Mar-99	On schedule

*Select module type	18-Mar-99	18-Mar-99	On schedule
*2nd proto. Design review	17-Sep-99	17-Sep-99	On schedule

LBNL and Oklahoma

1.1.1.5.1 Design/Engineering.

LBNL

Contact was made with a vendor for X-ray inspection of flip-chip assemblies. There are single or few channels failures seen in single-chip assemblies that we believe are caused by opens or shorts in the bump bonds. Larger areas of failures are observed in modules. Dummy mechanical modules with both indium and solder bumps were successfully X-ray with high resolution at X-Tek in Santa Clara. Active devices will be X-rayed in December.

1.1.1.5.2 Development and Prototypes

LBNL
Little new work has been performed on evaluating module performance in the last month. Further testing of the complete Flex module has been done to understand problems with one chip on the module. Obvious connection problems have been eliminated, but the problem is not yet understood.

Oklahoma
Internal charge injection is now working, allowing module scans to be completed in a few minutes, instead of many hours, as we experienced with external scans using a GPIB pulse generator. Full MCC mode has also been implemented. With these two improvements, UOK should be able to accomplish much more analyses and debugging of the module in December and January, before the module baseline decision at CERN in February. Understanding of the pixel test system and analysis software has also advanced. Close agreement has been achieved between our results and LBNL's for a single chip module shipped with the test system.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done

*FDR for 2nd ABC	23-Oct-98	19-Jan-98	Delayed
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	23-Dec-98	Delayed
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	31-Jan-98	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-98	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Delayed
*Submit 2ns ABCD	27-Jan-99	27-Jan-99	On Schedule
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	On Schedule
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	7-May-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	18-Jun-99	Delayed
*Test systems complete	26-Apr-99	26-Apr-99	OnSchedule
*1st ICs avail. For 2nd proto hybrid	18-May-99	11-Jul-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	11-Jun-99	OnSchedule

1.1.2.1.1 Design/Engineering

LBNL & UCSC

The mystery of larger resistance changes on CAFE-M parts under Co60 irradiation compared to proton irradiation is still not completely understood. We have confirmed with another proton irradiation that our 20%-30% increase is correct for that type. We are also going to irradiate some CAFE-M parts with minimum ionizing pions in December. At the present time, we are still struggling to understand the larger (approximately 50%) increase in resistance under Co60 irradiation. We are looking at possible errors in effective dosimetry for gammas and also at details of the structure of the resistors. Currently, we believe that the proton data is the valid measure. However, we have determined that the CAFE-P will still operate successfully with the 50% change. If that worst case scenario is determined to be a valid requirement, the CAFE-P will suffer a small degradation in efficiency for small amplitude signals due to broadened shaping times near the end of its ATLAS lifetime. With this understanding, we are proceeding with final verification of the design and a target to submit the chip for fabrication before Christmas break.

We had a design review of the ABC in November but it could not be considered the Final Design Review as too much was still left to be completed. We believe that all problems with the present chip are understood. Fixes are either complete or underway. A Final Design Review will be scheduled sometime in January with a goal of submission by end of January. We continue to suffer from lack of focused engineering support and leadership. In response to this, Gerrit Meddeler was sent to work at RAL for the second half of November and December to try to bring the design effort to completion.

The ABCD re-design is nearly complete. A partial review was held in November. The Final Design Review is scheduled for 15-Dec. The goal is to have the layout complete by

then and most but not all verification done. Final simulations and verification will be completed in early January.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

More effort was spent to understand the CAFE-M resistance changes under irradiation. See the discussion above. Also, more work was done on the CAFE-M/ABC module. Some errors were found in bypassing on the hybrid and now the module is working in a stable way.

1.1.2.1.3 Production

The Technical Specification for the Frame Contract with Temic and Honeywell was completed in early November and the Invitation to Tender was sent out on 9-Nov. It was agreed to have only general statements about Quality Assurance in the Technical Specification and leave specific negotiations about yield assurance for production releases at a later date.

1.1.2.2 Silicon Strip Hybrids(C. Haber)

Milestones	Baseline	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97	Complete
Complete fab of 1st prototype	2-Feb-98	23-Mar-98	Complete
Preliminary design review	3-Aug-98	10-Jan-98	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	1-Jan-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	1-Jan-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Jun-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Jun-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Jun-99	Delayed
*Compl. 2nd proto assembly	17-May-99	1-Jul-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	10-Jul-99	Delayed

No additional delays are reported this month.

LBNL

1.1.2.2.1 Design

A design for the hybrid jumper cable was completed. This is the cable that interconnects the front and backside hybrids.

1.1.2.2.2 Development and Prototypes

ABCD chips on hybrids were bonded to detectors and seen to oscillate. Work is underway to understand the origin of this problem.

An attempt was made to mount the kapton hybrid on a ceramic substrate. It was however damaged in the lamination process. A new, gentler process was suggested and was tested this month. It is seen to result in a non-uniform surface structure on test samples. Work on this is continuing.

A second possible vendor for hybrid production was identified. Preliminary discussions are underway aimed at obtaining a new price quote.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98	Complete
Prototype tooling complete	1-Apr-99	1-Apr-99	On schedule
*Compl. Design of proto assy/test	14-Jun-99	14-Jun-99	On schedule
*Compl. Fab of tooling for proto	14-Jun-99	14-Jun-99	On schedule

No additional delays are reported this month.

LBNL
1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

Design of a new calibration plate continued with the idea of using precision dicing to eliminate the use of the calibration bar. Discussions were held with a photo-mask vendor concerning the production of this plate. Additional comments were received at the SCT meeting at CERN. These have been added to the design and it was posted on the web for further review and comments from the SCT community.

Results on module metrology at the Rutherford Lab were received in October and studied. Transverse precision was similar to ours but module thickness variation was outside specifications. Following the discussion in the SCT meeting we are undertaking a

systematic study of the assembly fixtures to try and understand where these non-uniformities might be coming from.

In October, assembly was completed on a single sided module using working detectors. This has been successfully connected to a partially loaded Cafe-M/ABC hybrid and bonded. The module is seen to readout. It was found that the module is not stable unless analog and digital grounds are connected together. We don't understand this.

A second single sided module for the ABCD hybrid was assembled and bonded. While it operates the chips are unstable once bonded to silicon.

Further discussions with the dicing vendors concerning prototype work were held.

A literature survey and some vendor discussions concerning automated dispensing systems were undertaken.

Design was started on a folding fixture for the hybrids.

1.1.2.3.3 Production

No activity.

Milestones	Baseline	Current	Status
*Select PreROD implementation	30-Oct-98	4-Nov-98	Complete
*Requirements review	30-Nov-98	18-Nov-98	Complete
*Compl. System design	28-Dec-98	28-Dec-98	On schedule
*System design review	11-Jan-99	11-Jan-99	On schedule
*Compl. PreROD design	29-Jan-99	31-Mar-99	Delayed
*Compl. PreROD layout	15-Feb-99	15-Apr-99	Delayed
*Compl. PreROD procure	1-Mar-99	30-Apr-99	Delayed
*Compl. PreROD PCB fab	16-Mar-99	16-May-99	Delayed
*Compl. PreROD 1st assemble	30-Mar-99	31-May-99	Delayed
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	15-Jul-99	Delayed
*PreRODs complete	20-Aug-99	20-Aug-99	On schedule
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

1.1.3.1.1 Strip Test Beam Support

UC Irvine

New programmable logic (GALs) for the Silicon Low-Level Card (SLL) to be used with detector modules instrumented with ABC/D chips, as well as new system software for the DSP modules, were distributed to users in Sweden and Norway.

1.1.3.1.2 Pixel Test Beam Support

University of Wisconsin

The fabrication of the PLL cards for pixel test beam support is continuing. We have delivered all eight working readout cards to our collaborators. Boards have been received for the production of the second set of eight PLL. The first board was loaded at LBL and works. The remaining boards have been sent out to a commercial vendor for loading and are expected back any day now. These new boards will be burned in and tested in early January for delivery to the pixel collaboration.

1.1.3.2.1 ROD Requirements

UC Irvine and University of Wisconsin

ROD requirements are largely complete. Telephone meetings with UK collaborators working on other components of the off-detector electronics continued, culminating in a review of the requirements for all off-detector components during the November ATLAS Week. Some productive discussions relating to requirements, particularly concerning the consequences of back-pressure to the RODs from the Trigger/DAQ System, took place during the ATLAS ROD Workshop held at the University of Geneva during ATLAS Week. Other useful discussions at the workshop centered principally on system issues for off-detector electronics systems and their software.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No significant refinements of the essential model were made during November.

1.1.3.2.3 ROD Implementation Model

Development of the implementation model continues to be the focus of ROD design effort. Effort continued to focus on a hybrid approach in order to combine the best features of the FPGA-based and DSP-based approaches studied previously. Progress was made on the deployment of functionality among FPGAs

and DSPs. The decoder section of the favored approach utilizes both an FPGA and a DSP. Details of this approach, most notably details of buffering and data transfer between the FPGA decoder at the input and the subsequent decoder DSP, remain to be worked out. Pixel/SCT ROD implementations were presented at the ROD Workshop during the November ATLAS Week, as well as in the Pixel Working Group.

UC Irvine

Studies of the performance of DSPs in the decoder section of the ROD continued, including studies of DMA performance and processing performance with decoding performed in the decoder FPGA.

Various improvements to the ROD software development platform were explored. This platform is PC-based and utilizes a Texas Instruments DSP evaluation model (EVM). The possibility of using two evaluation modules at once was investigated. This would allow one EVM to emulate one of the decoder DSPs in the ROD and the other EVM to emulate the one ROD host DSP.

Issues regarding the host DSP were studied, and development of software to simulate host DSP software was started. The simulation software takes into account the various tasks of the host DSP without having to directly interface to the decoder DSPs in the simulation. This simulation is run on the EVM in the software development platform.

As part of an effort to estimate the overall latency for the delivery of *L1Accept* signals within the SCT system, the latency within the Pixel/SCT ROD was estimated.

University of Wisconsin

Simulation studies of the data flow through the DSP based gather continues. This work is to determine that there will be sufficient margins in the current hybrid model. Refinements is the FPGA code continues with simulation to confirm the viability.

1.1.3.3.7 Preprototype ROD

UC Irvine and University of Wisconsin

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed above under WBS 1.1.3.2.3.