

April 7, 1999

Silicon Subsystem Report

March 1999

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are currently within allocated amounts. The first internal review by U.S. ATLAS was completed and a response created to the report of the review committee. The pixel team found this review to very useful. Work on integration of services is progressing at CERN and at LBNL with detailed estimates, CAD modeling and the construction of a full-scale model(at LBNL) and a one-quarter section full-scale model in the UK. Preparations ramped up for the Inner Detector cooling review at the end of May, since there remain serious issues to address regarding the final choice of a cooling fluid. The contract for fabrication of the prototype frame was placed by LBNL. Some materials for this prototype were ordered to be purchased by Italy. The final selection of all of the composite materials for the prototype is delayed by one month to allow more design calculations to be made to assess impact on the material budget. Otherwise this effort is currently on schedule. Detailed evaluation of sector designs is continuing and is on schedule. Fabrication drawings and bids for a prototype sector support ring are complete but a six week delay in completion is currently projected. The design and orders for the 2nd prototype sensors are on schedule. The schedule for submission of the DMILL prototype, FE-D, has slipped by an additional few weeks, but substantial progress has been made in minimizing the size of layout of circuitry, which should allow additional functionality to be added or improved. Test die fabricated in Honeywell SoI are on schedule for delivery in early April. The design of a revised flex hybrid(version 1.x) is well advanced and a new schedule including additional prototype steps will be available next month. A solder-bumped module made by IZM in Berlin has been tested with very good results on threshold uniformity and noise. This clearly indicates that problems observed before with Boeing-indium-bumped modules are the result of bump resistance and flip chip problems.

1.1.2 Silicon Strip System

Costs are within allocated limits. Follow-ups to the final design reviews were held for the ABC and ABCD at the end of March. Although there remain concerns about the instability of the ABCD observed in tests, substantial changes have been made to the circuit design to address this issue. The prevailing opinion is that no additional insight is to be gained by additional simulation and that the chip should proceed to submission in the

next few weeks. Work on the final verification and simulation of the ABC is progressing more slowly than hoped, but no fundamental problems remain and it's hoped to submit this chip in about one month. The hybrid schedule is linked to the schedules for the ABC and ABCD and thus additional delays are now expected. The hybrid designers have taken advantage of this delay to contact other vendors that may offer a cheaper price for fabrication.

1.1.3 ReadOut Driver System

Costs are within allocated limits. Ongoing architectural studies have led to a delay in the schedule for the preprototype ROD. The delay encountered to date will not result in a delay to the SCT schedule because its need for SCT system tests has been delayed by other delays in SCT electronics development. Similarly no delays should result for the pixel system, since systems tests were in any case not planned until mid-2000. A review was held March 25-26 to recommend a single choice of architecture, a choice between the FPGA-based approach and the processor-based approach. The review committee recommended an approach using FPGAs only in the data stream and DSPs for other tasks such as monitoring and calibration. The schedule for the preprototype will be redrawn following the review. Support is ongoing for Pixel and SCT tests in laboratories and beams.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (E. Anderssen, D. Bintinger, M. Gilchriese)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	1-Feb-99	Complete
Select materials for frame proto.	15-Mar-99	7-Apr-99	Delayed
Complete fab 1 st prototype ring	1-Apr-99	15-May-99	Delayed
Complete frame Phase I	1-Jul-99	1-Jul-99	On Schedule
Complete fab 1 st prototype disk	1-Jul-99	1-Jul-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule
Complete frame Phase II	1-Oct-99	1-Oct-99	On Schedule
Complete frame Phase III	1-Feb-00	1-Feb-00	On Schedule

LBNL/CERN

1.1.1.1.1 Design

First draft for the design of the cable plant for detector was circulated for comment earlier in the month. Nominal design fits into envelopes as specified at the time of the TDR (May 98). Design suggests need for additional Patch Panel outside of Muon chambers as to

transition to larger cable sizes from those that fit up to PPB2. Smaller cable sizes are required in the PPB2/Muon region due to the limited space available for PPB2. Some freedom is available for increase in cross section between PPB1 and PPB2, and outside the Muon chambers. Space or material limitations dominate elsewhere. Feedback on this first draft indicates that the currents used to size the cables, though based on our present, power budget, are unrealistically low when compared to measurements of current prototype electronics. It is likely that our power budget will need to increase by approximately 60% in order to accommodate the new estimates of power consumption. Implications to the cooling system have yet to be assessed, though a rough plan of how to determine the impact has been generated and will proceed through May.

Trigger latency was determined to be a problem late last month. Worst case estimates for delays in the various components and fiber transit times, that added together with the L1 Trigger Latency, exceeded our electronics buffer (128 beam crossings) by 1-2 Beam crossings. Part of the problem arose from the realization that the fiber length was some 50m longer than anticipated. This was a particular problem for the SCT as they had just ordered their optical fiber. Worst case fiber routing occurs for the fibers on the far side of the detector from USA15. All services run more or less radially outward, though are bunched to exit in eighths from the Muon chambers. A lot of the extra length comes from going first the “wrong way” out and then having to go around the Muon chambers, some extra 40m. The designers laying out the rack space exacerbated the problem through poor choice of rack locations. A solution to the problem has been found through the prioritized routing of the fiber. Within the ID volume to take all of the fibers out on the side closest to USA15. Racks within USA 15 have preliminarily been reserved/requested as our ROD racks, which are closest to the Trigger racks—this awaits an official rack layout before finalization.

Pixel Services are being modeled both physically and with CAD to assess space allocation within Pixel volume, and to provide a cad interface for service integration with the ID support structure. An Acrylic full scale model of the Pixel end frame has been produced for studies at LBNL, and a similar $\frac{1}{4}$ (90Degree) full scale section has been produced and shipped to RAL for work on ID Service Integration. A design for an electrical prototype with similar properties, connectors, size and length to an actual cable has been circulated for comment. This should be fabbed and ready for use in the summer Flex Module testing.

Disk support ring prototype drawings were sent to ESLI, San Diego in preparation for fabrication. Fabrication of the prototype support ring is delayed by six weeks.

Specifications for the graphite-fiber honeycomb prototype from YLA Cellular to be used in the frame prototype were completed and the honeycomb ordered for delivery in April. Extensive design studies were completed to evaluate the effect on the natural frequency of the support frame from varying the modulus of the fiber material used in the flat-panel structure, from varying the thickness of the fiber layers and from modifying the end supports. A final selection of material will occur in early April, but it appears that higher

modulus fiber(eg. XN80 as compared to XN50) will be desirable although this will be more costly.

1.1.1.1.2 Development and Prototypes

TV Holography test were performed on aluminum tube sector 4 at Hytec, Inc to determine out-of-plane distortions as a function of temperature change and pressure within the cooling tube. A report on the results of the tests is being prepared. Also TV Holography tests were performed on silicon modules tacked with UV curing epoxy to carbon-carbon sector mockups to determine if the UV epoxy tacks cause excessive distortion.

Thermal tests of ESLI prototype sector 9 indicate that it will meet our thermal requirements. This sector has a flattened glassy carbon coolant tube to increase thermal conductivity between facings and coolant tube. However this sector had a leak in the coolant as is being returned to ESLI for analysis. ESLI sector 9 was also measured for distortions as a function of temperature change on a no-touch CMM at LBNL. Out-of-plane distortions from 10 degrees C to 40 degrees C are less than 15 microns. This is an acceptable distortion.

ESLI prototype sector 8 was cycled in pressure from 0 to 60 psi 33 times and then tested for thermal performance. Its thermal performance was the same after pressure cycles as before. In addition the power during the test was increased to 67% above nominal which resulted in an average temperature increase of approximately 5 degees C. Investigations are underway to determine if this temperature rise is acceptable or can be offset by increased cooling.

1.1.1.1.3 Disk Production

No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
*Start market survey	2-Nov-98	1-Dec-98	Completed
*2 nd prototype PDR	1-Dec-98	1-Dec-98	Completed
*Complete market survey	5-Mar-99	12-Feb-99	Completed
*2 nd prototype FDR	29-Mar-99	22-Feb-99	Completed
*Compl. Test 1 st prototypes	13-Apr-99	13-Apr-99	On schedule
*Compl. 2 nd prototype design	27-Apr-99	27-Apr-99	On schedule
*Compl. Fab of 2 nd prototypes	21-Sep-99	30-Aug-99	On schedule

1.1.1.2.1 Design

Design of the Second Prototypes is nearing completion based upon specifications that were ratified at the 22 February Pixel General Meeting. Members of the ATLAS Pixel Group will review the design electronically prior to 27 April.

1.1.1.2.2 Development and Prototypes

The Price Enquiry procedure was concluded, and quotations were received from 3 vendors/consortia. Documents necessary for ordering the Second Prototypes (including the non-disclosure agreement) were completed at CERN and will receive official approval during the week of 5 April.

Bumped and unbumped single-chip devices from Prototype 1b were characterized by ATLAS groups and irradiated at LBNL. Tests of modified p-spray and oxygen-diffused silicon devices continued.

1.1.1.2.3 Production

No activity.

1.1.1.3 Pixel Electronics (K. Einsweiler, R. Kass)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
Compl. Design HSOI test die	16-Apr-98	1-Nov-98	Completed
Compl. Fab HSOI test die	26-Aug-98	31-Mar-99	Delayed
Compl. Design DMILL test device	15-Dec-98	15-Dec-98	Completed
Submit 2 nd Honeywell SoI test die	15-Jan-99		Not known
1 st design review of DMILL proto	25-Jan-99	23-Feb-99	Completed
*FDR DMILL 1 st prototype	25-Jan-99	TBD	TBD
*Compl. Design DMILL 1 st proto.	26-Feb-99	1-May-99	Delayed
Compl. Fab DMILL test device	30-Apr-99	30-Apr-99	On schedule
1 st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule
Compl. Eval. DMILL test device	1-Jul-99	1-Jul-99	On schedule
Compl. Eval. HSOI test die	1-Jul-99	1-Jul-99	On schedule
*FDR Honeywell SoI 1 st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Oct-99	Delayed
*Compl. Fab of DMILL 1 st proto.	23-Jul-99	7-Sep-99	Delayed
*Compl. Fab of Honey. SoI 1 st proto	25-Aug-99	15-Feb-00	Delayed
*Compl eval. DMILL prototype	9-Dec-99	1-Jun-00	Delayed
*Compl eval HSOI prototype	15-Feb-00	1-Jun-00	Delayed
*Review design approach	19-Jan-00	15-Jun-00	Delayed
*Select rad-hard vendor	29-Jan-00	15-Jul-00	Delayed.

1.1.1.3.1 Design

LBNL

Our highest priority remains the DMILL front-end chip submission ("FE-D"). We have worked to transfer design knowledge from our departing engineer (A. Joshi) to the remaining engineers on the project.

We have also spent some weeks optimizing the layout, as the integration of the different blocks was proving very challenging. This has been a collaborative effort with Bonn. The column-pair layout (digital circuitry in the back of the pixel and the bottom of the column to read out the data) is now finalized, and an additional 25 μ of space in the pixel has been gained. This will allow us to add back the digital injection test feature we had removed previously. This feature is quite important in providing the means to test all buffers and data paths on the die during wafer probing in order to make sure a given die is really good enough for flip-chip assembly. We can also probably switch to the higher performance BiCMOS front-end design, which should provide improved timewalk performance. The EOC buffer layout has also been improved, gaining a significant amount in vertical pitch. This appears as though it will allow us to implement a full 25 buffer EOC block (the required value for the disks and outer layers suggested by detailed architecture simulations), and provide an additional 150 μ of vertical space for inter-block routing. The additional vertical space is badly needed to complete the interconnections on the chip while trying to maintain the layout rules advised by TEMIC (there are design rules and advised design rules, and the differences are most significant for large busses with narrow traces). All of this new layout work should be completed within another week or so, and will result in a chip with significantly better performance.

We have now succeeded in implementing the necessary node labeling and netlist extraction from hierarchical layout that we need in order to carry out large SPICE simulations in Cadence using ELDO. The default behavior of the Cadence netlister was not adequate in this respect, requiring us to extract flat netlists (which are enormous and very hard to work with) or to lose the ability to look at nodes inside of blocks far down in the hierarchy. Using these improvements, we are now proceeding with our SPICE simulation program of the digital readout. This is providing us with detailed results for our circuits, including the performance with the worst case models (“irradiated” these results, we continue to find roughly a factor of 4-5 difference in circuit performance as we go from the best case (“pre-rad fast-fast”) to the worst case. This makes it almost certain that if we ever have die with the worst case performance, they will need to be operated at about 3.5V digital supply voltage instead of the 3.0V that has been our goal. Nevertheless, measurements of existing chips suggest only about a 20% increase in digital supply current is to be expected with this change in operating voltage, and so this is considered acceptable.

This recent progress has been slower than expected, but we are getting very close to completing our portion of the FE-D chip. We would expect to validate all layout with detailed simulation and then continue to study the performance of the circuitry over the next 2-3 weeks, after which we expect to have completed our deliverables for the DMILL submission. We will have the first in a series of technical phone conferences with TEMIC next week to finalize details of the submission, and to discuss remaining small issues with the reticle layout and the design rules, particularly the relationship between the “advice” rules and the expected yield.

Ohio State

Work is ongoing to adapt the design of the DORIC4 IC used by the SCT for optical transmission. The existing DORIC4 chip uses BICMOS technology with only NPN transistors to achieve a radiation tolerant design. We are developing a version of the DORIC4 chip using a radiation hard CMOS process (Honeywell SOI and/or DMILL). In consultation with the team that designed the DORIC4 we have put together a spice model of the chip which uses n-FETs and p-FETs. The building blocks of this chip (preamp, edge detector, D flip-flop, delay, exclusive OR, and D control) have been simulated individually and together. We are negotiating with Honeywell for use of their SOI models.

1.1.1.3.2 Development and Prototypes

LBNL

We have also received a single chip assembly using the FE-C (Bonn/Marseille) front-end chip. Recall that the new DMILL FE chip, FE-D, is based on the FE design of FE-C and the digital readout of FE-B, making it very interesting for us to study the performance of the FE-C front-end in our own lab. These measurements show several significant performance problems with the FE-C digital readout, which do make the characterization of the front-end performance more difficult. First results indicate that the FE-C front-end performance in a complete pixel array with a realistic detector are not as good as previously claimed by our collaborators. This is cause for some concern, and we will be further investigating this during the coming weeks. So far, the observed front-end performance in the FE-C chip is no better than, and in some cases worse than, the performance observed in the FE-B chip. In particular, there are significant performance issues with threshold dispersion, TOT uniformity, and timewalk performance. The FE-C uses a CMOS version of the CPPM front-end design, and it has always been claimed that the BiCMOS front-end design gives better performance in threshold dispersion and timewalk. This is one of the reasons why it now seems quite important to implement the BiCMOS front-end design in the FE-D chip.

The Honeywell SOI multi-project submission which we made in Nov. 98 is also approaching completion. Honeywell has shipped the 30 test chips and 10 process monitor bars, all from a single wafer, that we have ordered. We expect them to arrive any day now at LBL (they had to be shipped via OSU for purchasing reasons). The designer of these devices will come to LBL for two weeks during April to assist with the testing and evaluation of the circuits. These test devices include complete front-end designs (improved over that of the FE-B chips), and will allow us to make a detailed evaluation of the use of the HSOI process for analog design. We will irradiate several of these devices, along with the associated single transistor PM bars, in order to make sure we understand the behavior of the circuit designs and their analog performance under irradiation. The evaluation of these devices is a critical next step towards the submission of a complete pixel array later this year in the Honeywell SOI process.

1.1.1.3.3 Production

No activity.

1.1.1.4 Pixel Hybrids (R. Boyd)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
* Compl. Assembly of 1 st proto.	14-Jan-99	10-Nov-98	Complete
* 1 st prototype design review	18-Feb-99	18-Feb-99	Complete
* Compl. Tests of 1.0 protos.	15-Apr-99	15-Mar-99	Complete
* Select hybrid type	15-Apr-99	1- Mar-99	Complete
* Compl. 1.x base proto	(1)	1 - Apr- 99	Complete
* Proto. 1.x base design review	(1)	8 - Apr-99	On schedule
* Compl. 1.x proto. designs & submissions to vendors	(1)	25-May-99	On schedule

⁽¹⁾ not included in the original baseline. We are in the process of including additional milestones to account for all of the prototype steps now foreseen, including those not included in the baseline schedule.

Oklahoma

1.1.1.4.1 Design

A new schedule is being defined based on lessons learned from the version 1.0 Flex Hybrid prototypes module prototypes. This schedule is also more in line with the realities of the deliveries of other components including the FE-D, rad-hard MCC, first prototype Optical Links, bumped bare modules and the different design rules provided by various flex manufacturers. In addition, the increased number of prototypes allows for evaluation of more flex manufacturers, which should lead to reduced costs and higher quality for the production Flex Hybrids. The '.x' is a place holder which will be replaced by a number representing the manufacturer specific design.

The functional features of each prototype are:

③1.x

- Enhancements to layout and component selection
- 0603 SMT decoupling capacitors where there is room
- Distance between MCC bond pads and corresponding bond pads on Flex Hybrid increased for easier wire bonding
- "H" buss layout
- Use of area outside bond pads on Flex Hybrid for buss routing
- Addition of separate return pads for each power supply
- Addition of Pt1000 and pads for temperature monitoring
- Addition of sensor bias and return pads, and sensor bias decoupling capacitor on Flex Hybrid
- Increased power buss width for all supplies (including returns)
- Space reserved for first Optical Link prototype

③ 2.x

Capability for direct connection of power tape and stand alone operation (support card not required)

Support for FE-D

Support for first prototype Optical Link and or alternative Optical Link prototype from OSU

The base design for the 1.x Flex Prototype has been completed (based on the CERN fabrication design rules). A design review is to take place the first week of April, quickly followed by submission to CERN for fabrication. Work is under way to identify tasks to be performed in connection with Flex Hybrid development through next summer. Components sent to LBNL for irradiation were returned in late March and are currently undergoing evaluation. Results will be available in April.

1.1.1.4.2 Development

Oklahoma

We have begun simulations of past, present and future Flex Hybrid layouts using Maxwell SpiceLink from Ansoft. We have purchased a license for this product.

Custom fabricated Thermaphase adhesive/heat sink compound from Orcus has been received. We are currently developing a method of application which eliminates air bubbles in the final assembly.

Plans to build a 16 chip, FE only module have been scrapped as the problems we were planning to investigate seem to have been resolved (these appear to have been due to high resistance in the In bumped modules - see the module section).

Albany

Albany is developing a procedure to measure the ATLAS Flex Hybrids. On a conventional probe station, with one Computer Aided probe, it can be done in four passes. First, the corresponding pins of chips on the opposite sides of the flex are tested for continuity and shorts. Next, the signal pairs, 2 lines per chip, from the front-ends to the MCC are tested. Then the signal lines from the MCC to the outside world are tested. Last, the power bus from the input to the MCC is tested. Although this technique works, the best one could hope for is to test two flex circuits per day.

For this reason, quotations have been requested for probe cards, which would significantly reduce the time required to perform the tests. Two probe cards would be required: one to measure the FE chip lines one pair at a time (this will have between 55 and 60 pins), the other to cover all single connections from the MCC to the outside world, covering the whole area of the flex and having about 170 pins.

A VMUX64 chip (developed by Oklahoma) can then be used to multiplex the resistance signals to a meter. Early indications are that these probe cards can be had for a reasonable price.

The components required to assemble a PixelDAQ test station have been ordered and are beginning to arrive.

1.1.1.4.3 Production

No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, K. K. Gan, M. Gilchriese)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
*Compl. 1 st proto. Design	29-Oct-98	1-Mar-99	Delayed
*1 st proto. Design review	18-Feb-99	18-Feb-99	Complete
*Compl. Tests of 1 st protos.	18-Mar-99	17-Sep-99	Delayed
*Select module type	18-Mar-99	22-Feb-99	Complete
*2 nd proto. Design review	17-Sep-99	10-Sep-99	On schedule

1.1.1.5.1 Design/Engineering.

No activity.

1.1.1.5.2 Development and Prototypes

LBNL

The characterization work for the IZM module we received last month has now been completed. Complete absolute charge calibrations have been performed on all FE chips by comparing a Cd109 source peak on each pixel with the injected-charge versus TOT curves derived from calibration runs. The result is that the absolute charge scale for the module is wrong by roughly 10%, so all claimed thresholds are actually about 10% lower than would be expected based on the calculated capacitance values. The module has been operated at several thresholds. In addition to the nominal operation at 3Ke and 4Ke thresholds (real thresholds would be 10% lower than this value), a minimum threshold operating point was also found, at about 2.5Ke (or about 2.3Ke absolute threshold). Operation at the 3Ke threshold was studied extensively, including source scans in which all pixels on all FE chips were simultaneously enabled for readout. The resulting trigger rate from the internal FastOR, after eliminating a modest number of noisy pixels, was only about 10 Hz. This is an even more stringent test than actual LHC readout, since all pixels are enabled for readout AND the readout is self-triggered. Source runs with the global FastOR were performed using the Cd109 source (the self-trigger rate with all 16 chips enabled is about 70 KHz with this source – roughly identical to the real LHC trigger rate). Also, threshold scans were performed to measure the noise while simultaneously operating all chips in readout-all mode with the Cd109 source. This does produce a great deal of asynchronous readout activity on the module, but does not accurately simulate LHC operation (which would require that the module hit rate would be more than 50 MHz, well beyond the capability of laboratory sources). Nevertheless, under these conditions, no change in the measured noise value was observed, indicating that the additional digital activity had no significant effect on the module operation. We eagerly await receiving more such modules using solder bumps to confirm this performance with larger statistics, and with the next generation of Flex hybrid prototypes.

The final measurements we hope to make with this module, prior to bringing it to the H8 testbeam, include evaluations of the needs for local decoupling capacitors. Now that we have a module which achieves our performance requirements, albeit with large local

decoupling on each FE chip, we will explore how much of this decoupling can be removed while still retaining this desired performance. Also, we are working on getting our IR laser test stand operational so that we can make absolute timing measurements over a complete module and verify that we can satisfy our timing requirements not just at the single chip level, but at the full module level. Additional issues can arise due to distribution of critical timing signals (like the 40 MHz clock) around the module, as well as due to additional dispersion effects when combining results from 16 FE chips. The laser is working, and provides a pulse height and spot size appropriate for our testing, but we have realized that there is a limitation in our VME test board that does not allow proper synchronization of the laser with the internal 40 MHz clock, and thereby limits our ability to perform precise timing measurements. We are presently modifying a PLL test board to solve this problem, and hope to produce new results in the next few weeks.

Plans have been made for the next set of single-chip and module assemblies to be fabricated by IZM using FE-B devices. There will be a total of 10 new single chip devices, using the new prototype 1.5 sensor designs which need to be evaluated in the May H8 testbeam . There will also be two new modules, which will be assembled with the new Flex Hybrid 1.x design and the new Flex Support Card to provide the first realistic Flex prototypes which are expected to meet performance requirements. The previous Boeing-bumped assemblies had poor noise performance and did not meet all of our requirements.

More generally, a bump bonding plan for the next year is under development with Bonn and Genoa to systematically address all fundamental and production issues. A draft plan was circulated for discussion.

Wire bonding tests of flex 1.0 hybrids mounted on aluminum dummy modules to evaluate the performance of different adhesives and to begin to develop automated wire bonding started this month. A number of adhesives and encapsulants will be evaluated.

Ohio State

We are designing the optical package that couples the optical fibres to the VCSEL's and PIN diodes. The package is designed to operate like a connector: a cap with three holes for the fibres and a base with deposited wire bonding traces and pads for PIN and VCSEL placements. Some prototype caps and bases (Version 1.0) have been successfully produced using aluminum silicate, a machinable ceramic. This proves the principle of the design. The design has been improved (Version 2.0) to include precisely machined pockets for VCSEL and PIN placements. Prototyping of this design reveals that it is difficult to machine small pockets (350 microns x 350 microns) with sharp edges for precise chip placements. Alternative machining techniques are being explored. The design has been further refined (Version 2.1) to be comparable with the trace layout of the SCT optical package to ease the comparison of the two packages. The prototypes have also been tested fired with various firing temperatures and schedules. We now have a firing recipe that produces strong ceramic-like products. We are currently prototyping the three dimensional mask for the wire bonding trace deposition. It is difficult to produce stainless steel mask with small slits (100 microns wide) for the gold deposition without breaking the

drill. Alternative drill size, drilling speed, and mask metal are being investigated. We have attempted to deposit traces using a prototype mask with incomplete slits and the result looks promising. After a mask has been successfully produced, we will deposit traces on the base, mount and wire bond the VSCEL's, and place fibres on the cap. Jigs for wire bonding and fibre placements have been designed and fabricated. We will study the optical and electrical properties of the prototypes produced. If the design is proved to be successful, we will investigate alternative machinable materials and the possibility of using injection molding instead of machining for cost saving.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2 nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2 nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2 nd ABC	23-Oct-98	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2 nd CAFÉ-M	30-Oct-98	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2 nd ABC	16-Nov-98	30-Apr-99	Delayed
*FDR for 2 nd ABCD	11-Dec-98	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Done
*Submit 2 nd ABCD	27-Jan-99	15-Apr-99	Delayed
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	Done
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2 nd CAFÉ-M	19-Apr-99	16-Jun-99	Delayed
*Compl. Fab of 2 nd ABC	19-Apr-99	15-Sep-99	Delayed
*Test systems complete	26-Apr-99	31-Jul-99	Delayed
*1 st ICs avail. For 2 nd proto hybrid	18-May-99	30-Sep-99	Delayed
*Compl. Fab of 2 nd ABCD	30-Jun-99	31-Aug-99	Delayed

1.1.2.1.1 Design/Engineering

LBNL & UCSC

Two design reviews were held for the ABCD and ABC chips during March. These will be the last formal reviews before submission of the two designs. The ABCD layout has been changed in several ways to improve the stability by improving ground current paths. Also,

more information concerning substrate coupling in the DMILL process that affects the instability problems has been learned and measures have been taken to mitigate them in the layout. It is still not clear if all the improvements are sufficient to cure the unstable performance but we have determined that we have gone as far as we can with simulations and more will only be learned after these improvements are put into silicon. The ABCD is scheduled for submission in early April.

Much progress has also been made on bringing the ABC design to completion. All problems of the previous iteration have been fixed. Measures have been taken to speed up slow sub-circuits so that the simulations now work above 100 MHz with standard models. The full chip has been built and passed LVS check. What remains now is one final look at power bussing in the overall layout, final extraction of the netlist with parasitics and final top level Verilog simulations with back annotation. Submission should be before the end of April.

Work on the CAFE-P wafer tester is proceeding. A draft test specification is complete but more work is needed before giving it to Maxim for review. The test setup at UCSC is functional with the old probe card and correctly tests partial chips (not all channels) using the old CAFE-M probe card. The extra electronics to test all 128 channels is on order. The new probe card has not yet been ordered but a circuit design is complete and we are waiting for a bid from the vendor. The full system will not be ready by the original milestone of 26-April but is on track to be ready well before the wafers arrive from Maxim in mid-June.

Work is also proceeding with test facilities for the ABC/ABCD at LBNL. The designs of two VME boards are nearly ready for layout to commence. Software will represent much of the work in coming months. Like with the CAFE-P test equipment, development is behind the original schedule due to extended work testing prototypes, however, the facilities should be ready before the wafers arrive since the ICs have not yet been submitted for fabrication.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

No activity.

1.1.2.1.3 Production

No activity.

1.1.2.2 Silicon Strip Hybrids (C. Haber)

Milestones	Baseline	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97	Complete
Complete fab of 1st prototype	2-Feb-98	23-Mar-98	Complete

Preliminary design review	3-Aug-98	1-May-99	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	15-May-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	15-May-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	15-May-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Aug-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Aug-99	Delayed
*Compl. 2nd proto assembly	17-May-99	15-Aug-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	1-Sep-99	Delayed

LBNL

1.1.2.2.1 Design

A final design review was held of the ABC chip this month. One result of that review was a proposal to add an additional pad servicing Vdd for the input receiver circuits. This pad would require an additional Vdd pad on the hybrid as well. The current hybrid design was examined and it was determined that such a connection can (and will) be added. Another result of the ABC review process was a plan to change the pull on the ID-4 pad. This creates an option to connect ID-4 to the SELECT line. The hybrid design was examined and will be modified to allow for the optional connection of ID-4 to SELECT and to Vdd. To date though the final ABC layout still is not available. Completion of the hybrid requires this layout.

1.1.2.2.2 Development and prototype fab

A fab requires the completed hybrid layout and that requires the ABC layout. We still await this. The primary hybrid fabrication vendor was contacted and advised of this continuing delay. We were told that they were prepared to service us as soon as we deliver the new design. We also contacted the second vendor who will do the fab using silver based conductors. We were approached by a third vendor who is interested in working with BeO substrates. We are preparing a package of documentation for their review.

A new UV cure encapsulant was identified and samples procured. It appears to behave well. We will do a full evaluation on bonded devices in the coming month.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
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*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98	On schedule
Prototype tooling complete	1-Apr-99	1-Aug-99	Delayed
*Compl. Design of proto assy/test	14-Jun-99	15-Nov-99	Delayed
*Compl. Fab of tooling for proto	14-Jun-99	15-Nov-99	Delayed

As noted below the tooling workshop will be held in late May. The module construction and evaluation activity is hostage, in part, to the lack of good front end ASICs. The delay indicated above reflects the slip in the time of the tooling workshop as well as the requirement to have built prototype modules with chips from the next submission. The 1-Aug-99 date for the completion of prototype tooling describes tooling which will have been tested only on dummy modules. The 15-Nov-99 date refers to electrically working modules.

LBNL

1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation. A new set of drawings for a number of the assembly fixtures was received from the group at RAL. We reviewed these but will defer fabrication until after the May tooling workshop. The fixtures we presently have are sufficient for the ongoing studies.

1.1.2.3.2 Development and prototypes

A tooling workshop will be held at the Rutherford Lab in the UK the week of May 24, 1999. This was originally planned for March of 1999.

Design of a new calibration plate was completed in January 1999. Work began to prepare the GDS-2 file needed for fabrication in February and a GDS-2 file was completed this month. In the process we discovered an inconsistency in the detector spacing within the module among various "official" module drawings and specifications. This spacing is written into the plate so we must be sure it is correct and consistent with the errors expected in the wafer dicing. A detailed message was sent to all the people involved. We were told that "it was being looked into..." We received price quotations from the photo mask maker for the fabrication of the this new calibration plate and distributed these to the interested groups.

Design continued on a folding fixture for the hybrids.

The process of training a new technician on the assembly system began. This individual is expected to be the lead technician on the module assembly during the construction phase.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford/R. Jared)

<u>Milestones</u>	<u>Baseline</u>	<u>Current</u>	<u>Status</u>
*Select PreROD implementation	30-Oct-98	26-Mar-99	Complete
*Requirements review	30-Nov-98	18-Nov-98	Complete
*Compl. System design	28-Dec-98	TBD	TBD
*System design review	11-Jan-99	TBD	TBD
*Compl. PreROD design	29-Jan-99	TBD	TBD
*Compl. PreROD layout	15-Feb-99	TBD	TBD
*Compl. PreROD procure	1-Mar-99	TBD	TBD
*Compl. PreROD PCB fab	16-Mar-99	TBD	TBD
*Compl. PreROD 1 st assemble	30-Mar-99	TBD	TBD
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	TBD	TBD
*PreRODs complete	20-Aug-99	TBD	TBD
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

A new schedule will be developed after the review of March 25-26. The dates shown above are preliminary.

1.1.3.1.1 Strip Test Beam Support (A. Lankford)

UC Irvine

Hardware and software support for laboratory and beam tests of SCT electronics and modules continued. An additional DSP readout system was delivered to users at CERN for future module testing. Technical support was given to users at Prague for external triggering of the DSP readout system.

1.1.3.1.2 Pixel Test Beam Support (R. Jared)

University of Wisconsin

Hardware for the support of the beam test software is being debugged. Effort was also committed to update the code for the PLL.

1.1.3.2.1 ROD Requirements (A. Lankford)

Definition of ROD requirements is largely complete. During the design review, the need was identified for a new requirement that configuration data for the front-end chips should be stored locally in the ROD.

UC Irvine (A. Lankford)

A detailed study of ROD input-link mapping was performed. The distribution of input links to the RODs should average the occupancy that is seen by each ROD. The mapping should also distribute the links in a fashion that is reasonable from a geometry perspective. The inputs of each ROD should be fully occupied. A detailed mapping scheme was proposed. A spreadsheet will be produced specifying the entire mapping of detector modules to RODs and of RODs in crates.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin (A. Lankford)

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No refinements of the essential model were made during March.

1.1.3.2.3 ROD Implementation Model (A. Lankford)

A review was held March 25-26 to recommend a single choice of architecture from between the FPGA-based approach and the processor-based approach. The review committee recommended an approach using FPGAs only in the data stream and DSPs for other tasks such as monitoring and calibration.

UC Irvine (A. Lankford)

Studies of various aspects of the DSP implementation model continued in March. Decoder performance in the DSP-based implementation was studied using emulation on a DSP evaluation model. SCT data for these studies was generated according to hit distributions from Monte Carlo results. These studies demonstrated ample decoder performance for eight input links per decoder and trigger rates of 100kHz at all occupancies that do not saturate the output Readout Link. Work continued on a ROD software development platform using two cooperating TI DSP evaluation modules, one to emulate a Decoder DSP and one to emulate the Host DSP. A great deal of preparation took place for the ROD review that was held at UCSC on March 25-26.

Recent changes to the LBL/Wisconsin FPGA design approach were studied and evaluated.

University of Wisconsin (R. Jared)

Simulation of the FPGA implementation model were performed in March for the SCT version of the ROD. These simulations have an event generator

follower by either the FPGA simulation or a behavioral model of the ROD in C. The simulation showed that both models give the same outputs and buffer occupancies. Further studies with the behavioral model were then used to show how the ROD performed under varying conditions. These performance studies showed that the decoder and gatherer would handle the maximum data rates with adequate reserve capabilities. Much work was put into preparing for the ROD review that was held on March 25-26 at UCSC.

Understanding of the maximum trigger rate showed that 95kHz is the expected. This information was communicate to Irvine so that we could improve the event generators.

1.1.3.3.7 Preprototype ROD

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed primarily above under WBS 1.1.3.2.3.

UC Irvine (A. Lankford)

IBIS simulation of ROD99 DSP data and address busses continued.

University of Wisconsin (R. Jared)

Behavioral and VHDL simulation of the FPGA continue.