February 14, 1999

Silicon Subsystem Report

January 1999

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress.

1.1.1 Pixel System

Costs are currently within allocated amounts. The cost of the prototype program for the support frame is still uncertain, but discussions with vendors are underway to firm up ROM estimates and obtain fixed price quotes. Completion of the design of the front-end, rad-hard electronics continues to be delayed relative to the baseline schedule but a first design review of FE-D has been scheduled. There are minor delays still present in the mechanics (selection of the concept for the prototype disk ring support), in the completion of the design of the 2nd prototype sensors and in the first prototype module design. No additional delays relative to last month are evident.

1.1.2 Silicon Strip System

Costs are within allocated limits. The CAFE-P was submitted. There are further delays in the submission of the ABC and ABCD beyond those reported last month. There are no fundamental problems with the ABC and the additional delays are caused by the limited manpower and the need to complete detailed, and duplicate, simulations to ensure a good submission. The additional delay in submitting the ABCD is caused by lack of complete understanding of the stability of existing prototypes when connected to detectors. This will be reviewed in mid-February. The hybrid schedule is linked to the schedules for the ABC and ABCD and thus additional delays are now expected.

1.1.3 ReadOut Driver System

Costs are within allocated limits. Since November, development of an implementation model has been focused on coupling high-performance FPGAs and DSPs for the decoding and gathering functions. This implementation model was well advanced; however, by the end of January, simulations of data flow suggested that the joint FPGA-DSP design is probably inferior to either the FPGA-based decoder/gatherer or the DSP-based decoder/gatherer designs previously developed. The system design review has been delayed until these architectural issues are resolved and additional delays are surely to result. This situation will be reviewed in early February.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (D. Bintinger, M. Gilchriese)

Milestones	Baseline	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98	Complete
Select prototype ring concept	1-Nov-98	1-Feb-99	Delayed
Complete fab 1st prototype ring	1-Apr-99	1-Apr-99	On Schedule
Complete fab 1st prototype disk	1-July-99	1-July-99	On Schedule
*Select sector baseline concept	1-Sep-99	1-Sep-99	On Schedule
*Module attachment CDR	1-Sep-99	1-Sep-99	On Schedule
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	On Schedule

LBNL

1.1.1.1.1 Design

Hytec, Inc made preliminary disk support ring drawings. LBNL and Hytec reviewed the drawings. Calculations were done of construction tolerances, post construction measurement tolerances and tolerances for distortion due to temperature change for pixel disk sectors.

Analysis of the overall support frame design continued at Hytec, Inc. The focus of the activities was on providing sufficient stiffness in the disk frame section to achieve deflection requirements. It appears that additional stiffening members at the end of the disk frame will be needed to meet distortion requirements. Two composite manufactures were visited - Composite Horizons and Allcomp. The design was reviewed with these vendors and their preliminary ROM quotes discussed.

1.1.1.1.2 Development and Prototypes

Additional test mockups of aluminum tube sector 4 were sent to Hytec, Inc. to measure distortions due to temperature change with TV Holography. The test mockups were fabricated with stiffer core-to-facing adhesives including a low temperature cure cyanate ester adhesive. Aluminum tube sector 4 will be rebuilt based on the results of these tests.

Hytec, Inc. conducted a vibration mode analysis of ESLI sector 8. The fundamental cantilever mode frequency is approximately 300 Hz with some less prominent modes of lower frequencies at approximately 100 Hz. These less prominent modes may be vibrations of the individual sector faces. ESLI sector 8 meets stiffness requirements.

Irradiation of aluminum tube sector 3 was completed at the LBNL cobalt 60 source. The sector has been exposed to approximately 23 Mrads. Infrared images of the irradiated sector were taken under nominal power load. The infrared images indicated that the temperatures of the dummy silicon modules on the sector after irradiation were in general

within 1 degree C of the temperatures before the irradiation for similar power and coolant conditions. All temperatures after irradiation were within specifications.

Tests of adhesive shear moduli continued on silicon module-to-sector structure adhesives.

1.1.1.1.3 Disk Production
No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Current	Status
*Start market survey	2-Nov-98	20-Nov-98	Completed
*2nd prototype PDR	1-Dec-98	7-Dec-98	Completed
*Complete market survey	5-Mar-99	5-Mar-99	On schedule
*2nd prototype FDR	29-Mar-99	29-Mar-99	On schedule
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99	On schedule
*Compl. 2nd prototype design	27-Apr-99	27-Apr-99	On schedule
*Compl. Fab of 2nd prototypes	21-Sep-99	21-Sep-99	On schedule

1.1.1.2.1 Design

No activity.

1.1.1.2.2 Development and Prototypes

Responses to the Market Survey have been received from 5 companies, some of them grouped as consortia. A committee consisting of Seidel, D'Auria, Vrba, Wunstorf, and Rohe met by phone and qualified 4 of the companies. A late response from a sixth company is expected and will likely also qualify. Detailed discussion of the variety of technologies to be included in the Second Prototype order occurred. It was decided that the Second Prototypes will examine p-spray as well as moderated p-spray, conventional high-resistivity silicon as well as oxygen-enriched silicon, and wafers of thicknesses 250 and 200 microns. The order for the Second Prototypes is expected to be placed on 29 March.

A batch of pixel prototypes fabricated by IRST/ICT was received by the Udine group and has been tested with encouraging results. IRST/ICT is included in one of the consortia that are now qualified to participate in the Second Prototype and Production orders.

The ROSE collaboration has announced significant improvement in the radiation tolerance of oxygen-enriched silicon; this work is being followed closely by ATLAS for possible application to the production pixel wafers.

The detailed design of the Second Prototype wafers is nearing completion at MPI.

The LBNL Pixana software has been installed at New Mexico for use with the ATLAS DAQ test stand. A comparative noise measurement has been performed with the linear stage motors off and on; no significant noise difference was observed between the two cases.

Several First Prototype single chip devices were mounted in pc boards for electrostatic characterization. The inter-pixel capacitance of an unirradiated ST2 device was measured and compared with results from irradiated devices. A three-dimensional inter-pixel capacitance calculation was performed using the Integrated Engineering Software electrostatic program---the results are consistent with measurements and with a 2-d simulation.

1.1.1.2.3 Production

The New Mexico clean room components have been received from the vendor. The laboratory area has been readied for clean room installation. A detailed AutoCAD design of the clean room layout is underway.

1.1.1.3 Pixel Electronics (K. Einsweiler)

Milestones	Baseline	Current	Status
Submit 1st Honeywell SoI test die	15-Nov-98	15-Nov-98	Completed
Submit 2nd Honeywell SoI test die	15-Jan-99		Not known
1st design review of DMILL proto	25-Jan-99	23-Feb-99	Delayed 2 weeks
*FDR DMILL 1st prototype	25-Jan-99	15-Mar-99	Delayed
*Compl. Design DMILL 1st proto.	26-Feb-99	7-Apr-99	Delayed
1st design review of Honey. Proto	1-Jun-99	1-Jun-99	On schedule
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Jul-99	Delayed
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Sep-99	Delayed
*Compl. Fab of DMILL 1st proto.	23-Jul-99	7-Sep-99	Delayed
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	7-Jan-00	Delayed

The date for submission of a 2nd set of test die to Honeywell is not known at this time. We continue to negotiate with Honeywell for a date for a next multi-project wafer run. The schedule for the first DMILL design review has slipped by two weeks due to both difficulties in organizing the review and some delay in completing the deliverables for this review, particularly the documentation. Submission of the Honeywell rad-hard prototypes is delayed by comparison to our original schedule due to the decision to focus all resources on the DMILL submission first.

LBNL

1.1.1.3.1 Design

Our highest priority remains the DMILL front-end chip submission ("FE-D"). Significant progress has been made on our contribution in the last four weeks. The complete column-pair readout, revised bottom-of-column and end-of-column circuitry is now complete. This is the basic building block for the readout of the chip. The present layout provides all necessary buffering and functions in the agreed space in the floorplan. All known problems in the previous FE-B design have been fixed, and the improved design now uses low-swing data transmission to get the data out of the active pixel array and into the end-of-column buffering where it waits for the trigger decision (this is the same technique used to speed up modern SRAM memory chips). We have invested significant effort in simulating the individual blocks using the complete set of DMILL models, especially the extreme corner models which are the "fast-fast pre-rad" and the "slow-slow 25 MRad". These two models alone differ in performance (speed) by almost a factor of four. This has required adding some adjustment capability at critical parts of the circuits. For example, the sense amplifiers that receive the low-swing data and convert it to full-swing CMOS in the bottom-of-column circuitry have a typical, a fast, and a slow operating configuration to simultaneously control the power and speed of these circuits. There are 22 of these amplifiers per column pair, or 198 per chip. If they were simply designed for the worst case, then their power consumption would be about half the total digital power consumption of the entire chip if the die received were from a fast-fast run.

The final block that we need to deliver is almost complete. This is the trigger memory and readout control logic that forms the sequencing brain of the chip. The layout for this block is complete, but is being refined in order to fit in the allowed footprint. This should be completed within one week. In parallel with completing the layout and schematic work, work has been proceeding on complete Verilog and SPICE simulations of the blocks. The Verilog libraries are complete, and have been tuned using HSPICE simulations to give roughly the correct delay modeling under parasitic loads. A framework has been set up to conveniently generate test vectors for the simulation, and allow automatic comparison of the detailed Verilog model extracted from the schematic with a more ideal behavioral model. Over the coming month, the simulation work will continue in order to completely verify the performance of our blocks. We will also build a simple digital test chip that includes all of this circuitry, along with many buffered test points, to allow us to fully characterize the performance of the digital readout circuits after irradiation.

We are preparing for the first design review for FE-D, scheduled to take place on Feb. 23 at CERN. In addition, we have a 2-day working meeting (with critical designers staying for a week) in Bonn to integrate together all of the parts of the FE-D chip in a preliminary way, on Feb. 16-17. We are presently in good shape to deliver all of the above work at this working meeting. This should keep us on an aggressive but fairly credible track for a submission of the FE-D array in early April 99.

1.1.1.3.2 Development and Prototypes

Further lab work has been carried out this month to complete our basic characterization of single chip devices, and to further explore the performance of our modules.

For single chip devices, we have been performing extensive timewalk measurements, in which the charge and time of arrival of input pulses is systematically varied. This allows us to extract the real timing performance of the combined FE chip and detector. Our measurements show a stronger-than-expected dependence of the timewalk on the preamplifier feedback current in the FE-B chip. A large performance penalty is paid when using a slow shaping (typically used in the 98 test beam in order to stretch out the time-over-threshold and improve the charge measurement). For the nominal shaping, in which the pulse from one MIP returns to baseline in about 500ns, we observe somewhat more timewalk than we had expected based on single channel measurements in test chips. We find that an overdrive (charge above threshold) of about 1.5Ke is required to achieve an in-time response. What this means is that if the timing is adjusted so that the beginning of the 25ns time bucket corresponds to the signal from a 50Ke input charge, then the smallest charge value which produces an output within 25ns is 1.5Ke above whatever threshold is set on the chip. For a typical threshold setting of about 3Ke, this would lead to an "in-time threshold" of about 4.5Ke. While this is still acceptable, we had expected that with our dual-threshold design, the overdrive would be close to 0. We are exploring more fully how such performance, measured in the lab, can best be translated into a realistic specification on the front-end timing performance, keeping in mind the difficulty in distributing a uniformly timed 40 MHz clock to all 30K chips in the pixel detector. It looks likely that we should tighten our specification for a single chip to 20ns. In addition, we are measuring the timewalk performance of many chips in order to better understand dispersion issues within chips, chip to chip variations, etc. A realistic timewalk specification must not be based just on the difference in mean arrival time of pulses with different charges, but must include the widths of these time distributions. Distributions for individual channels vary due to noise fluctuations, and there is dispersion across a chip and between chips because of variations in channel performance, internal signal distribution uniformity, etc. We will use our present lab measurements to define a simple lab specification that is still meaningful in terms of actual detector operation (in which one defines an algorithm for timing the detector, and then wants to know the hit detection efficiency for single-crossing readout).

We have also been measuring single chip devices that are made with the MCM-D interconnection technology. This is one of two candidate methods for constructing complete modules. It involves deposition of a 4-layer high-density copper interconnect (like a high density PC board) directly on the detector wafer before bump bonding. There was some concern that this would impact the performance of the detectors, as well as introduce additional capacitance and cross-talk into the front-ends of the pixel array. We have now measured the performance of two chips, each with several different types of interconnect geometry, and have confirmed that for the types of interconnection proposed for ATLAS, there is no significant impact on the sensor/electronics performance.

We have spent some time trying to understand the noise performance observed in single chip assemblies using different bump-bonding vendors. One problem is that a new Italian bumping vendor, Alenia, working closely with Genova, has produced a number of

assemblies. These assemblies have unacceptably poor noise performance, at a level never observed in our previous prototypes. This has caused us to return to our data and study the issue in more detail. It is known that Indium bumps always come with a thin oxide layer between the two halves of the bump, and sometimes also between the bump and the Aluminum trace on the chip. In mechanical prototypes, this effect has been observed to disappear after applying small (1V) DC voltages. However, such voltages will only develop in a real assembly if the initial resistance between sensor and preamplifier is very high. There are some indications that this may not always be the case. We have also noted that among all of the assemblies we have built so far, all of the low noise devices used solder bumps. There is only one type of detector for which assemblies were made using both Indium and Solder, and in this case the Indium assembly shows worse noise performance. The effort to understand these issues will continue over the coming months, and is particularly relevant because all of our modules so far used Indium bumps.

Finally, we have received the nine loaded PLL boards (the LBL/Wisconsin-designed VME board used for all lab test work) which we expected before Christmas. They have been inspected and are undergoing preliminary tests. So far, five of the nine boards appear to be working well in the lab, and will now undergo more extensive burn-in testing before delivery. The remaining boards are being debugged between the many other measurement activities in our lab. We hope to complete this work by the end of Feb.

1.1.1.3.3 Production
No activity.

1.1.1.4 Pixel Hybrids (R. Boyd))

Milestones	Baseline	Current	Status
*Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98	Complete
*1st prototype design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	15-Apr-99	15-Apr-99	On schedule
*Select hybrid type	15-Apr-99	1-Mar-99	Ahead
*2nd proto design review	28-Apr-99	28-Apr-99	On schedule
*Compl. 2nd proto design	25-May-99	25-May-99	On schedule

Oklahoma
1.1.1.4.1 Design
The floor plan sketch for the version 1.x prototypes has been completed. The 1.x prototype will incorporate design modifications arising from the experience of testing the first prototypes. Reviews and comments by LBNL and Genova are being incorporated into a final floor plan for review at CERN in mid-February. This version corrects some (nonfatal) omissions from the first version and implements several improvements by taking advantage of all the substrate area for routing.

A detailed cost analysis has been added to a yield and cost model for modules developed by M. Gilchriese. These costs and yields are based on experience with flex circuit

fabrication by General Electric Corporate Research and Development. R&D Circuits (Edison, NJ) has provided a quotation for fabrication of prototype and production flex circuits that is substantially cheaper than GE and work is in progress to assess the capabilities of this vendor. They are also able to provide testing and laser singulation, and the quotation is for 100% working parts. In addition, two other vendors have been identified who can perform flying probe circuit testing. One quote, by Zero Defects (Milpitas, CA) is for less than 2 cents US per test point.

1.1.1.4.2 Development

We are currently examining waveforms at the FE bond pads to insure that the Flex Hybrid is performing as designed. It appears that there are no ill affects from impedance mismatch. Indeed, there is no discernible difference in the waveform quality among any tested so far. We will continue with these tests in order to debug the 4 non-working FE's on the module.

1.1.1.4.3 Production
No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, M. Gilchriese)

Milestones	Baseline	Current	Status
*Compl. 1st proto. Design	29-Oct-98	1-Mar-99	Delayed
*1st proto. Design review	18-Feb-99	18-Feb-99	On schedule
*Compl. Tests of 1st protos.	18-Mar-99	18-Mar-99	On schedule
*Select module type	18-Mar-99	1-Mar-99	Ahead
*2nd proto. Design review	17-Sep-99	17-Sep-99	On schedule

We are projecting additional delays this month for the completion of the 1st prototype design, which is directly tied to the completion of the flex hybrid design. Although a 1st generation prototype design has been completed, and modules assembled, we have decided to implement a 1.x generation design that includes improvements but is not yet a 2nd prototype. See the discussion under 1.1.1.4.1.

1.1.1.5.1 Design/Engineering.

No activity.

1.1.1.5.2 Development and Prototypes

LBNL
A single-chip assembly mounted on a support card was received from Genoa. As already noted in 1.1.1.3, this assembly has high noise. It was X-rayed and some misregistration of the bumps was observed, but this does not explain the high noise.

We have spent quite some effort on characterization of our three prototype modules in a systematic way. The two modules mounted on PC boards (so called “bare” modules) have reasonable performance in many ways, although not yet acceptable for ATLAS. Distributions of noise and threshold for the 25K channels which can be read out using FE-B chips are reasonable (noise of about 200e and dispersion of about 300e). However, there is clear evidence of coherent “digital crosstalk” effects, in that a FE chip that has reasonable single-channel noise performance may fail to operate properly when all channels are simultaneously enabled (as they would be in the real experiment). It is not yet clear how much of this is direct crosstalk between the FE chip and the detector, and how much occurs through the power supplies or possibly the chip substrates. These modules also suffer from significant bump-bonding problems, as described in previous reports, and imaged using high-resolution X-ray techniques. New prototypes are being built to address some of these possible solutions. In particular, a new solder-bumped module is now available to be mounted on an improved next-generation PC card for testing. This should happen within the next week.

The one realistic prototype module we have, built using 150μ thinned electronics die, and a UOK Flex hybrid for interconnections, has also been extensively tested. This module operates acceptably (one of the 16 chips fails to see external charge injection), however the noise level is unacceptably high. The high noise level can be controlled by biasing many of the FE chips in such a way that they are effectively shut off. This is very similar to the behavior first observed in the bare modules when they were operated without adequate decoupling on the LV power supplies. It seems to arise because one mis-behaving chip modulates the analog power supplies with noise in a frequency range that has a significant effect on the neighboring chips. This problem should be eliminated in the next generation of Flex hybrid which will have pads suitable for mounting larger decoupling capacitors (it seems that 0.1 μF per chip is really necessary, instead of the 0.01μF in the present Flex prototype). Thus, it is expected that the next generation of Flex module should have noise behavior which is close to acceptable, albeit at some cost in material. The Flex module has also been characterized with a Cd109 photon source. However, with the additional material between the source and the sensor (namely the hybrid, and passive components), this source is not very useful. A barely visible 0402 capacitor is enough to attenuate the source by a factor of about 100, making uniformity studies almost impossible with such a source. Real characterization of modules may require a higher energy beta source, which in turn will lead to significantly lower counting rates and longer testing times.

Oklahoma

No solution has yet been found for the "high current" problem on the Oklahoma flex hybrid module reported here previously. We are unable to ground the substrates of the FE chips that were used in its construction and this may prove the only reliable way to solve this problem. So, we continue testing one FE at a time. We have received an external chopper circuit from LBNL which allows us to perform rapid threshold scans (under 6 minutes) without the severe threshold shift (> 9000 e^-) that is typical of internal scans. Thus, we have been able to perform tuned threshold scans for several of the chips in preparation for readout of a laser source. Our first attempts at this revealed a coherent

noise problem which overwhelms the readout when all pixels are activated. This problem has been seen in board modules also and is not understood at this time. In addition, we need to provide hit bus triggering to enable this type of readout, as the present flex module support card does not provide this capability.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	1-Mar-99	Delayed
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	Done
*Submit 2nd ABCD	27-Jan-99	31-Mar-99	Delayed
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	On Schedule
*Frame contract in place	15-Apr-99	15-Apr-99	On Schedule
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	1-Jun-99	Delayed
*Compl. Fab of 2nd ABC	19-Apr-99	15-Jul-99	Delayed
*Test systems complete	26-Apr-99	26-Apr-99	On Schedule
*1st ICs avail. For 2nd proto hybrid	18-May-99	15-Aug-99	Delayed
*Compl. Fab of 2nd ABCD	30-Jun-99	15-Aug-99	Delayed

1.1.2.1.1 Design/Engineering

LBNL & UCSC

The CAFE-P was released for production just before month end. The design was actually sent to Maxim earlier in the month but it took some time to clear all design rule check violations and sign off on the release for fabrication.

The formal Final Design Review was held for the ABC on 26-Jan. The review included Brig Williams and 3 other designers that Brig coerced into spending the 9 hours looking at all the details of the design. At the finish of the review, work still remains with regard to

simulations and verification. The plan will be to distribute all the simulation results to the reviewers as well as the ABC/ABCD design team but not to have another formal meeting before chip submission. The actual submission date is still difficult to pin down given the normal manpower issues that have plagued this re-design effort. Optimistic guess is end of February.

The ABCD has not yet been submitted, primarily due to the oscillation problem with the existing prototype that was discovered in December and has still not been resolved. See below for more information.

Work has started in earnest on the CAFE-P wafer tester. Results using a periodic calibration signal and integrating output signals into a DVM appears to adequately test the data channel. Correct gains have been obtained using the technique. The next step is to test known faulty channels to check its ability to distinguish good from bad devices. We have also had productive discussions with our probe card vendor and with Maxim concerning the possibility of transferring this test scheme to Maxim for use in production. We need to finalize a test specification in order for further negotiations with Maxim to proceed.

Detailed design for an improved IC test system for ABC and ABCD started at LBNL. This will require fabrication of a new VME board and other boards for wafer-scale testing as well as test board and hybrid testing at frequencies up to about 80MHz.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

The irradiation of 2 CAFE-M chips at the PSI in Switzerland with 300 MeV pions proved to be bust. There were problems with the target box which ended the irradiation prematurely before the chips had received even 0.5 Mrads of dose and an unexpected non-uniformity in the beam profile across the chips resulted in an uncertainty of $\pm$50% in the absolute dose received. This made it impossible to accurately compare the results with previous gamma and proton irradiations. The results are in a steep part of the damage curve and the errors span the range of values seen with the two previous types of irradiations. This will be repeated as soon as we can get more time at the PSI.

The unstable operation of ABCD prototypes when connected to full length detectors which was discovered in December has continued to be studied but is as yet not understood. There is evidence that altering the detector biasing circuit and the ground planes of the hybrid can improve the operation but it is still not clear what the exact cause of the instability is. LBNL has added some test pads to two chips with more FIB time in an effort to track the signal after each amplification stage. Work is continuing at LBNL, CERN and Liverpool to try to understand the problem.

1.1.2.1.3 Production

The tendering for the rad-hard IC frame contract was closed and sealed bids were received from Honeywell and Temic as well as a few others with whom we do not have previous experience. The proposal for the frame contract was sent to the CERN Finance Committee so that looks like it is on track for approval in March.

1.1.2.2 Silicon Strip Hybrids(C. Haber)

Milestones	Baseline	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97	Complete
Complete fab of 1st prototype	2-Feb-98	23-Mar-98	Complete
Preliminary design review	3-Aug-98	20-Feb-99	Delayed
*Compl. 2nd proto subs. design	29-Oct-98	15-Mar-99	Delayed
*Compl. 2nd proto cable design	29-Oct-98	15-Mar-99	Delayed
*Compl. 2nd proto fanout design	29-Oct-98	15-Mar-99	Delayed
*Compl fab of 2nd proto substrate	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto cable	11-Mar-99	1-Aug-99	Delayed
*Compl fab of 2nd proto fanout	11-Mar-99	1-Aug-99	Delayed
*Compl procure of 2nd proto comps	11-Mar-99	1-Aug-99	Delayed
*Compl. 2nd proto assembly	17-May-99	15-Aug-99	Delayed
*1st 2nd proto hybrids available	14-Jun-99	1-Sep-99	Delayed

The hybrid design delays have increased since they are linked to the completion of the layout of the ABC/ABCD chips and to the fabrication schedule for these chips.

LBNL
1.1.2.2.1 Design

A visit was made to the vendor that manufactured the hybrid prototypes. We discussed various changes to the design to optimize yield and mechanical performance. We reviewed a new set of check prints and received new price quotes.

1.1.2.2.2 Development and prototype fab

ABCD chips on hybrids were bonded to detectors and seen to oscillate in already in November. Studies of this effect continued including use of individual test capacitors.

A second possible vendor for hybrid production was identified earlier. A documentation packet and RFQ were sent to the vendor in December. A quote was prepared by them and received in January. The prices appear to be a good improvement. Discussions on technical issues are continuing. They also offer the possibility to use silver conductors rather than gold. This will yield some radiation length improvement and a significant price improvement. We are studying the technical documentation to understand all the implications of this approach.

Flex cables for the front to back connection were received from the vendor. They are acceptable.

A prototype hybrid set was soldered together using the new jumpers. It will be wrapped around a dummy detector sandwich in a removable way as a test.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	Delayed
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98	Complete
Prototype tooling complete	1-Apr-99	1-Apr-99	On schedule
*Compl. Design of proto assy/test	14-Jun-99	14-Jun-99	On schedule
*Compl. Fab of tooling for proto	14-Jun-99	14-Jun-99	On schedule

LBNL
1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

Design of a new calibration plate was completed.

We have obtained thin electron-microscope "targets" which were suggested as a tool for use in measuring surface shape in January. We studied these and they don't appear to be an improvement over simple graphite marks on the baseboards.

A visit from the Smart Scope representative occurred and the new software was evaluated in December. We received a quote for an upgrade to our system in January and expect to place an order in February.

Design continued on a folding fixture for the hybrids.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford/R. Jared)

Milestones	Baseline	Current	Status
*Select PreROD implementation	30-Oct-98	4-Nov-98	Complete
*Requirements review	30-Nov-98	18-Nov-98	Complete
*Compl. System design	28-Dec-98	28-Dec-98	Complete
*System design review	11-Jan-99	8-Mar-99	Delayed
*Compl. PreROD design	29-Jan-99	31-Mar-99	Delayed
*Compl. PreROD layout	15-Feb-99	15-Apr-99	Delayed
*Compl. PreROD procure	1-Mar-99	30-Apr-99	Delayed
*Compl. PreROD PCB fab	16-Mar-99	16-May-99	Delayed
*Compl. PreROD 1st assemble	30-Mar-99	31-May-99	Delayed
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	On schedule
*Compl. Test stand essential mod.	12-May-99	12-May-99	On schedule
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	On schedule
*Compl. PreROD assembly	9-Jul-99	15-Jul-99	Delayed
*PreRODs complete	20-Aug-99	20-Aug-99	On schedule
*Test stand design review	21-Sep-99	21-Sep-99	On schedule
*Compl. Design of test stand	28-Sep-99	28-Sep-99	On schedule
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	On schedule
*ROD Common design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD strip design PDR	1-Oct-99	1-Oct-99	On schedule
*ROD pixel design PDR	1-Oct-99	1-Oct-99	On schedule

1.1.3.1.1 Strip Test Beam Support

UC Irvine

Hardware and software support for laboratory and beam tests of SCT electronics and modules continued. In January, a version of DSP system code was modified to allow for more flexible readout using burst mode. Burst mode readout only transfers events from input FIFOs on the Silicon Low Level (SLL) card to DSP memory in bursts as opposed to event by event. Code was added to monitor the DSP memory and only transfer events when the memory reaches a certain threshold, thus allowing for better use of the memory with multiple size events from different detectors.

1.1.3.1.2 Pixel Test Beam Support

University of Wisconsin

Fabrication of the eight PLL cards has been completed. Hardware debugging of the PLL cards continues. Debugging is expected to be completed in February. Additions to code in the PLL has been an active item is January. These additions will add new capabilities that have been requested by the pixel group. General support of the hardware and software continues.

1.1.3.2.1 ROD Requirements

UC Irvine and University of Wisconsin

Definition of ROD requirements is largely complete. Although no new requirements were defined in January, the latency for delivery of *L1Accept* signals through the ROD was further studied as part of studies of the overall level 1 latency through the SCT system. Documents describing the ROD/TIM (TTC Interface Module) and ROD/BOC (Back-of-Crate Card) interface timing were prepared with the U.K. groups.

1.1.3.2.2 ROD Essential Model

UC Irvine and University of Wisconsin

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No significant refinements of the essential model were made during January.

1.1.3.2.3 ROD Implementation Model

ROD design effort continued to focus on a combined FPGA/DSP implementation in order to combine the best features of the FPGA-based and DSP-based approaches studied previously. Studies centered on the decoder section, which in the combined approach utilizes both an FPGA and a DSP. Two scenarios for processing data in the FPGA before transfer to the DSP were studied in detail. In the first approach, zeroes are added to the data in order to make all event fragments of fixed length. In the other approach, a summary word is used to minimize data length. Both approaches strive to facilitate the transfer of data by DMA to the DSP. A simulation of the flow of data from the links through the FPGA and through the DSP was written by the Wisconsin group to study buffer sizes and occupancies. Although these studies were not yet complete at the end of January, the simulation revealed that occupancy of the buffers in the FPGA occasionally becomes large for buffers of practical size, suggesting that data loss may occasionally occur. Although the amount of data loss may not be large, the frequency of buffer overflow at the very large data rates of the SCT may be difficult to manage in a simple fashion. Studies involving variation of parameters and more statistics were still in progress at the end of the month.

UC Irvine

The primary focus of activity at UCI in January was exploring how various schemes of FPGA decoding and data transfer would impact the DSP in the combined FPGA/DSP decoder. The central issue is how to decode and transfer in a manner that reduces related tasks in the DSP, in order to make available more DSP processing power for other tasks.

Host DSP issues were further evaluated, and development of software to simulate DSP host software continued. The simulation software was modified to include data to account for empty/not ready decoders. Work also continued on a ROD software development platform using two cooperating TI DSP evaluation modules.

University of Wisconsin

The work in this are has been in collaboration with UCI to understand the operation of the hybrid model of the ROD. This model uses a combination of DSP and FPGA hardware. The main effort was the writing, debugging and running a simulator of the operation of the hybrid. The early results of this simulation have shown some problem. More simulation is required to understand if there is a configuration that will work satisfactorily.

1.1.3.3.7 Preprototype ROD

UC Irvine and University of Wisconsin

The implementation model for the preprototype ROD is being developed in tandem with the model for the production ROD. Progress on the implementation model is discussed above under WBS 1.1.3.2.3.